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A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

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Abstract

A novel Monolithic Active Pixel Sensor (MAPS) for charged particle tracking made in a standard CMOS technology is proposed. The sensor is a photodiode, which is readily available in a CMOS technology. The diode has a special structure, which allows the high detection efficiency required for tracking applications. The partially depleted thin epitaxial silicon layer is used as a sensitive detector volume. Semiconductor device simulation, using either ToSCA based or 3-D ISE-TCAD software packages shows that the charge collection is efficient, reasonably fast (order of 100 ns), and the charge spreading limited to a few pixels only. A first prototype has been designed, fabricated and tested. It is made of four arrays each containing 64×64 pixels, with a readout pitch of 20 μm in both directions. The device is fabricated using standard submicron 0.6 μm CMOS process, which features twin-tub implanted in a p-type epitaxial layer, a characteristic common to many modern CMOS VLSI processes. Extensive tests made with soft X-ray source (^{55}Fe) and minimum ionising particles (15 GeV/c pions) fully demonstrate the predicted performances, with the individual pixel noise (ENC) below 20 electrons and the Signal-to-Noise ratio for both 5.9 keV X-rays and Minimum Ionising Particles (MIP) of the order of 30. This novel device opens new perspectives in high-precision vertex detectors in Particle Physics experiments, as well as in other application, like low-energy beta particle imaging, visible light single photon imaging (using the Hybrid Photon Detector approach) and high-precision slow neutron imaging.

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1. Introduction

In the early 1990s monolithic pixel sensors have been proposed as a viable alternative to CCD's in visible imaging (see, for example, Ref. [1] for a historical perspective and a complete bibliography). These sensors are made in a standard VLSI technology, usually CMOS, which is the reason why they are often called CMOS imagers. Two main types of sensors exist: the Passive Pixel Sensor (PPS) or the Active Pixel Sensor (APS). In the former, a photodiode is integrated in a pixel together with selection switches, which connect the photodiode directly to

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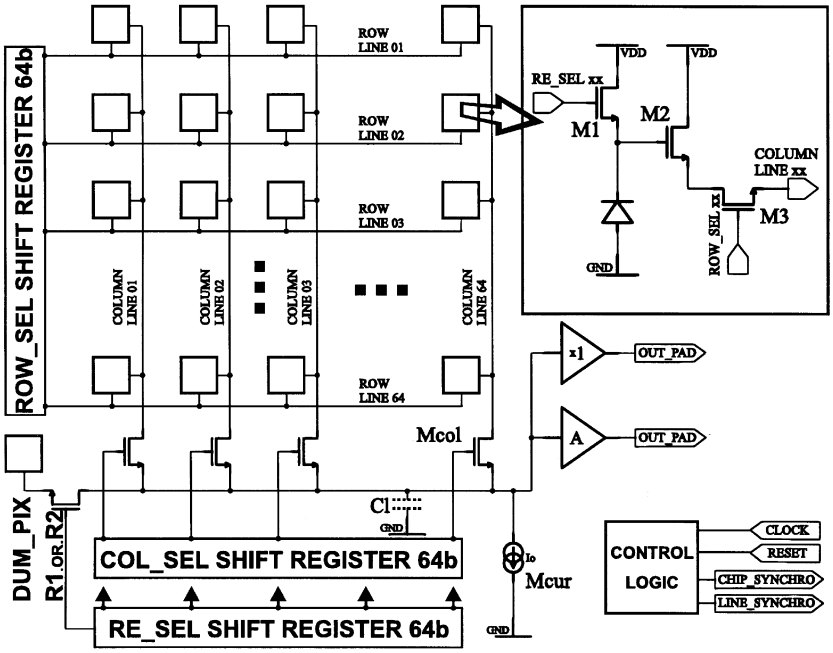

Fig. 1. Simplified block diagram of a single array of the MIMOSA circuit. In the inset (right top) is the baseline architecture of a CMOS imager. Transistor M1 resets the photosite to reverse bias, transistor M3 is a row switch, while transistor M2 is the input of a source follower. The source follower current source (common to the entire row) and the column selection switch are located outside the pixel.

the output line for readout. In the latter, an amplifier integrated in each pixel directly buffers the charge signal. Today most CMOS imagers have an APS structure because of its better performances. The baseline architecture is shown in the inset of Fig. 1. A photosite, usually a photodiode or a photogate, is integrated in a pixel with three transistors: a reset switch M1, the input M2 of a source follower and a selection switch M3. Noise levels of $5e^-$ rms have been obtained with such architecture at room temperature [2].

A great interest in CMOS sensors in visible light applications exists because of their characteristics:

- low cost, since they are fabricated in a standard VLSI technology;
- low power, since the circuitry in each pixel is active only during the readout and, contrary to CCD's, there is no clock signal driving large capacitances: the total power dissipation is usually in the range of 100 mW for a few millions pixel device even with integrated analogue-to-digital conversion (see, for example, Ref. [3]);
- random access, since each pixel can be addressed directly for readout;
- increased functionalities, taking advantage of the full capabilities of the CMOS technology: the control logic, the analogue-to-digital converter or other signal processing blocks can be integrated in the same substrate as the sensor array.

Because of these features, CMOS sensors are the favoured technology for demanding application, which are typically found in space science.

They also look attractive for tracking applications because of the following features:

- spatial resolution: the pixel size is usually between 10 and 20 times the Minimal Size Feature (MSF) of the fabrication process, which means that 10 μm or smaller pitch is possible, and hence spatial resolution better than 3 μm even with a binary readout. Taking advantage of possible analogue readout and natural charge spread between neighbouring pixels, for

very demanding application the spatial resolution can possibly be pushed down to less than 1 μm;
- very low multiple scattering: since the substrate can, in principle, be thinned down to a few tens of microns;
- radiation tolerance, taking advantage of the reduced radiation sensitivity offered by nowadays submicron VLSI processes.

The straightforward application of a CMOS sensor in a tracking detector is nevertheless not possible because of its poor fill factor. For visible light applications this number is defined as the fraction of the pixel area that is sensitive to the radiation. Because of the transistors and metal interconnections; it is usually in the range of 20–30%, an unacceptable low value for particle tracking application; In order to overcome this limitation, one of us [4] proposed to integrate a sensor in a twin-tub process with an n-well/p substrate diode. This technique has already proved its effectiveness in visible light applications [5] reducing the blind area only to the routing metal lines, which absorb the visible light but have no effect on the detection of minimum ionising particles.

Since the proposed device is an Active Pixel Sensors (APS) fabricated on a single substrate, we call it Monolithic APS or MAPS.

In the past, other pixel technologies have been proposed and developed for tracking. We will mention here those with the detectors fabricated on high-resistivity silicon [6] and the Charge-Coupled Devices (CCD) [7,8].

Based on high-resistivity detectors, both hybrid (see, for example, Ref. [9]) and monolithic [10,11] Active Pixel Sensors exist. The main advantage of using a high resistivity substrate stands in the fact that a relatively thick depletion region (typically of 300 μm) can be obtained. This means that a large charge signal is generated by the impinging particles and signal over noise ratios in excess of 100 can be achieved. Both hybrid and monolithic approaches suffer from the complexity of the technology used, which in turn implies high costs. In the case of the monolithic approach, both detectors and VLSI technologies are combined in a single, complicated process, which consistently has a poor yield. In the hybrid approach, the detector and VLSI electronics are fabricated on two different substrates, which are then connected together by complicated and expensive bump bonding techniques. In both approaches, the front-end electronics is relatively complicated and this forces a large pitch (over one hundreds μm) in at least one direction. As a consequence, micron spatial resolution cannot be obtained in both directions, unless analogue signal processing techniques are used (see, for example, Ref. [12]).

CCD are fabricated on a low-resistivity substrate with a specially tailored CMOS process. The detection principle is basically the same as the one used in the proposed MAPS. CCDs can be fabricated on a single wafer, covering several square centimetres. Connections to the related electronics are done only at the edge by standard ultrasonic wire bonding. The signal over noise and the spatial resolution that can be achieved in CCDs are basically the same as for the MAPS. CCDs have a poor radiation resistance [13] compared to the expected resistance of MAPS and very little flexibility with respect to the readout strategy.

In this paper, we describe the principle of the proposed structure, the related device simulations, the design and the experimental results of a first prototype made in a standard CMOS 0.6 μm technology. This first prototype is named MIMOSA for *Minimum Ionising particle MOS Active pixel*. It has been tested with soft X-rays in order to get an absolute calibration of its charge sensitivity (the charge-to-voltage conversion factor) and with minimum ionising particles (MIP) in order to prove the detection principle. A more detailed analysis of the beam test data is currently under way and will be presented elsewhere.

As it will become clear in the following, off-the-shell sensors are in general not suitable for tracking applications, because the efficiency of the device depends in a crucial way on details of the fabrication technology as well as of the design.

2. Detector principle

In a CMOS sensor, the detector part is integrated on low-resistivity silicon, the standard sub-

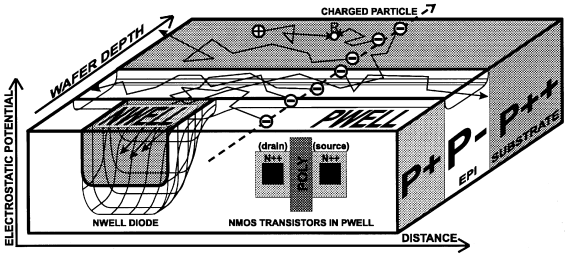

Fig. 2. Sketch of the internal structure of a pixel for charged particle tracking. The circuit's three transistors are integrated in the p-well (p^+) while the charge-collecting element is an n-well diode (n^+) on the p-epitaxial layer. Because of the difference in doping level (of the order of three orders of magnitude), the p-well and the p^{++} substrate act as reflective barriers. The trend of the electrostatic potential (white lines) is shown at two cross-sections. The generated electrons are collected in the n-well diode.

strate for VLSI technologies. The depletion region is shallow and consequently the charge collection efficiency poor. Moreover, the detector element covers only a fraction of the full pixel area. In order to overcome these limitations, a novel structure is proposed (Fig. 2). It takes full advantage of the substrate structure of most modern VLSI technologies, which feature twin (p and n) tubs, implanted in lightly doped, p-epitaxial silicon, grown on a highly doped p^{++} substrate. The photodiode is made of the junction existing between the n-well and the p-type epitaxial layer. Because the epi-layer doping is a few orders of magnitude smaller than that of the p-well or the p^{++} substrate, potential barriers exist at its boundaries. The height of the potential barriers is of the order of [5]

$$V = \frac{kT}{q} \ln \frac{N_{\text{sub}}}{N_{\text{epi}}} \quad (1)$$

where k is the Boltzmann constant, q is the electron charge, T is the absolute temperature and N_{sub} and N_{epi} are, respectively, the doping of the substrate and of the epitaxial layer. The barriers act like mirrors for the excess electrons (minority charge carriers). The electrons produced by the radiation in the epitaxial layer diffuse towards the n-well diode contacts. The substrate is formed of "low-quality" silicon, which behaves as a getter for the impurities. The recombination time in this region is relatively short, which explains why only a small fraction of the charge created there may be able to drift towards the epitaxial layer and possibly be seen by the collecting electrodes. Because of the reflective potential barriers, the sensor is fully sensitive over the whole pixel surface.

Tracking in Particle Physics experiments requires the detection of MIPs, with high efficiency and good spatial localisation. A relativistic charged particle releases only a fraction of its energy in a thin layer of matter, it generates typically 80 pairs of electron–holes per micron of silicon. Depending on the geometry of the device and the relative position of the impact point, the charge can be shared between two or more pixels.

In order to get the required detection efficiency, the processing technology as well as the design must be carefully considered. We identified the thickness of the epitaxial layer, as the key technology parameter. A 0.6 μm, triple-metal layer process has been chosen, because about 1000 electron/hole pairs are produced by a MIP in the thick epitaxial layer (between 12 and 16 μm). For the sensor design, the basic diode is formed by a 3 μm side square N-well structure, that paves the way for the epitaxial layer forming the potential well that collects the charge. Structures with 1 and 4 diodes per pixel have been designed and simulated. The four-diode sensor is supposed to reduce the charge spreading between neighbouring pixels.

3. Device simulation

2-D as well as 3-D simulations have been performed in order to understand the charge collection in the proposed structure. The accuracy of both simulations depend on details of the geometry and doping of the epitaxial layer, details which are generally known with poor accuracy. The results presented here must be considered as preliminary. In order to get better results, it is necessary to fine tune the simulation parameters with some experimental results. Measurements of details of the charge collection in the proposed structures are underway and will be presented elsewhere.

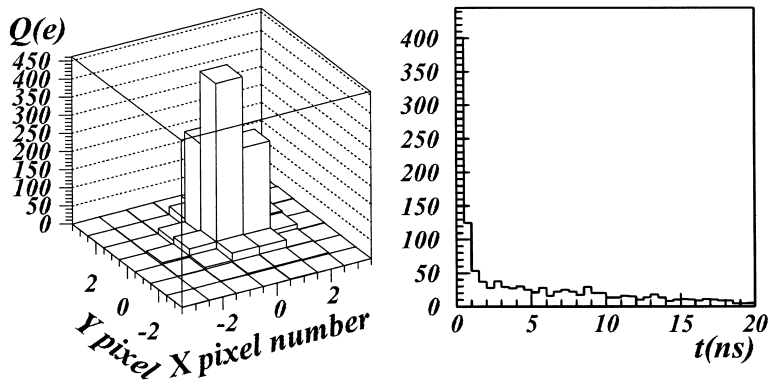

Fig. 3. Example of Monte-Carlo results: 3-D charge spreading and collection time distribution for a 'on edge' hit.

3.1. 2-D Monte-Carlo study

The advantage of the 2-D simulation originates mainly in its speed and flexibility, the 3-D simulation having the advantage of being more refined and accurate. The movement of the carriers in the proposed structure is mainly due to the thermal diffusion and to an additional electric field generated by doping differences in a few regions (see Eq. (1)): the boundaries of the epitaxial layer and the collection diode. This consideration motivates the use of a Monte-Carlo simulation. The electric field profiles are deduced from two-dimensional device simulations made with ToSCA [14]. The recombination time of the minority carriers was considered as poorly known and, therefore, varied over a range of possible values. Device parameters like d_{EZ} and d_N are given by the manufacturer with quite rather modest accuracy: they were thought to be in the range of 12–15 μm and 2–4 μm, respectively. For the epi-substrate interface, the fact that the wafer is processed at high temperature implies that in the simulation one needs to consider also a wide transition zone: sensible values for this width range between 2 and 5 μm. In the simulation, we compared "central" hits (particles traversing the centre of the pixel), to the most unfavourable situation when a particle crosses one corner of the pixel and the charge is shared between four neighbouring pixels. The 2-D device simulation has been coupled to a 3-D Monte Carlo in order to get a 3-D view of the charge collection. A typical outcome of the simulation is shown in Fig. 3. Tables 1 and 2 summarise the results. The full details of these studies may be found elsewhere [15,16].

Besides the collected charge in the central pixel (Q_c), which is of paramount importance for cluster search, we defined three other output variables: the charge spreading between adjacent pixels (Δ_Q), the average signal in the cluster (Q_{clu}), and the collection time (t_{coll}) in each pixel of a cluster. The charge spreading Δ_Q is defined as the root mean square of the projected distribution of the collected charge (see example in Fig. 3). Because of the projection, only relative variations of Δ_Q are indicative and not the absolute value of Δ_Q. A 3×3-pixel sub-array centred on the pixel showing the largest signal defines a cluster.

For a given pixel size, we identified four physical parameters which mostly affect the above defined variables: the thickness d_{EZ} of the epitaxial layer, the width d_{EZP} of the boundary region between the epitaxy and the p^{++} substrate (which acts as a smooth gradient of potential), the depth d_N of the N-well collecting diode and the electron recombination time τ_R.

As expected (see Table 1) increasing the thickness of the epitaxial layer, the charge generated by a MIP is increased as well as the number of pixels involved in each event (charge sharing within a cluster) and the collection time.

Table 1 gives the results for the single-diode geometry. It compares the most favourable case and the worst one, depending on the track position

Table 1
Charge collection efficiency parameters for a single MIP particle as a function of the epitaxial layer d_{EZ} thickness and of the position of the hit in the pixel. Q_c is the charge collected by the central pixel, Q_{clu} is the average signal in the cluster, Δ_Q is a measure of the charge spreading between adjacent pixels (see text for an explanation), t_{coll} is the collection time

	'Central' hit			'On corner' hit		
d_{EZ}	9 μm	12 μm	15 μm	9 μm	12 μm	15 μm
Q_c (electrons)	740	750	760	160	165	170
Q_{clu} (electrons)	900	1000	1100	720	800	850
Δ_Q (pix)	0.30	0.40	0.51	0.73	0.87	0.92
t_{coll} (ns)	5.1	10.2	14.5	17.3	23.0	26.4

Table 2
Charge collection efficiency parameters for a central hit as a function of the depth d_N of the N-well collecting diode and of the electron recombination time τ_R (see Table 1 caption for the signification of Q_c, Q_{clu}, Δ_Q and t_{coll})

	d_N as a variable			τ_R as a variable		
	2 μm	3 μm	4 μm	150 ns	300 ns	600 ns
Q_c (electrons)	660	750	830	670	680	700
Q_{clu} (electrons)	1000	1100	1160	990	1010	1040
Δ_Q (pix)	0.53	0.51	0.44	0.19	0.40	0.45
t_{coll} (ns)	18.7	14.5	12.3	13.3	15.1	17.2

inside the pixel: these calculations show that MIMOSA will provide a high charge signal for single MIPs independent of the track impact point. They also show that the charge in the central pixel of the cluster is always substantial enough to allow efficient cluster selection, even if the electronics noise amounts to a few tens of electrons.

The N-well diode depth d_N and the electron recombination time τ_R may have important effects on the charge collection. In Table 2, we summarise the sensitivity of the charge collection to these two other parameters. The major effect of increasing the diode depth is an increase in the charge collected by the central pixel as well as a reduction of the charge spread. The collection efficiency has very little dependence on the recombination time τ_R, at least in the considered range of values. In high-quality epitaxial silicon, we expect the recombination to have a limited impact on the charge collection efficiency. The conclusion of this study is that a minimum ionising particle provides a cluster total signal of about 900 electrons, for any reasonable assumption of the process parameters.

3.2. 3-D simulation

The usefulness of 2-D simulations for pixel detectors, which are actually 3-D devices, is limited. Advanced tools for technological process analysis and 3-D device modelling are essential. The commercially available ISE-TCAD [17] package was used. The simulated structure is described by the boundary inside which the mesh and the doping profiles are defined. The granularity of the mesh is adjusted to the gradient of the impurity concentration and to the demanded calculation precision in some critical parts of the detector volume. Thanks to the VLSI foundry, it was possible to carry out 3-D simulation using doping profile definitions that are very close to the real 0.6 μm CMOS process in which our detector was fabricated. In spite of a theoretically unlimited number of grid points, on which ISE-TCAD can work, the number of mesh vertices used in the simulation was limited to the reasonable value of 50 000–60 000. This comes from the limited memory and processing speed of the computer used (HP9000/778). The most important benefits, coming from the use of the ISE-TCAD package, are the use of advanced physical models. The most appropriate physical models for the effective intrinsic density, the carrier mobility, the recombination and the impact ionisation have been chosen and their parameters were calculated either on the basis of the impurity concentration or given explicitly taking into account standard parameters of silicon. The drift–diffusion model has been chosen for solving the problem of charge collection; 3×3 pixel structures were simulated. Due to the reflective (Neumann) boundary conditions, an additional volume of silicon was added on every side of the core cluster. The thickness of the detector used in the simulation was limited to 25 μm including 15 μm of epitaxial layer, which is a typical value in the selected process. We account only for 10 μm of substrate because – in first approximation – the substrate was assumed to be of no importance for

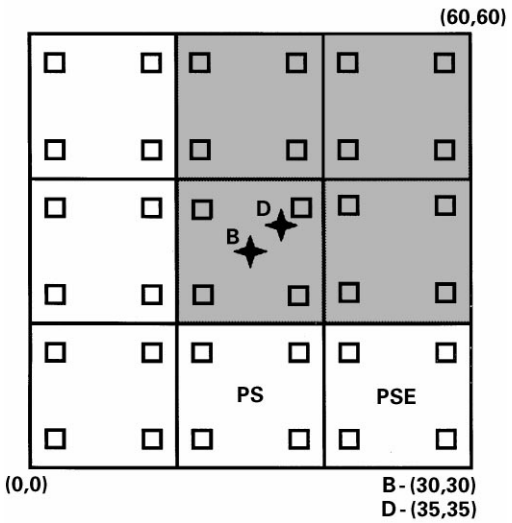

Fig. 4. Particle impact position for four-diode. The terminology used in the simulation results is highlighted in this figure. The (x,y) co-ordinates (μm) of the bottom-left and top-right corners are given as well as those of the impact point (D) and of the centre of the cluster (B).

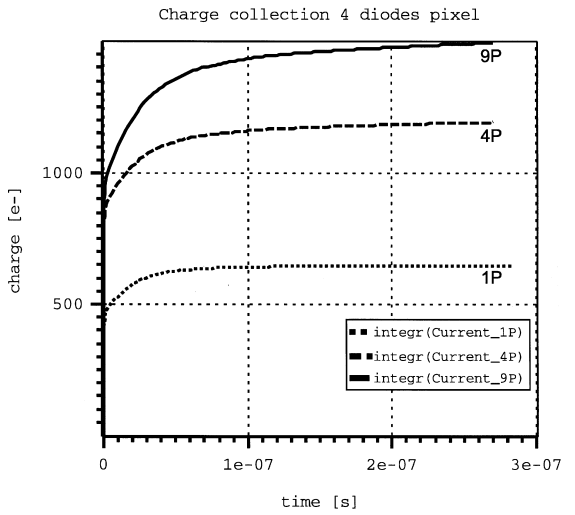

Fig. 5. Example of simulation results obtained with the ISE-TCAD package. The charge collected is shown as a function of time in the cluster of four-diode type pixel array in case of a side hit (see Fig. 4). The curves represent the charge collected, respectively, by: the full cluster (9P), the central pixel (1P) and the 4 pixels closest to the impact position (4P, see grey area in Fig. 4).

the useful signal. A more realistic simulation with a detailed description of the substrate would require the knowledge of other substrate properties like the trap densities or the recombination time. The so-called "α-particle model" with a gaussian dependence on radial co-ordinates was chosen for charge generation. Simulations were carried out with a charge of 80 electron/hole pairs created per μm along the track of the particle. The simulation methodology applied in ISE-TCAD is different from the 2-D Monte-Carlo approach presented above. Instead of tracing each carrier separately, the collected charge is obtained by current integration. Both simulation methods give comparable results, which are in good agreement with the measurements (see Section 5). Further improvements in the simulation precision and a better understanding of the charge collection in the MAPS need much more accurate technological information. The geometry used for these simulations is shown in Fig. 4. A typical result obtained with the ISE-TCAD package is shown in Fig. 5.

From the simulation, it can be deduced that the central pixel always collects between 25 and 50% of the total charge found in the cluster of 3×3 pixels. The remaining charge is collected by the neighbouring pixels. For the single as well as for four-diode pixel, a 2×2 subset of pixels collects about 70–75% of the charge found in the complete 3×3 cluster. These remarks can be taken as useful guidelines in the analysis of real data, when trying to define the signal cluster in order to optimise the overall signal over noise ratio.

Concerning the collection time, we observe no significant difference between the central or neighbouring pixels in the cluster. On the contrary, the collection time is significantly shorter for the four-diode configuration (about 100 ns) than for the single diode one (about 150 ns).

The discrepancies between the 2-D and 3-D simulations on charge spread and charge collection time depend on details of the models. Experimental measurements are in progress to determine the true collection time. This is likely to be found in the range of 10–100 ns as defined by the simulations. Beam tests (see Section 5) can give an accurate measurement of the charge spread between pixels.

4. Prototype design

4.1. Main features

The prototype chip consists of four independent arrays of active pixels with slightly different design [18]. Each array is made up of 4096 pixels laid down in 64 rows and 64 columns with a pitch of 20 μm in both directions. The first and basic detector structure is the n-well/p-epi diode (right-hand side in Fig. 6). Because of its very low capacitance (3.1 fF), it is the best solution with respect to the noise and the conversion gain. The second detector structure is a four-diode architecture, based on the first one. As shown in the previous section, this should give a reduced charge spreading at the expenses of a higher input capacitance, hence a higher noise and a decreased conversion gain. In the third array, the same geometry as in the first structure was used, but with an enclosed layout of the reset transistor to give a higher radiation resistance. The first structure was also the baseline for the pixel in the fourth array, where no substrate connection for the NMOS transistors was drawn out in the individual pixels.

Because of the relatively small dimensions of the arrays, all the pixels in one array are multiplexed on a single source follower (Fig. 1). The output can be taken directly from the source follower or alternatively amplified by an on-chip amplifier with a voltage gain of 5. The latter was introduced in order to avoid possible degradations of the overall performances, due to possible external noise sources. The dummy pixel, shown in the block diagram, is connected to the output line during the reset phase. This limits the output recovery time after a reset cycle. Three 64-bit shift registers are used to control each array. Each bit in the first one (RE_SEL) drives the reset for all the pixels in one line. The reset operation must be repeated for every few frames in order to avoid the saturation of the diodes due to the leakage current. The minimum reset frequency depends on the exact value of the leakage current, which in turn is a steep function of the operating temperature. The two other 64-bit shift-registers are used to enable the readout of any single pixels.

The chip is powered between ground and two positive power supplies. Each array has its own analogue power supplies, bias currents and analogue outputs, while a unique power supply biases all the digital parts. The analogue and digital grounds are also common. The entire array of active pixels as well as the analogue part is surrounded by a double guard ring in order to reduce the interference from other blocks. The third metal layer is used to shield the readout electronics and the pixel arrays from electromagnetic interference

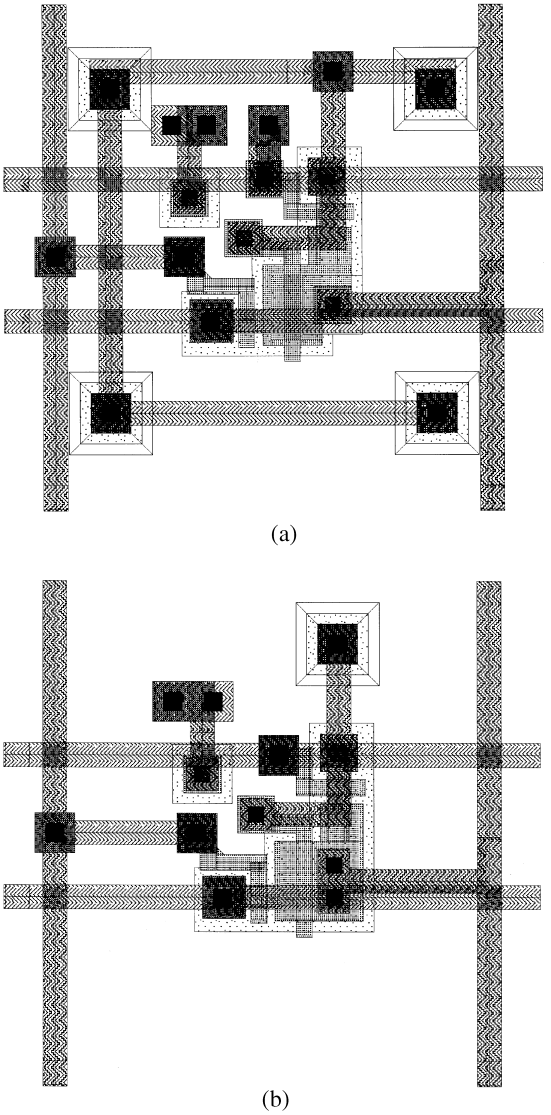

Fig. 6. Example of basic cell layout: four-diode pixel (a) and single-diode pixel (b). Metal 3 layer not shown.

and visible light. However, the shield on the sensors is only partial in order to allow optical testing.

4.2. Noise analysis

The temporal noise must be carefully analysed because it can limit the performance of the active pixel sensors, especially with regard to the small signals produced by minimum ionising particles. The noise analysis is complicated by the non-linearities in the charge to voltage conversion and in the reset transistor. The noise analysis must be done separately for the three phases of operation, i.e. the reset, the integration and the readout. This is presented in the following sections. In the experimental results presented in this paper, Correlated Double Sampling (CDS) has been used by off-line subtraction of subsequent frames. The use of CDS is beneficial in the reduction of the overall noise for several reasons. First, it reduces the influence of the low-frequency ($1/f$) noise. This means that, for the analysis of our data and within the purpose of this paper, $1/f$ noise can be neglected. Secondly, CDS removes the reset noise (kTC). Last, the noise components deriving from non-uniformity in the array (the so-called, Fixed Pattern Noise, FPN) are effectively removed by CDS.

As a first approach, the noise generated in the output voltage amplifier as well as in the off-chip circuitry can be neglected.

4.3. Noise during reset

During the reset, the transistor M3 (Fig. 1) is turned off and a positive voltage pulse is applied to the gate of M1. This transistor is saturated during a short time and then it goes below threshold for the rest of the reset phase. If the reset time t_r is much greater than the settling time t_{settle}, it can be said that the steady state has been achieved. The time t_{settle} represents the moment when the reset transistor subthreshold current equals the value of the diode leakage current. The average reset noise power can be calculated in this case by means of the commonly known expression

$$\overline{V_{n,res}^2} = \frac{kT}{C_d} \tag{2}$$

Here, C_d represents the total node capacitance that is found at the input of the source follower. However, in real systems the steady state is sometimes not obtained because of the insufficient duration of the reset time. It can be shown [19] that in this case, the average reset noise power is given by

$$\overline{V_{n,res}^2} = \frac{1}{2}\frac{kT}{C_d}. \tag{3}$$

As noticed above, the reset noise is removed by the CDS technique.

4.4. Noise during integration

The dominant noise source during the integration phase is the shot noise due to the diode leakage current i_{leak}. At room temperature the mean value of this current is in the order of several fA, and the related noise contribution is not significant for an integration time of a few milliseconds, corresponding to the one we used in the tests. However, this type of noise should be taken into account when the integration time increases. For a more precise analysis one should also take into account the change of the diode capacitance during the integration time. This latter is a second-order effect and is thus neglected. The mean square value of the noise sampled at the end of integration (t_{int}) is given by

$$\overline{V_{n,int}^2(t_{int})} = \frac{q i_{leak}}{C_d^2} t_{int}. \tag{4}$$

4.5. Noise during readout

During readout, the transistors M2, M3 as well as the column switch M_{col} and the source follower current source M_{cur} with line capacitance C_l (Fig. 1) are the main noise sources. The noise contributions introduced by each transistor can be calculated according to the expressions given below

$$\overline{V_{n,read,M2}^2} = \frac{2}{3}\frac{kT}{C_l}\frac{1}{1+\dfrac{g_{m,M_2}(g_{ds,M_{col}}+g_{ds,M_3})}{g_{ds,M_3}g_{ds,M_{col}}}} \tag{5}$$

Table 3
Basic design parameters of the MIMOSA prototype

Supply voltage	single 4 to 5V	Active diode dimensions	$3\,\mu m \times 3\,\mu m$
Die dimensions	$3.750 \times 4.050\,mm^2$	Reset transistor leakage current	24 aA
Fabrication process	CMOS 0.6 μm (3M + 2P, p-epi)	Active diode leakage current	2.9 fA
Pixel structure	Three-transistor active pixel	Conversion gain	1 diode pixel — $16\,\mu V/e^-$ 4 diodes pixel — $6\,\mu V/e^-$
Number of active pixels	Four arrays 64×64 pixels each	Noise	1diode = $49e^-$ rms ENC = $11e^-$ rms, kTC = $47e^-$ rms 4 diodes = $73e^-$ rms ENC = $25e^-$ rms, kTC = $68e^-$ rms
Pixel dimensions	$20\,\mu m \times 20\,\mu m$	Readout speed	up to 10 MHz

$$\overline{V^2_{n,read,M3}} = \frac{kT}{C_1}\frac{1}{g_{ds,M_3}(1/g_{ds,M_3} + 1/g_{ds,M_{col}} + 1/g_{m,M_2})} \quad (6)$$

$$\overline{V^2_{n,read,M_{col}}} = \frac{kT}{C_1}\frac{1}{g_{ds,M_{col}}(1/g_{ds,M_{col}} + 1/g_{ds,M_3} + 1/g_{m,M_2})} \quad (7)$$

$$\overline{V^2_{n,read,M_{cur}}} = \frac{2}{3}\frac{kT}{C_1} g_{m,M_{cur}}\left(\frac{1}{g_{ds,M_3}} + \frac{1}{g_{ds,M_{col}}} + \frac{1}{g_{m,M_2}}\right) \quad (8)$$

where $g_{ds,Mx}$ et $g_{m,Mx}$ are, respectively, the output conductance and the transconductance of transistor Mx. All the noise contributions mentioned in formulae (5)–(8) are of similar order of magnitude.

4.6. Total noise

The total noise $\overline{V^2_n}$ at the output stage of the pixel is given by the quadratic sum of the previously calculated noise components:

$$\overline{V^2_n} = \overline{V^2_{n,res}} + \overline{V^2_{n,electron}} \quad (9)$$

where

$$\overline{V^2_{n,electron}} = \overline{V^2_{n,int}} + \overline{V^2_{n,read,M2}} + \overline{V^2_{n,read,M3}} + \overline{V^2_{n,M_{col}}} + \overline{V^2_{n,read,M_{cur}}}. \quad (10)$$

Eq. (10) contains all the contributions to the total noise that are not suppressed by CDS. These are the noise contributions which effectively enter in the noise measurements presented below.

4.7. Main parameters and estimated performance of the MIMOSA prototype.

Simulations results were obtained for $T = 27°C$ and VDD = 5 V with a reset transistor of dimensions $W/L = 0.8/0.6$. The noise is calculated for a line capacitance C_1 of 300 fF and the integration noise is not included. Table 3 resumes the basic parameters and the estimated performance of the MIMOSA prototype.

5. Experimental test results

The prototype chip MIMOSA has been extensively tested using soft X-rays (5.9 keV from ^{55}Fe source) and high-energy minimum ionising particles (15 GeV/c pions from CERN PS). The readout has been done using a VME Flash ADC unit (VFAS) [20]. The VFAS unit is a general-purpose ADC converter having two analogue inputs per VME module, 12-bit resolution, 40 MHz maximum conversion rate and a memory of 8192 samples/channel. The module also provides several digital I/O ports driven by a XILINX based, programmable logic unit. Two of these ports are used to drive the CLOCK and RESET signals, and two

others receive the control pulses from the chip (CHIP-SYNCHRO and LINE-SYNCHRO) for timing verification. Two I/Os provide handling of a trigger signal from scintillation detectors and synchronisation with a high-resolution reference telescope equipped with silicon strip detectors [21]. For this test purpose, the VFAS acquisition module memory has been organised as a circular buffer, with enough space to store two consecutive MIMOSA frames. Following a reset pulse, the MIMOSA output is constantly sampled at the readout frequency. When the readout of the first frame is finished, the trigger receiver is activated. After trigger, the data acquisition is continued for another 4096 samples and then it is stopped. Owing to this readout method an image of the entire array with its state before and after particle arrival becomes available for the analysis. This approach, which takes advantage of the trigger, is obviously possible only in the case of MIPs. During the tests with X-ray photons, where no trigger is available, the acquisition is stopped immediately after the second frame. The useful signal is calculated as the difference (for each pixel) between the second and first frame. Such a signal calculation corresponds to a Correlated Double Sampling (CDS) with the sampling time difference (charge integration) equal to the readout time of one full frame. The readout frequency was set to 2.5 MHz, translating into a charge integration time of 1.6 ms. The dominant noise source (kTC) is therefore suppressed and individual array pixel dispersions (except the leakage current) automatically compensated. Most of the tests were performed at low temperature (about -20°C), also allowing comfortably long time (>100 ms) between reset and random trigger arrival.

In order to measure the basic prototype parameters, a ^{55}Fe source was used, which emits 5.9 keV photons. Each photon generates a charge of 1640 electrons, so that the measurement of the X-ray peak position allows (supposing 100% efficient charge collection) the calculation of the total conversion gain. Then the individual pixel Equivalent Noise Charge (ENC) can be estimated from the variation around the pedestal after CDS. Because the CDS value is a result of two independent measurements, the actual pixel ENC (other than kTC) is equal to the measured rms value divided by the square root of 2. The pedestal value after CDS is due to the individual pixel leakage current. For the measurement of the conversion gain at the pixel level, it was assumed that the total charge generated by each 5.9 keV photon is totally collected within a cluster of 25 pixels (5×5 cluster) around the photon impact point. The central pixel is identified as the highest signal in a cluster. Table 4 shows the total charge collected (5.9 keV photon peak position) as a function of the cluster's size. The relatively small difference between the charge collected on a 3×3 cluster with the respect to the 5×5 cluster justifies the assumption above. It is also consistent with our device simulation results. Fig. 7 shows the experimental distribution of the 3×3 cluster signal sum for the main three types of pixels: single diode, four diode and single diode with edgeless reset transistor. The summary of the calibration measurements is given in Table 5. The measured performances agree well to the estimated ones, presented in Table 3. The width of the calibration peak is dominated by the dependence of the charge collection efficiency on the position of the impact point.

Table 4
Cluster total charge (in ADC units and equivalent number of electrons) experimentally measured as a function of the cluster size for X-ray photons (5.9 keV) (the conversion factors are 43.7 electrons/ADC unit for the single-diode structure and 99.4 electrons/ADC unit for the four-diode structure)

	Cluster size		
	1 pixel	3×3 pixels	5×5 pixels
Single diode			
Charge in ADC units	10.5	33.5	37.5
Charge in electrons	458	1464	1640
Four diode			
Charge in ADC units	9.5	16.5	16.5
Charge in electrons	944	1640	1640

In order to test the performances of the MIMOSA sensor in tracking MIPs, tests were performed with high-energy 15 GeV/c pions at the CERN PS. A very preliminary analysis done with an on-line program indicates a signal-to-noise ratio of about 30, with practically 100% efficiency. The S/N is defined as the ratio between the total charge

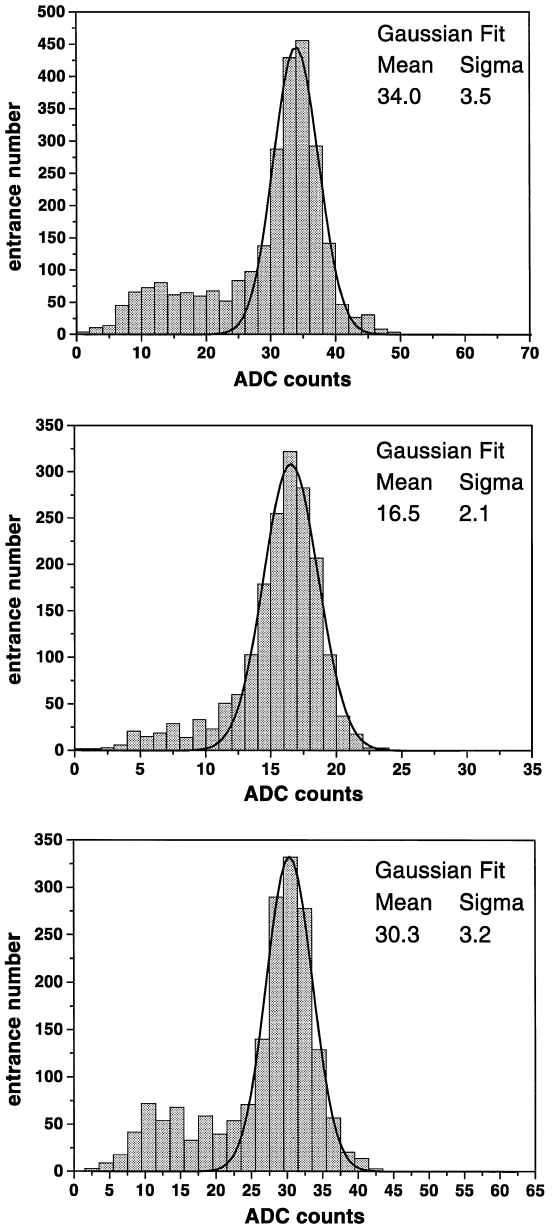

Fig. 7. Calibration results with 5.9 keV X-ray photons for three major pixel structures: single-diode (upper), four-diode (central) and edgeless reset transistor type, single-diode structure (lower). The first two measurements have been done at $-20^{\circ}C$, while the third one has been done at room temperature. The conversion factors (ADC units to electrons) are given in the caption to Table 4.

collected in a cluster around the impact position and an individual pixel noise. The total collected charge is about 1000 electrons, in agreement with the device simulations. A detailed analysis of the beam tests, including a measurement of the detection efficiency and the spatial resolution, is currently under way, and the results will be published elsewhere [22].

Table 5
Measured performance of the MIMOSA prototype (these experimental values must be compared with the design ones given in Table 3)

Pixel geometry	Conversion gain ($\mu V/e$)	ENC (except kTC) (e^- rms)	Leakage current (fA) ($-20^{\circ}C/20^{\circ}C$)
Single diode	15.0	15	1.3/27
Four-diode	6.1	31	2.7/30

6. Conclusion

In this paper, we presented a novel Monolithic Active Pixel Sensor (MAPS) for the detection of charged particles. As APS used in visible light applications, it is manufactured in a standard VLSI CMOS technology. The detector with all the front-end and the control electronics integrated on a single chip is an attractive feature with respect to other solutions like Hybrid Active Pixel Sensors or CCD's. The design is relatively straightforward and other functionalities can be integrated on a chip.

In order to achieve high charge collection efficiency for charged particle detection, a special pixel architecture is used. It makes use of the widely used cross-section of present CMOS technologies, where twin wells are made in a slightly doped p-type epitaxial layer grown on the p^{++} substrate. If the n-well/p-epi diode is used as the collecting element, all the front-end electronics can be integrated in a p-well. The impinging radiation creates charge particularly in the partially depleted thick epitaxial layer. Because of the difference in doping levels, a potential barrier is present at the boundaries between the epitaxial layer on one side and the p-well or the p-substrate on the other. By diffusion and drift, the excess electrons in the epitaxial layer move towards the n-well/p-epi diode where they are collected.

We have designed a prototype device (MIMOSA = Minimum Ionising particle MOS Active pixel sensor) to test the effectiveness of this concept. This prototype consists of four arrays of 64×64 elements at 20 μm pitch. In each array a different pixel design has been implemented. Two different semiconductor device simulators (ToSCA and ISE-TCAD) have been used to calculate the charge transport performances of the structure, like collection time and charge spread. The collection time is relatively fast (in the order of 100 ns) and the charge is confined to a few pixels, the spread magnitude depending on the pixel geometry. The prototype has been tested with MIPs (15 GeV/c pions) as well as with low-energy X-rays from a ^{55}Fe source. The experimental results are in good agreement with the simulation and a signal-over-noise ratio of the order of 30 is obtained in both cases. A detailed analysis of the MIP data is under way and will be presented elsewhere.

The characteristics and performances of this device make it very attractive for vertex and tracking detectors in high-energy physics, as well as in many other applications requiring imaging of charged particles, such as beta imaging, visible light single photon imaging (using the Hybrid Photon Detector approach) or high-precision slow neutron imaging.

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