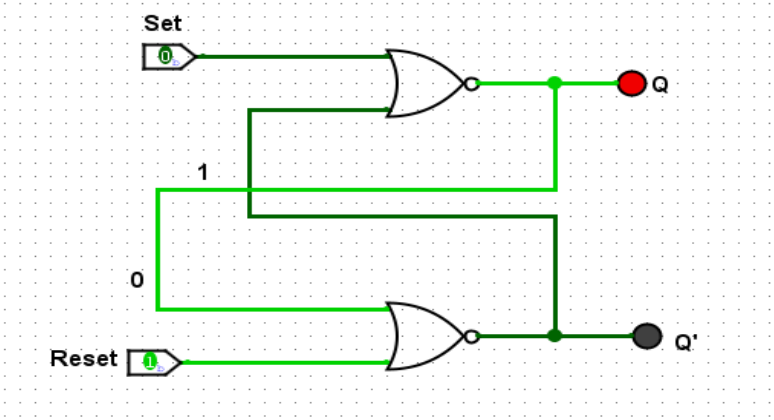
Q6/ R-S Flip Flop using pair of input NOR gates

Set	Reset	Q	Q’
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0



Q7/ Describe in a sentence, the behaviour of the circuit when one of the inputs are 1 (but not both) and why this is useful for digital circuit design.

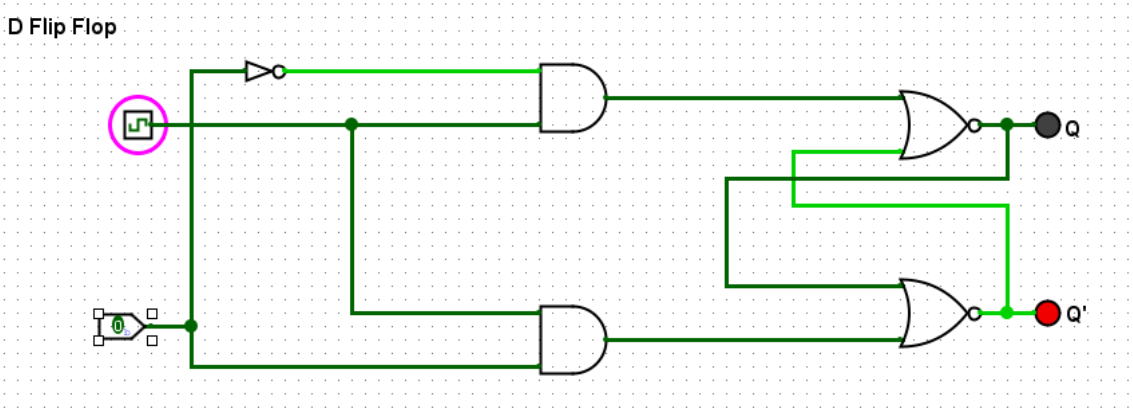
In its initial stage aka reset state (Q=0) , applying a set input of 1 will cause the flip-flop to transition to the set state. As a result , the output Q will become 1. Similarly, when the flip-flop is in the set state (Q=1) , and a reset input of 1 is applied , the flip-flop will shift to the reset state. Consequently , Q will become 0 , and its complementary output Q’ will become 1.
This is useful for digital circuit design because the design can be used to store data by setting and resetting.

Q8/ What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design?

Both times when the inputs were set to 1, the LED bulb did not light up, this is a problem in digital circuit design because the output state is unsure and will take a considerable amount of time to restable.

Q10/ D Flip Flop

Clock	Pin	Q	Q’
0	0	0	1
0	1	0	1
1	1	1	0
1	0	0	1



Q11/ Briefly explain the behaviour of a D Flip Flop and how it is useful for a digital circuit design.

In the D Flip Flop , if the clock is 0 then the D Flip Flop stays on with its previous state ; if the clock is 1 then the state of the clock changes according to that. If the D (pin) is 1 then it would enter its set state and output become 1 and if D is the inverse , output would also be inverse therefore in D Flip Flop , both inputs are never equal to 1.
This D Flip Flop is useful for digital circuit design because it can be used to synchronise the data and store a single bit of memory in digital circuits.

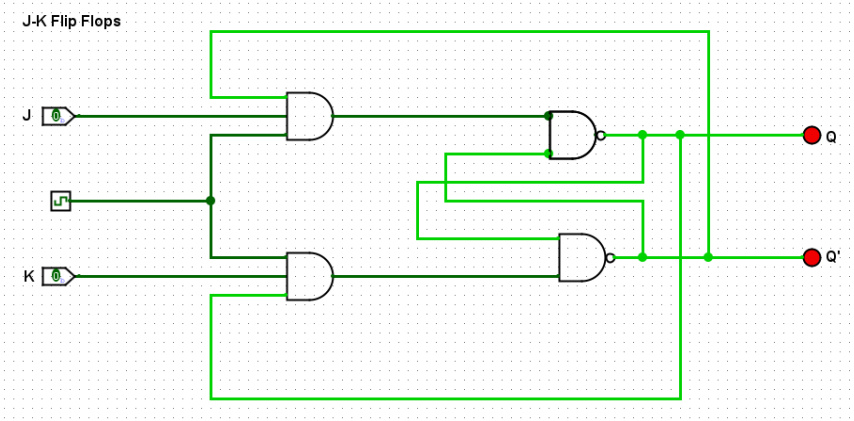
Q12/ What is the role of the clock? How does it impact the changing state of Q and Q’?

The main role of the clock is to synchronise the transfering time of data.It impacts Q and Q’ by making sure the data is transferred correctly.

Q13/ Why is it generally preferred over the R-S Flip Flop?

I believe it is because the D Flip Flop doesn’t come with an unstable state when both inputs become high , as well as it can synchronize the transfer of data compared to the R-S Flip Flop.

Q15/J-K Flip Flops



J	K	Q(clocked)	Q'(clocked)
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0

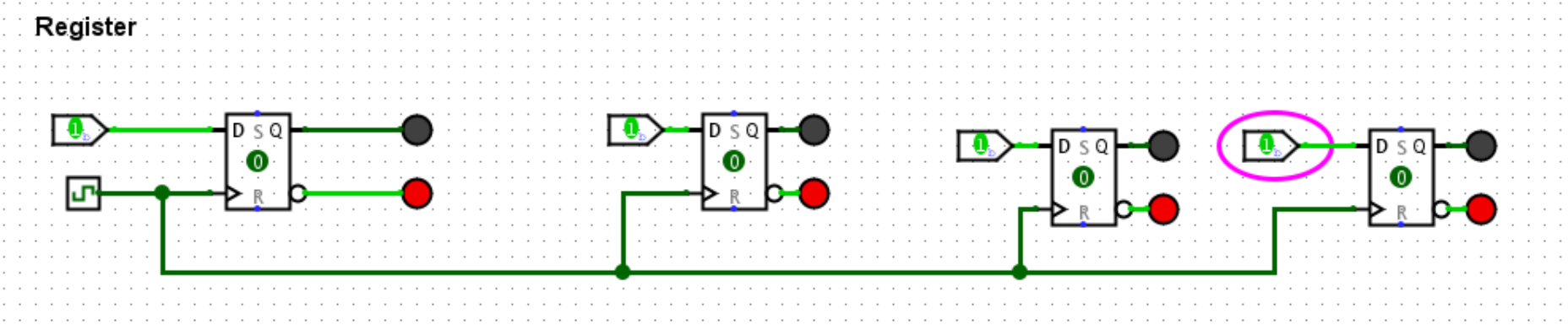
Q16/ How can a J-K Flip Flop be made to behave like a D Flip Flop.

We can make a J-K Flip Flop behave like a D Flip Flop by connecting the J & K inputs together and then add the D input by combining a wire together.

Q17/How can a J-K Flip Flop be made to behave like a toggle (T Flip Flop)?

We can make a J-K Flip Flop toggle like a T Flip Flop by combining both respective inputs together (J&K) and connect them to the output of the J-K Flip Flops.

Q19/ Registers



Ox	Input Binary	Output Binary
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
5	0101	0101
A	1010	1010
B	1011	1011
C	1100	1100
D	1101	1101
E	1101	1101
F	1111	1111