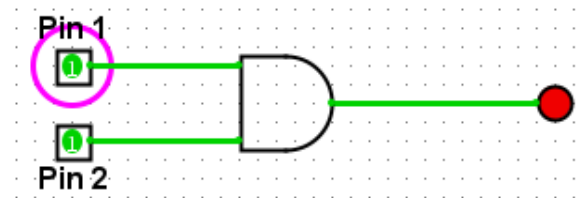
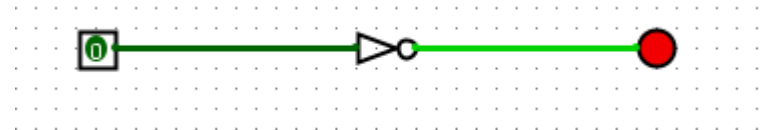


Q5**AND GATE**

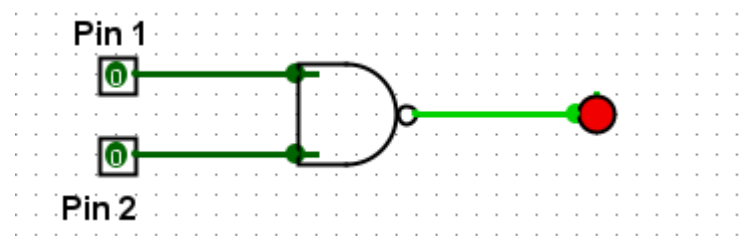
Pin 1	Pin 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

**Q8****OR Gate**

Input	Output
0	1
1	0

**Q10****NAND Gate**

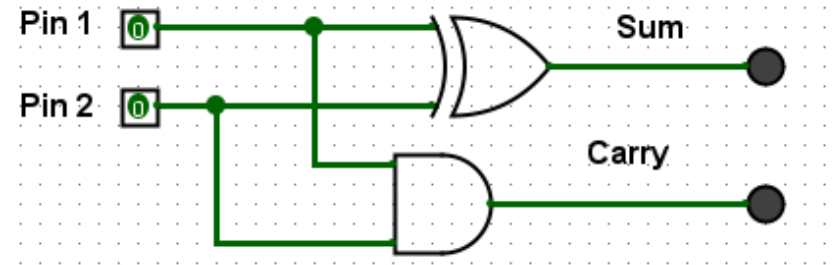
Pin 1	Pin 2	Output
0	0	0
0	1	0
1	0	0



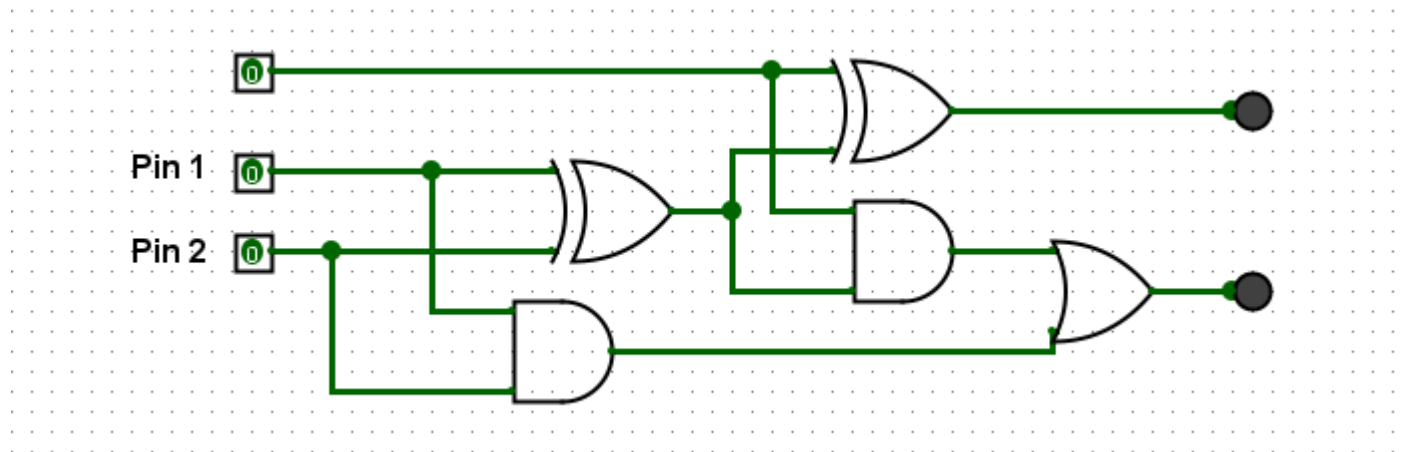
1	1	1
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Q12

Pin 1	Pin 2	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Q15



Input 1	Input 2	Carry (IN)	Sum	Carry (OUT)
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

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