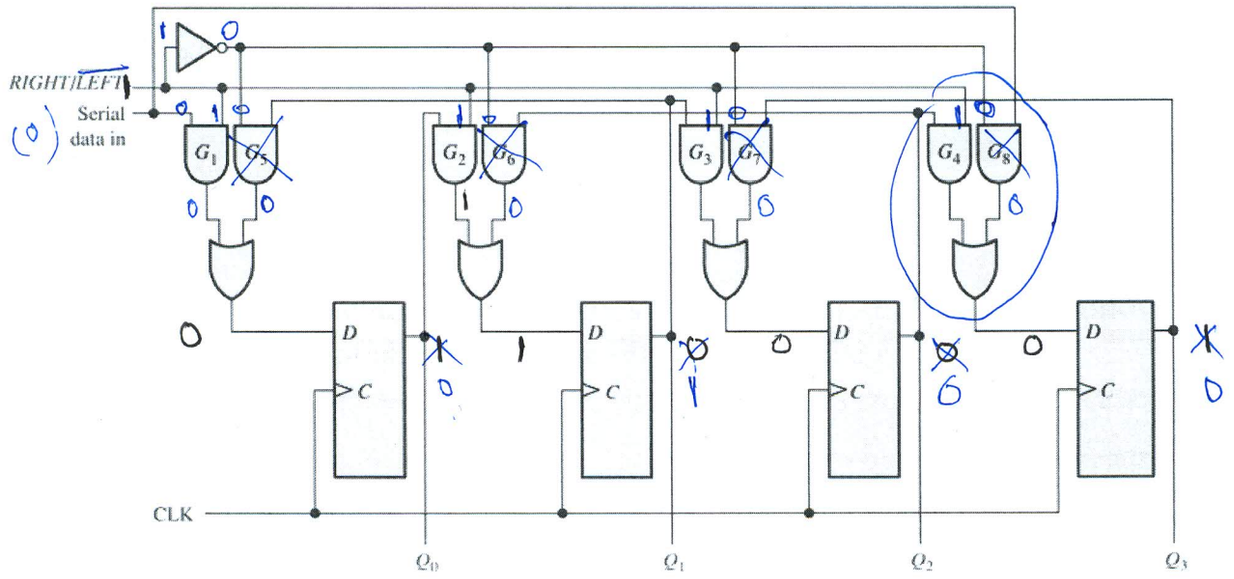
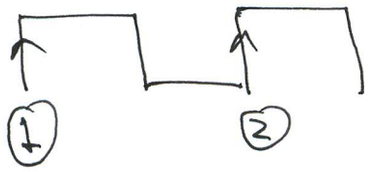
Bidirectional Shift Registers

The parallel in/parallel out register employs both methods. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.

~~RIGHT/LEFT~~ RIGHT/LEFT





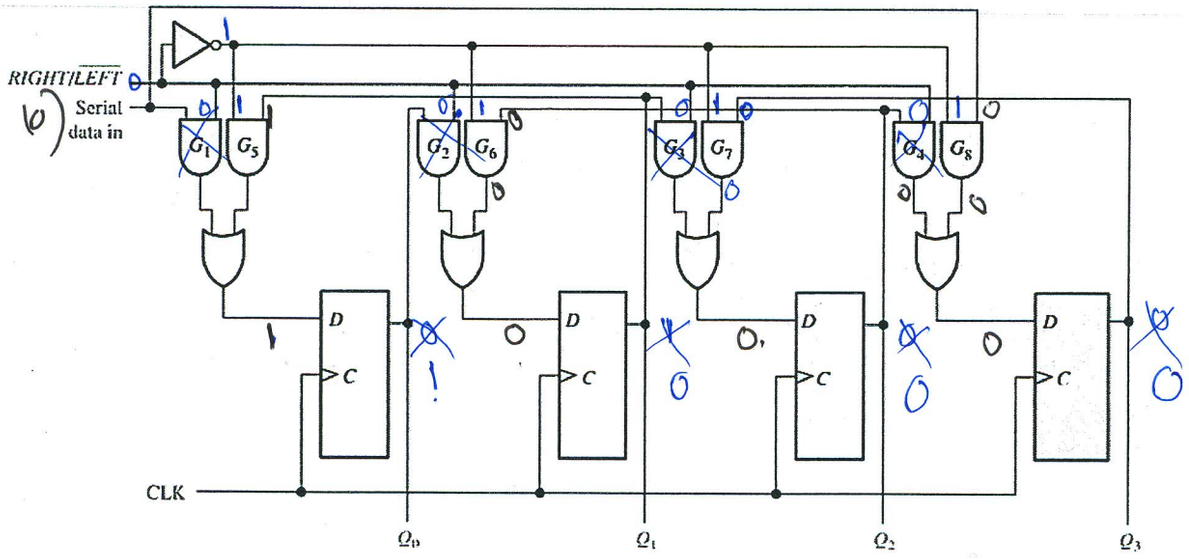
Q_0	Q_1	Q_2	Q_3
1	0	0	1
0	1	0	0
1	0	0	0

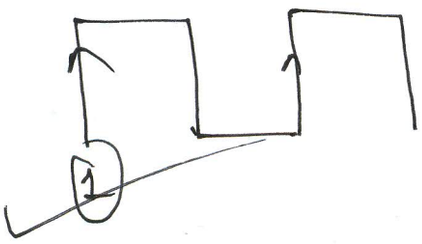
→ (1) shift right

(2) shift Left

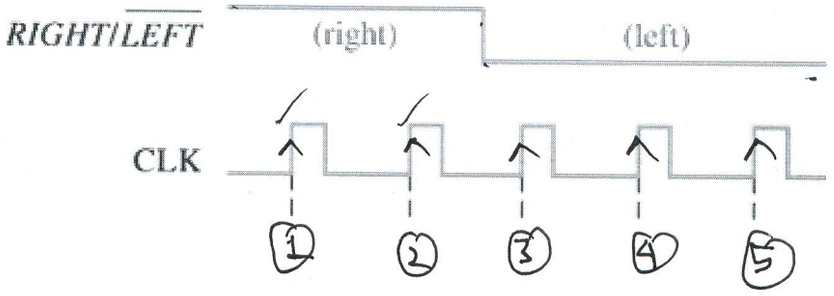
Bidirectional Shift Registers

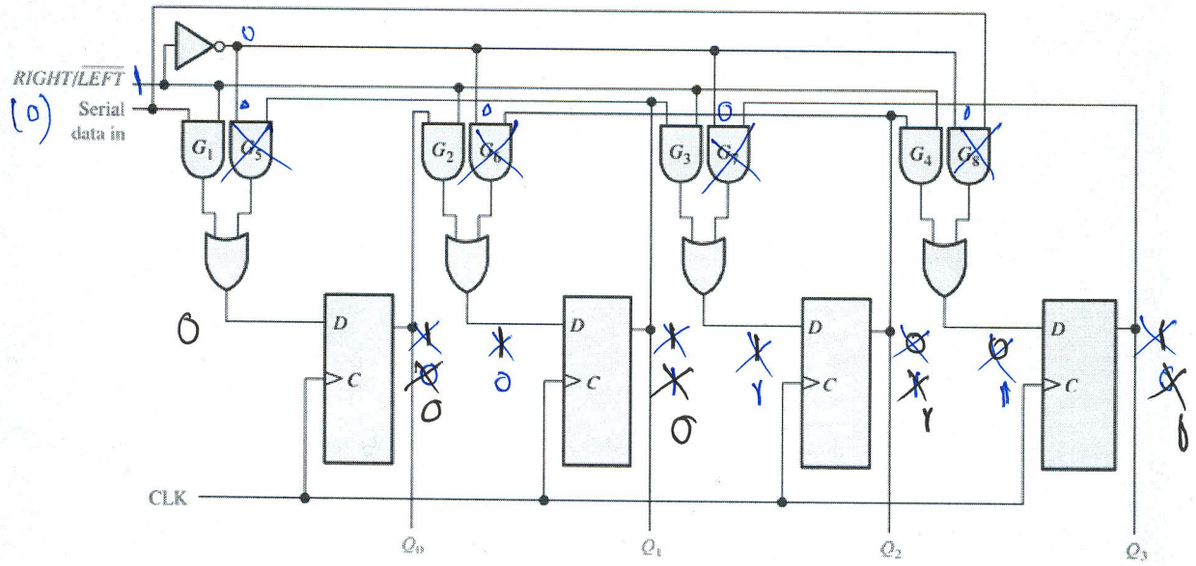
The parallel in/parallel out register employs both methods. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.



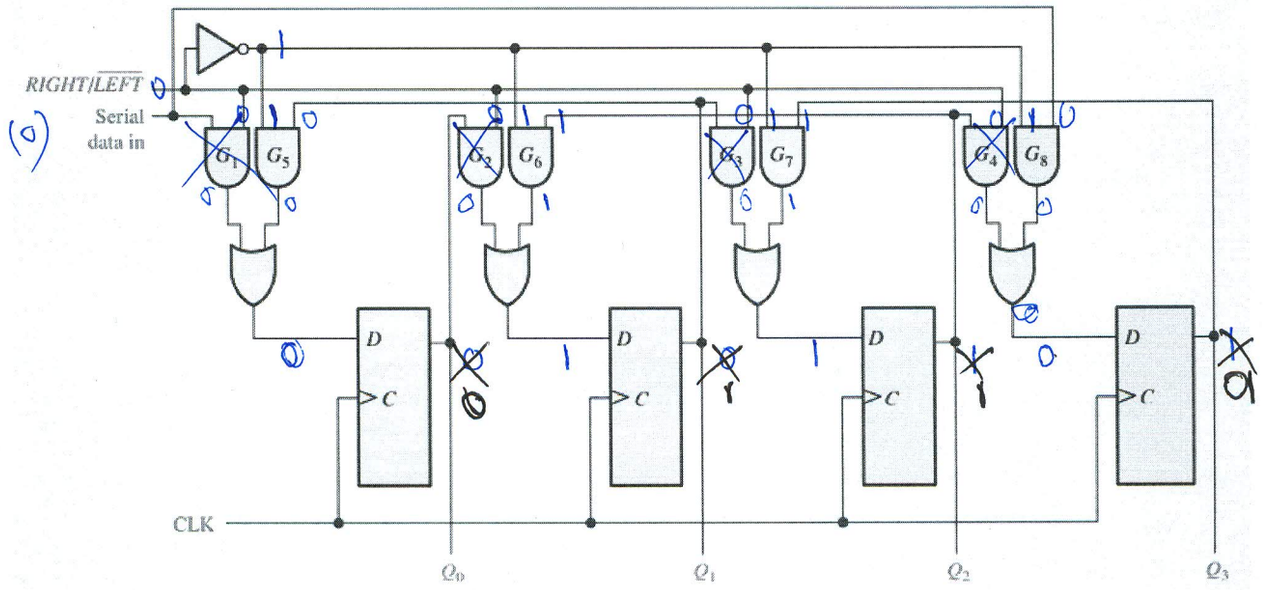


Problem: Determine the state of the shift register after each clock pulse for the given RIGHT/LEFT control input waveform. Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.



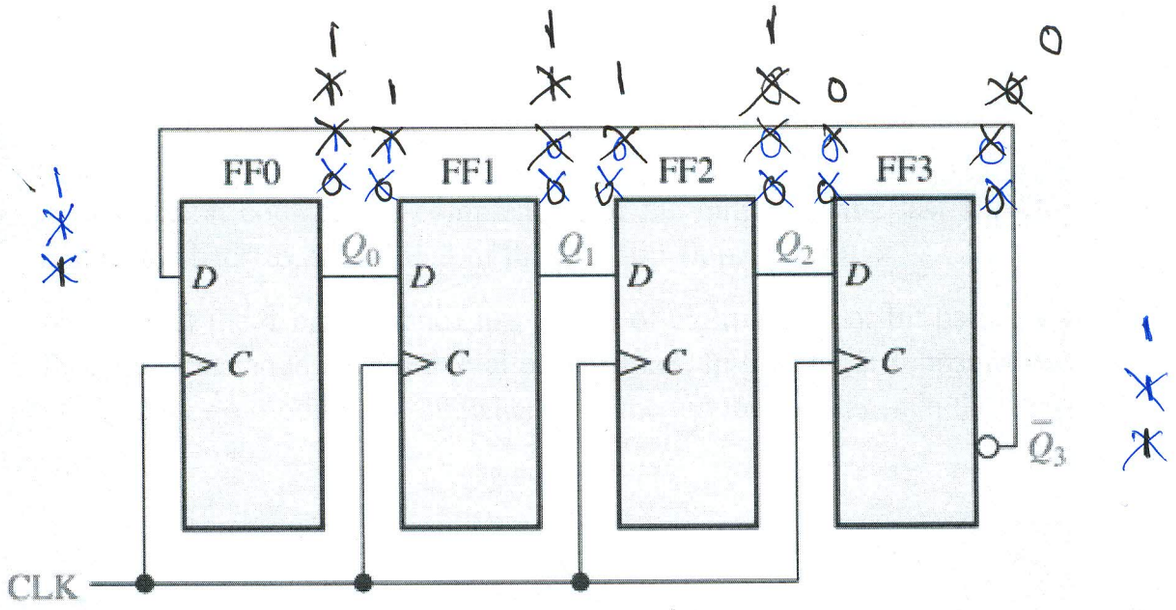


	Q_0	Q_1	Q_2	Q_3
	1	1	0	1
Right (1st)	0	1	1	0
Right (2nd)	0	0	1	1
Left (3rd)	0	1	1	0
Right (4th)	1	1	0	0


RIGHT/LEFT
Serial data in
G_1
G_5
G_2
G_6
G_3
G_7
G_4
G_8
D
C
CLK
Q_0
Q_1
Q_2
Q_3

The Johnson Counter

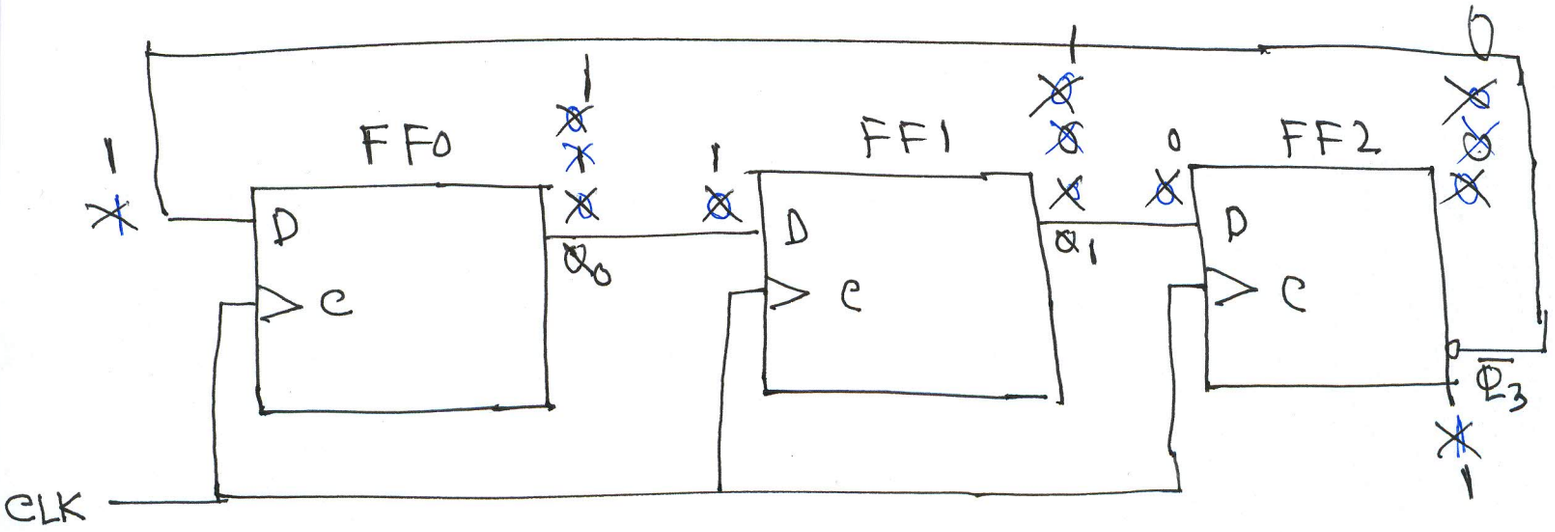
- In a Johnson counter the complement of the output of the last flip-flop is connected back to the D input of the first flip-flop.
- Notice that the 4-bit sequence has a total of eight states, or bit patterns, and that the 5-bit sequence has a total of ten states. In general, a Johnson counter will produce a modulus of 2n, where n is the number of stages in the counter.



	Q_0	Q_1	Q_2	Q_3	
0	0	0	0	0	(0)
1	1	0	0	0	(1)
2	1	1	0	0	(3)
3	1	1	1	0	(7)

010

Write the sequence of states for a 3-bit Johnson counter starting with 000.



	Q_0	Q_1	Q_2
	0	0	0
(1)	1	0	0
(2)	1	1	0
(3)	1	1	1

000 100 110

111 011 001 000