

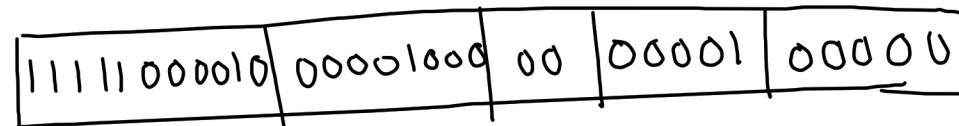
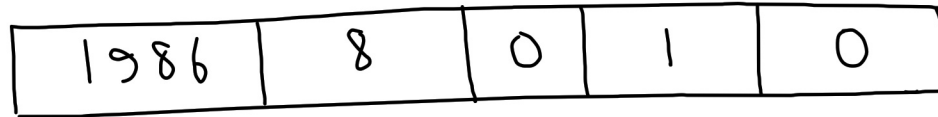
LDUR X0, [X1, #8]



opcode	address	op2	Rn	Rt
11 bits	9 bits	2 bits	5 bits	5 bits

Load/store instructions

- Rn: base register
- address: constant offset from contents of base register (+/- 32 double words)
- Rt: destination (load) or source (store) register number
- Example of D-type instructions are:



← 32 machine code

LDUR X0, [X1, #8]

Assume, $x1 = 30$

$$x1 + 8 = 30 + 8 = 38$$

LE 64 bit

Registers

X0	12
X1	30
X2	
X3	
X4	
X5	
X31	

64 bit

Memory

12
⋮
⋮
⋮

0xFFFFFFFFFFFFFFFF

38 ← $x1 + 8$

37

36

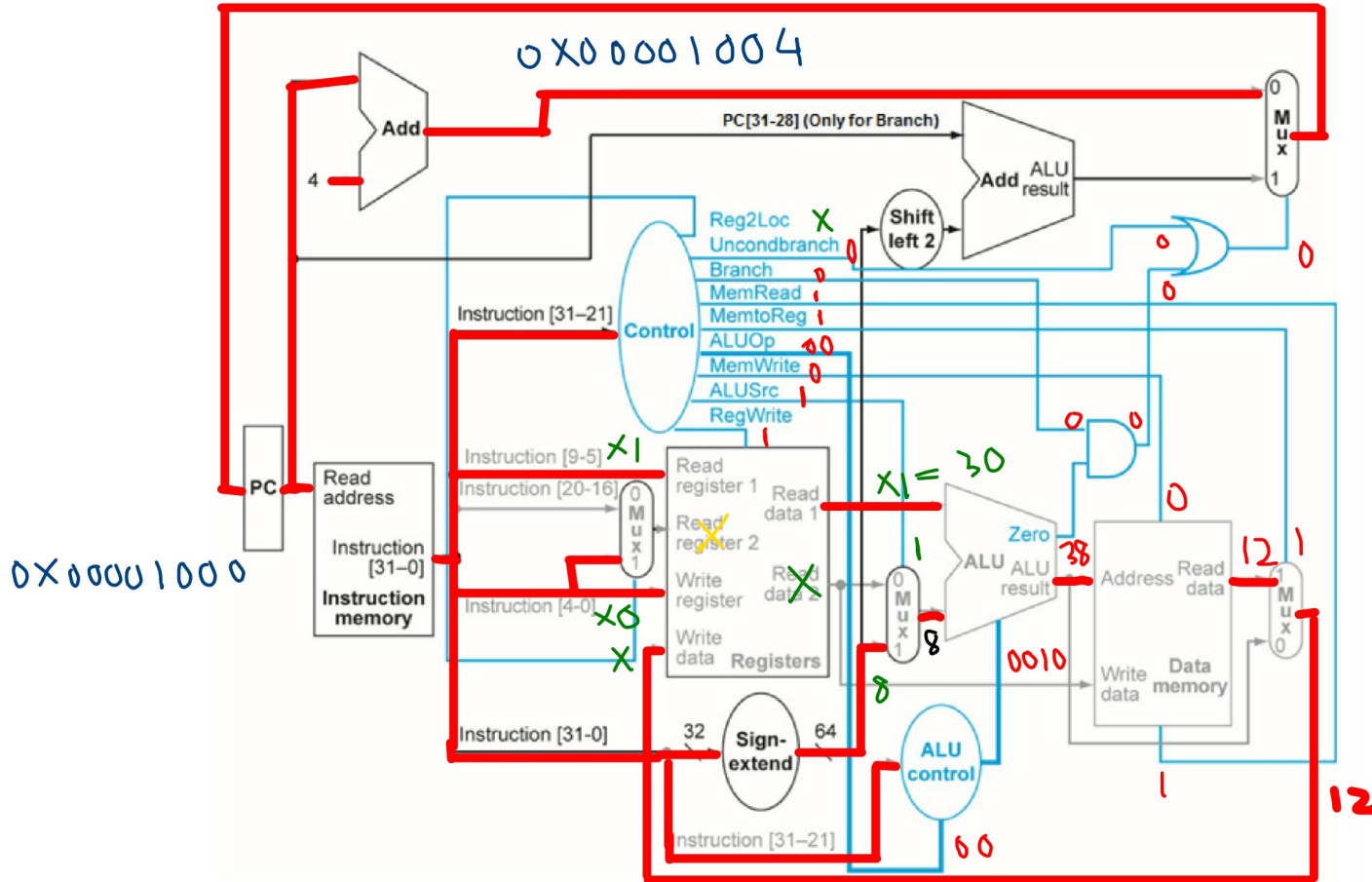
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0X0000000000000000 (0)

Memory Content
(8 bit)

Memory address
(64 bit)

Tracing Datapath: LDUR X0, [X1, #8]



Reg2Loc = X
 Uncondbranch = 0
 Branch = 0
 MemRead = 1
 MemtoReg = 1
 ALUOp = 00
 MemWrite = 0
 ALUSrc = 1
 RegWrite = 1

0x00001000

LDUR X0, [X1, #8]

0x00001004