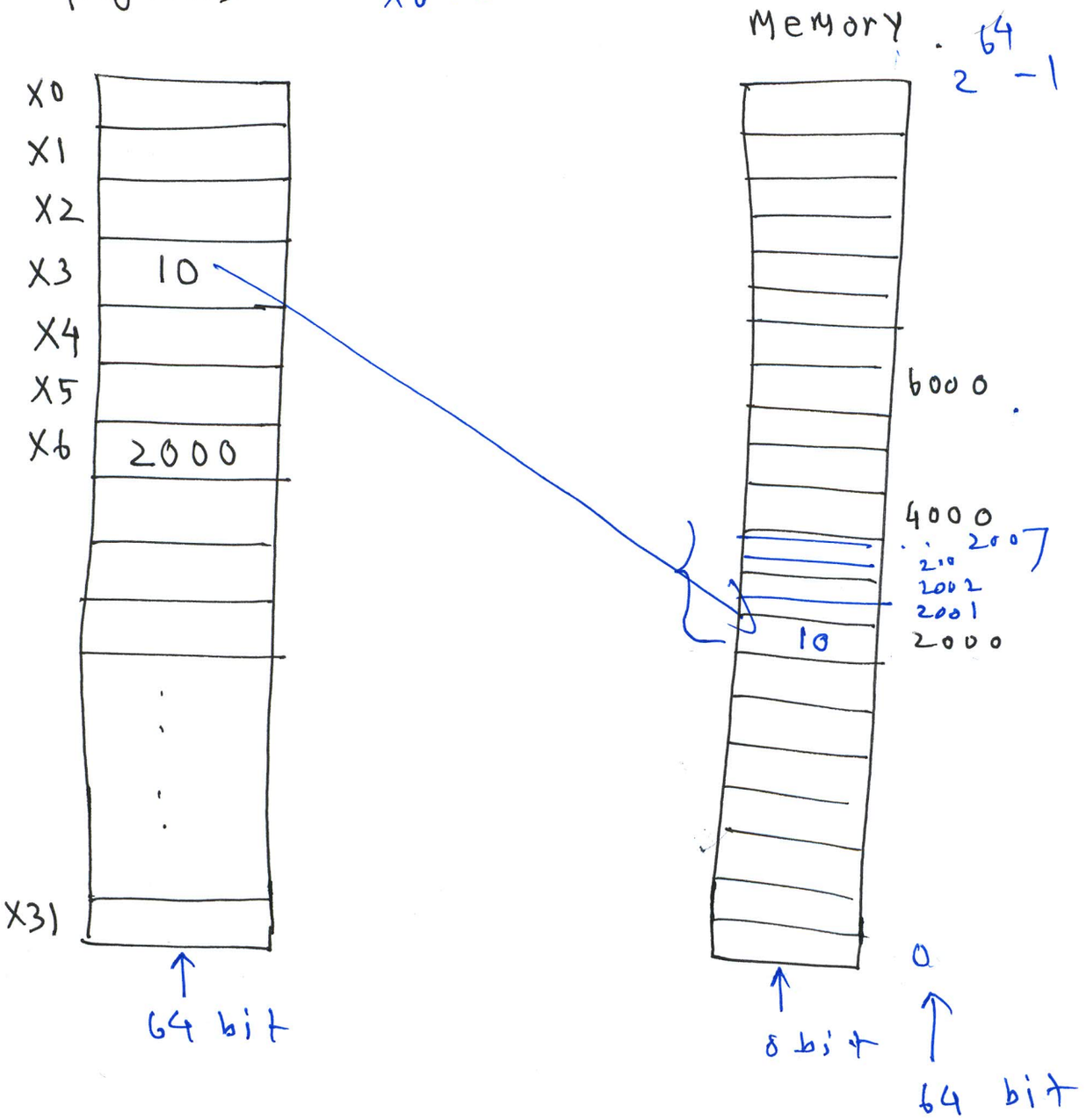
10

* STUR X.3, [X6, #0] → What will happen after executing this instruction, if X3 = 10, X6 = 2000

Register

X6 + 0 = 2000 + 0 = 2000

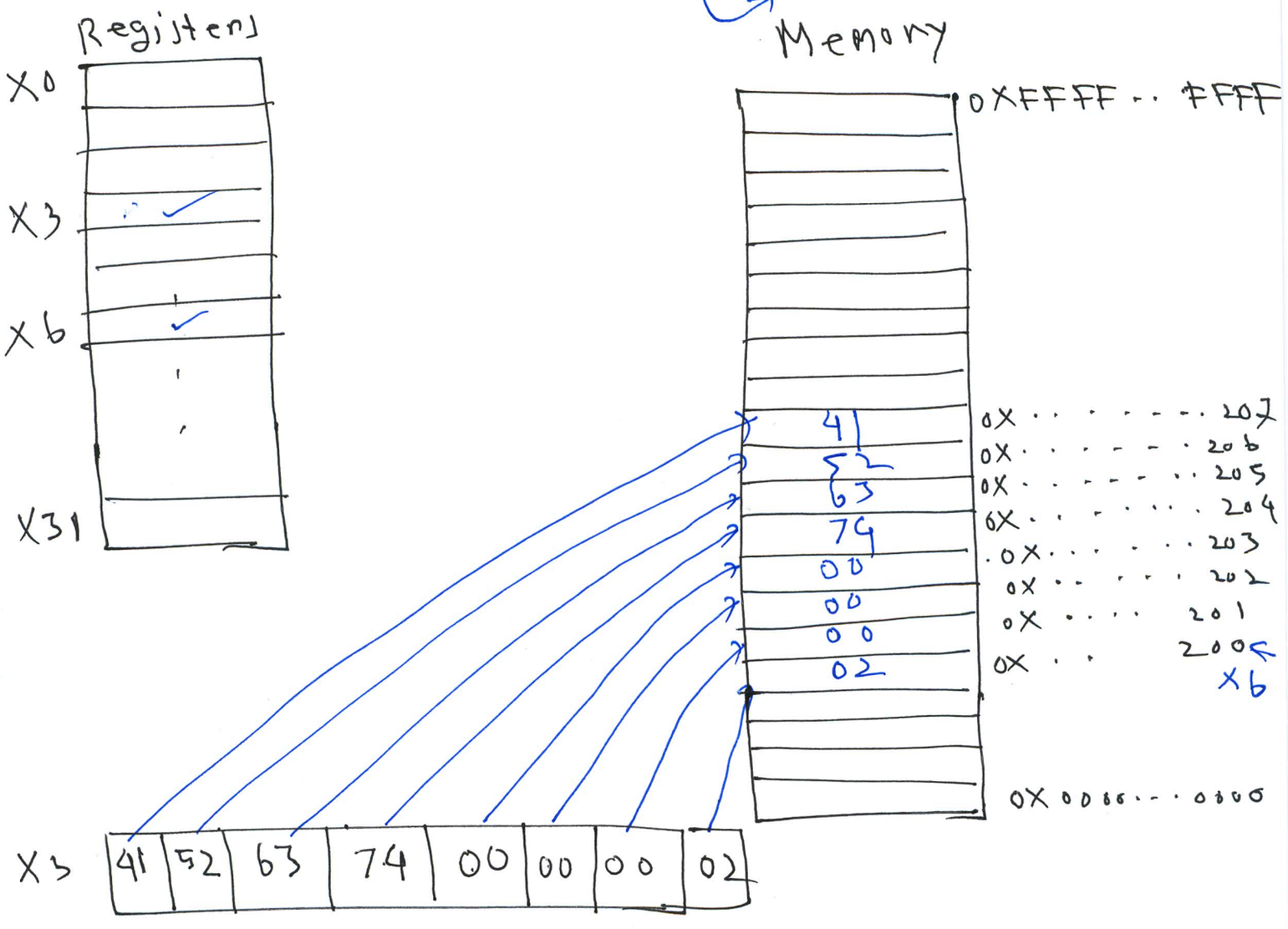


Store Instruction

- The STUR instruction tells the CPU to store (copy) the contents of CPU register to a memory location pointed by destination register.
- Since the CPU registers are 64 – bit (8 byte) wide, we need 8 consecutive memory locations to store the contents of the register.

1 byte = 8 bit.

Problem: Assume that X6 = 0X4000000000000200 and X3 = 0X4152637400000002.What will happen after running the following instruction: STUR X3, [X6, #0].



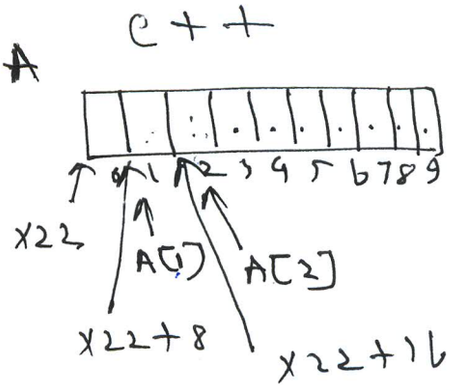
64 bit

Example: Convert the following C++ code to LEGv8 Assembly code. Assume A is an Array of 10 doublewords, variable h is associated with register X21, and base address of the array A is in X22.

A [2] = h + A [1];

X21

C++




```
LDUR  X9, [X22, #8]    // X9 = A[1]
ADD   X9, X9, X21      // X9 = h + A[1]
                       //      A[1]  h
STUR  X9, [X22, #16]   // A[2] = h + A[1]
```

Representing Instructions in the computer (Translating a LEGV8 assembly instruction into a Machine instruction)

Instruction Format: The layout of an instruction is called the instruction format. LEGv8 instructions are 32 bit long.

Instruction	Format	opcode	Rm	shamt	address	op2	Rn	Rd
ADD (add)	R	1112_{ten}	reg	0	n.a.	n.a.	reg	reg
SUB (subtract)	R	1624_{ten}	reg	0	n.a.	n.a.	reg	reg
ADDI (add immediate)	I	580_{ten}	reg	n.a.	constant	n.a.	reg	n.a.
SUBI (sub immediate)	I	836_{ten}	reg	n.a.	constant	n.a.	reg	n.a.
LDUR (load word)	D	1986_{ten}	reg	n.a.	address	0	reg	n.a.
STUR (store word)	D	1984_{ten}	reg	n.a.	address	0	reg	n.a.

ADDITON
SUBTRACTION

C = A + B
X9 X20 X21

LEGV8 R-Format Instructions:

opcode	Rm	shamt	Rn	Rd
11 bits	5 bits	6 bits	5 bits	5 bits

ADD X9, X20, X21
opcode 1112 — Rd — Rn — Rm.

opcode : Operation code

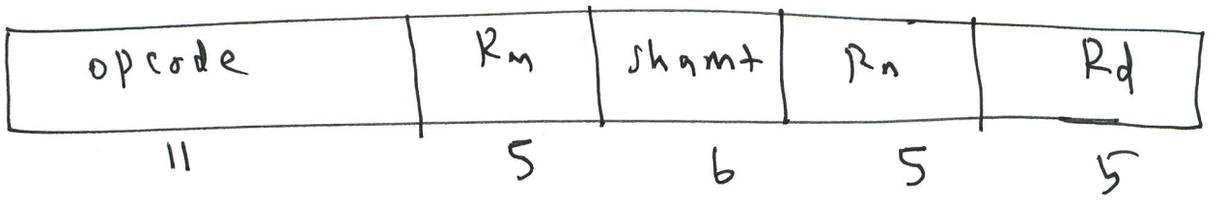
Rm : Operand 2

shamt : shift amount (0)

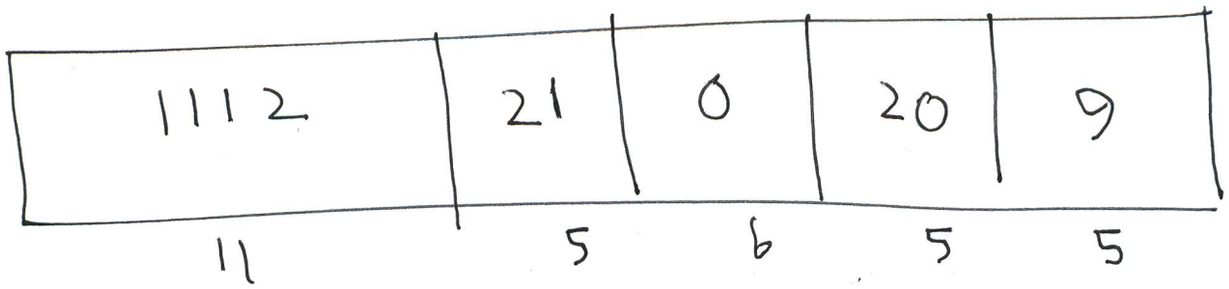
Rn : Operand 1

Rd : Destination Registen.

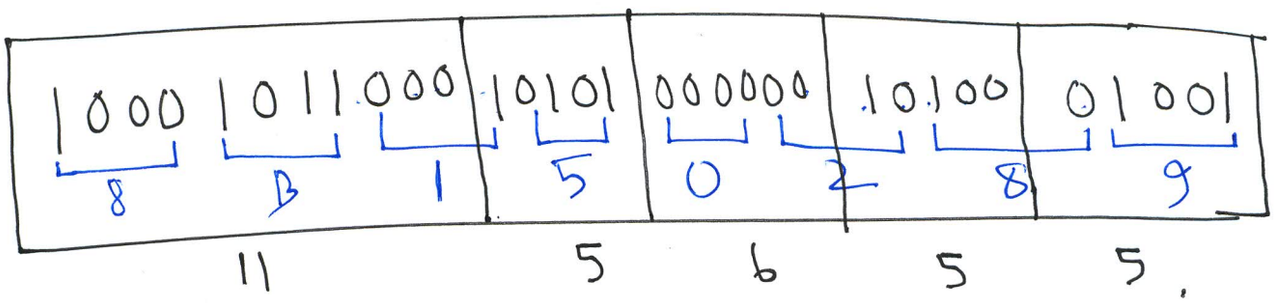
Translate the following LEGV8 assembly instruction into a machine instruction: **ADD X9, X20, X21**



Decimal →



Binary



Hex value: $8B150289_{16}$

1986 → 11111000010

LDUR

STUR .

LEGv8 D-Format Instructions:

opcode	address	op2	Rn	Rt
11 bits	9 bits	2 bits	5 bits	5 bits
		0		

Rn : Base Register

address: Constant offset

Rt : destination (load) or source (store) register number

LDUR X9, [X10, #8] ← offset/address

LDUR → 1986; X9 → (Rt) destination register; X10 → Rn Base Register

Translate the following LEGV8 assembly instruction into a machine instruction:

LDUR X9, [X10, #8]

Decimal

1986	8	0	10	9
11	9	2	5	5

Binary

11111000010	000001000	00	01010	01001

F 8 4 0 8 1 4 9

Hex value : F840 8149$_{16}$