

74. USB High-Speed Module (HS-USB)

R-Car H3	R-Car D3
R-Car M3-W	R-Car M3-N
R-Car V3M	
R-Car V3H	

74.1 Overview

This module is a USB controller provided with the function controller function, and high-speed transfer and full-speed transfer are available. Provided with an on-chip USB transceiver, this module also supports all transfer types defined by the USB Specification.

This module can use up to twelve pipes when the function controller is selected. Furthermore, for pipes 1 to F, arbitrary endpoint numbers can be allocated according to peripheral devices to be communicated and user systems.

74.1.1 Features

- (1) On-chip USB transceiver
- (2) Achieves space-saving mount with less external elements

- On-chip D+ pull-up resistor (function operation mode)
- On-chip D+/D- terminating resistors (high-speed operation mode)
- On-chip D+/D- output resistors (full-speed operation mode)

(3) All Types of USB Transfers Supported

- Control transfer
- Bulk transfer
- Interrupt transfer (except for high bandwidth)
- Isochronous transfer (except for high bandwidth)

(4) Dedicated DMA interface

- On-chip 4-channel DMA interface

(5) Pipe configuration

- Up to sixteen pipes are selectable (including the default control pipe)
- Programmable pipe configuration
- Arbitrary endpoint numbers can be allocated to pipes 1 to F.
- Settable transfer conditions for each pipe are as follows:

Pipe 0: A pipe only for control transfer with a 64-byte (fixed) single buffer

Pipes 1 and 2: Bulk transfers/isochronous transfer, continuous transfer mode, programmable buffer size (up to 2-Kbytes: double buffer can be specified)

Pipes 3 to 5 and B to F: Bulk transfer, continuous transfer mode, programmable buffer size (up to 2-Kbytes: double buffer can be specified)

Pipes 6 to 8: Interrupt transfer, 64-byte fixed single buffer

Pipes 9: Bulk transfer, programmable buffer size (up to 512-bytes: double buffer can be specified)

Pipes A: Bulk transfer, continuous transfer mode, programmable buffer size (up to 64-bytes: double buffer can be specified)/Interrupt transfer, 64-byte fixed single buffer

74.1.2 External Pins

Table 74.1 lists the input and output pins of the USB.

Table 74.1 Pin Configuration of USB

Name	Pin Name	I/O	Description	Third Generation R-Car Series Products						
				R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
Clock input for USB	USB_EXTAL	I	Used as an external clock input pin(50MHz)	✓	✓	—	—	—	✓	—
	USB_XTAL	O	Outputs amplified negative feedback of EXTAL (50MHz)	✓	✓	—	—	—	✓	—
USB D+ data	[R-Car H3/M3-W/M3-N] DPn/USB2_CH3_D P [R-Car D3] USB_DP [R-Car E3] USB0_DP0	I/O	D+ Input/output of the on-chip transceiver Connect this pin to the D+ pin of the USB bus.	✓	✓	—	—	✓	✓	✓
USB D- data	[R-Car H3/M3-W/M3-N] DMn/USB2_CH3_D M [R-Car D3] USB_DM [R-Car E3] USB0_DM0	I/O	D- Input/output of the on-chip transceiver Connect this pin to the D- pin of the USB bus.	✓	✓	—	—	✓	✓	✓
USB Identification	IDn/USB2_CH3_ID	I/O	Connect to the pin on the Micro connectors that is used to differentiate a Micro-A plug from a Micro-B plug.	✓	✓	—	—	✓	—	—
USB VBUS	VBUSt/USB2_CH3_VBUS	I/O	Connect to USB VBUS with external $30k\Omega \pm 1\%$ series resistor.	✓	✓	—	—	✓	—	—
USB external reference resistor	[R-Car H3/M3-W/M3-N] TXRTUNE _n [R-Car D3] USB_RREF [R-Car E3] USB0_RREF	I/O	[R-Car H3/M3-W/M3-N] Connect to external $200\Omega \pm 1\%$ resistor. [R-Car D3/E3] Connect to external $1.8k\Omega \pm 1\%$ resistor.	✓	✓	—	—	✓	✓	✓

- Notes:
1. The VBUS of USB connector must not connect directly to VBUSt/USB2_CH3_VBUS pin.
 2. VBUSt pin must be isolated by an external $30k\Omega \pm 1\%$ series resistor.
 3. Suffix "n" of pin names is 0 or 2 for H3, 0 for M3-W/D3/M3-N/E3.
 4. IDn and VBUSt pins are not implemented R-Car D3 and E3

74.1.3 Register Configuration

Table 74.2 HS-USB Base Address

HS-USB Base Address	Base Address	R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
Channel 0	H'E659 0000	√	√	—	—	√	√	√
Channel 3	H'E659 C000	√	—	—	—	—	—	—

Table 74.3 lists the registers used in this module. Table 74.4 lists the register states in each processing mode.

Table 74.3 Register Configuration

Register Name	Abbreviation	R/W	Address Offset	Access Size	Third Generation R-Car Series Products						
					R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
System configuration control register	SYSCFG	R/W	H'000	16	√	√	—	—	√	√	√
CPU bus wait register	BUSWAIT	R/W	H'002	16	√	√	—	—	√	√	√
System configuration status register	SYSSTS	R	H'004	16	√	√	—	—	√	√	√
Device state control register	DVSTCTR	R/W	H'008	16	√	√	—	—	√	√	√
Test mode register	TESTMODE	R/W	H'00C	16	√	√	—	—	√	√	√
CFIFO port register	CFIFO	R/W	H'014	32	√	√	—	—	√	√	√
CFIFO port select register	CFIFOSEL	R/W	H'020	16	√	√	—	—	√	√	√
CFIFO port control register	CFIFOCTR	R/W	H'022	16	√	√	—	—	√	√	√
D0FIFO port select register	D0FIFOSEL	R/W	H'028	16	√	√	—	—	√	√	√
D0FIFO port control register	D0FIFOCTR	R/W	H'02A	16	√	√	—	—	√	√	√
D1FIFO port select register	D1FIFOSEL	R/W	H'02C	16	√	√	—	—	√	√	√
D1FIFO port control register	D1FIFOCTR	R/W	H'02E	16	√	√	—	—	√	√	√
Interrupt enable register 0	INTENB0	R/W	H'030	16	√	√	—	—	√	√	√
BRDY interrupt enable register	BRDYENB	R/W	H'036	16	√	√	—	—	√	√	√
NRDY interrupt enable register	NRDYENB	R/W	H'038	16	√	√	—	—	√	√	√
BEMP interrupt enable register	BEMPENB	R/W	H'03A	16	√	√	—	—	√	√	√
SOF output configuration register	SOFCFG	R/W	H'03C	16	√	√	—	—	√	√	√
Interrupt status register 0	INTSTS0	R/W	H'040	16	√	√	—	—	√	√	√
BRDY interrupt status register	BRDYSTS	R/W	H'046	16	√	√	—	—	√	√	√
NRDY interrupt status register	NRDYSTS	R/W	H'048	16	√	√	—	—	√	√	√
BEMP interrupt status register	BEMPSTS	R/W	H'04A	16	√	√	—	—	√	√	√
Frame number register	FRMNUM	R/W	H'04C	16	√	√	—	—	√	√	√
μ frame number register	UFRMNUM	R/W	H'04E	16	√	√	—	—	√	√	√
USB address register	USBADDR	R	H'050	16	√	√	—	—	√	√	√

Abbreviation	Power-On Reset	Module Standby
D2FIFOCTR	Initialized	Retained
D3FIFOSEL	Initialized	Retained
D3FIFOCTR	Initialized	Retained
LPSTS	Initialized	Retained
BCCTRL	Initialized	Retained
UGCTRL* ¹	Initialized	Retained
UGCTRL2	Initialized	Retained
UGSTS* ¹	Initialized	Retained
USB20_CLKSET0* ²	Initialized	Retained

Notes: 1. UGCTRL and UGSTS registers are implemented R-Car D3 and E3
 2. USB20_CLKSET0 is only in Channel 0

74.1.4 Connected Module

Table 74.5 The connected modules to the HS-USB

Module name	Connected module name	Function of connected module
HS-USB	AP-System Core	Access the Register
	CPG	Output Clocks
	PFC	Select External pins
	Module Standby, Software Reset	Control to stop clocks, Execute software reset
	INTC, INTC-AP, INTC-RT	Control to interrupt
	EHCI/OHCI	USB2.0 Host (EHCI/OHCI)

74.2 Register Description

[Legend for the Register Description]

A bit assignment figure is shown for each register. The initial value and R/W attribute are indicated for each bit.

Bit: Bit number or bit range

Bit Name: Bit name or field name

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

RW0C: Readable/writable. The bit is initialized when 0 is written. Writing 1 is ignored.

RW1C: Readable/writable. The bit is initialized when 1 is written. Writing 0 is ignored.

R: Read-only. The write value should always be 0. (If there is a direction on a read or write value in the Description column, set the bit as directed.)

74.2.1 System Configuration Control Register (SYSCFG)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

SYSCFG enables or disables high-speed operation, controls the DPn/USB_DP pin, and enables or disables the operation of this module.

Note: "n" of pin names is 0 or 3 for H3, 0 for M3-W/D3/M3-N/E3

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HSE	—	—	DPRPU	—	—	—	USBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	HSE	0	R/W	High-Speed Operation Enable 0: High-speed operation is disabled. Full-speed operation only 1: High-speed operation is enabled. (This module detects the transmission rate.) When HSE is 0, this module performs full-speed operation. When HSE is 1, this module executes the reset handshake protocol, and according to the result, this module automatically performs high-speed or full-speed operation. Change this bit while the DPRPU bit is 0.
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DPRPU	0	R/W	D+ Line Resistance Control Enables or disables pull-up of the D+ line. 0: Pull-up is disabled. 1: Pull-up is enabled. When this bit is set to 1, this module pulls up the D+ line at 3.3V, and informs the USB host of ATTACH. Clearing this bit to 0 cancels the pull-up of the D+ line, and informs the USB host of DETACH. Set this bit to 1 before using this module. Set this bit to 0 when this module is not used. (when EHCI/OHCI Host function is used or USB is not used).
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	USBE	0	R/W	USB Module Operation Enable Enables or disables the USB module operation. 0: The USB module operation is disabled. 1: The USB module operation is enabled. Tables 74.6 list the registers and bit names initialized when this bit is cleared to 0.

74.2.2 CPU Bus Wait Register (BUSTWAIT)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

BUSTWAIT specifies the number of access waits from the CPU to this module.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSTWAIT[3:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	BUSTWAIT[3:0]	1111	R/W	CPU Bus Wait Specify the number of access waits to this module. 0000: 0 waits (2 access cycles) 0001: 1 wait (3 access cycles) 0010 to 1110: 2 to 14 waits (4 to 16 access cycles) 1111: 15 waits (17 access cycles) initial value The following restriction is provided for access cycles to the registers of addresses beginning with H'04 of this controller. Restriction for wait: The cycle of continuous accesses to the registers of this controller must be 80 ns or more. To satisfy this restriction, control waits using the frequency of system clock S3D2φ. Choose the best value within the initial value of 17 clock cycles (maximum). This setting is the same as the waits in accesses to the FIFO port register. The maximum speed of accesses to the FIFO port is as follows: MBW = B'10 (32-bit width): Max. 48 Mbytes/s MBW = B'01 (16-bit width): Max. 24 Mbytes/s MBW = B'00 (8-bit width) : Max. 12 Mbytes/s

74.2.3 System Configuration Status Register (SYSSTS)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

SYSSTS monitors the USB data bus line status (D+ and D- lines).

This register is initialized by a power-on reset or a USB reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LNST[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	LNST[1:0]	Undefined*	R	USB Data Line Status Monitor Indicate the USB data bus line (D+ and D- lines) status. Table 74.7 shows the USB data bus line status. Read these bits after the attach processing (DPRPU = 1).

Note: * These bits depend on the state of the DPn/USB_DP and DMn/USB_DM pins.

"n" of pin name is 0 or 3 for H3, 0 for M3-W/D3/M3-N/E3

Table 74.7 USB Data Bus Line Status

LNST[1]	LNST[0]	Full-Speed Operation	High-Speed Operation	Chirp Operation
0	0	SE0	Squelch	Squelch
0	1	J-State	UnSquelch	Chirp J
1	0	K-State	Invalid	Chirp K
1	1	SE1	Invalid	Invalid

Legend:

Chirp: The reset handshake protocol (RHSP) is being executed with high-speed operation is enabled (HSE = 1 in SYSCFG).

Squelch: SE0 or idle state

UnSquelch: High-speed J-State or high-speed K-State

Chirp J: Chirp J-State

Chirp K: Chirp K-State

Invalid: Invalid

74.2.4 Device State Control Register (DVSTCTR)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

DVSTCTR controls and monitors the USB data bus state.

This register is initialized by a power-on reset. The WKUP bit is initialized and the RESUME bit becomes undefined by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	WKUP	—	—	—	—	—	—	—	RHST[2:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	WKUP	0	R/W	Wakeup Output Enables or disables the remote wakeup (resume signal output) to the USB bus. 0: The remote wakeup signal is not output. 1: The remote wakeup signal is output. This module controls the remote wakeup signal output time. When this bit is set to 1, this module outputs 10 ms K-State and then clears this bit. The USB Specification requires the USB bus idle state to be maintained for at least 5 ms before transmitting the remote wakeup signal. For this reason, this module outputs K-State after waiting for 2 ms even if 1 is written in this bit immediately after the suspended state is detected. Write 1 in this bit only when the device is in the suspended state (DVSQ = 1xx in INTSTS0) and remote wakeup is enabled by the USB host. When setting this bit to 1, do not stop the internal clock even in the suspended state (Write 1 in this bit with SUSPM set to 1).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	RHST[2:0]	000	R	Reset Handshake Indicate the reset handshake state. 000: Transmission rate is undefined. 100: The reset handshake processing is in progress. 010: Full-speed connection 011: High-speed connection When this module detects a USB bus reset with the HSE bit set to 1 for the port, these bits become B'100. After that, when this module outputs ChirpK and detects ChirpJK from the USB host three times, these bits become B'011. Unless high-speed mode is fixed within 2.5 ms after the ChirpK output, these bits become B'010. When this module detects a USB bus reset with the HSE bit set to 0 for the port, these bits become B'010. When the RHST bits are fixed to B'010 or B'011 after this module detected a USB bus reset, the DVST interrupt occurs.

74.2.5 Test Mode Register (TESTMODE)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
✓	✓	—	—	✓	✓	✓

TESTMODE controls the USB test signal output in high-speed operation mode.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	UTST[3:0]	0000	R/W	Test Mode Table 74.8 shows the test mode operation of this module. Control the USB test signal output in high-speed operation mode. These bits are valid only in high-speed operation mode. Use this test mode when the RHST bits in DVSTCTR are B'011. After the test with these bits, cancel this test mode by a power-on reset. Set these bits according to the SetFeature request from the USB host during high-speed communication. While these bits are B'0001 to B'0100, this module does not enter the suspended state.

Table 74.8 Test Mode Operation

Test Mode	UTST Bits Setting
Normal operation	B'0000
Test_J	B'0001
Test_K	B'0010
Test_SE0_NAK	B'0011
Test_Packet	B'0100
Test_Force_Enable	—
Reserved	B'0101 to B'0111

74.2.6 CFIFO Port Register (CFIFO)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

CFIFO is a port register to read data from or write data to the FIFO buffer memory.

Each FIFO port consists of this register (CFIFO) for data read/write from/to the FIFO buffer memory, the select registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL) to select pipes to be allocated to a FIFO port, and the control registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR).

Each FIFO port provides the following features.

- Make accesses to the FIFO buffer for DCP through the CFIFO port.
- Make accesses to the FIFO buffer with DMA transfers through the DMAC module for USB high-speed only.
- When using a function specific to FIFO ports (DMA transfer function, etc.), the pipe number (selected pipe) specified by the CURPIPE bits cannot be changed.
- Register groups of a FIFO port do not affect other FIFO ports.
- Do not allocate the same pipe number to different FIFO ports.
- There are two FIFO buffer states where the access mastership is on the CPU side and on the SIE side. When the FIFO buffer access mastership is on the SIE side, the CPU cannot make an access to the FIFO buffer.

This register is initialized by a power-on reset.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FIFOPORT[31:16]																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W															
FIFOPORT[15:0]																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W															

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FIFOPORT [31:0]	All 0	R/W	<p>FIFO Port</p> <p>Read receive data from the FIFO buffer or write transmit data to the FIFO buffer using these bits.</p> <p>Access to this register is enabled only when the FRDY bit in each control register (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR) is set to 1.</p> <p>Valid bits in this register vary with the value of the MBW bits. Table 74.9 shows the valid bits in this register.</p>

Table 74.9 Operation of This Register when Accessed

Access Size	Bits 31 to 24	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0
32 bits	N + 3 address	N + 2 address	N + 1 address	N + 0 address
16 bits	Write: Invalid, Read: Prohibited*		N + 1 address	N + 0 address
8 bits	Write: Invalid, Read: Prohibited*			N + 0 address

Note: * Reading an invalid register with word access or byte access is prohibited.

74.2.7 FIFO Port Select Registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL, D3FIFOSEL)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL select pipes to be allocated to FIFO ports and control accesses to each FIFO port.

Do not specify the same pipe number for the CURPIPE bits in CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL. When the CURPIPE bits in D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL are set to B'000, no pipe is specified.

Do not change any pipe number when DMA transfer is enabled.

This register is initialized by a power-on reset.

(1) CFIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	—	—	MBW[1:0]	—	—	—	—	—	ISEL	—	CURPIPE[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R/W: R/W R/W R R R/W R/W R R R R/W R R/W R/W R/W R/W R/W R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	<p>Read Count Mode Specifies read mode of the DTLN bits in CFIFOCTR. 0: Clears the DTLN bits after reading all receive data in the CFIFO (or after reading receive data of one side of the double buffer). 1: Counts down the DTLN bits at each reading of CFIFO receive data.</p>
14	REW	0	R/W*	<p>Buffer Pointer Rewind Specifies whether to rewind the buffer pointer or not. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.) Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1. To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.</p>
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

74.2.8 FIFO Port Control Registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR, D3FIFOCTR)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

CFIFOCTR and D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR specify buffer memory write end and CPU buffer clear, as well as indicate whether the FIFO port is accessible or not. These registers correspond to each FIFO port.

These registers are initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVAL	BCLR	FRDY	—												DTLN[11:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15	BVAL	0	R/W ^{*1}	<p>Buffer Memory Enable Flag</p> <p>This flag is set to 1 upon completion of data write in the FIFO buffer of the CPU of the pipe selected by the CURPIPE bits.</p> <p>0: Invalid</p> <p>1: Write end</p> <p>When the selected pipe is in the transmit direction, set this bit to 1 in the following cases. This module sets the FIFO buffer of the CPU to the SIE side to enable data transmission.</p> <p>To send a short packet, set this bit to 1 upon completion of data write.</p> <p>To send a Zero-Length packet, set this bit to 1 before writing data to the FIFO buffer.</p> <p>For pipes of continuous transfer mode, set this bit to 1 after writing data that is a positive integer multiple of MaxPacketSize and less than the BufferSize value.</p> <p>When data with the size specified by MaxPacketSize is written to a pipe of continuous transfer mode, this module writes 1 in this bit and sets the FIFO buffer of the CPU to the SIE side to enable data transmission.</p> <p>Set this bit to 1 when this module shows FRDY = 1.</p> <p>When the selected pipe is in the receive direction, do not set this bit to 1.</p>
14	BCLR	0	R/W ^{*2}	<p>CPU buffer clear</p> <p>Clears the CPU side FIFO buffer of the selected pipe.</p> <p>0: Invalid</p> <p>1: Clears the CPU side FIFO buffer.</p> <p>When the FIFO buffer assigned to the selected pipe is set to a double buffer, and even when both sides of the buffer are readable, this module clears only one side of the FIFO buffer.</p> <p>When the selected pipe is DCP, this module clears the FIFO buffer when this bit is set to 1 irrespective of whether the FIFO buffer is on the CPU side or SIE side. When clearing the SIE side FIFO buffer, be sure to set the PID bits in DCP to NAK and then set the BCLR bit to 1.</p> <p>When the selected pipe is in the transmit direction, and if 1 is written in the BVAL and BCLR bits at the same time, this module clears the previously written data, and makes a Zero-Length packet transmittable.</p> <p>When the selected pipe is not DCP, write 1 in this bit while the FRDY flag indicates 1.</p>

74.2.9 Interrupt Enable Register 0 (INTENB0)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

INTENB0 specifies masking of each interrupt when selection for function controller. When this module detects an interrupt for which 1 is written in the corresponding bit in this register by the software, this module generates a USB interrupt.

When interrupt source detection conditions are satisfied irrespective of the register setting (interrupt enable/disable), this module sets the corresponding status bit in INTSTS0.

When the software changes an interrupt enable bit (0 to 1) whose interrupt source status bit in INTSTS0 is set to 1, this module generates a USB interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDY	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R/W: R/W R/W R/W R/W R/W R/W R/W R/W R R R R R R R R R

Bit	Bit Name	Initial Value	R/W	Description
15	VBSE	0	R/W	VBUSn [R-Car H3/M3-W/M3-N] /OVC signal status [R-Car D3/E3] Interrupt Enable Enables or disables USB interrupt outputs when the VBINT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	RSME	0	R/W	Resume Interrupt Enable Enables or disables USB interrupt outputs when the RESM interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	SOFE	0	R/W	Frame Number Update Interrupt Enable Enables or disables USB interrupt outputs when the SOFR interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	DVSE	0	R/W	Device State Transition Interrupt Enable Enables or disables USB interrupt outputs when the DVST interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	CTRE	0	R/W	Control Transfer Stage Transition Interrupt Enable Enables or disables USB interrupt outputs when the CTRT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

74.2.10 BRDY Interrupt Enable Register (BRDYENB)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

BRDYENB enables or disables the BRDY bit to be set to 1 when the BRDY interrupt of a pipe is detected.

When this module detects the BRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBRDY bit of the pipe in BRDYSTS and also sets the BRDY bit in INTSTS0 and generates the BRDY interrupt.

When one or more PIPEBRDY bits in BRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BRDY interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BRDYE	PIPEE BRDYE	PIPED BRDYE	PIPEC BRDYE	PIPEB BRDYE	PIPEA BRDYE	PIPE9 BRDYE	PIPE8 BRDYE	PIPE7 BRDYE	PIPE6 BRDYE	PIPE5 BRDYE	PIPE4 BRDYE	PIPE3 BRDYE	PIPE2 BRDYE	PIPE1 BRDYE	PIPE0 BRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W															

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BRDYE	0	R/W	Pipe F BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BRDYE	0	R/W	Pipe E BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BRDYE	0	R/W	Pipe D BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BRDYE	0	R/W	Pipe C BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BRDYE	0	R/W	Pipe B BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA BRDYE	0	R/W	Pipe A BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BRDYE	0	R/W	Pipe 9 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BRDYE	0	R/W	Pipe 8 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BRDYE	0	R/W	Pipe 7 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

74.2.11 NRDY Interrupt Enable Register (NRDYENB)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

NRDYENB enables or disables the NRDY bit to be set to 1 when the NRDY interrupt of a pipe is detected.

When this module detects the NRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPENRDY bit of the pipe in NRDYSTS and also sets the NRDY bit in INTSTS0 and generates an NRDY interrupt.

When one or more PIPENRDY bits in NRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates an NRDY interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF NRDYE	PIPEE NRDYE	PIPED NRDYE	PIPEC NRDYE	PIPEB NRDYE	PIPEA NRDYE	PIPE9 NRDYE	PIPE8 NRDYE	PIPE7 NRDYE	PIPE6 NRDYE	PIPE5 NRDYE	PIPE4 NRDYE	PIPE3 NRDYE	PIPE2 NRDYE	PIPE1 NRDYE	PIPE0 NRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W															

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF NRDYE	0	R/W	Pipe F NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE NRDYE	0	R/W	Pipe E NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED NRDYE	0	R/W	Pipe D NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC NRDYE	0	R/W	Pipe C NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB NRDYE	0	R/W	Pipe B NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA NRDYE	0	R/W	Pipe A NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 NRDYE	0	R/W	Pipe 9 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 NRDYE	0	R/W	Pipe 8 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 NRDYE	0	R/W	Pipe 7 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

74.2.12 BEMP Interrupt Enable Register (BEMPENB)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

BEMPENB enables or disables the BEMP bit to be set to 1 when the BEMP interrupt of a pipe is detected.

When this module detects the BEMP interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBEMP bit of the pipe in BEMPSTS and the BEMP bit in INTSTS0 and generates the BEMP interrupt.

When one or more PIPEBEMP bits in BEMPSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BEMP interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BEMPE	PIPEE BEMPE	PIPED BEMPE	PIPEC BEMPE	PIPEB BEMPE	PIPEA BEMPE	PIPE9 BEMPE	PIPE8 BEMPE	PIPE7 BEMPE	PIPE6 BEMPE	PIPE5 BEMPE	PIPE4 BEMPE	PIPE3 BEMPE	PIPE2 BEMPE	PIPE1 BEMPE	PIPE0 BEMPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W															

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BEMPE	0	R/W	Pipe F BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BEMPE	0	R/W	Pipe E BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BEMPE	0	R/W	Pipe D BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BEMPE	0	R/W	Pipe C BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BEMPE	0	R/W	Pipe B BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA BEMPE	0	R/W	Pipe A BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BEMPE	0	R/W	Pipe 9 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BEMPE	0	R/W	Pipe 8 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BEMPE	0	R/W	Pipe 7 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

74.2.13 SOF Output Configuration Register (SOFCFG)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

SOFCFG specifies an effective period of transactions, the BRDY interrupt status clear timing, and others.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	BRDY M	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	BRDYM	0	R/W	Status Clear Timing of Each Pipe BRDY Interrupt Specifies the timing to clear the BRDY interrupt status of each pipe. 0: The software clears the status. 1: This module clears the status by reading or writing the FIFO buffer.
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

74.2.14 Interrupt Status Register 0 (INTSTS0)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

INTSTS0 can know the interrupt generation by referring to the register when the function controller is selected.

Permit interrupt by the status change that each bit of this register shows only when you select the function.

This register is initialized by a power-on reset. The DVSQ2 to DVSQ0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBINT	RESM	SOFR	DVST	CTRTR	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]	VALID	CTSQ[2:0]				
Initial value:	0	0	0	0/1	0	0	0	0	0/1	0	0	0/1	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15	VBINT	0	RW0C	VBUSn [R-Car H3/M3-W/M3-N] /OVC signal status [R-Car D3/E3] Interrupt Status*4*5 0: No VBUS interrupt is generated. 1: A VBUS interrupt is generated. This bit indicates 1 when this module detects a change in the VBUSn [R-Car H3/M3-W/M3-N] /OVC signal status [R-Car D3/E3] pin input level (high to low or low to high level). This module indicates the VBUSn [R-Car H3/M3-W/M3-N] /OVC signal status [R-Car D3/E3] pin input value using the VBSTS bit. When a VBINT interrupt occurs, read the VBSTS bit several times by the software and confirm that the read value is equal each time to eliminate chattering.
14	RESM	0	RW0C	Resume Interrupt Status*4*5 0: No resume interrupt is generated. 1: A resume interrupt is generated. This bit indicates 1 when this module detects a falling of the DP_0 pin level in the suspended state (DVSQ = 1XX).
13	SOFR	0	RW0C	Frame Number Update Interrupt Status*4 0: No SOF interrupt is generated. 1: An SOF interrupt is generated. This module indicates SOFR = 1 at the frame number update timing. (This interrupt is detected every millisecond.) Even when an SOF packet from the USB host is corrupted, this module detects an SOFR interrupt using the internal interpolation.
12	DVST	0/1*1	RW0C	Device State Transition Interrupt Status*4 0: No device state transition interrupt is generated. 1: A device state transition interrupt is generated. When this module detects a change in device state, this module updates the DVSQ value and set this bit to 1. When this interrupt occurred, clear the status before this module detects the next device state transition.

74.2.15 BRDY Interrupt Status Register (BRDYSTS)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

BRDYSTS indicates the BRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BRDY	PIPEE BRDY	PIPED BRDY	PIPEC BRDY	PIPEB BRDY	PIPEA BRDY	PIPE9 BRDY	PIPE8 BRDY	PIPE7 BRDY	PIPE6 BRDY	PIPE5 BRDY	PIPE4 BRDY	PIPE3 BRDY	PIPE2 BRDY	PIPE1 BRDY	PIPE0 BRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W															

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBRDY	0	R/W* ¹	Pipe F BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBRDY	0	R/W* ¹	Pipe E BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBRDY	0	R/W* ¹	Pipe D BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBRDY	0	R/W* ¹	Pipe C BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBRDY	0	R/W* ¹	Pipe B BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABRDY	0	R/W* ¹	Pipe A BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BRDY	0	R/W* ¹	Pipe 9 BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BRDY	0	R/W* ¹	Pipe 8 BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BRDY	0	R/W* ¹	Pipe 7 BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BRDY	0	R/W* ¹	Pipe 6 BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BRDY	0	R/W* ¹	Pipe 5 BRDY Interrupt Status* ² 0: No interrupt is generated. 1: An interrupt is generated.

74.2.16 NRDY Interrupt Status Register (NRDYSTS)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

NRDYSTS indicates the NRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF NRDY	PIPEE NRDY	PIPED NRDY	PIPEC NRDY	PIPEB NRDY	PIPEA NRDY	PIPE9 NRDY	PIPE8 NRDY	PIPE7 NRDY	PIPE6 NRDY	PIPE5 NRDY	PIPE4 NRDY	PIPE3 NRDY	PIPE2 NRDY	PIPE1 NRDY	PIPE0 NRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFNRDY	0	R/W*	Pipe F NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEENRDY	0	R/W*	Pipe E NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDNRDY	0	R/W*	Pipe D NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECNRDY	0	R/W*	Pipe C NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBNRDY	0	R/W*	Pipe B NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEANRDY	0	R/W*	Pipe A NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9NRDY	0	R/W*	Pipe 9 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8NRDY	0	R/W*	Pipe 8 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7NRDY	0	R/W*	Pipe 7 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6NRDY	0	R/W*	Pipe 6 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5NRDY	0	R/W*	Pipe 5 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

74.2.17 BEMP Interrupt Status Register (BEMPSTS)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

BEMPSTS indicates the BEMP interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BEMP	PIPEE BEMP	PIPED BEMP	PIPEC BEMP	PIPEB BEMP	PIPEA BEMP	PIPE9 BEMP	PIPE8 BEMP	PIPE7 BEMP	PIPE6 BEMP	PIPE5 BEMP	PIPE4 BEMP	PIPE3 BEMP	PIPE2 BEMP	PIPE1 BEMP	PIPE0 BEMP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W															

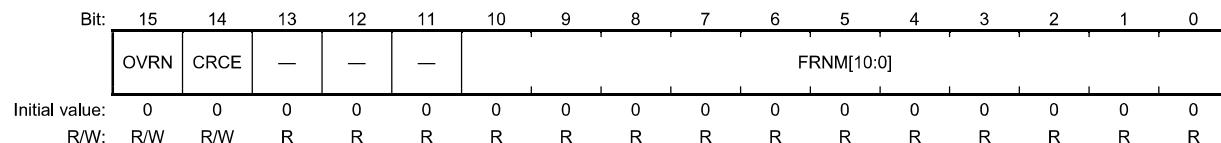
Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBEMP	0	R/W*	Pipe F BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBEMP	0	R/W*	Pipe E BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBEMP	0	R/W*	Pipe D BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBEMP	0	R/W*	Pipe C BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBEMP	0	R/W*	Pipe B BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABEMP	0	R/W*	Pipe A BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BEMP	0	R/W*	Pipe 9 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BEMP	0	R/W*	Pipe 8 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BEMP	0	R/W*	Pipe 7 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BEMP	0	R/W*	Pipe 6 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BEMP	0	R/W*	Pipe 5 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

74.2.18 Frame Number Register (FRMNUM)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

FRMNUM indicates the sources of isochronous errors and a frame number.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15	OVRN	0	RW0C	<p>Overrun/Underrun Detect Status Indicates whether an overrun or underrun error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. This module indicates OVRN =1 in any of the following cases. When the IN token is received when transmit data write to the FIFO buffer is not completed in a transmit direction pipe of isochronous transfer type When the OUT token is received with no side of the FIFO buffer empty in a receive direction pipe of isochronous transfer type</p>
14	CRCE	0	RW0C	<p>Receive Data Error Indicates whether a CRC error or bit stuffing error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. When a CRC error is detected, this module does not generate an internal NRDY interrupt request.</p>
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	FRNM [10:0]	H'000	R	<p>Frame Number This module modifies this bit when an SOF is received and indicates the latest frame number. Read these bits twice and confirm that the read value is equal each time.</p>

74.2.19 μ Frame Number Register (UFRMNUM)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

UFRMNUM indicates a μ frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	UFRNM[2:0]	000	R	μ Frame Indicate a μ frame number. In high-speed operating mode, these bits indicate a μ frame number. In other operating modes, these bits indicate B'000. Read these bits twice and confirm that the read value is equal each time.

74.2.20 USB Address Register (USBADDR)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

USBADDR indicates a USB address.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	USBADDR[6:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	USBADDR[6:0]	H'00	R	USB Address Indicate the USB address allocated by the host when the SET_ADDRESS request is successfully processed. When this module detects a USB reset, these bits indicate H'00.

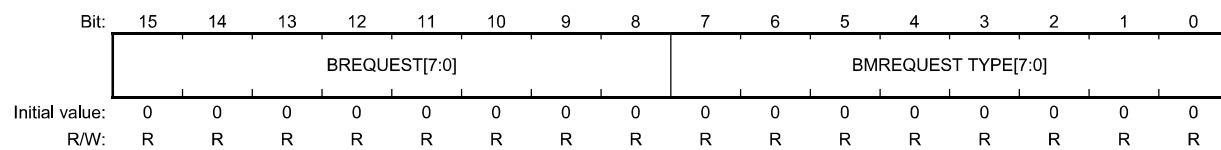
74.2.21 USB Request Type Register (USBREQ)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

USBREQ stores the setup request for control transfers.

USBREQ stores the values of received bRequest and bmRequestType.

This register is initialized by a power-on reset or USB bus reset.



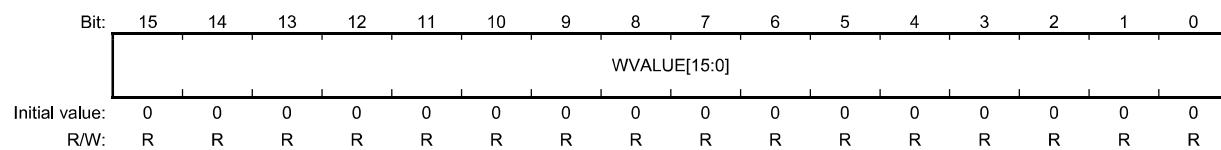
Bit	Bit Name	Initial Value	R/W	Description
15 to 8	BREQUEST [7:0]	H'00	R	Request Store the value of USB request bRequest. Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.
7 to 0	BMREQUEST TYPE[7:0]	H'00	R	Request Type Store the value of USB request bmRequestType. Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.

74.2.22 USB Request Value Register (USBVAL)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

USBVAL stores the value of received wValue.

This register is initialized by a power-on reset or USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WVALUE [15:0]	H'0000	R	Value Store the value of USB request wValue. Indicate the value of USB request wValue received in the SETUP transaction. These bits cannot be modified.

74.2.23 USB Request Index Register (USBINDX)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

USBINDX stores the setup request for control transfers.

USBINDX stores the value of received wIndex.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WINDEX[15:0]																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WINDEX [15:0]	H'0000	R	Index Store the value of USB request wIndex. Indicate the value of USB request wIndex received in the SETUP transaction. These bits cannot be modified.

74.2.24 USB Request Length Register (USBLENG)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

USBLENG stores the setup request of control transfers.

USBLENG stores the value of received wLength.

This register is initialized by a power-on reset or USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WLENGTH[15:0]																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WLENGTH [15:0]	H'0000	R	Length Store the value of USB request wLength. Indicate the value of USB request wLength received in the SETUP transaction. These bits cannot be modified.

74.2.25 DCP Maximum Packet Size Register (DCPMaxP)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

DCPMaxP specifies the maximum packet size of the DCP.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	—	—	—	—	—	MXPS[6:0]				
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	MXPS [6:0]	H'40	R/W	Maximum Packet Size Set the payload of DCP data (maximum DCP packet size) in these bits. The initial value of these bits is H'40 (64 bytes). Set a value in the MXPS bits based on the USB Specification. Set the MXPS bits when PID = NAK, and the CURPIPE bits are not set. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS bits are 0 or set the PID bits to BUF.

74.2.26 DCP Control Register (DCPCTR)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

DCPCTR is used to monitor the buffer memory status, change/check the data PID sequence bit, and set the response PID for a DCP.

This register is initialized by a power-on reset. The PID2 to PID0 bits in CCPL are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	—	—	—	—	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	<p>Buffer Status</p> <p>Indicates whether the DCP FIFO buffer is accessible or not.</p> <p>0: The buffer is not accessible.</p> <p>1: The buffer is accessible.</p> <p>This bit indicates as follows depending on the ISEL value.</p> <p>When ISEL = 0, this bit indicates whether the buffer is ready to read receive data.</p> <p>When ISEL = 1, this bit indicates whether the buffer is ready to write transmit data.</p>
14 to 9	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
8	SQCLR	0	R/W*	<p>Toggle Bit Clear</p> <p>The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA0.</p> <p>0: Invalid</p> <p>1: The expected value is set in DATA0.</p> <p>This bit always indicates 0.</p> <p>Do not set the SQCLR and SQSET bits to 1 at the same time.</p> <p>Set this bit to 1 when PID = NAK, and the CURPIPE bits are not set.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
7	SQSET	0	R/W*	<p>Toggle Bit Set</p> <p>The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA1.</p> <p>0: Invalid</p> <p>1: The expected value is set in DATA1.</p> <p>Do not set the SQCLR and SQSET bits to 1 at the same time.</p> <p>Set this bit to 1 when PID = NAK, and the CURPIPE bits are not set.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

74.2.27 Pipe Window Select Register (PIPESEL)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

Make settings for pipes 1 to F using PIPESEL, PIPECFG, PIPEBUF, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN.

Specify a pipe to be used with PIPESEL, and then make function settings for each pipe in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI. The PIPEnCTR, PIPnTRE, and PIPnTRN registers can be set independently from pipe selection using PIPESEL.

Not only the selected pipe but also the corresponding bits in registers for all pipes are initialized by a power-on reset or USB bus reset.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	PIPESEL [3:0]	0000	R/W	Pipe Window Select Specify a pipe number corresponding to PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI to be read or written. 0000: No pipe is selected. 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A 1011: Pipe B 1100: Pipe C 1101: Pipe D 1110: Pipe E 1111: Pipe F PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI corresponding to the pipe number specified by these bits can be read and written. When these bits are set to B'0000, all bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI are read as 0 and cannot be modified.

74.2.28 Pipe Configuration Register (PIPECFG)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint number for pipes 1 to F, selects continuous transfer mode or discontinuous transfer mode, and single buffer or double buffer, and also specifies whether to disable the operation of each pipe when data transfer finishes.

This register is initialized by a power-on reset. The TYPE1 and TYPE0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE[1:0]	—	—	—	BFRE	DBLB	CNTMD	SHTNAK	—	—	—	DIR	EPNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

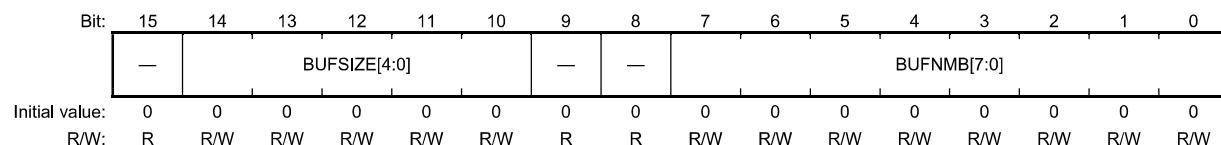
Bit	Bit Name	Initial Value	R/W	Description
15, 14	TYPE[1:0]	00	R/W	<p>Transfer Type</p> <p>Select the transfer type of the pipe specified by the PIPESEL bits (selected pipe).</p> <p>Pipes 1 and 2</p> <ul style="list-style-type: none"> 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Isochronous transfer <p>Pipes 3 to 5, 9 to F</p> <ul style="list-style-type: none"> 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Setting prohibited <p>Pipes 6 to 8</p> <ul style="list-style-type: none"> 00: No pipe is used. 01: Setting prohibited 10: Interrupt transfer 11: Setting prohibited <p>Before setting the selected pipe for PID = BUF (before starting USB communication using the selected pipe), be sure to set these bits to a value other than B'00.</p> <p>Modify these bits when the PID bits of the selected pipe are set to NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
13 to 11	—	All 0	R	Reserved
				These bits are always read as 0. The write value should always be 0.

74.2.29 Pipe Buffer Register (PIPEBUF)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

PIPEBUF specifies the buffer size and buffer number for pipes 1 to F.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 10	BUFSIZE [4:0]	H'00	R/W	Buffer Size Specify the buffer size of the pipe specified by the PIPESEL bits (selected pipe) in units of blocks. One block is 64 bytes. 00000 (H'00): 64 bytes 00001 (H'01): 128 bytes : 11111 (H'1F): 2 Kbytes When DBLB = 1 is set by the software, this module allocates the FIFO buffer size specified by these bits to the selected pipe for two sides. Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: $(\text{BUFSIZE} + 1) \times 64 \times (\text{DBLB} + 1)$ [bytes] A value that can be set in these bits varies depending on pipes selected. For pipes 1 to 5, 9 to F: Set BUFSIZE to H'00 to H'1F. For pipes 6 to 8: Set BUFSIZE to H'00. When using the buffer with CNTMD = 1, set a value in multiples of MaxPacketSize in these bits. Modify these bits when PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

74.2.30 Pipe Maximum Packet Size Register (PIPEMAXP)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

PIPEMAXP specifies the maximum packet size for pipes 1 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MXPS[10:0]																
Initial value:	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R/W										

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	MXPS[10:0]	*	R/W	Maximum Packet Size Specify the payload of data (maximum packet size) of the selected pipe. The settable value range for each pipe is as follows: Pipes 1 and 2: 1 byte (H'001) to 1024 bytes (H'400) Pipes 3 to 5, 9 to F: 8 (H'008), 16 (H'010), 32 (H'020), 64 (H'040), or 512 bytes (H'200) (MXPS2 to MXPS0 bits are not provided.) Pipes 6 to 8: 1 byte (H'001) to 64 bytes (H'040) Set a value in the MXPS bits based on the USB Specification for each transfer type. To transmit an isochronous pipe in split transactions, set a value of 188 bytes or less in the MXPS bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS = 0 or set the PID bits to BUF.

Note: * The initial value is H'000 (when no pipe is selected by the PIPESEL bits in PIPESEL) or H'040 (when a pipe is selected).

74.2.31 Pipe Cycle Control Register (PIPEPERI)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

PIPEPERI specifies whether to activate the buffer flush function or not at the time of an interval error during the isochronous IN transfer, and also specifies the interval error detection interval for pipes 1 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	—	IITV[2:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	IFIS	0	R/W	Isochronous IN Buffer Flush Specifies whether to flush the FIFO buffer when the pipe specified by the PIPESEL bits (selected pipe) is isochronous IN transfer type. 0: The FIFO buffer is not flushed. 1: The FIFO buffer is flushed. Buffer flush is a function that this module automatically clears the FIFO buffer when this module does not receive IN-Token from the USB host in a (μ) frame for each interval specified in the IITV bits when the selected pipe is isochronous IN transfer type. When double buffer is selected (DBLB = 1), this module clears data of only the older side. The FIFO buffer is cleared when an SOF packet is received immediately after the (μ) frame where IN-Token is to be received. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time when the SOF packet is to be received using the internal interpolation. When the selected pipe is not isochronous transfer type, set this bit to 0.
11 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	IITV[2:0]	000	R/W	Interval Error Detection Interval Specify the interval error detection interval of the selected pipe with a value of 2's n-th power of the frame timing. Set these bits when PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. To change the setting of these bits after USB communication, set PID = NAK and then set ACLRM = 1 to initialize the interval timer. These bits are not provided for pipes 3 to F. Set B'000 in the position of these bits corresponding to pipes 3 to F.

74.2.32 Pipe n Control Register (PIPEnCTR) (n = 1 to F)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

PIPEnCTR monitors the buffer memory status, changes/checks the data PID sequence bits, selects whether to use auto-response mode and buffer auto-clear mode, and specifies a response PID for pipes 1 to F. This register can be set independently of the pipe selection using PIPESEL.

This register is initialized by a power-on reset. The PID1 and PID0 bits are also initialized by a USB bus reset.

(1) PIPEnCTR (n = 1 to 5, 9 to F)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	—	PID[1:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	<p>Buffer Status Indicates the FIFO buffer status of the pipe. 0: The buffer is not accessible from the CPU. 1: The buffer is accessible from the CPU. The meaning of this bit differs depending on the settings of the DIR, BFRE, and DCLRM bits as shown in table 74.10.</p>
14	INBUFM	0	R	<p>Transmit Buffer Monitor Indicates the FIFO buffer status of the selected pipe in the transmit direction. 0: The buffer memory contains no transmittable data. 1: The buffer memory contains transmittable data. When transmit direction (DIR = 1) is set for the pipe, this module sets this bit to 1 when the software (or DMAC) finishes writing data to the FIFO buffer for at least one register set. When this module finishes sending all data on the register set (writing is completed) of the FIFO buffer, this bit indicates 0. In the case of a double buffer (DBLB = 1), when this module finishes sending all data on both register sets and the software (or DMAC) has not completed writing of data for one register set, this bit indicates 0. When receive direction (DIR = 0) is set for the selected pipe, this bit indicates the same value as the BSTS bit.</p>
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

74.2.33 Pipe n Transaction Counter Enable Register (PIPnTRE) (n = 1 to 5, 9 to F)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

PIPnTRE enables or disables the transaction counter function and clears the counter for pipes 1 to 5, 9 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	TRENB	0	R/W	Transaction Counter Enable Enables or disables the transaction counter function. 0: The transaction counter function is disabled. 1: The transaction counter function is enabled. When the software sets the number of total packets in the TRNCNT bits in PIPnTRN for the receive pipe and then sets this bit to 1, this module controls the following when it received the same number of packets as the setting of the TRNCNT bits. When continuous communication mode is used (CNTMD = 1), this module toggles the received data to the CPU even if the FIFO buffer is not full at the end of reception. When SHTNAK = 1, this module changes the PID bits for the corresponding pipe to NAK when this module received the same number of packets as the setting of the TRNCNT bits. When BFRE = 1, this module asserts the BRDY interrupt when this module received the same number of packets as the setting of the TRNCNT bits and read the receive data completely. For transmit pipes, set this bit to 0. When the transaction counter function is not used, set this bit to 0. When using the transaction counter function, set the TRNCNT bits and then set this bit to 1. Furthermore, set this bit to 1 before receiving the first packet that is included in the transaction count range.
8	TRCLR	0	R/W	Transaction Counter Clear Clears the current count value of the transaction counter for the pipe and indicates TRCLR = 0. 0: Invalid 1: The current count value is cleared.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Change the bits in this register when PID = NAK.

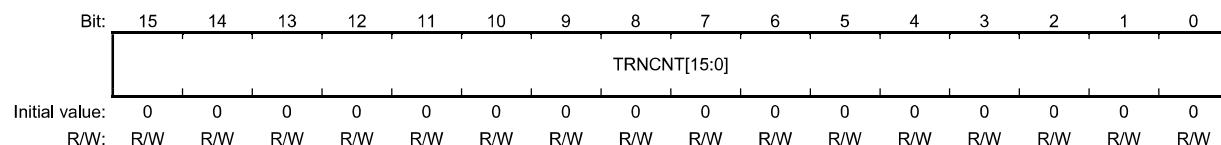
When changing the bits in this register after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

74.2.34 Pipe n Transaction Counter Register (PIPE_nTRN) ($n = 1$ to 5, 9 to F)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

PIPE_nTRE is a transaction counter for pipes 1 to 5, 9 to F.

This register is initialized by a power-on reset, but the setting of this register is retained through a USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT [15:0]	All 0	R/W	<p>Transaction Counter</p> <p>Writing:</p> <ul style="list-style-type: none"> Specify the number of transactions of DMA transfer. <p>Reading:</p> <ul style="list-style-type: none"> When TREN_B = 0, the set number of transactions is indicated. When TREN_B = 1, the number of current transactions is indicated. <p>This module increments (+1) the value of these bits when the following conditions are all satisfied.</p> <ul style="list-style-type: none"> TREN_B = 1 TRCNT value ≠ current count value +1 when a packet is received. The payload of the received packet equals the value of the MXPS bits. This module clears these bits to 0 when any of the following is satisfied. When the following conditions are all satisfied <ul style="list-style-type: none"> — TREN_B = 1 — TRCNT value = current count value +1 when a packet is received. — The payload of the received packet equals the value of the MXPS bits. When the following conditions are all satisfied <ul style="list-style-type: none"> — TREN_B = 1 — A short packet is received. When the following conditions are all satisfied <ul style="list-style-type: none"> — TREN_B = 1 — The software sets the TRCLR bit to 1. <p>For transmit pipes, set these bits to all 0.</p> <p>When the transaction counter function is not used, set these bits to all 0.</p> <p>Change these bits when PID = NAK and TREN_B = 0.</p> <p>When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p> <p>When changing these bits, set TRCNT = 1 and then set TREN_B = 1.</p>

74.2.35 Low Power Status register (LPSTS)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

This register provides low power management control.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SUSPM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	SUSPM	0	R/W	SuspendM control 0: UTMI suspend mode 1: UTMI normal mode This bit should set to 1 when normal operating. UTMI clock is halted if this bit set to 0. Note: This controller deny register access without as follow registers if this bit set to 0. SYSCFG0 BUSWAIT INTENB0 LPSTS BCCTRL UGCTRL * UGCTRL2 UGSTS *
13 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: * UGCTRL and UGSTS are implemented R-Car D3 and E3.

74.2.36 Battery Charging Control Register (BCCTRL)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

This register provides battery charging control signals and status signals for embedded USB PHY with battery charging.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PRTBLDET	CHGDET	—	—	—	VDM_SRCEN	PRTBLDETEN	VDP_SRCEN	CHGDETEN	IDP_SRCEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PRTBLDET	0	R/W	PRTBLDET status 0: PRTBLDET is low level 1: PRTBLDET is high level
8	CHGDET	0	R/W	CHGDET status 0: CHGDET is low level 1: CHGDET is high level
7, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VDM_SRCEN	0	R/W	VDM_SRC control Peripheral mode: Set this bit to 1 in secondary detection. Note: SYSSFG.DRPD should be set to 0 before setting this bit. Host mode: Set this bit to 1 if connection of the portable device is detected. 0: VDM_SRC disabled 1: VDM_SRC enabled
3	PRTBLDETEN	0	R/W	PRTBLDET control Peripheral mode: Set this bit to 1 in secondary detection. Note: SYSSFG.DRPD should be set to 0 before setting this bit. Host mode: Set this bit to 1 if connection of the portable device is detected. 0: PRTBLDET disabled 1: PRTBLDET enabled
2	VDP_SRCEN	0	R/W	VDP_SRC control Peripheral mode: Set this bit to 1 in primary detection. Note: SYSSFG.DRPD should be set to 0 before setting this bit. 0: VDP_SRC disabled 1: VDP_SRC enabled
1	CHGDETEN	0	R/W	CHGDET control Peripheral mode: Set this bit to 1 in primary detection. Note: SYSSFG.DRPD should be set to 0 before setting this bit. 0: CHGDET enabled 1: CHGDET disabled

74.2.37 USB General Control Register (UGCTRL)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
—	—	—	—	√	—	√

This register provides embedded USB PHY control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CONNECT	0	R/W	USB connect control 0: PHY receiver halted 1: PHY receiver enabled
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	PLLRESET	1	R/W	PLL Reset 0: PLL reset release 1: PLL reset assert

74.2.38 USB General Control Register 2 (UGCTRL2)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	√	√	√

This register provides embedded USB PHY control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	VBUSS SEL	—	—	—	—	USB0SEL	—	—	—	—	—
Initial value:	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	VBUSSSEL	1	R/W	VBUS drive control select 1: VBUS drive is controlled by PORTSC1.PP of EHCI/OHCI 0: VBUS drive is controlled by VBCTRL.VBOUT
9 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	USB0SEL ^{*2}	11 ^{*1}	R/W	USB2.0 Ch.0/Ch.3 Selection 01: Select EHCI/OHCI host module for USB2.0 ch0/ch.3 10: Select HS USB module for USB2.0 ch0/ch.3 11: Select USB OTG function for USB2.0 ch0/ch.3
3 to 0	—	0001	R	Reserved These bits are always read as B'0001. The write value should always be B'0001.

Notes: 1. R-Car D3/E3: B'01

2. ch.3 is implemented only R-Car H3

74.2.39 USB General Status Register (UGSTS)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
—	—	—	—	√	—	√

This register provides embedded USB PHY status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	LOCK	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	R	R	0	R	R	R	R	R	R	R	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved
8	LOCK	0	R	Embedded USB PHY PLL Lock status 1: Embedded USB PHY Lock completed 0: Embedded USB PHY Lock halted
7 to 0	—	H'01	R	Reserved The write value should always be same value.

74.2.40 USB XTAL/EXTTAL control register (USB20_CLKSET0)

R-Car H3	R-Car M3-W	R-Car V3M	R-Car V3H	R-Car D3	R-Car M3-N	R-Car E3
√	√	—	—	—	√	—

This register provides USB_XTAL/USB_EXTAL control.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	INCLK_SEL	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
11	INCLK_SEL	0	R/W	USB_XTAL/USB_EXTAL to USB3 path control 0: Connects the crystal oscillator to the USB_EXTAL and USB_XTAL 1: Inputs an external oscillator to the USB_EXTAL
10 to 0	—	H'001	R	Reserved The write value should always be same value.

Note: This register is only in Channel 0.

74.3 Operation

R-Car H3	R-Car D3
R-Car M3-W	R-Car M3-N
R-Car V3M	R-Car E3
R-Car V3H	

74.3.1 System Control and Oscillation Control

This section describes register operations required for the initial settings of this module.

(1) Power control and Initialization

The following is the initialize power on procedure of USB subsystem.

[R-Car H3/M3-W/M3-N]

1. Supply 3.3 V
2. Release HS-USB module stop and assert module reset.
3. Set LPSTS.SUSPM to normal mode.
4. Set UGCTRL2.USB0SEL bits to B'10 to select HS USB module.
5. Wait 45 μ s for USB PHY to stabilize, and then start normal operation.

[R-Car D3/E3]

1. Supply 1.8 V
2. Supply 3.3 V (Note: Do not supply 3.3 V when 1.8 V is not supplied.)
3. Wait 100 μ s for USB PHY power stable.
4. HS-USB and EHCI module stop release and module reset assert.
5. UGCTRL.PLLRESET release
6. UGCTRL2.USB0SEL[1:0] should be set to B'10 for HS-USB.
7. LPSTS.SUSPM set to normal mode.
8. Check PLL Lock status by USB General status register (UGSTS)
9. Starting normal operation after PLL Lock status enabled.
10. UGCTRL.CONNECT bit set to 1

The following is the power off procedure of USB subsystem

[R-Car H3/M3-W/M3-N]

1. Normal operation finished
2. Module stop enable.
3. Shut off powers.

[R-Car D3/E3]

1. Normal operation finished
2. UGCTRL.CONNECT bit set to 0
3. PLL disable by UGCTRL.PLLRESET assert
4. Shut off 3.3V (VD331)
5. Shut off 1.8V (VD181) (Note: Do not shut off 1.8 V while 3.3 V is being supplied.)
6. Module stop enable.

74.3.2 Interrupt Function

Table 74.14 lists the interrupt generating conditions of this module.

When any of the following interrupt generating conditions are satisfied and the interrupt output is enabled by the corresponding interrupt enable register, this module outputs a USB interrupt request to the interrupt controller (INTC).

Table 74.14 Interrupt Generating Conditions

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
VBINT	VBUS interrupt	When VBUS input pin state change is detected (both L to H and H to L)	VBSTS	—
RESM	Resume interrupt	When a USB bus state change is detected in the suspended state (J-State to K-State or J-State to SE0)	—	—
SOFR	Frame number update interrupt	SOFRM = 0: When an SOF packet with a different frame number is received SOFRM = 1: When an SOF packet with a μ frame number of 0 cannot be received due to damage, etc.	—	—
DVST	Device state transition interrupt	When a device state transition is detected USB bus reset detected Suspended state detected SET_ADDRESS request received SET_CONFIGURATION request received	DVSQ	—
CTRT	Control transfer stage transition interrupt	When a control transfer stage transition is detected Setup stage completed Control write transfer status stage shifted Control read transfer status stage shifted Control transfer completed Control transfer sequence error occurred	CTSQ	—
BEMP	Buffer empty interrupt	When the buffer becomes empty after sending all buffer memory data When a packet with a size exceeding the maximum packet size is received	BEMPSTS.PIPEBEMP	—
NRDY	Buffer not ready interrupt	When NAK is sent in response to IN token, OUTtoken, or PING token When a CRC error or bit stuffing error occurred during data reception in isochronous transfer When an overrun or underrun error occurred during data reception in isochronous transfer	NRDYSTS.PIPENRDY	—
BRDY	Buffer ready interrupt	When the buffer becomes ready for reading or writing	BRDYSTS.PIPEBRDY	—
OVRCR	OVRCR interrupt	When an OVC input pin state change is detected	OVMON	—

Note: These bits in this table are those of INTSTS0 if any register's name is not indicated.

74.3.3 Pipe Control

Table 74.15 lists the pipe settings of this module. In the USB data transfer, data must be transmitted or received using virtual pipes called “endpoint.” This module is provided with ten pipes for data transfer. Set each pipe according to system specifications.

74.3.4 FIFO Buffer Memory

(1) Allocating FIFO Buffer Memory

Figure 74.9 shows an example of the FIFO buffer memory map of this module. The FIFO buffer memory is an area shared by the CPU and this module. There are two FIFO buffer memory states where the access right is given to the system (CPU) or to this module (SIE).

The FIFO buffer memory provides independent areas for each pipe. A memory area is set with the block start number and the number of blocks (BUFNMB and BUFSIZE bits in PIPEBUF) in 64-byte units as one block.

When continuous transfer mode is selected by the CNTMD bit in PIPEnCFG, be sure to set the BUFSIZE bits to a value in integral multiples of the maximum packet size. When double buffer is selected by the DBLB bit in PIPEnCFG, two sides of the memory area specified by the BUFSIZE bits in PIPEBUF are provided for the same pipe.

Furthermore, three FIFO ports are used for accesses (data read/write) to the buffer memory. The number of a pipe to be allocated to the FIFO ports is specified by the CURPIPE bits in CFIFOSEL and DnFIFOSEL.

The buffer status of each pipe can be monitored by the BSTS and INBUFM bits in DCPCTR and PIPEnCTR. The access right to the FIFO ports can be checked by the FRDY bit in CFIFOCTR and DnFIFOCTR.

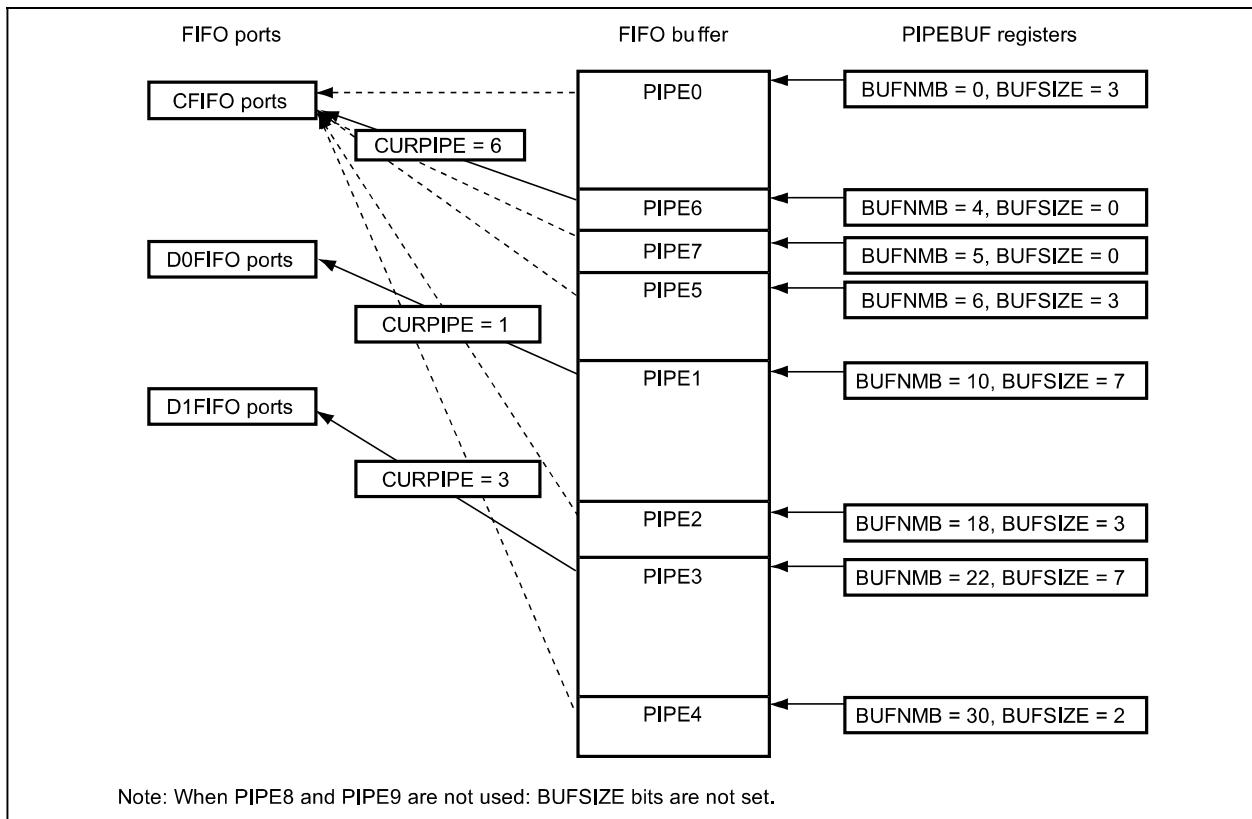


Figure 74.9 Example of Buffer Memory Map

74.3.5 Control Transfer (DCP)

The default control pipe (DCP) is used for data transfer in the control transfer data stage. The buffer memory for the DCP is a 64-byte single buffer of a fixed area used for both control read and control write. The buffer memory can be accessed only by the CFIFO ports.

(1) Setup Stage

1. This module always sends ACK in response to a normal setup packet to this module. The following describes the operation of this module in the setup stage.

When this module receives a new setup packet, this module sets the following bits.

- The VALID bit in INTSTS0 to 1
- The PID bits in DCPCTR to NAK
- The CCPL bit in DCPCTR to 0

2. When this module receives a data packet following a setup packet, this module stores the USB request parameters in USBREQ, USBVAL, USBINDEX, and USBLENG.

Be sure to process responses to control transfers while VALID = 0. The PID bits cannot be set to BUF when VALID = 1, and therefore the data stage cannot be completed.

With the VALID bit function, this module can suspend the ongoing request processing if this module receives a new USB request during a control transfer, and send a response to the latest request.

This module also determines the direction bit (bit 8 of bmRequestType) of the received USB request and the request data length (wLength), identifies a control read transfer, control write transfer, and control write no-data transfer, and controls stage transitions. For an incorrect sequence, a sequence error of the control transfer stage transition interrupt occurs, and the error is reported to the software. For the stage control of this module, see figure 74.7.

(2) Data Stage

Transfer data in response to the received USB request using the DCP. Before making an access to the DCP buffer memory, specify the access direction by the ISEL bit in CFIFOSEL.

When the transfer data size is larger than the DCP buffer memory size, use a BRDY interrupt for control write transfers and a BEMP interrupt for control read transfers.

In the high-speed control write transfer, this module sends responses using the NYET handshake according to the buffer memory status.

(3) Status Stage

Setting the CCPL bit to 1 with the PID bits in DCPCTR set to BUF finishes a control transfer.

After these settings, this module executes the status stage as follows according to the data transfer direction determined in the setup stage:

- Control read transfer
This module sends a Zero-Length packet and receives an ACK response from the USB host.
- Control write transfer, no-data control transfer
This module receives a Zero-Length packet from the USB host and sends an ACK response.

(4) Control Transfer Auto-Response Function

This module automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, the software must respond to the error.

- Other than control read transfer: bmRequestType ≠ H'00
- Request errors: wIndex ≠ H'00
- Other than no-data control transfer: wLength ≠ H'00
- Request errors: wValue > H'7F
- Control transfer of device state errors: DVSQ = B'011 (configured)

All requests other than SET_ADDRESS require a response made by the software.

74.3.6 Bulk Transfer (Pipes 1 to 5, 9 to F)

The buffer memory usage (single buffer/double buffer setting or continuous/discontinuous transfer mode setting) can be selected for bulk transfers. The buffer memory size can be set to up to 2 Kbytes. This module manages the buffer memory status and automatically responds to a PING packet and an NYET handshake.

(1) NYET Handshake Control

Table 74.24 lists NYET handshake responses of this module. This module sends a NYET response under the following conditions. However, when this module receives a short packet, this module sends ACK instead of NYET. The same is true of the control write transfer data stage.

Table 74.24 NYET Handshake Responses

Setting of PID Bits in DCPCTR	Buffer Memory Status	Token	Response	Remarks
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY1	OUT/PING	ACK	Receives a data packet when receiving an OUT token.
	RCV-BRDY2	OUT	NYET	Receives a data packet. Sends a “reception disable” response.
	RCV-BRDY2	OUT (Short)	ACK	Receives a data packet. Sends a “reception enable” response.
	RCV-BRDY2	PING	ACK	Sends a “reception enable” response.
	RCV-NRDY	OUT/PING	NAK	Sends a “reception disable” response.
	TRN-BRDY	IN	DATA0/1	Sends a data packet.
	TRN-NRDY	IN	NAK	TRN-NRDY

[Legend]

- RCV-BRDY1: The buffer memory has available space for two packets or more when receiving an OUT or PING token.
- RCV-BRDY2: The buffer memory has available space for only one packet when receiving an OUT token.
- RCV-NRDY: The buffer memory is occupied when receiving an PING token.
- TRN-BRDY: The buffer memory contains transmit data when receiving an IN token.
- TRN-NRDY: The buffer memory contains no transmit data when receiving an IN token.

74.3.7 Interrupt Transfer (Pipes 6 to 8)

This module performs interrupt transfer following the cycles controlled by the host controller. In interrupt transfers, this module ignores PING packets (no response), sends no NYET handshake, and sends ACK, NAK, and STALL responses.

This module does not support the High-Bandwidth interrupt transfer.

74.3.8 Isochronous Transfer (Pipes 1, 2)

This module is provided with the following functions for isochronous transfers.

- Reporting isochronous transfer error information
- Interval counter (IITV bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (IFIS bit)

This module does not support the isochronous High-Bandwidth transfer.

(1) Isochronous Transfer Error Detection

This module is provided with a function to detect the following error information so that the software can manage isochronous transfer errors. Tables 74.25 and 74.26 show the error detection priority of this module and interrupts generated as a result of error detection.

1. PID error
 - When the PID in a receive packet is invalid
2. CRC error, bit stuffing error
 - When a CRC error is found in a receive packet or bit stuffing is invalid
3. Maximum packet size exceeded error
 - When the data size of a receive packet is over the maximum packet size setting
4. Overrun/underrun error
 - When the buffer memory contains no data when this module receives an IN token in the IN direction (transmission) transfer
 - When the buffer memory is occupied when this module receives an OUT token in the OUT direction (reception) transfer
5. Interval error

This module generates an interval error in the following cases.

 - When no IN token can be received in interval frames in the isochronous IN transfer
 - When this module receives an OUT token other than interval frames in the isochronous OUT transfer

74.3.9 SOF Interpolation Function

In case this module cannot receive SOF packets at intervals of 1 ms (full-speed operation) or 125 µs (high-speed operation) due to damage or missing of SOF packets, this module interpolates the SOF. The SOF interpolation starts functioning when SYSCFG.USBE = 1, LPSTS.SUSPM= 1, and at the SOF packet receive timing. Furthermore, the interpolation function is initialized in the following cases.

- Power-on reset
- USB bus reset
- When the suspended state is detected

The SOF interpolation functions with the following specifications.

- The frame intervals (125 µs or 1 ms) conform to the result of the reset handshake protocol.
- The SOF interpolation does not function until this module receives an SOF packet.
- After receiving the first SOF packet, 125 µs or 1 ms is counted by the internal 48-MHz clock to interpolate the SOF.
- After receiving the second SOF packet or a following packet, the SOF is interpolated using the previous receive intervals.
- The SOF interpolation does not function in the suspended state and during a USB bus reset.
(When this module enters the suspended state in high-speed operation, the SOF interpolation continues for 3 ms from the final packet.)

This module activates the following functions based on the reception of SOF packets. When one or more SOF packets are lost, normal operation can be continued to perform the SOF interpolation.

- Updating frame numbers and µ frame numbers
- SOFR interrupt timing and µ SOF lock
- SOF pulse output
- Isochronous transfer interval count

When one or more SOF packets are lost in full-speed operation, the FRNM bits in FRMNUM are not updated. When one or more µ SOF packets are lost in high-speed operation, the UFRNM bits in the UFRMNUM are updated. However, when a µ SOF packet with UFRNM = B'000 is lost, the FRNM bits are not updated even if following µ SOF packets with UFRNM ≠ B'000 are successfully received.

74.4 Guidelines for Designing USB2.0 Hi-Speed Boards

R-Car H3	R-Car D3
R-Car M3-W	R-Car M3-N
R-Car V3M	R-Car E3
R-Car V3H	

74.4.1 USB Transmission Line

The USB transmission line indicates the pattern that connects the USB connector and the USB transceiver with built-in this LSI.

The USB2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The transmission speed in the Hi-Speed mode is 480 Mbps. Therefore, the USB transmission line must be designed as a high-frequency circuit. Impedance control is required for the USB transmission line.

- The characteristic impedance required for the USB Hi-Speed transmission line is differential impedance $90\ \Omega$ ($\pm 15\%$).
- The pattern width and pattern pitch for impedance control vary depending on the board thickness, material and layer configuration. For details, consult the board manufacturer.
- A maximum delay of 1 ns is allowed from the USB connector to this LSI. Therefore it is recommended that the pattern length from the USB device to the USB connector is less than 50 mm and the difference between the pattern lengths for D+ and D– is less than 2.5 mm for a generic PCB.
- The lower layer of the USB transmission line must be a solid ground plane. The ground must be wider than the USB transmission line by 2 mm or more. The power supply for a solid ground plane is DG33.
- Do not allocate other signal lines near to the USB transmission line. In particular, lines carrying widely fluctuating signals, such as clock and data bus lines, must be assigned far from the USB transmission line. Furthermore, layout of the USB transmission lines must be such that they do not cross with other signal lines.
- Locate the USB transmission line on the same layer without passing it through a through-hole. Do not create stubs.
- Place the USB transmission lines so that they are equally spaced from each other.
- Locate the USB transmission line as far as possible from the oscillator, power supply circuit, and other I/O connectors.
- Try to avoid bending the USB transmission line as far as possible. If it is absolutely necessary to bend it, do not bend it at acute or right angles. Bend it moderately, at not more than 45 degrees, or bend it into an arc.
- It is recommended to guard ring the clock, reset, read, write and chip select signals with grounds.

When a resistance is connected to the USB transmission line, locate it near to the USB transmission line. The connecting wire must be as short as possible.

74.4.2 Power Supply and Ground Pattern

Refer to serial interface PCB design guideline.

74.4.3 Oscillation

- USB clock is supplied by the internal PLL.
- Provide an oscillation circuit near the clock input pin for USB (EXTAL). It is recommended to guard ring EXTAL with a ground.
- When using a crystal resonator, consult its manufacturer to determine the circuit constant.

Note: * R-Car D3/E3 supply 48MHz reference clock from EXTAL/XTAL instead of USB_EXTAL/USB_XTAL.

74.4.4 VBUS

[R-Car H3/M3-W/M3-N]

- This HS-USB must not connect directly to the 5V VBUS. The VBUSn pin must be isolated by an $30k\Omega \pm 1\%$ external resistor.

[R-Car D3/E3]

- This HS-USB subsystem cannot connect 5 V signals so that vbus status is informed by OVC signal status.

74.4.5 TXRTUNEn/USB_RREF Pin

- Provide a resistor (hereafter called reference resistor)*¹, between the TXRTUNEn/USB_RREF pin and AVSS, PVSS.

Note: 1. R-Car H3/M3-W/M3-N : $200\Omega \pm 1\%$, R-Car D3/E3 : $1.8k\Omega \pm 1\%$

- Locate the reference resistor as close as possible to this LSI.
- The RREF pin, the reference resistor, PVSS and AVSS should be wired on wide areas and the shortest length.
- Use a wiring pattern for and only for the reference resistor, PVSS and AVSS. The pattern should be connected to the analog ground. The pattern should be designed avoiding the possibility for common impedance between RREF and other signals.
- To prevent cross talk, very-frequently switched signals such as DP, DM, clocks, and control signals for addresses and data, should not be placed near to the reference resistor, and their patterns should neither get across nor go parallel to the wiring pattern between the reference resistor and the RREF pin.

It is recommended to guard ring the reference resistor and its wiring pattern with ground.

74.5 Battery Charging Control

R-Car H3	R-Car D3
R-Car M3-W	R-Car M3-N
R-Car V3M	
R-Car V3H	

Figure 74.17 shows embedded USB PHY battery charging control. BCCTRL, UGCTRL, and UGSTS provide battery charging control. The embedded USB PHY supports only D+ and D- signals.

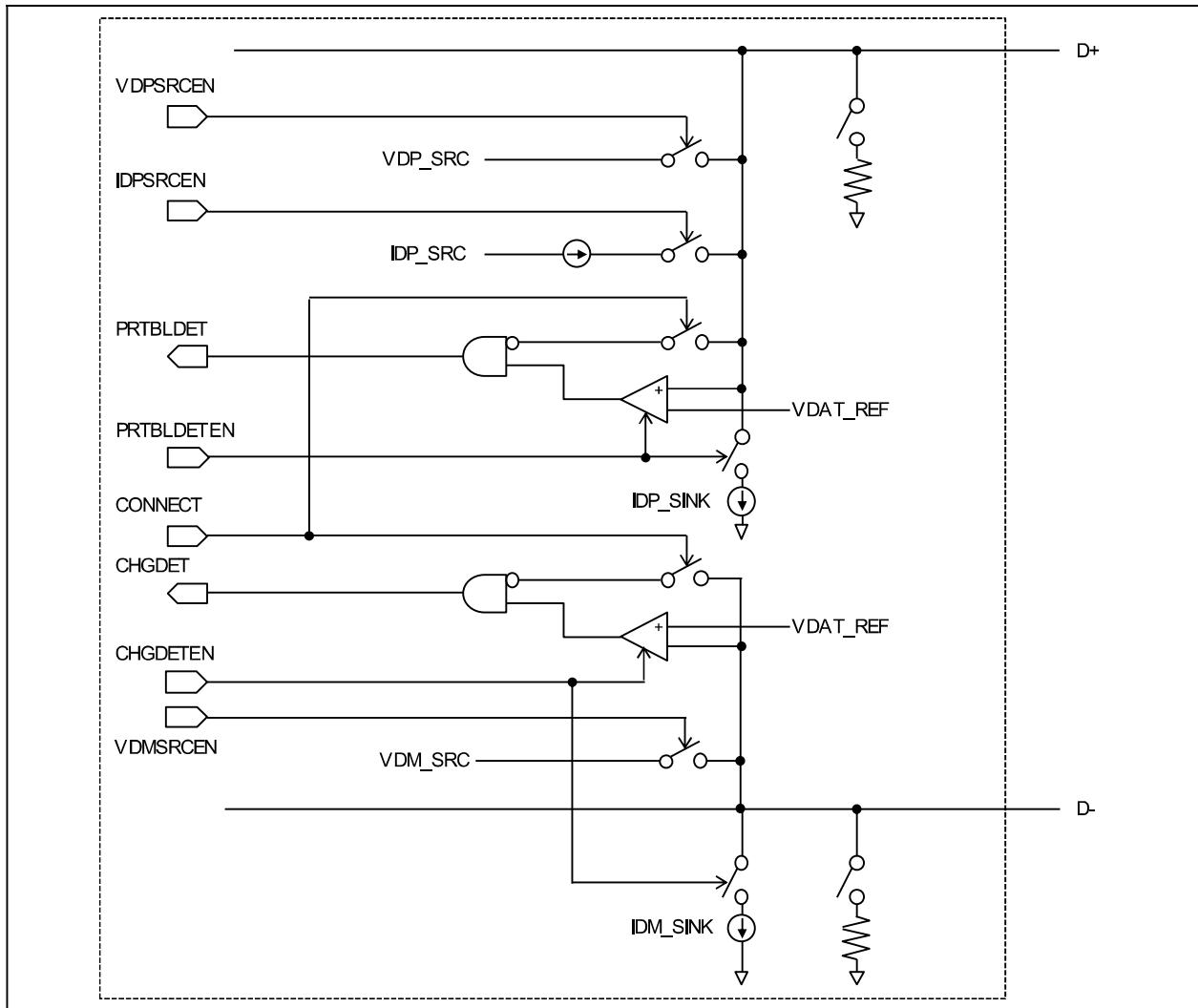


Figure 74.17 Circuit of Battery Charging Control