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ECSE 4770

Lab Assignment 1 - Observing Transmission Line Effects: Report

The objective of this lab is to observe the problems associated with driving computer busses by examining reflections in a 50-ohm coaxial transmission line.

Part 1

a) In this step, we build the circuit shown in Figure 1 below. For C1, we chose to use a 0.1 uF capacitor as it is a standard capacitance value and is referenced several times throughout the datasheet. After setting up our circuit, as shown in Figure 2, we attached the oscilloscope probe to the output pin of the 555 Timer and observed the signal shown in Figure 3.

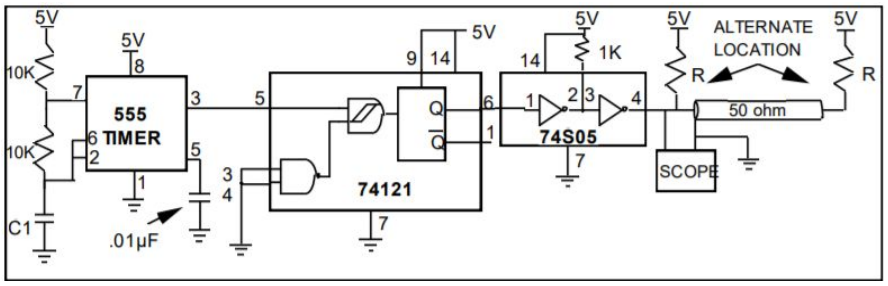

***Figure 1**: Wiring Diagram for Part 1*

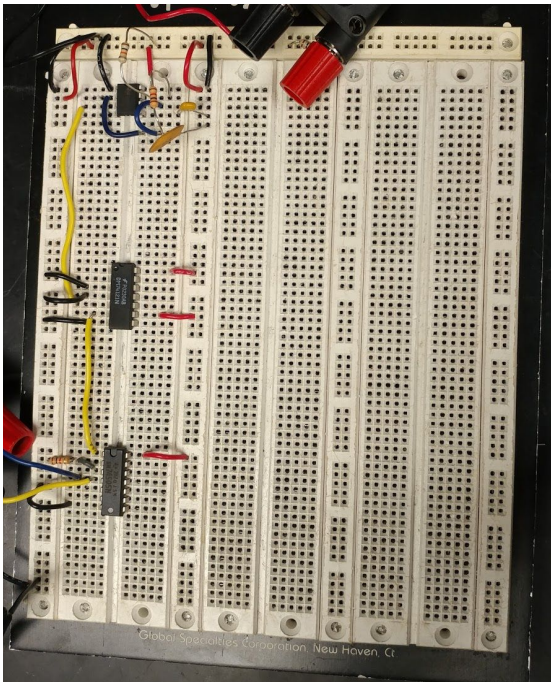

***Figure 2:** Wired circuit*

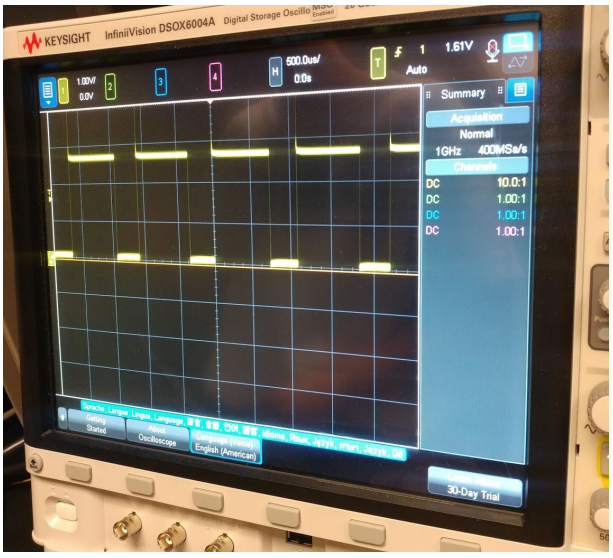

Figure 3: *Original output*

Note: The output pictured above in Figure 3 is not fully correct due to an extra wire connecting to the 74S05 chip that was later removed.

b) We attempted to obtain a stable trace, but first had to use the horizontal delay and runt triggering modes to check our signal. The horizontal delay mode allowed us to check the stability of the signal by traversing it horizontally. The runt triggering mode detects a pulse that crosses the first threshold but not the second. It was helpful for understanding whether the circuit was functioning as expected and if anything should be adjusted. As mentioned above, the circuit was not fully performing as expected after observing the modes and was debugged accordingly. Outputs pictured in Figure 4.

c) We adjusted the capacitor value on pins 2 and 6 from 0.1uF to 10uF to see how the output would be affected. We observed that the output became more pronounced as the time delay increased in response to the higher RC value.

Figure 4: *Effect of 10uF capacitor on pins 2 and 6*

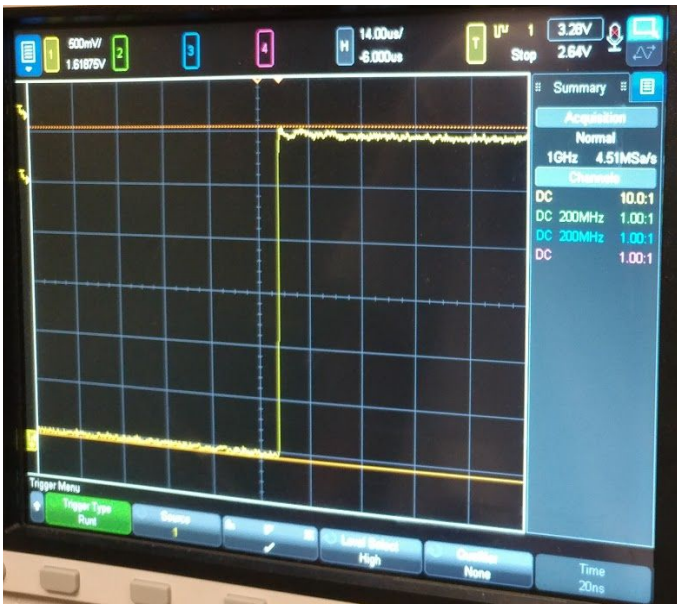

Figure 5: *Outputs using horizontal delay and run triggering modes*

d) In this step, we were supposed to change one of the 10-Kohm resistors and observe the effect. Our output did not significantly differ from the increased capacitance output in Figure 4 above.

Part 2

In this part, we moved the probe to the output of the 74S05.

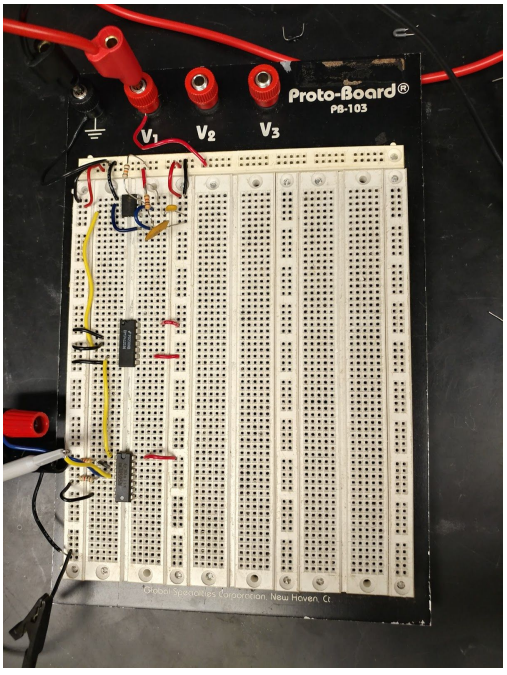

Figure 6: *Circuit after moving scope probe to 74S05 output (in front of coax cable)*

a) After referencing the data sheet, we determined that it will not be possible to correctly drive the 50-ohm impedance cable because the 74S05 open collector Schottky gate only has 20 mA of sinking capability.

b) We used a 1 Kohm resistor for R and placed it at the end of the 50-ohm cable, which was 1-meter long. Figure 6 below shows the line reflections that we observed.

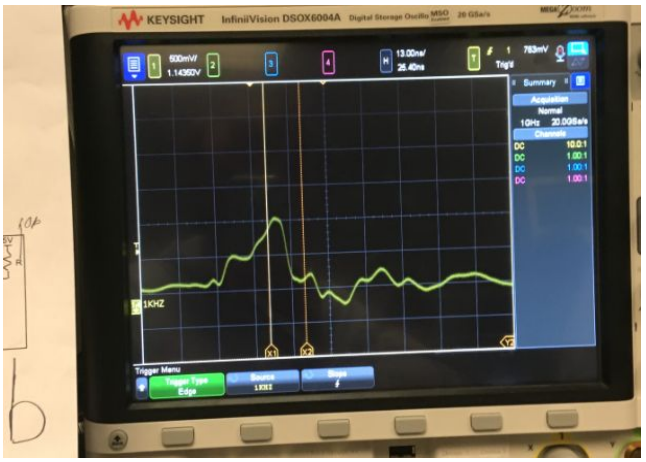

Figure 7: *Line reflections due to 1 Kohm resistor*

Next, we had to show how to measure the velocity of propagation in the cable using the line reflections. To do this, we lined up the two vertical cursors as seen in Figure 6. The line X1 shows the generated pulse and X2 shows the pulse that is coming back. We measured the time between these two lines to be 10ns. Next, we had to arrive at this result through calculations. The first thing we noted is that the velocity in a cable is ⅔ the speed of light which is 2x10^8 m/s. Rearranging the velocity equation and solving for time, we obtained:

$$t=d/v$$

Where d is twice the length of the cable since a pulse goes and comes back. Solving for the time delay, we got:

$$t=(2 \text{ meters}/2\text{x}10^8 \text{ meters/second}) = 10\text{ns}$$

c) In this step, we repeated part b with R relocated at the output of the 74S05. Still using the 1-meter long cable, we observed the following, shown in Figure 7.

Figure 8: *Line reflections with R located at the 74S05 output*

We observed again that the time delay between the pulse and its reflection was 10ns, as expected through our calculations.

d) This time we repeated part b with a 1.5-meter long cable and observed the following, shown in Figure 8.

Figure 9: *Line reflections with a 1.5 meter long cable*

The value of d this time is 3 meters, since the cable length was increased to 1.5 meters.

Solving for the time delay, we obtained:

t=(1.5 meters/2x10^8 meters/second) = 15ns

e) The leading edge of the pulse looks different from the falling edge because these two pulses happen at different rates of speed. For example, the falling edge is a high-to-low transition which is much faster than a leading edge which is a low-to-high transition.

f) We were supposed to observe out the smallest safe value for R. Rather than be systematic about it, we decided to use a 10-ohm resistor. It was later found out that this was a non-safe value to use here, as it could damage the chips in the circuit due to excess current. Figure 9 below shows the drastic effect that the 10-ohm resistor had on the circuit.

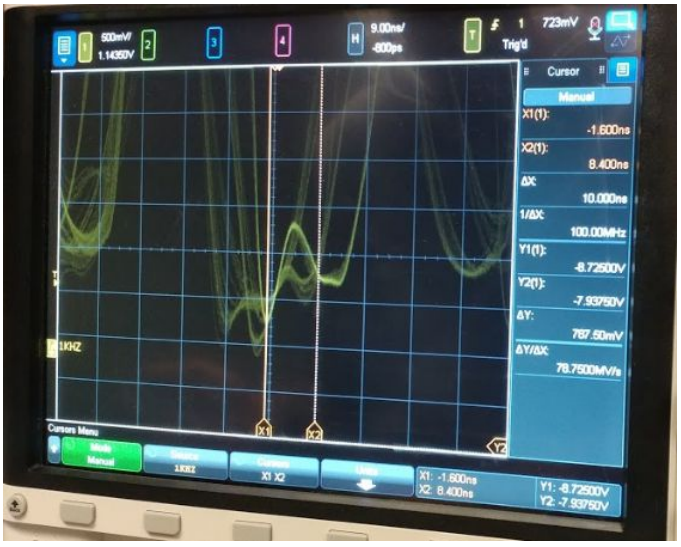

Figure 10: *Effect of using a 10-ohm resistor for R*

After learning that this was the incorrect approach, we calculated what the smallest safe value of R is by taking into consideration that we were using a 5-volt supply voltage and the sinking capability is only 20 mA. Using this, we performed the following calculation:

$$R=V/I = 5V/20x10^{-3}A = 250 \text{ ohms}$$

Because there were no 250-ohm resistors available in the inventory, we decided to use the next best value which was a 270-ohm resistor. Using the correct smallest value of R, we observed the following in Figure 10 below.

Figure 11: *Effect of using a 270-ohm resistor for R*

g) In this step, we used the criteria we found in part f, to redesign the termination to have both a pull-up and pull-down resistor, R1 and R2. Again, we had to match the safe minimum value of R and then repeat part b with the new termination. Knowing that we wanted the value of R to be 50-ohms to match that of the cable, we chose both R1 and R2 to be 100 ohms, since their equivalent parallel resistance would yield 50 ohms.

Figure 12: *Effect of using a 270-ohm resistor for R*

Part 3

In this part, we replaced the 74S05 chip with a 74128 TTL chip, which is designed for driving a 50-ohm cable.

a) In this step, we observed the reflections shown in Figure 12 below.

Figure 13: *Reflections due to 74128 chip*

b) In this step, we recalculated the minimum safe value of R. We referred to the datasheet of the 74128 and found that the 74128 can sink 48 mA of current. Using this, we performed the following calculation:

R=V/I = 5V/48x10^-3A = 104.17 ohms

Because there were no 104-ohm resistors available in the inventory, we decided to use a 120-ohm resistor. Then, combining the 120-ohm in parallel with a 100-ohm, the equivalent resistance came out to be 54.5 ohms.

c) We adjusted the value of R to minimize the line reflections as shown in Figure 13 below.

Figure 14: *Minimization of reflections due to new 120-ohm as new R*

Part 4
Omitted

Part 5
In this part, we assembled a 7474 Edge Triggered Flip-flop out of individual gates. To do so, we used two 7410 chips because they each contain three 3-input NAND gates. Figure 14 shows the schematic we drew out in order to aid in building the physical circuit.

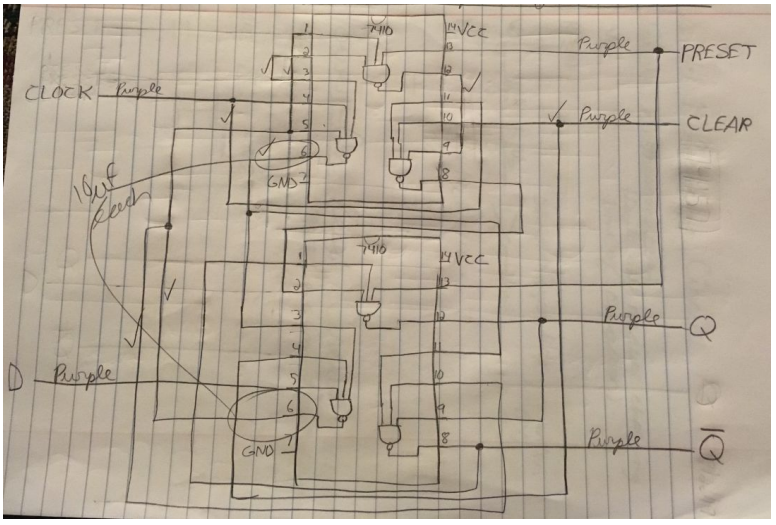

Figure 15: *Schematic of 7474 Edge Triggered Flip-Flop using two 7410 chips*

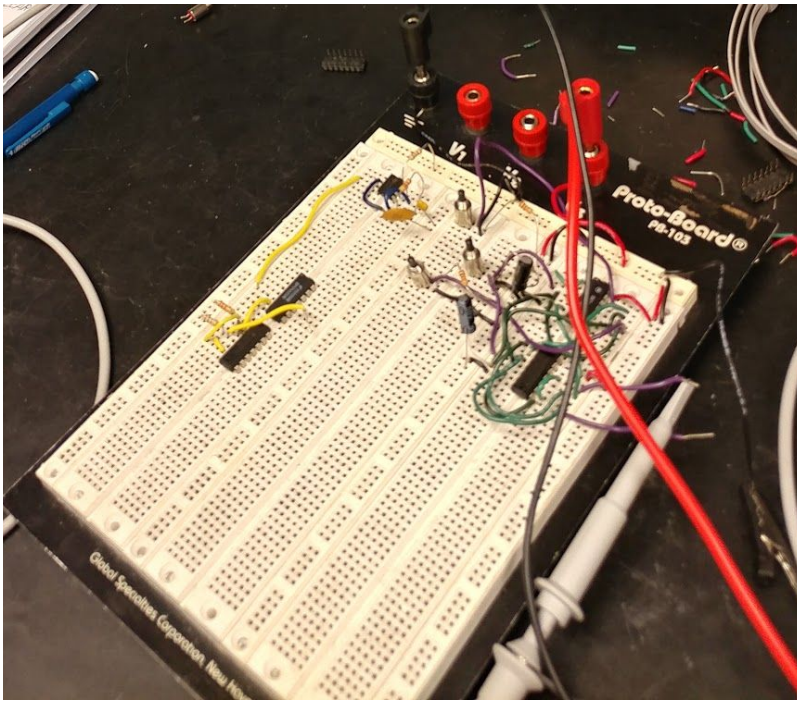

Figure 16: *Assembled 7474 Edge Triggered flip-flop circuit*

a) We observed the edge triggering by testing out the scenarios as shown in Figure 17 below.

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going transition of the clock.
Q_0 = The output logic level of Q before the indicated input conditions were established.

Figure 17: *Function Table of the 7474 Edge Triggered Flip-flop*

To observe the edge-triggering of the flip-flop, we tested out each output in order to observe the behavior, pictured below in Figures 18 and 19. The outputs demonstrated how they adjust as a switch is pushed, driving them either low or high and reacting with a slight delay, dependent on the clock cycle. The behavior of the flip-flop was, for the most part, predictable and outputted the expected results.

Figure 18: *Low Q or Q' output*

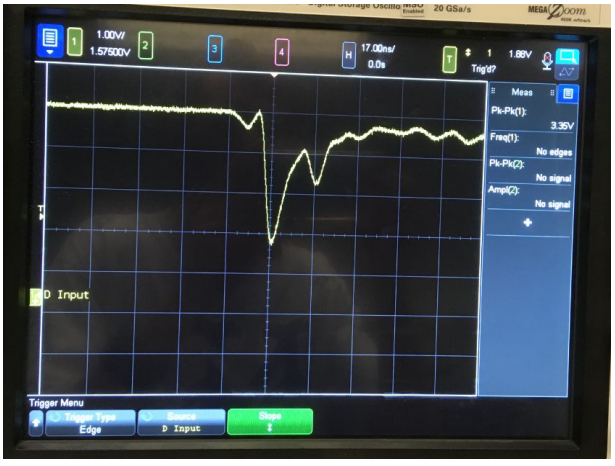

Figure 19: *High Q or Q' output*

b) We attempted to excite a race condition by driving both the data and the clock inputs simultaneously. The setup for this is shown in Figure 20 as both the data and clock are tied to the same pushbutton.

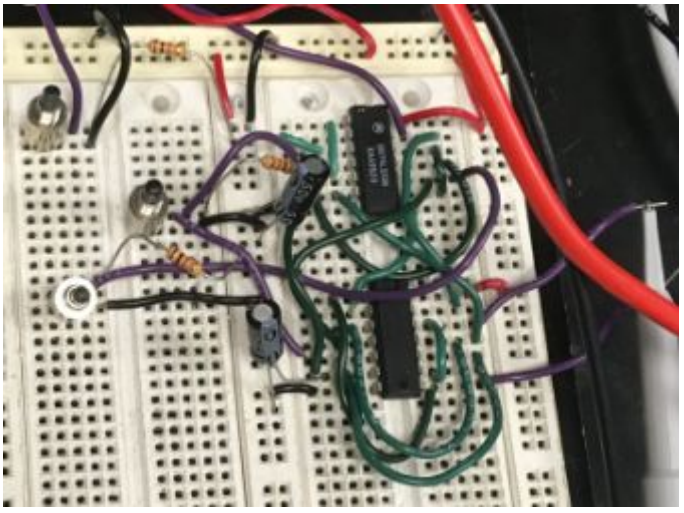

Figure 20: *7474 Edge Triggered Flip-flop 2 7410 chips*

c) In this step, we added some small parasitic capacitance on some gate outputs to influence the outcome. After placing a 10 uF capacitor at each output of the 7410 gates, we observed the results in Figure 21.

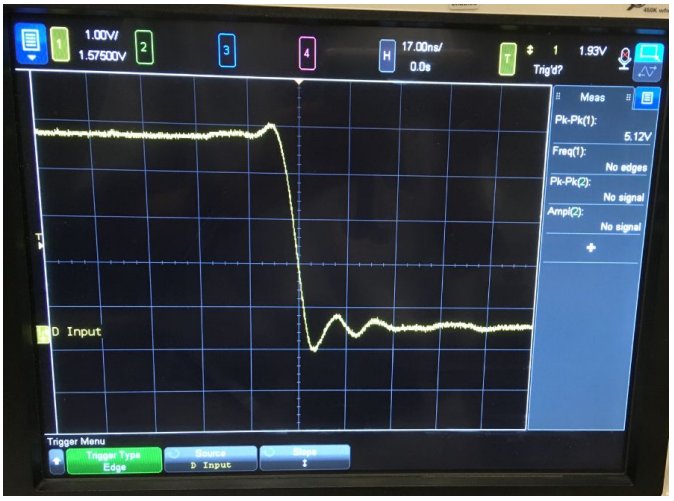

Figure 21: *Effect of adding 10 uF of parasitic capacitance to output gates*

Figure 22: *Effect of adding 10 uF of parasitic capacitance to output gates*

d) In this step, we swapped out the 7410's for 74S10 parts and observed the following, shown in Figure 23 below.

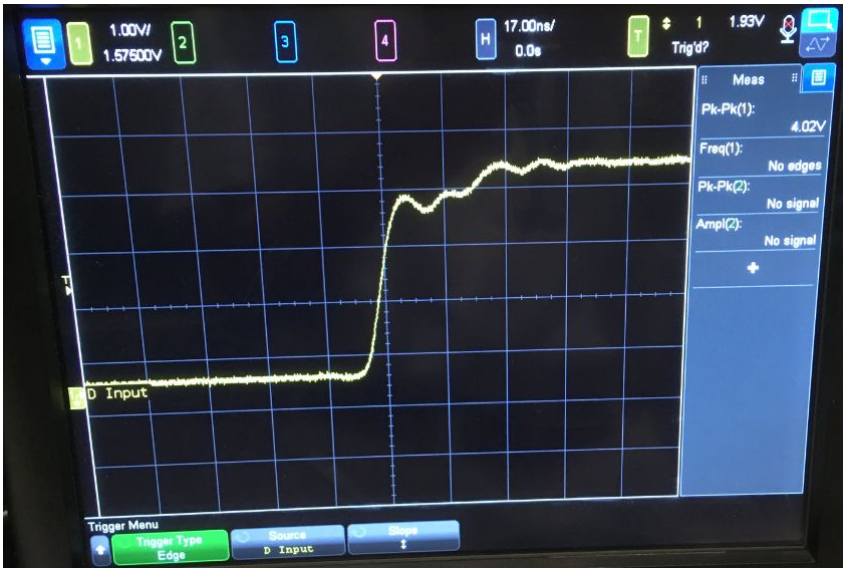

Figure 23: *Effect of using 74S parts*