Rensselaer Polytechnic Institute

VLSI Design
ECSE 4220

Report

Project #2
Final Design Write-up Assignment

Nikoleta Koleva

TA: Sagnik Nath
Date: 13-Dec-2019
Instructor: Tong Zhang

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0. Introduction

Throughout this report, the Cadence IC design tool was used to build and simulate f=(AB+C)’, using 3 pfets and 3 nfets. First, an ideal version of this circuit was built, after which a real-world simulation was compared. The circuit was first tested in ideal circumstances, after which a layout was built upon it but using real-world setbacks, such as parasitic capacitance and resistance. The responses were then compared and a conclusion was drawn.

1. Circuit Schematic

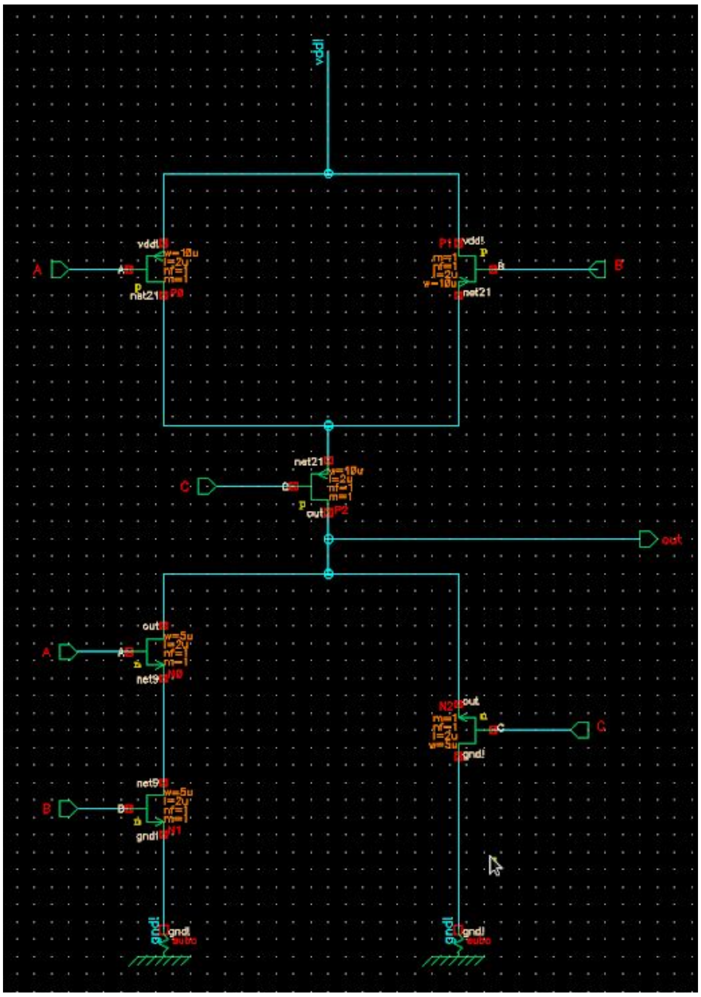
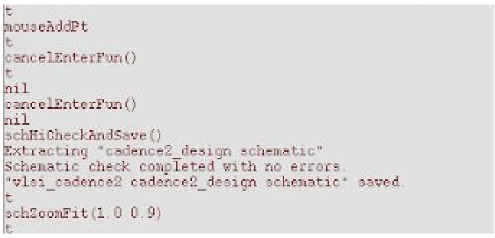


Figure 1: f=(AB+C)’ schematic



```
t
mouseAddPt
t
cancelEnterFun()
t
nil
cancelEnterFun()
nil
schHiCheckAndSave()
Extracting "cadence2_design schematic"
Schematic check completed with no errors.
"vlsi_cadence2 cadence2_design schematic" saved.
t
schZoomFit(1.0 0.9)
t
```

Figure 2: Check and Save output

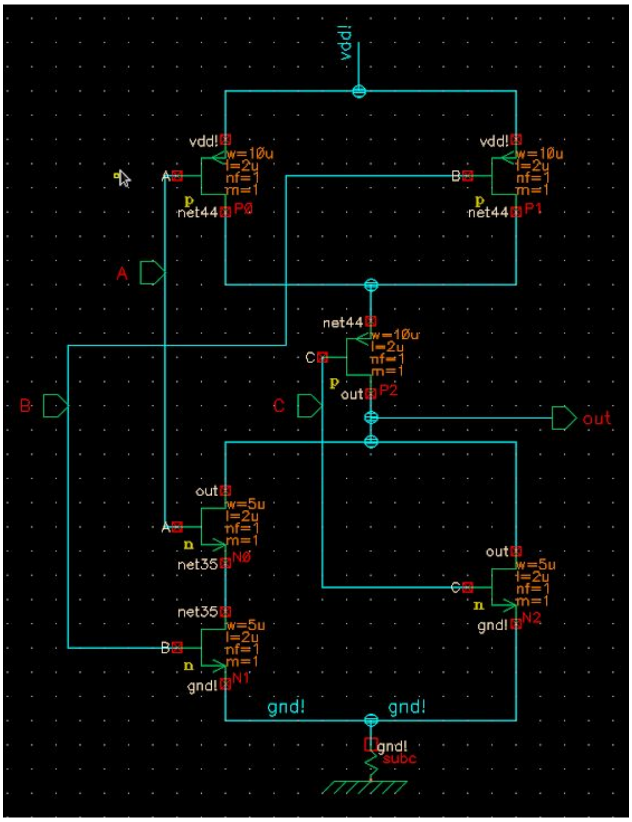


Figure 3: Updated Schematic with no repeating pins

Figure 1 above displays the initial built circuit in Cadence. This circuit later failed due to wire and pin names that were the same and was later changed to the circuit displayed in Figure 3. As can be seen in Figure 2, at the final ‘Check and Save’ run, there were no errors found by the program. The same numbers for the pfet and nfet lengths were used as in the tutorial.

2. **Schematic Simulation Results**

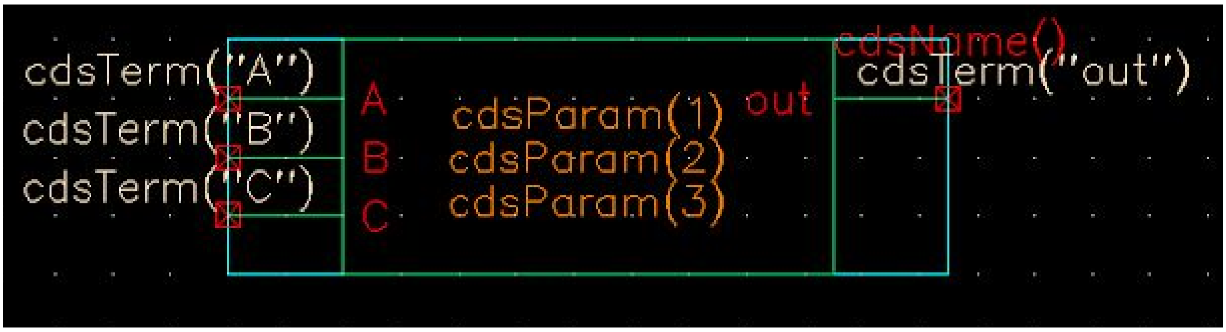


Figure 4: Confirmation of symbol creation

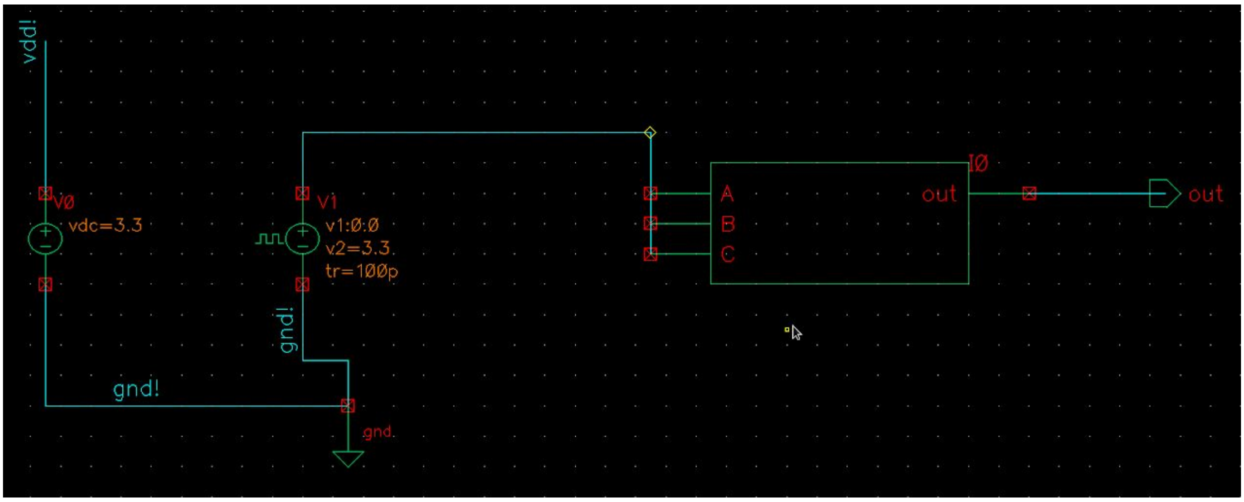
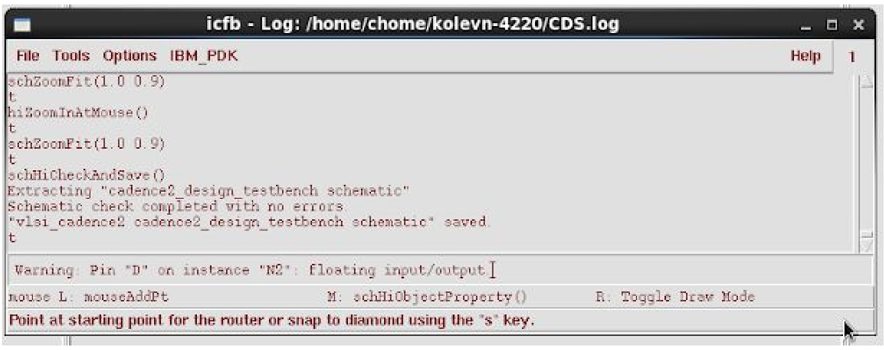


Figure 5: Schematic testbench circuit setup

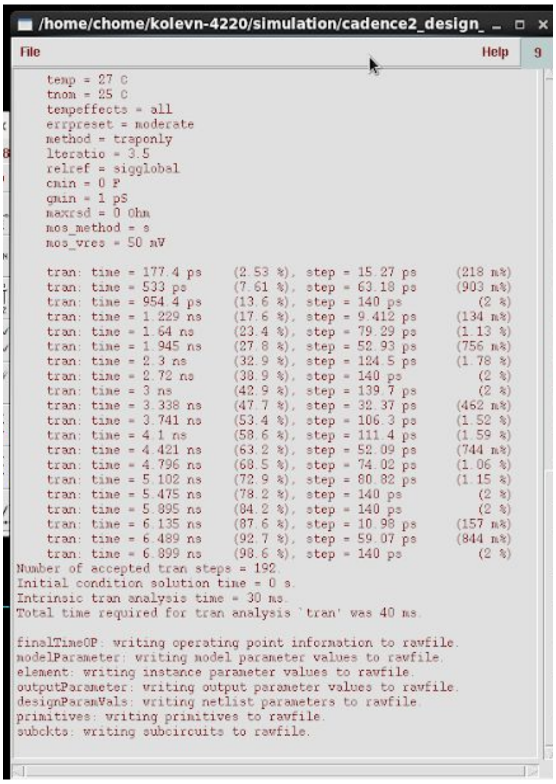


```
schZoomFit(1.0 0.9)
t
hiZoomInAtMouse()
t
schZoomFit(1.0 0.9)
t
schHiCheckAndSave()
Extracting "cadence2_design_testbench schematic"
Schematic check completed with no errors
"vlsi_cadence2 cadence2_design_testbench schematic" saved
t
```

```
Warning: Pin "D" on instance "N2": floating input/output
mouse L: mouseAddPt                 M: schHiObjectProperty()          R: Toggle Draw Mode
Point at starting point for the router or snap to diamond using the "s" key.
```

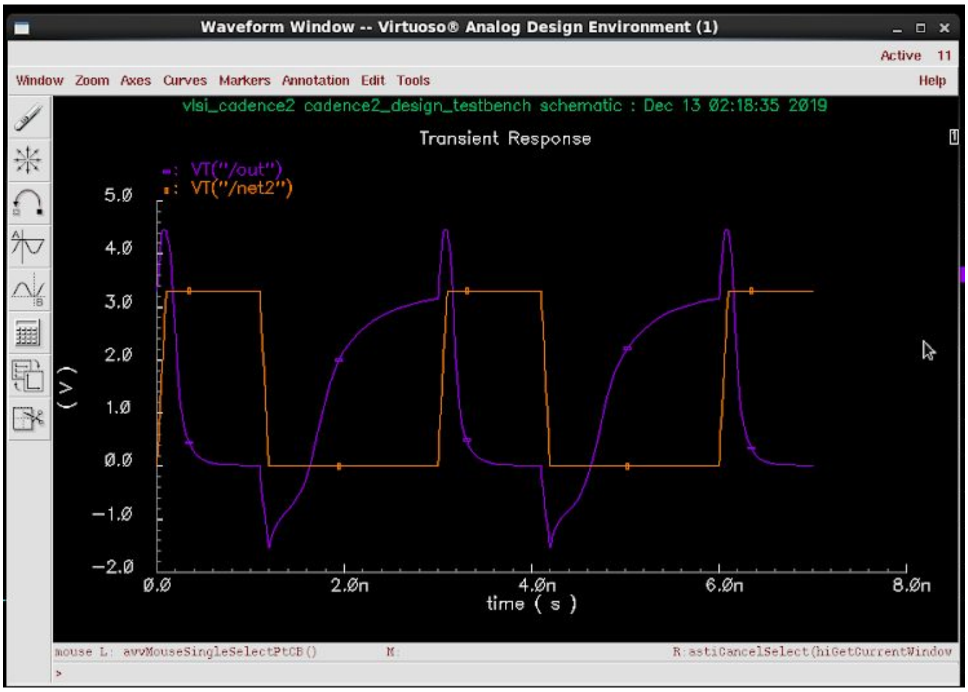
Figure 6: Schematic testbench circuit 'Check and Save' result

For the simulation, a testbench cellview was built to implement the (AB+C)' circuit previously built as a schematic. Additionally, ground, VDC and VPULSE sources were added. The values used for the voltage sources were the same as provided in the class tutorial. Once, this was built anc checked successfully, the simulation was initiated.



```
    temp = 27 C
    tnom = 25 C
    tempeffects = all
    errpreset = moderate
    method = traponly
    lteratio = 3.5
    relref = sigglobal
    cmin = 0 F
    gmin = 1 pS
    maxrsd = 0 Ohm
    mos_method = s
    mos_vres = 50 mV

    tran: time = 177.4 ps    (2.53 %), step = 15.27 ps     (218 m%)
    tran: time = 533 ps      (7.61 %), step = 63.18 ps     (903 m%)
    tran: time = 954.4 ps    (13.6 %), step = 140 ps          (2 %)
    tran: time = 1.229 ns    (17.6 %), step = 9.412 ps     (134 m%)
    tran: time = 1.64 ns     (23.4 %), step = 79.29 ps     (1.13 %)
    tran: time = 1.945 ns    (27.8 %), step = 52.93 ps     (756 m%)
    tran: time = 2.3 ns      (32.9 %), step = 124.5 ps     (1.78 %)
    tran: time = 2.72 ns     (38.9 %), step = 140 ps          (2 %)
    tran: time = 3 ns        (42.9 %), step = 139.7 ps        (2 %)
    tran: time = 3.338 ns    (47.7 %), step = 32.37 ps     (462 m%)
    tran: time = 3.741 ns    (53.4 %), step = 106.3 ps     (1.52 %)
    tran: time = 4.1 ns      (58.6 %), step = 111.4 ps     (1.59 %)
    tran: time = 4.421 ns    (63.2 %), step = 52.09 ps     (744 m%)
    tran: time = 4.796 ns    (68.5 %), step = 74.02 ps     (1.06 %)
    tran: time = 5.102 ns    (72.9 %), step = 80.82 ps     (1.15 %)
    tran: time = 5.475 ns    (78.2 %), step = 140 ps          (2 %)
    tran: time = 5.895 ns    (84.2 %), step = 140 ps          (2 %)
    tran: time = 6.135 ns    (87.6 %), step = 10.98 ps     (157 m%)
    tran: time = 6.489 ns    (92.7 %), step = 59.07 ps     (844 m%)
    tran: time = 6.899 ns    (98.6 %), step = 140 ps          (2 %)
Number of accepted tran steps = 192.
Initial condition solution time = 0 s.
Intrinsic tran analysis time = 30 ms.
Total time required for tran analysis `tran' was 40 ms.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
```

Figure 7: Simulation/Testbench netlist results


Waveform Window -- Virtuoso® Analog Design Environment (1)
Active 11
Window Zoom Axes Curves Markers Annotation Edit Tools
Help
vlsi_cadence2 cadence2_design_testbench schematic : Dec 13 02:18:35 2019
Transient Response
VT("/out")
VT("/net2")
5.0
4.0
3.0
2.0
1.0
0.0
−1.0
−2.0
(V)
0.0
2.0n
4.0n
6.0n
8.0n
time (s)

```
mouse L: awvMouseSingleSelectPtCB()        M:        R:astiCancelSelect(hiGetCurrentWindow
>
```

Figure 8: Schematic simulation result

In Figure 8 above, the results of the simulation can be observed. It was done with a 7ns stop time and done for the schematic file of the circuit.

3. **Full Layout**

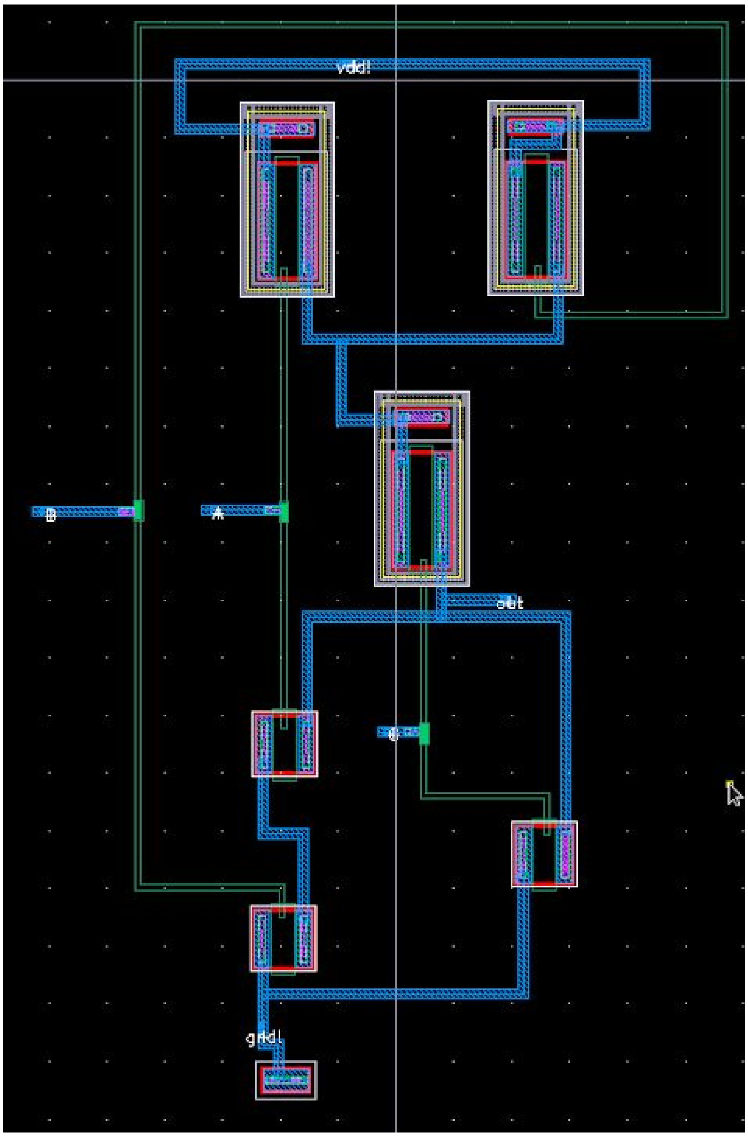


Figure 9: Full layout of f=(AB+C)' circuit, original

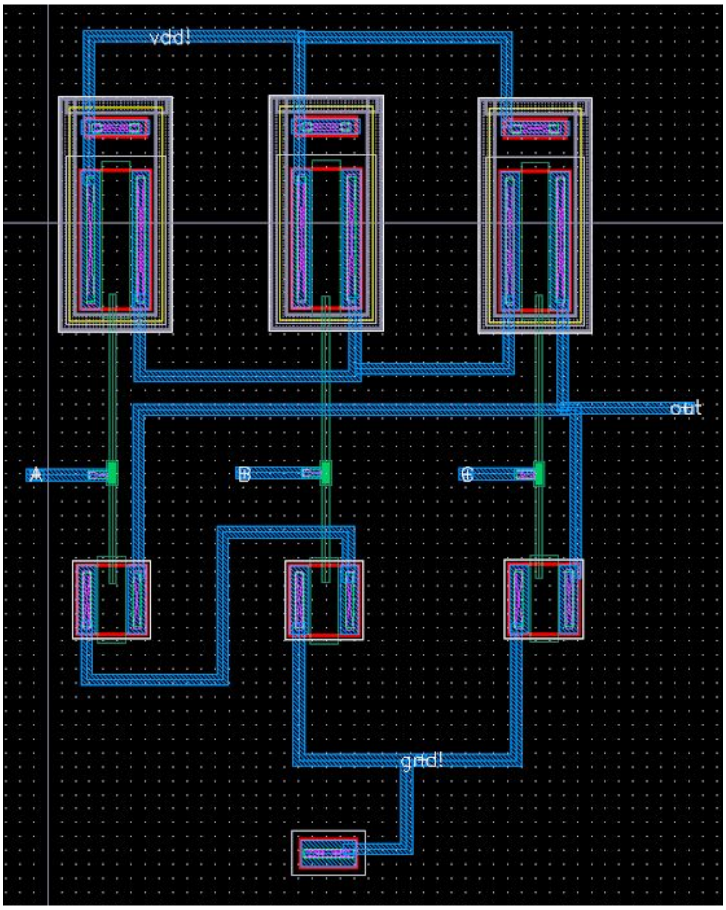
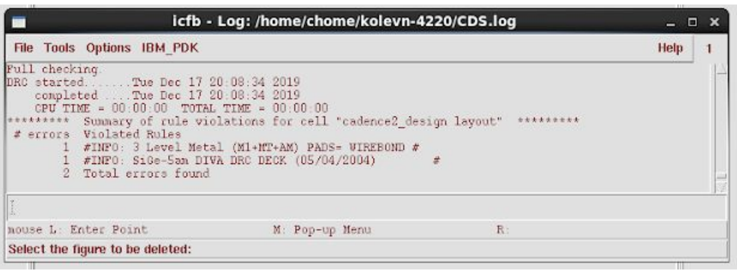


Figure 10: Full layout of modified f=(AB+C)' circuit

The layout of the circuit was initially built as shown in Figure 9 and worked as intended but in an effort to improve legibility and design, the design was later modified to what can be observed in Figure 10. This design was deemed more intuitive and easier to visualize in a physical implementation.

4. Design Rule Check (DRC) of the layout



```
Full checking.
DRC started.......Tue Dec 17 20:08:34 2019
    completed ....Tue Dec 17 20:08:34 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********  Summary of rule violations for cell "cadence2_design layout"  *********
 # errors  Violated Rules
        1  #INFO: 3 Level Metal (M1+MT+AM) PADS= WIREBOND #
        1  #INFO: SiGe-5am DIVA DRC DECK (05/04/2004)        #
        2  Total errors found
```

```
mouse L: Enter Point                M: Pop-up Menu                R:
Select the figure to be deleted:
```

Figure 11: DRC check of result

In Figure 10 above is the compact cell constructed, which passes DRC, as can be seen in Figure 11 (with only two INFO errors, which are stated as normal and expected as in the tutorial document). While DRC and LVS checks passed, there was an initial netlist mismatch with the schematic file, which was later resolved. It was due to wiring issues and discrepancies between the layout and schematic. This was fixed with the design change mentioned in Section 3 above.

5. Layout Extraction and Layout vs. Schematic (LVS) check result

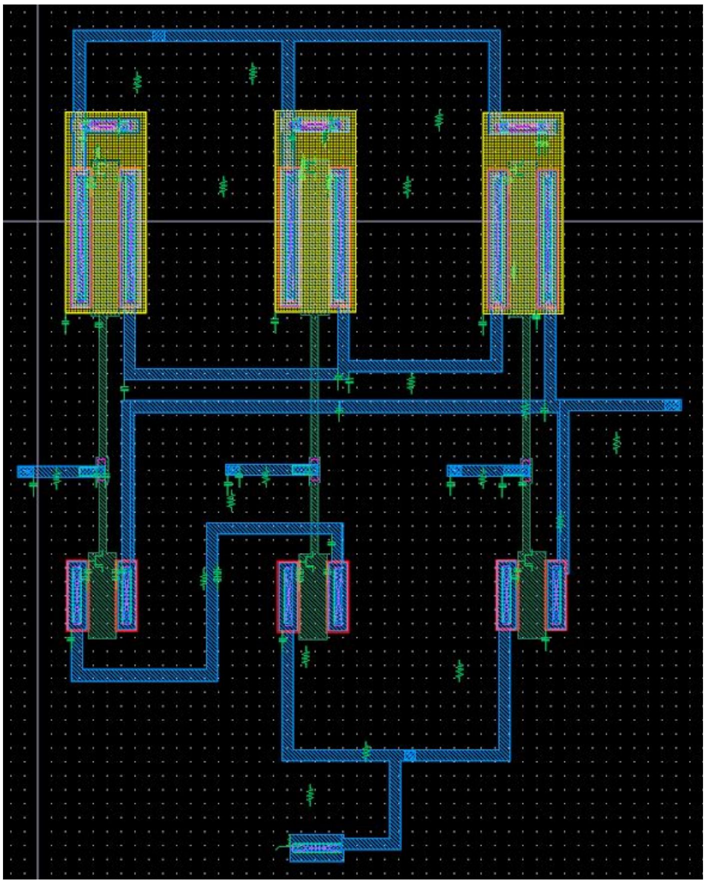
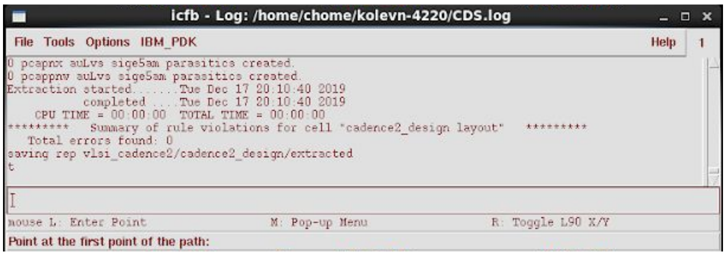


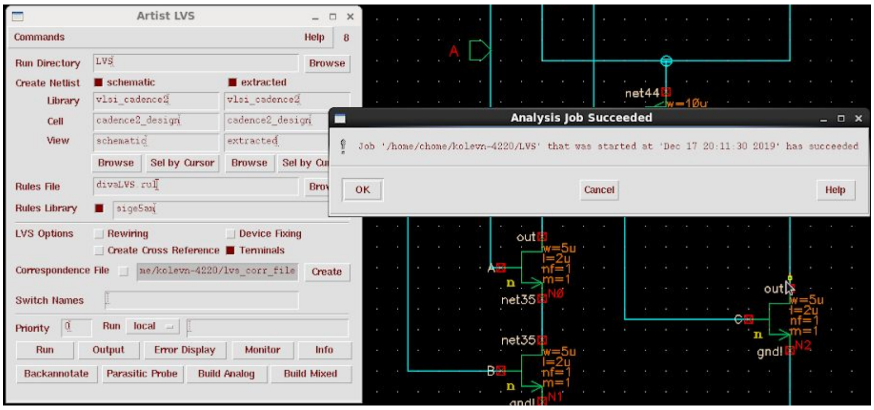
Figure 12: Extracted view of the layout



icfb - Log: /home/chome/kolevn-4220/CDS.log
File Tools Options IBM_PDK
Help
1

```
0 pcapnx auLvs sige5am parasitics created.
0 pcappnv auLvs sige5am parasitics created.
Extraction started......Tue Dec 17 20:10:40 2019
           completed ....Tue Dec 17 20:10:40 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "cadence2_design layout"   *********
   Total errors found: 0
saving rep vlsi_cadence2/cadence2_design/extracted
t

mouse L: Enter Point                    M: Pop-up Menu                    R: Toggle L90 X/Y
Point at the first point of the path:
```

Figure 13: Extraction error results



Artist LVS

Run Directory: LVS

Create Netlist: ■ schematic ■ extracted

	schematic	extracted
Library	vlsi_cadence2	vlsi_cadence2
Cell	cadence2_design	cadence2_design
View	schematic	extracted

Rules File: divaLVS.rul

Rules Library: ■ sige5am

LVS Options: □ Rewiring □ Device Fixing □ Create Cross Reference ■ Terminals

Correspondence File: □ me/kolevn-4220/lvs_corr_file

Switch Names:

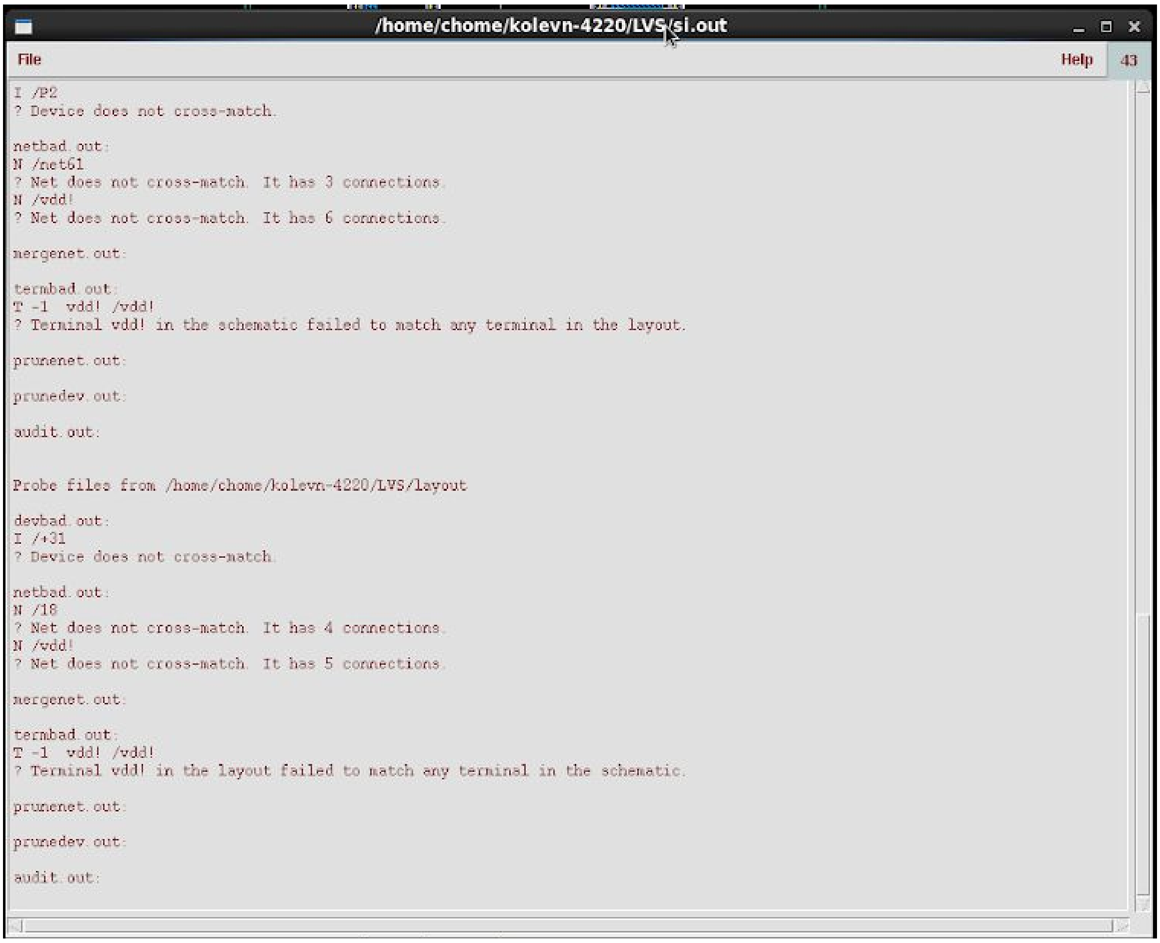
Priority: 0 Run: local

Analysis Job Succeeded

Job '/home/chome/kolevn-4220/LVS' that was started at 'Dec 17 20:11:30 2019' has succeeded

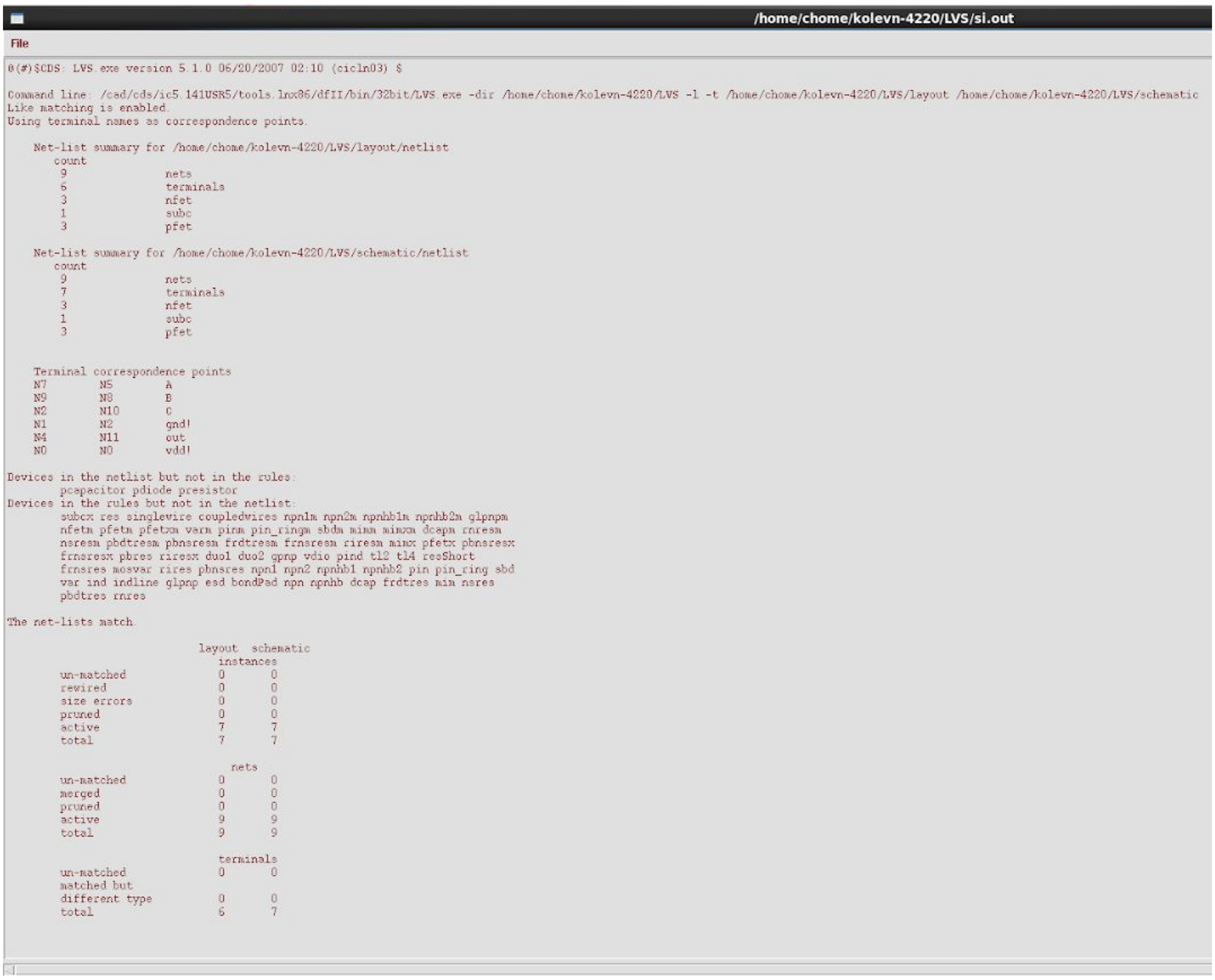
Figure 14: LVS check results

The layout extraction can be seen in Figure 12 above. It came out with no errors, as can be seen in Figure 13. Afterwards, the LVS check was run on the layout and succeeded once problems such as misaligned contacts were fixed. Once fixed, the layout passed through DRC and was re-extracted, the LVS check was successful, as can be observed in Figure 14.



```
I /P2
? Device does not cross-match.

netbad.out:
N /net61
? Net does not cross-match.  It has 3 connections.
N /vdd!
? Net does not cross-match.  It has 6 connections.

mergenet.out:

termbad.out:
T -1  vdd! /vdd!
? Terminal vdd! in the schematic failed to match any terminal in the layout.

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/chome/kolevn-4220/LVS/layout

devbad.out:
I /+31
? Device does not cross-match.

netbad.out:
N /18
? Net does not cross-match.  It has 4 connections.
N /vdd!
? Net does not cross-match.  It has 5 connections.

mergenet.out:

termbad.out:
T -1  vdd! /vdd!
? Terminal vdd! in the layout failed to match any terminal in the schematic.

prunenet.out:

prunedev.out:

audit.out:
```

Figure 15: Netlists match check, original

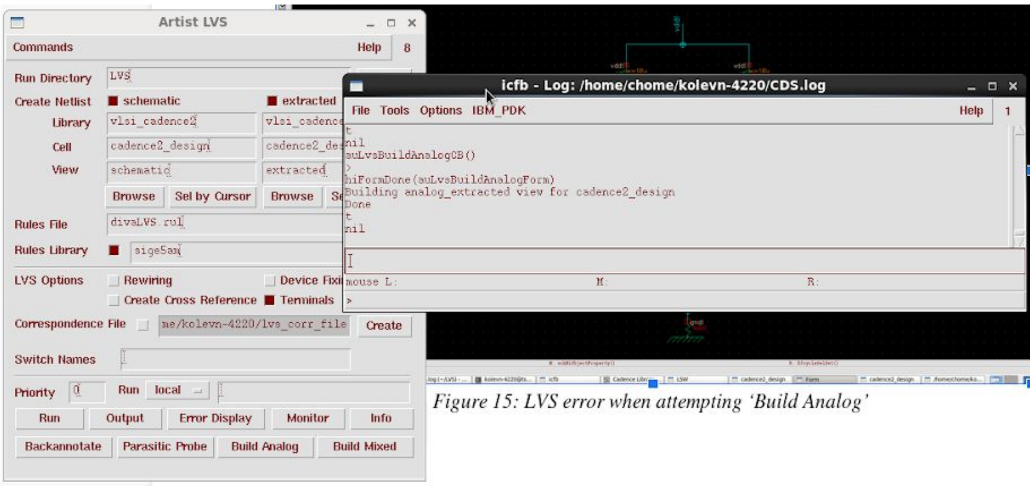


```
@(#)$CDS: LVS.exe version 5.1.0 06/20/2007 02:10 (cicln03) $

Command line: /cad/cds/ic5.141USR5/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/chome/kolevn-4220/LVS -l -t /home/chome/kolevn-4220/LVS/layout /home/chome/kolevn-4220/LVS/schematic
Like matching is enabled.
Using terminal names as correspondence points.

    Net-list summary for /home/chome/kolevn-4220/LVS/layout/netlist
       count
        9               nets
        6               terminals
        3               nfet
        1               subc
        3               pfet

    Net-list summary for /home/chome/kolevn-4220/LVS/schematic/netlist
       count
        9               nets
        7               terminals
        3               nfet
        1               subc
        3               pfet


    Terminal correspondence points
    N7        N5        A
    N9        N8        B
    N2        N10       C
    N1        N2        gnd!
    N4        N11       out
    N0        N0        vdd!

Devices in the netlist but not in the rules:
        pcapacitor pdiode presistor
Devices in the rules but not in the netlist:
        subcx res singlewire coupledwires npn1m npn2m npnhb1m npnhb2m glpnpm
        nfetm pfetm pfetxm varm pinm pin_ringm sbdm mimm mimxm dcapm rnresm
        nsresm pbdtresm pbnsresm frdtresm frnsresm riresm mimx pfetx pbnsresx
        frnsresx pbres riresx duo1 duo2 gpnp vdio pind tl2 tl4 resShort
        frnsres mosvar rires pbnsres npn1 npn2 npnhb1 npnhb2 pin pin_ring sbd
        var ind indline glpnp esd bondPad npn npnhb dcap frdtres mim nsres
        pbdtres rnres

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  7       7
        total                   7       7

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  9       9
        total                   9       9

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   6       7
```

Figure 16: Net-list match check, fixed

Lastly, before attempting the post-layout simulation, the si.out file was checked to ensure that the netlists of the schematic and layout matched, in order to ensure that the simulation would run successfully. They initially did not due to misaligned wires that could not be adjusted without re-doing the layout schematic. This error prevented further build-analog actions, since parts of the LVS tests were failing. Therefore, the layout was redesigned to better match the schematic and re-extracted, as mentioned above. This redesign fixed the mismatch error, as can be seen in Figure 16 above, and allowed for the simulation to be completed. The process of simulation build can be observed in the following section and figures.

6. Post-Layout Simulation



Artist LVS

Run Directory: LVS

Create Netlist: ■ schematic ■ extracted

Library: vlsi_cadence2 | vlsi_cadence

Cell: cadence2_design | cadence2_des

View: schematic | extracted

Rules File: divaLVS.rul

Rules Library: ■ sige5am

LVS Options: □ Rewiring □ Device Fixi □ Create Cross Reference ■ Terminals

Correspondence File: □ me/kolevn-4220/lvs_corr_file

Switch Names:

Priority: 0 Run: local

icfb - Log: /home/chome/kolevn-4220/CDS.log

```
t
nil
auLvsBuildAnalogCB()
>
hiFormDone(auLvsBuildAnalogForm)
Building analog_extracted view for cadence2_design
Done
t
nil
```

```
mouse L:                    M:                    R:
>
```

Figure 15: LVS error when attempting 'Build Analog'

Figure 17: Build Analog after netlist match

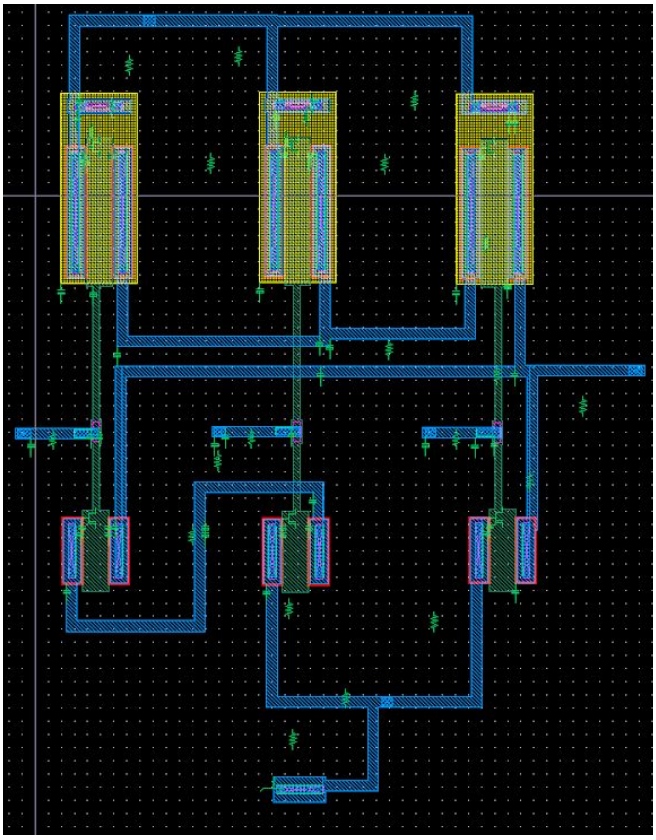
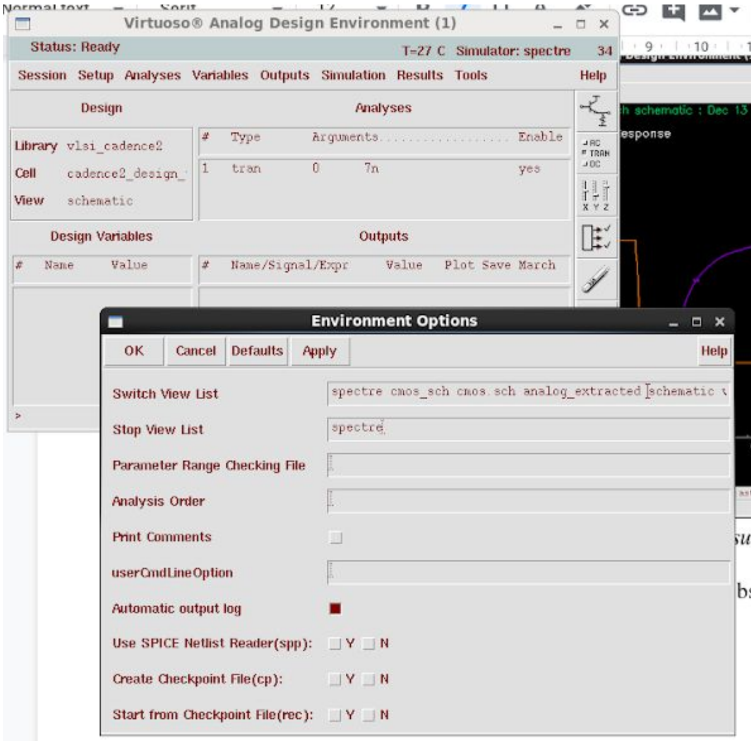


Figure 18: Analog_extracted file view


Virtuoso® Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre
34
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Analyses
Design Variables
Outputs
Environment Options
OK Cancel Defaults Apply Help

Library vlsi_cadence2
Cell cadence2_design_
View schematic

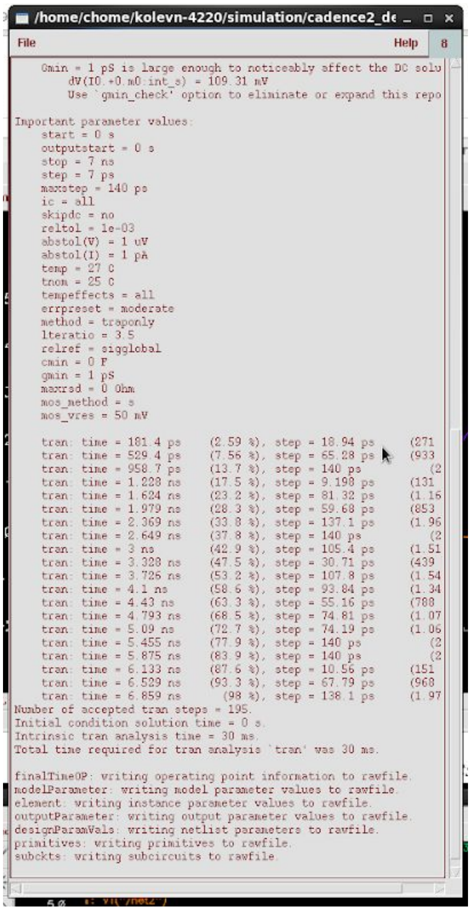
#	Type	Arguments................	Enable
1	tran	0 7n	yes

#	Name	Value

#	Name/Signal/Expr	Value	Plot	Save	March

Switch View List	spectre cmos_sch cmos.sch analog_extracted schematic v
Stop View List	spectre
Parameter Range Checking File	
Analysis Order	
Print Comments	□
userCmdLineOption	
Automatic output log	■
Use SPICE Netlist Reader(spp):	□ Y □ N
Create Checkpoint File(cp):	□ Y □ N
Start from Checkpoint File(rec):	□ Y □ N

Figure 19: Changing testbench environment options to analog_extracted file



```
    Gmin = 1 pS is large enough to noticeably affect the DC solu
        dV(I0.+0.m0:int_s) = 109.31 mV
        Use `gmin_check' option to eliminate or expand this repo

Important parameter values:
    start = 0 s
    outputstart = 0 s
    stop = 7 ns
    step = 7 ps
    maxstep = 140 ps
    ic = all
    skipdc = no
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 25 C
    tempeffects = all
    errpreset = moderate
    method = traponly
    lteratio = 3.5
    relref = sigglobal
    cmin = 0 F
    gmin = 1 pS
    maxrsd = 0 Ohm
    mos_method = s
    mos_vres = 50 mV

    tran: time = 181.4 ps    (2.59 %), step = 18.94 ps     (271
    tran: time = 529.4 ps    (7.56 %), step = 65.28 ps     (933
    tran: time = 958.7 ps    (13.7 %), step = 140 ps         (2
    tran: time = 1.228 ns    (17.5 %), step = 9.198 ps     (131
    tran: time = 1.624 ns    (23.2 %), step = 81.32 ps     (1.16
    tran: time = 1.979 ns    (28.3 %), step = 59.68 ps     (853
    tran: time = 2.369 ns    (33.8 %), step = 137.1 ps     (1.96
    tran: time = 2.649 ns    (37.8 %), step = 140 ps         (2
    tran: time = 3 ns        (42.9 %), step = 105.4 ps     (1.51
    tran: time = 3.328 ns    (47.5 %), step = 30.71 ps     (439
    tran: time = 3.726 ns    (53.2 %), step = 107.8 ps     (1.54
    tran: time = 4.1 ns      (58.6 %), step = 93.84 ps     (1.34
    tran: time = 4.43 ns     (63.3 %), step = 55.16 ps     (788
    tran: time = 4.793 ns    (68.5 %), step = 74.81 ps     (1.07
    tran: time = 5.09 ns     (72.7 %), step = 74.19 ps     (1.06
    tran: time = 5.455 ns    (77.9 %), step = 140 ps         (2
    tran: time = 5.875 ns    (83.9 %), step = 140 ps         (2
    tran: time = 6.133 ns    (87.6 %), step = 10.56 ps     (151
    tran: time = 6.529 ns    (93.3 %), step = 67.79 ps     (968
    tran: time = 6.859 ns      (98 %), step = 138.1 ps     (1.97
Number of accepted tran steps = 195.
Initial condition solution time = 0 s.
Intrinsic tran analysis time = 30 ms.
Total time required for tran analysis `tran' was 30 ms.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
```

Figure 20: Simulation log check successful

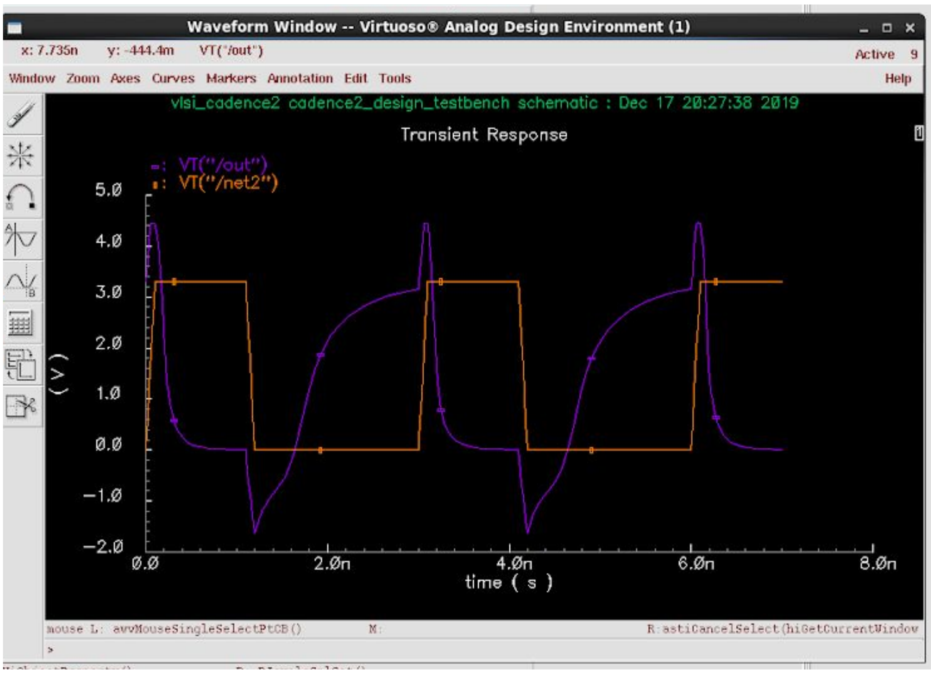

Waveform Window -- Virtuoso® Analog Design Environment (1)
x: 7.735n
y: -444.4m
VT("/out")
Active 9
Window
Zoom
Axes
Curves
Markers
Annotation
Edit
Tools
Help
vlsi_cadence2 cadence2_design_testbench schematic : Dec 17 20:27:38 2019
Transient Response
VT("/out")
VT("/net2")
5.0
4.0
3.0
2.0
1.0
0.0
−1.0
−2.0
(V)
0.0
2.0n
4.0n
6.0n
8.0n
time (s)
mouse L: avvMouseSingleSelectPtCB()
M:
R:astiCancelSelect(hiGetCurrentWindow
>

Figure 21: Analog_extracted post-simulation result

In the figures above, the process of building the analog_extracted view. The process begins with clicking the Build Analog option on the Artist LVS window, after which a new extracted view is built. Once this is done, the simulation view list is modified to include this analog_extracted view and the post-layout simulation is run. This post-layout simulation can be seen in Figure 21 above. It differs from the original because the analog_extracted file, which is built upon the layout, is referred to when running the simulation, as opposed to the base schematic file.

7. Simulation Results

As can be seen through the simulation results of the schematic and extracted analog files, an analysis of the transient response of f=(AB+C)’ can be made. This analysis can be further built upon the previous simulation with an inverter, namely that rise and fall times would be affected due to the parasitic elements present in the extracted layout file. This speculation ends up being correct, as can be observed in the two simulation images. Therefore, it can once again be concluded that parasitic elements change the behavior of circuits and should be accounted for prior to implementations. As this circuit contains a logic AND and OR gate, rather than just an inverter, the differences are more noticeable in the final simulation, further supporting the argument that larger and more complex circuits should definitely be simulated prior to physical implementation, since ideal behavior cannot be assumed in real-world situations.

8. Conclusion

Through these past two exercises in simulating an inverter and (AB+C)’, it can be predicted that while parasitic capacitance and resistance change the ideal response, they do not fundamentally change how the pre-analog circuit behaves. Though the circuit behaves differently due to its rise and fall times differing from ideal times, the output response remains the same in form and does not fundamentally change its main functionality or transient response. The response being altered due to parasitic elements is expected, based on the parasitic element definition studied in class. Lastly, these slight changes should definitely be noted and taken into account when building real-world circuits, as they can change a circuit’s response, leading to unexpected or unwanted results, especially when combining with more circuit elements or other factors that are not accounted for when designing on paper.