Rensselaer Polytechnic Institute

VLSI Design
ECSE 4220

Report

Project #1
Inverter Design Assignment

Nikoleta Koleva

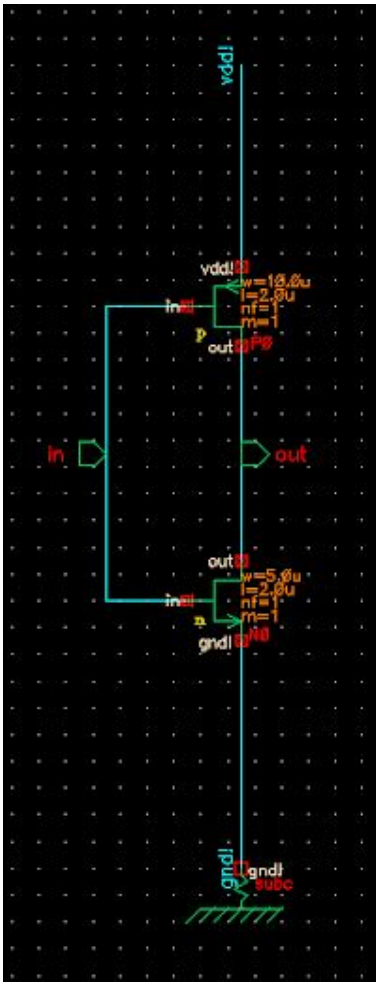
TA: Sagnik Nath
Date: 06-Dec-2019
Instructor: Tong Zhang

Table of Contents

0. **Introduction**

Throughout this report, the Cadence IC design tool was used to build and simulate an inverter, using a pfet and an nfet. First, an ideal inverter was built, after which a real-world simulation was compared. The inverter was first tested in ideal circumstances, after which a layout was built upon it but using a real-world setbacks, such as parasitic capacitance and resistance. The responses were then compared and a conclusion was drawn.

1. **Circuit Schematic**



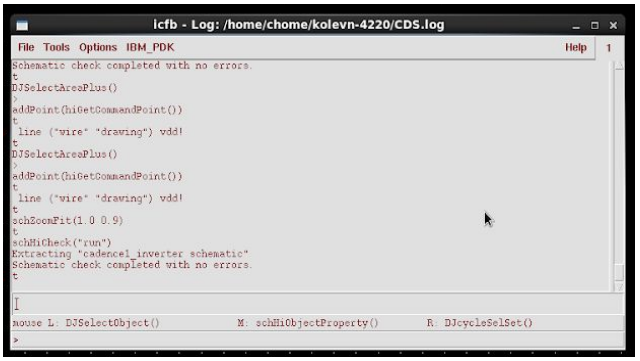


Figure 1: Full schematic of inverter circuit *Figure 2: Schematic 'Check' results*

Figure 1 above displays the inverter circuit initially built in Cadence. To create it, the pfet width was set to 10um and length to 2um. The nfet width was set as 5um and length as 2um. Initially, there were errors given when trying to connect the Input and Output pins but they were fixed, once the source and ground connections were adjusted to be 'vdd!' and 'gnd!' respectively. Figure 2 displays the results obtained by using the 'Check' option to look for any schematic errors. Furthermore, later on LVS was failing due to subc not being added to the schematic. Once this was done, LVS succeeded.

2. **Schematic Simulation Results**

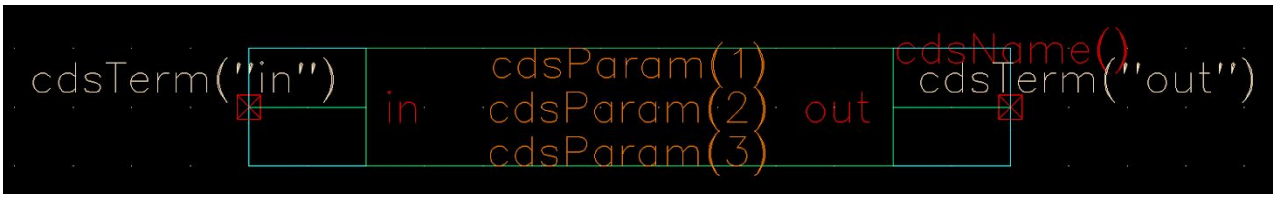


Figure 3: Confirmation of symbol creation

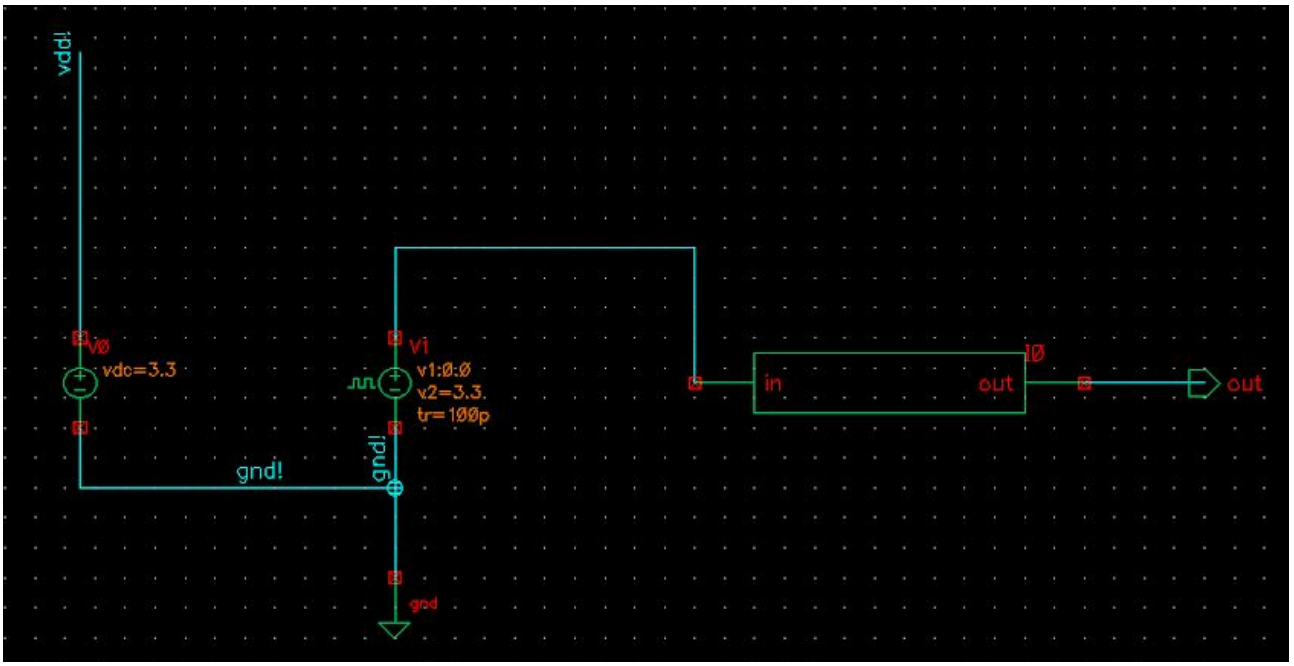


Figure 4: Schematic testbench circuit setup

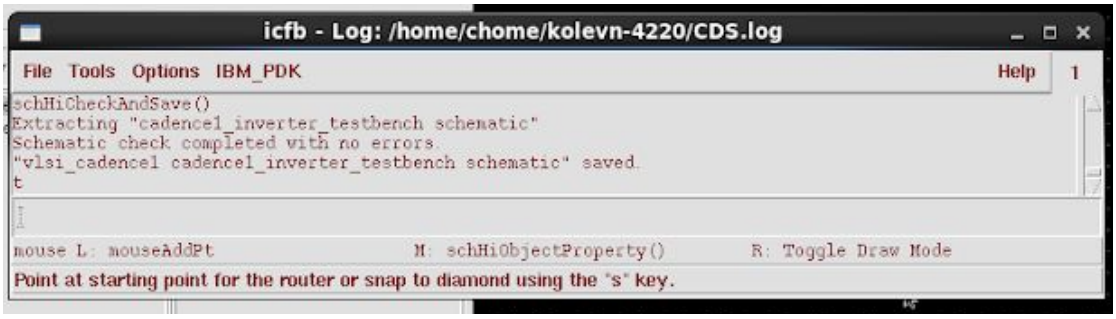


Figure 5: Schematic testbench circuit 'Check and Save' result

For the simulation, a testbench cellview was built to implement the inverter previously built. Additionally, ground, a VDC and a VPULSE sources were added. The VDC DC voltage was set to 3.3V and the VPULSE specs were as follows: DC voltage - 3.3V, Voltage 2 - 3.3V, Rise time - 100ps, Fall time - 100ps, Pulse width - 1ns, Period - 3ns. Once this was built and checked successfully, the simulation was initiated.

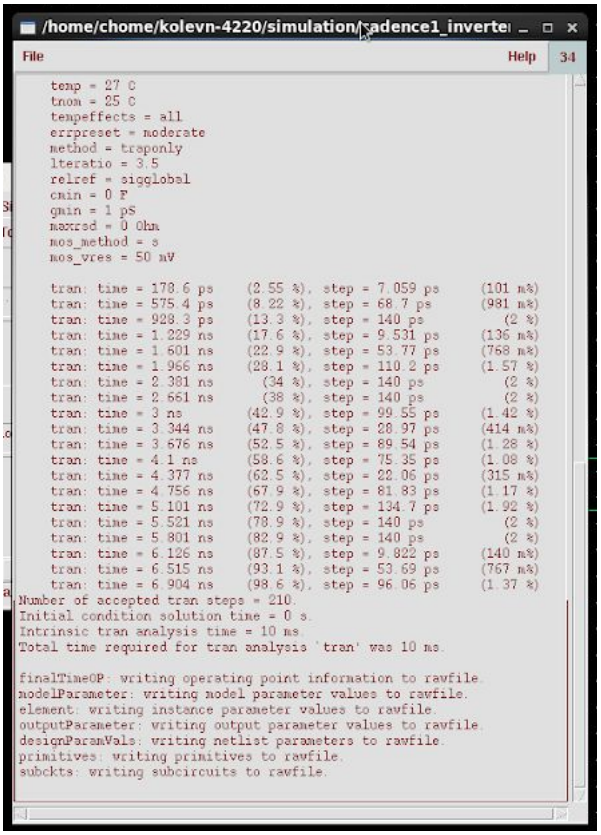


Figure 6: Simulation/Testbench netlist results

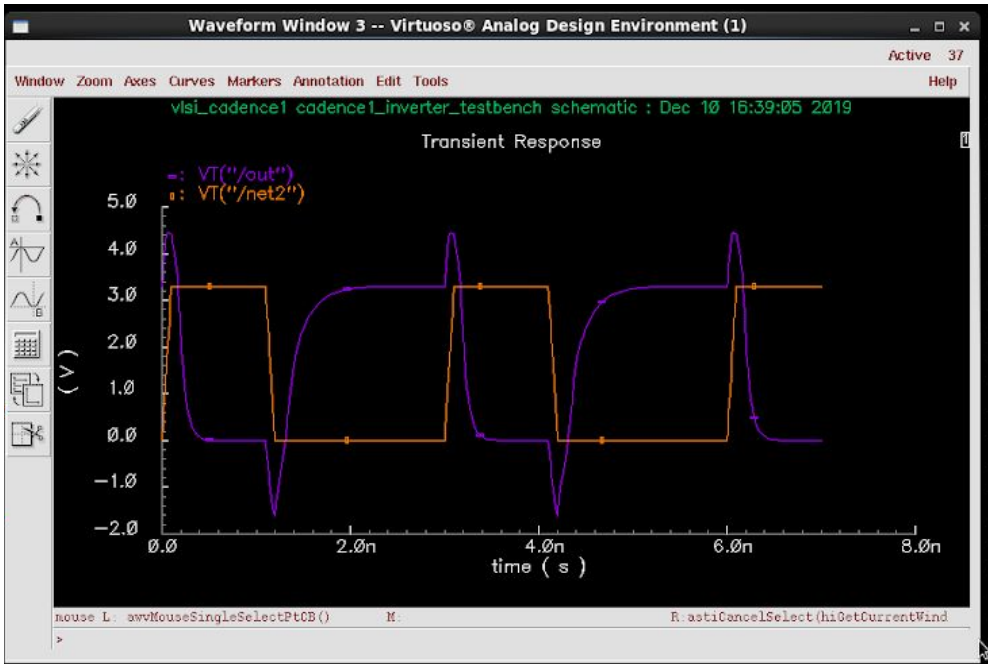


Figure 7: Schematic simulation result

In Figure 7 above, the result of the simulation can be observed. It was done with a 7ns stop time and done for the schematic file of the inverter. This is the ideal response for the inverter.

3. **Full Layout**

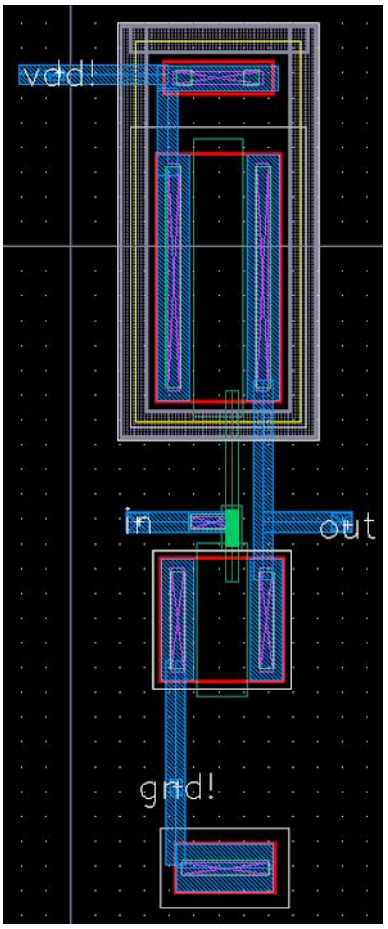


Figure 8: Full layout of inverter circuit

4. **Design Rule Check (DRC) of the layout**

```
*********************************************************************
* END OF ERROR REPORT SUMMARY FOR LINE MODE & ORTHOGONALITY *
*********************************************************************
Start Time = "Dec  9 13:07:57 2019"
Stop Time = "Dec  9 13:07:57 2019"
t
hiiSetCurrentForm('ivDRCOptionsForm)
t
hiFormDone(ivDRCOptionsForm)
DRC started at Mon Dec  9 13:08:01 2019
Validating hierarchy instantiation for:
library: vlsi_cadence1
cell:    cadence1_inverter
view:    layout
Rules come from library sige5am.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started ..... Mon Dec  9 13:08:01 2019
    completed ... Mon Dec  9 13:08:02 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********  Summary of rule violations for cell "cadence1_inverter layout"  *********
 # errors  Violated Rules
       1  #INFO: 3 Level Metal (M1+MT+AM) PADS= WIREBOND #
       1  #INFO: Si0e-5am DIVA DRC DECK (05/04/2004)        #
       2  Total errors found
t
```

Figure 9: DRC check of circuit

In Figure 8 above is the compact cell constructed, which passes DRC, as can be seen in Figure 9 (with only two INFO errors, which are stated as normal/expected in the tutorial document). Initially, there were problems with the contacts, specifically MC_M1 and it wanting to be placed touching the 'OUT' wire when trying to run DRC. When this was done, DRC passed but the compact cell was still incorrect. This was later fixed (as it's a contact for the pc and m1 layers for the 'IN' wire) by aligning it properly on the 'IN' wire. These errors were discovered when running LVS check later, as they did not show up in DRC.

5. **Layout Extraction and Layout vs. Schematic (LVS) check result**

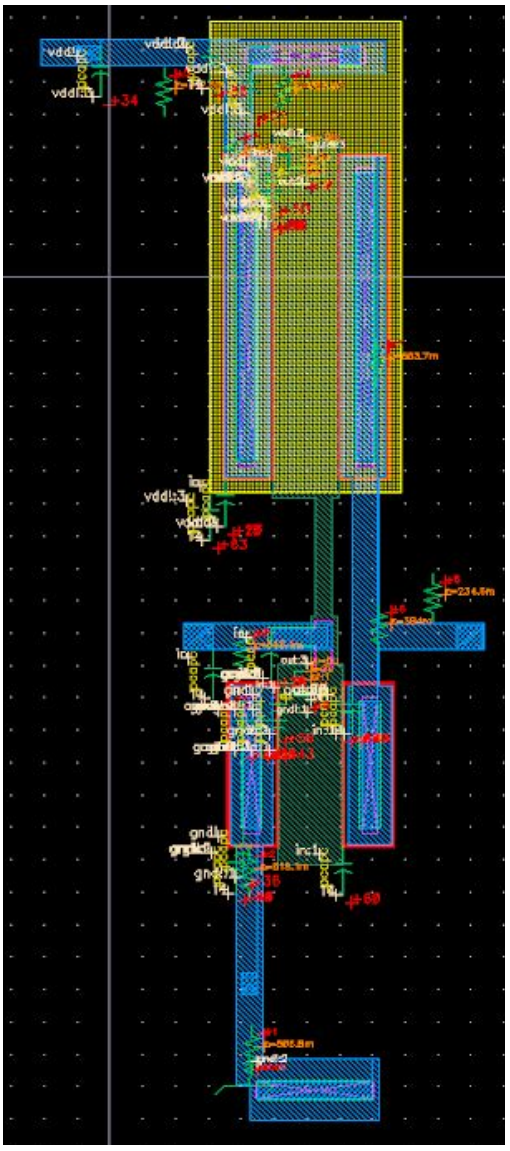


Figure 10: Extracted view of the layout

```
For layer sub_dev :
    1  shapes encountered.
    1  subcx suLvs sige5am devices well formed.
48 pcapc auLvs sige5am parasitics created.
1 pcapnwx auLvs sige5am parasitics created.
0 pcapnx auLvs sige5am parasitics created.
0 pcappnw auLvs sige5am parasitics created.
Extraction started.......Mon Dec  9 13:16:50 2019
            completed ....Mon Dec  9 13:16:51 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "cadence1_inverter layout"   *********
   Total errors found: 0
saving rep vlsi_cadence1/cadence1_inverter/extracted
t
```

Figure 11: Extraction error results

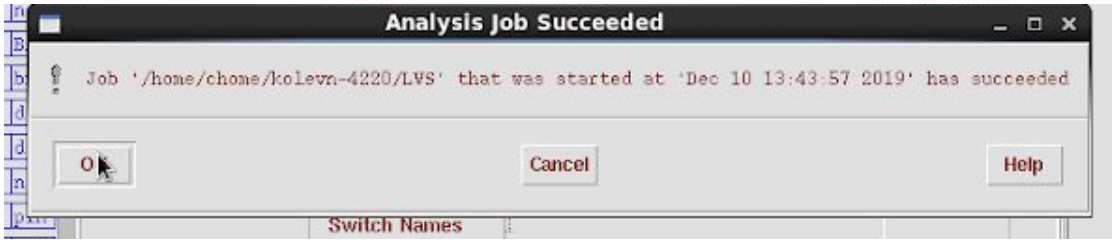


Figure 12: LVS check results

The layout extraction can be seen in Figure 10 above. It came out with no errors. Afterwards, the LVS check was run on the layout and succeeded once the layout and schematic problems were resolved. Those included added a missing subc to the schematic and fixing the contact issues for the 'IN' output. Once these were fixed, the layout passed through DRC and was re-extracted, the LVS check was successful, as can be observed in Figure 12.

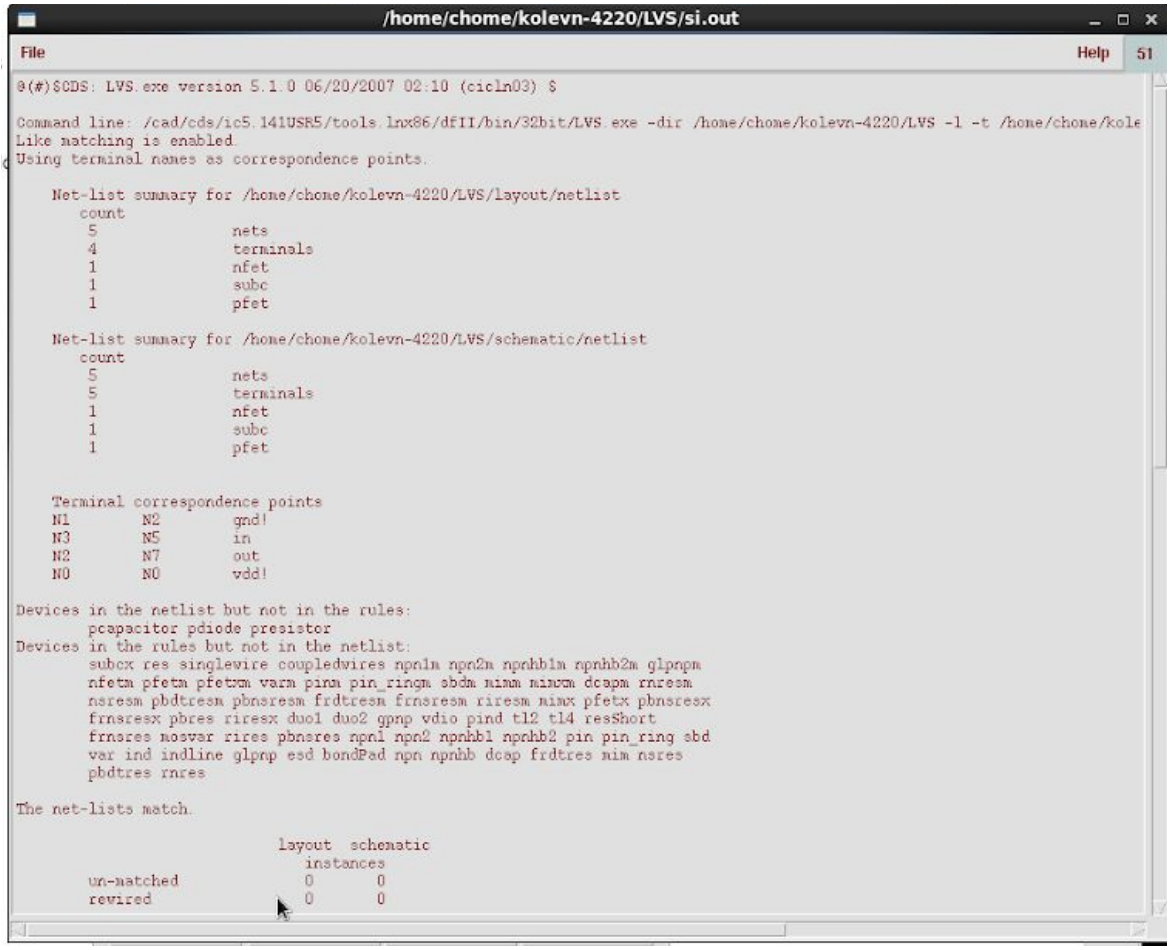


Figure 13: Netlists match check

Lastly, before attempting the post-layout simulation, the si.out file was checked to ensure that the netlists of the schematic and layout matched. This was initially not the case due to the wrong contacts on the 'IN' wire. Once fixed, the netlists matched as desired, as seen in Figure 13.

6. **Post-Layout Simulation**

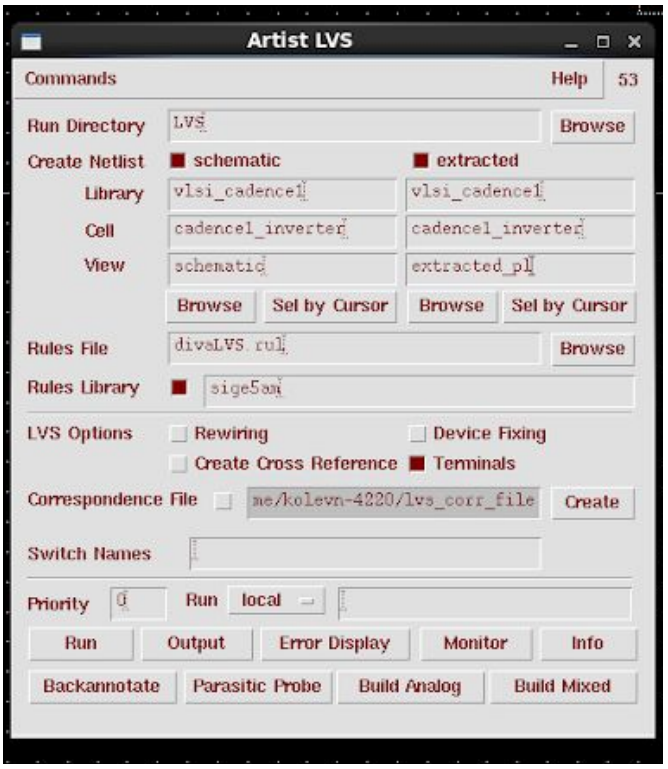


Figure 14: After redoing extraction, rerunning LVS and using 'Build Analog' for analog_extracted

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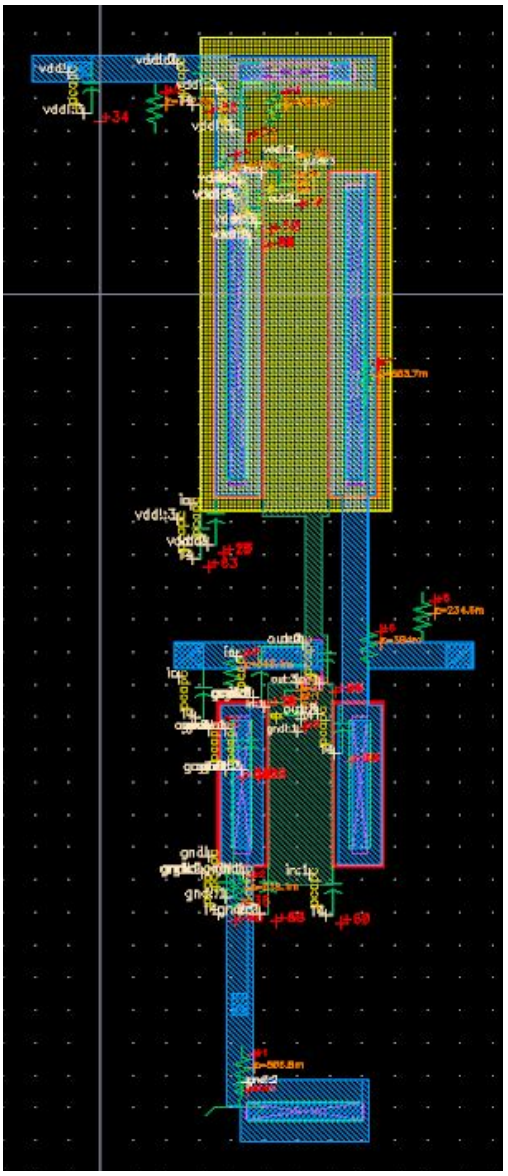

Figure 15: analog_extracted view

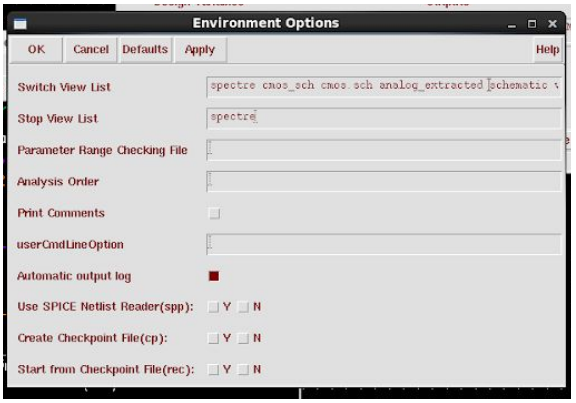

Figure 16: Changing view list in testbench simulation environment by adding analog_extracted for it to refer to that file

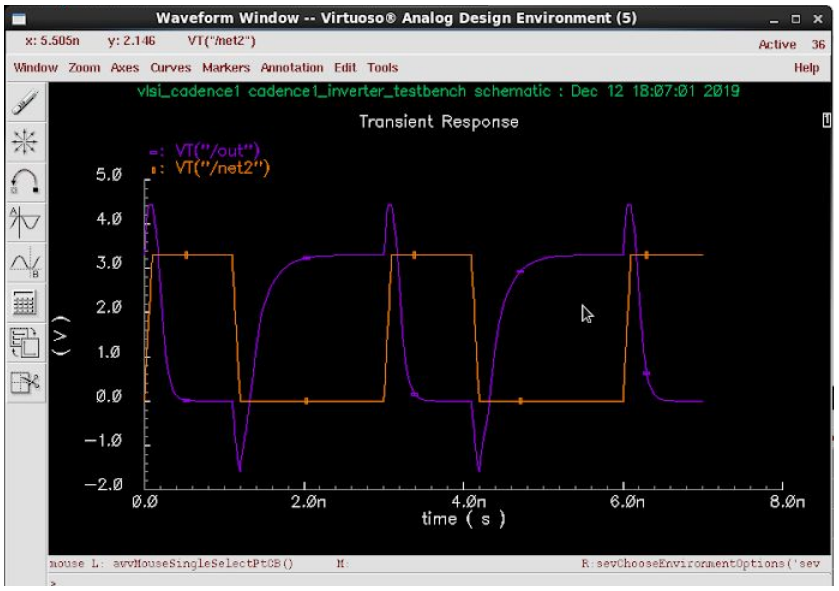

Figure 17: Post-layout simulation result

When preparing for the post-layout simulation, the extracted file had to be updated first to ensure that it was using the latest version of the layout. Once this was done, LVS was rerun (successfully) after which the 'Build Analog' option was selected, which can be seen in Figure 14. After this was done, the testbench circuit was opened once more and in the environment options, 'analog_extracted' was added prior to schematic for the simulation to access the extracted view, rather than the schematic file, as can be observed in Figure 16. Finally, a simulation was run, which can be seen in Figure 17.

7. Simulation Results

The results of the post-layout simulation look pretty similar when first observed but it can also be seen that the analog simulation has shorter rise and fall time compared to the original ideal simulation. These faster changes between states occur due to the parasitic capacitance and resistance added in the extracted layouts. They are problems that do not have to be taken into account when simulating an ideal inverter but should be considered for real-world simulations, as they can impact a bigger circuit's response. To see the changes more easily, the input frequency can be increased in order to see a more obviously different output response.

8. Conclusion

Through this exercise, it can be concluded that while parasitic capacitance and resistance change the ideal response, they do not fundamentally change how the pre-analog circuit behaves. Though the rise and fall time are altered, the output response keeps its form, meaning the circuit does not fundamentally change its function. This response is due to parasitic elements is expected, based on the parasitic element definition studied in class. However, these slight changes should be taken into account when building real-world circuits, as they can change a circuit's response, leading to unexpected or unwanted results.