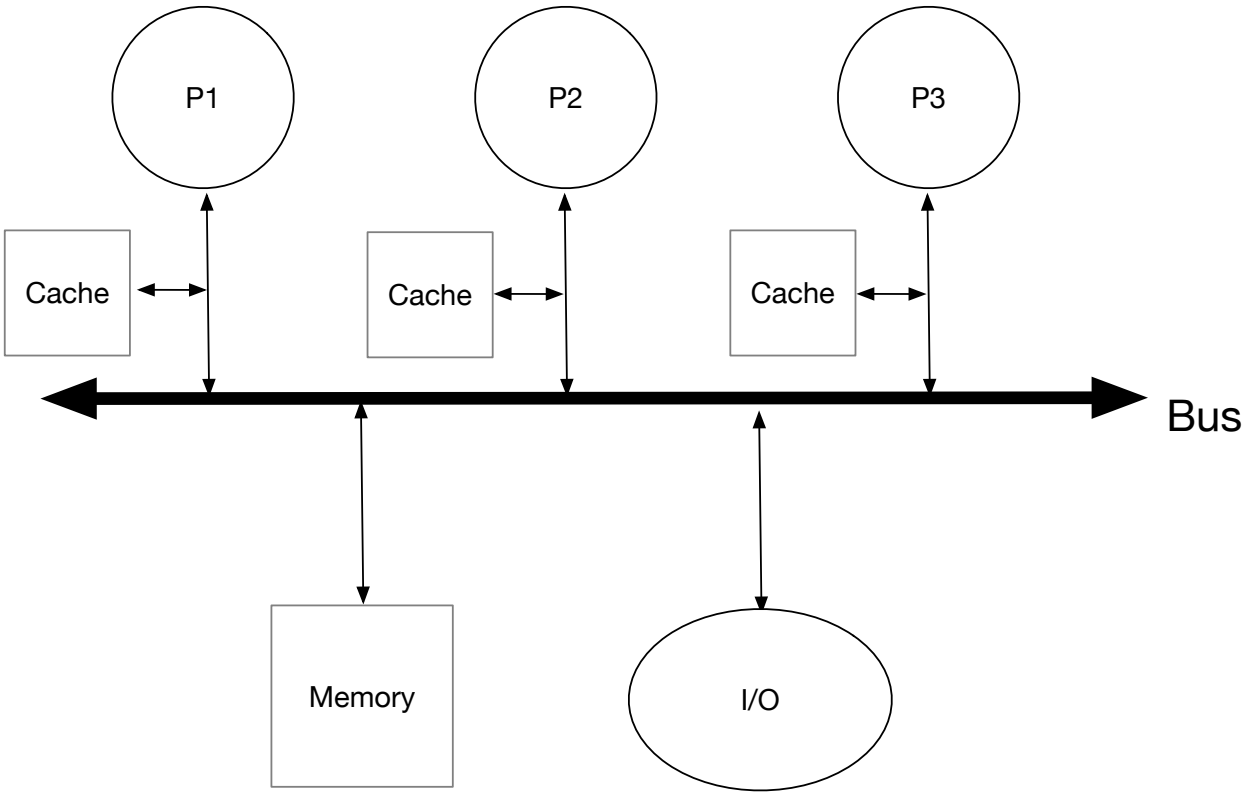
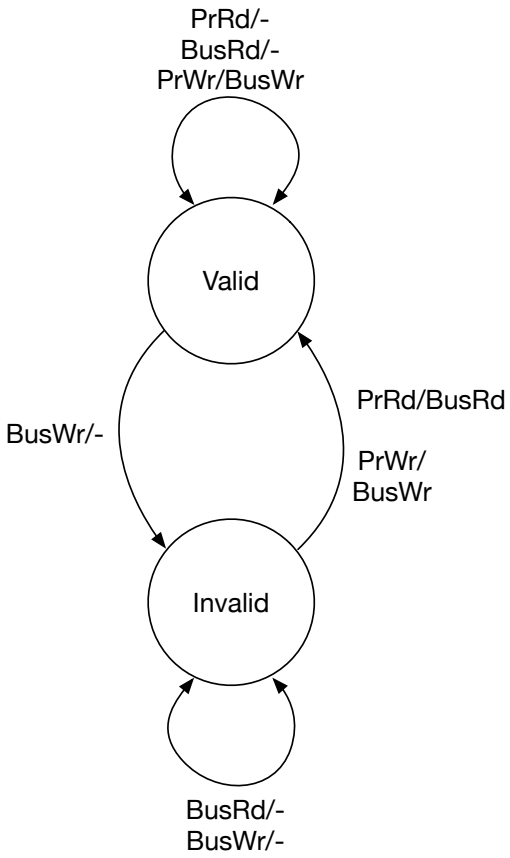


Bus-based Symmetric Multiprocessor



Simple Invalidation Protocol (Valid/Invalid):

Assumes cache is Write-through (memory is kept up-to-date with cache)

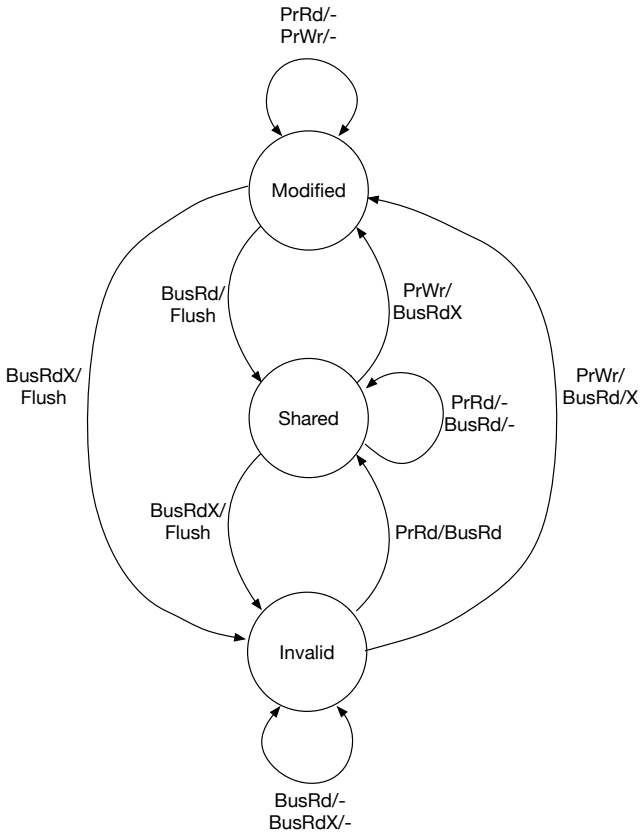
Two states:

Valid - Non-exclusive (i.e. potentially shared) valid state
Invalid - Block is not valid in the cache (includes block is not present in cache)

Actions:

Processor:
PrRd — Processor Read — This processor is reading the block
PrWr — Processor Write — This processor is writing the block

Bus Transactions:
BusRd — A processor requests to read the block from memory using the bus
BusWr —A processor requests to write the block in memory using the bus



MSI Protocol

Assumes cache is write-back (memory is not kept up-to-date with cache for every store). A cache block can be dirty until it is written back to memory

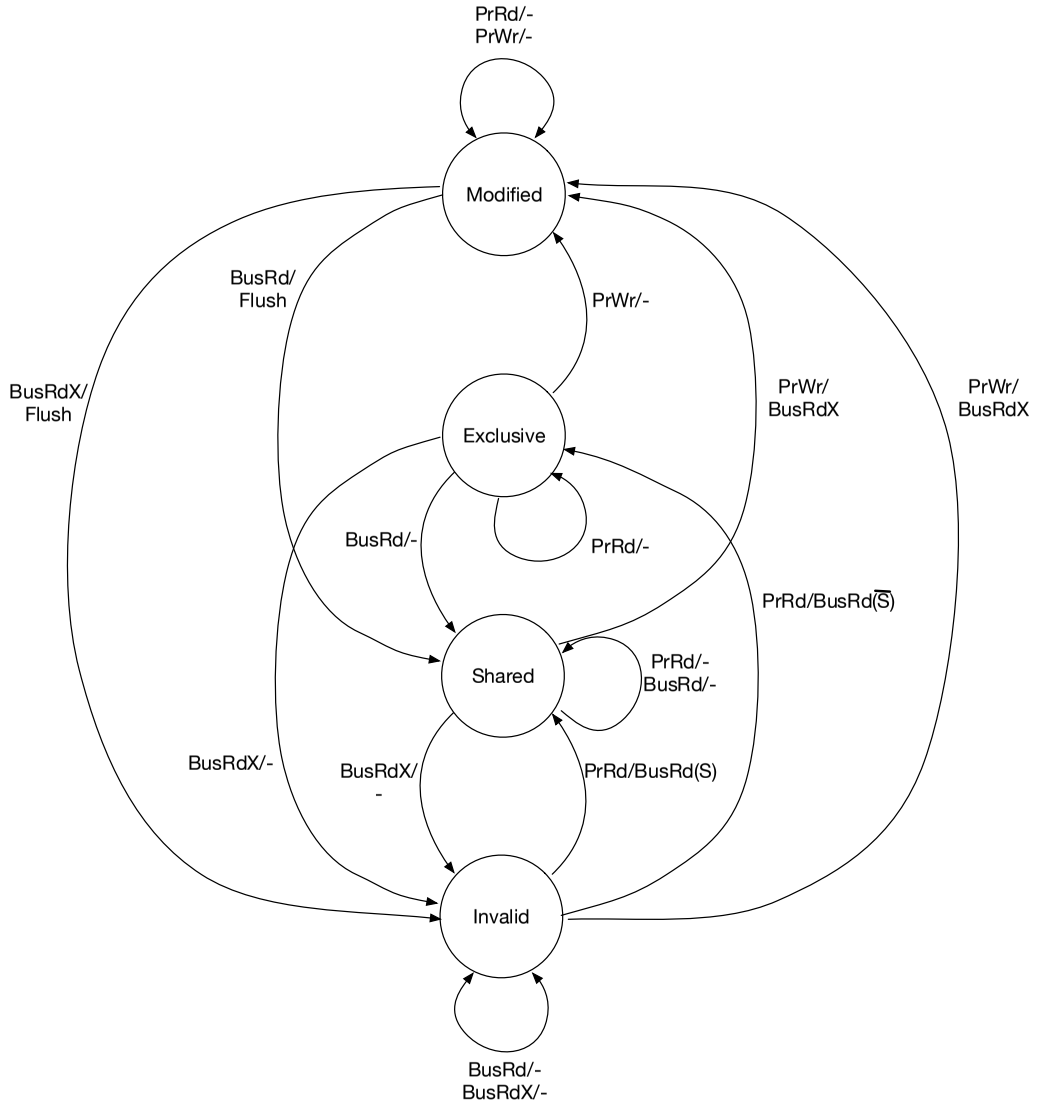
Three states:

Modified - Exclusive, dirty (with respect to memory) but valid state
Shared - Non-exclusive, potentially shared, clean, valid state
Invalid - Block is not valid in the cache (includes block is not present in cache)

Actions:

Processor:
PrRd — Processor Read — This processor is reading the block
PrWr — Processor Write — This processor is writing the block

Bus Transactions:
BusRd — A processor requests to read the block from memory using the bus
BusRdX —A processor requests to read the block from memory with exclusive ownership so it can modify the block
Flush — A processor writes a dirty block back to memory



MESI Protocol

Assumes cache is write-back (memory is not kept up-to-date with cache for every store). A cache block can be dirty until it is written back to memory

Four states:

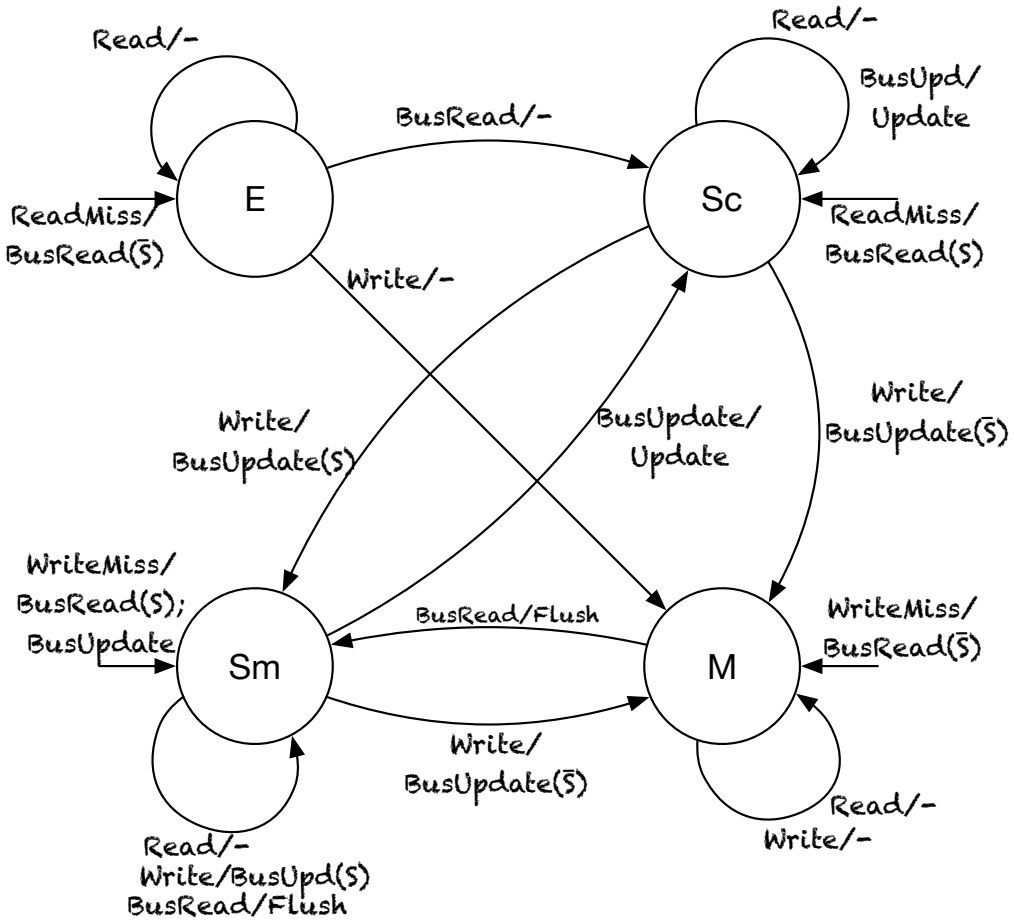
Modified - Exclusive, dirty (with respect to memory) but valid state
Exclusive - Exclusive and clean (with respect to memory), valid state
Shared - Non-exclusive, potentially shared, clean, valid state
Invalid - Block is not valid in the cache (includes block is not present in cache)

Actions:

Processor:
PrRd — Processor Read — This processor is reading the block
PrWr — Processor Write — This processor is writing the block

Bus Transactions:

BusRd(S)— A processor requests to read the block from memory using the bus and at least one other processor responds on wired-OR S bit that the block is shared
BusRd($\overline{S}$)— A processor requests to read the block from memory using the bus and no other processors respond on wired-OR S bit that the block is shared
BusRd— A processor requests to read the block from memory using the bus (Whether shared or not)
BusRdX —A processor requests to read the block from memory with exclusive ownership so it can modify the block
Flush — A processor writes a dirty block back to memory



Dragon Update Protocol