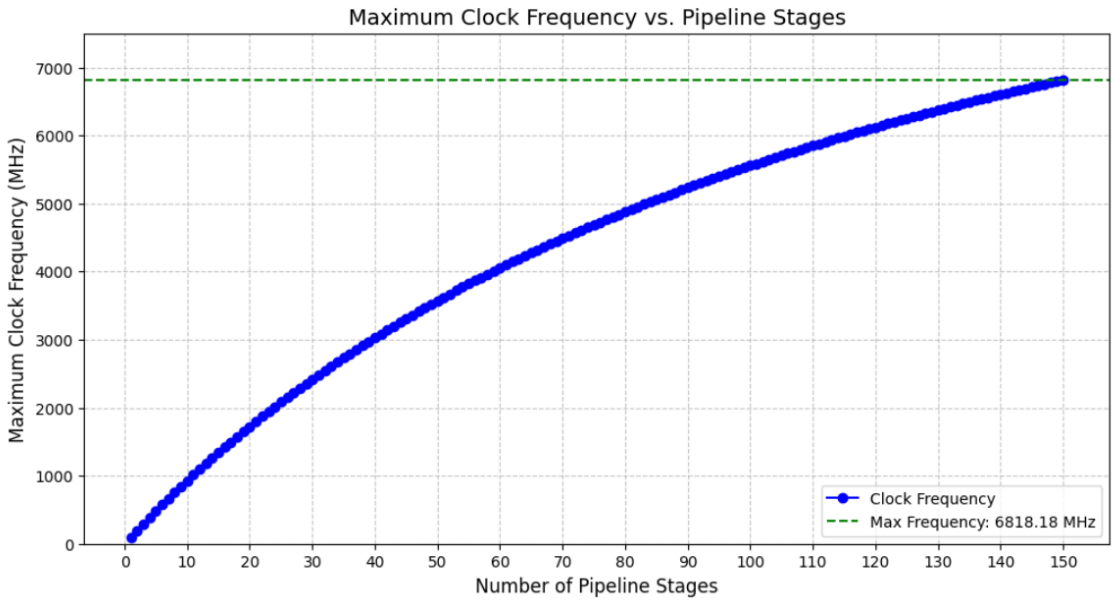
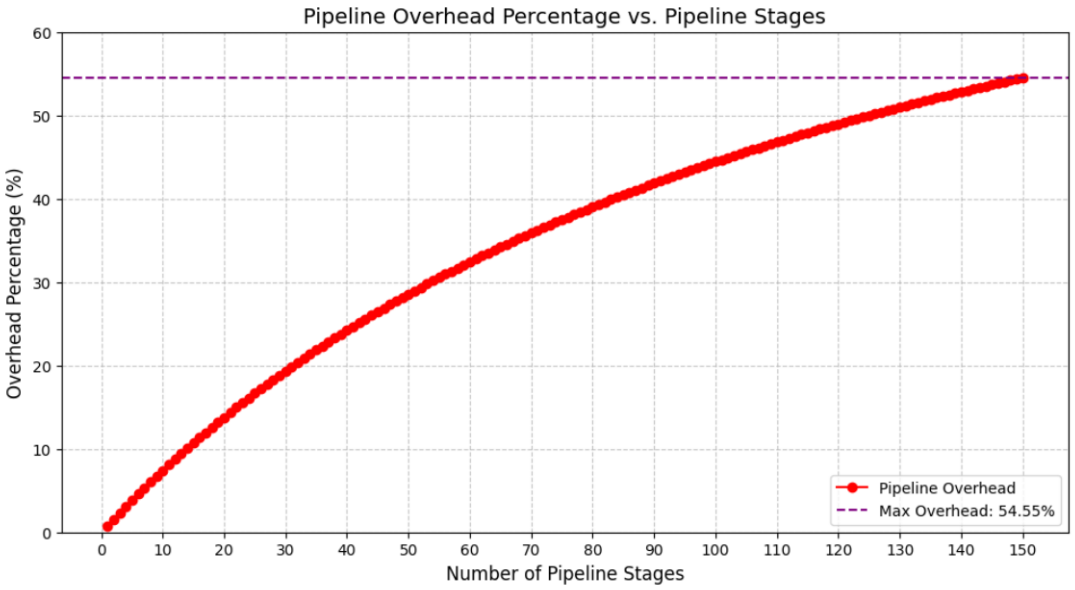
Question 1

i. Maximum Clock Frequency:



ii. Percentage Overhead VS Pipeline Stages



Question 2:

The maximum theoretical frequency would be:

Formula:

$$f_{max} = \frac{1}{T_{slowest\ stage}}$$

Frequency impact of latches Even assuming no internal fragmentation, $f_{max\ /\ pipelined} = \frac{1}{(T)_{stage} + T_{latch}}$. For an infinitely deep pipeline, $f_{max\ /\ pipelined} = \frac{1}{T_{latch}}$. Thus, there are diminishing returns from ever-deeper pipelines, with the limit of the performance improvement determined by the latency of the latch used.

Given

Latency = 80 ps = 80 * 10^{-12} seconds

Therefore

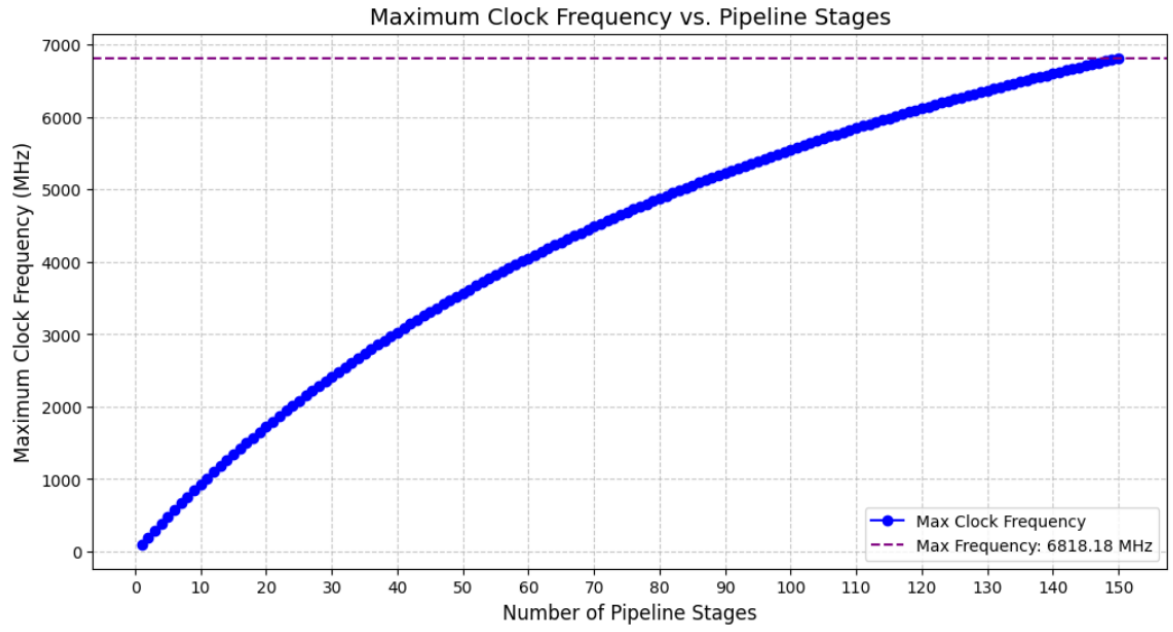
$f_{\max} = \frac{1}{80*10^{-12}}$

12.5 GHz

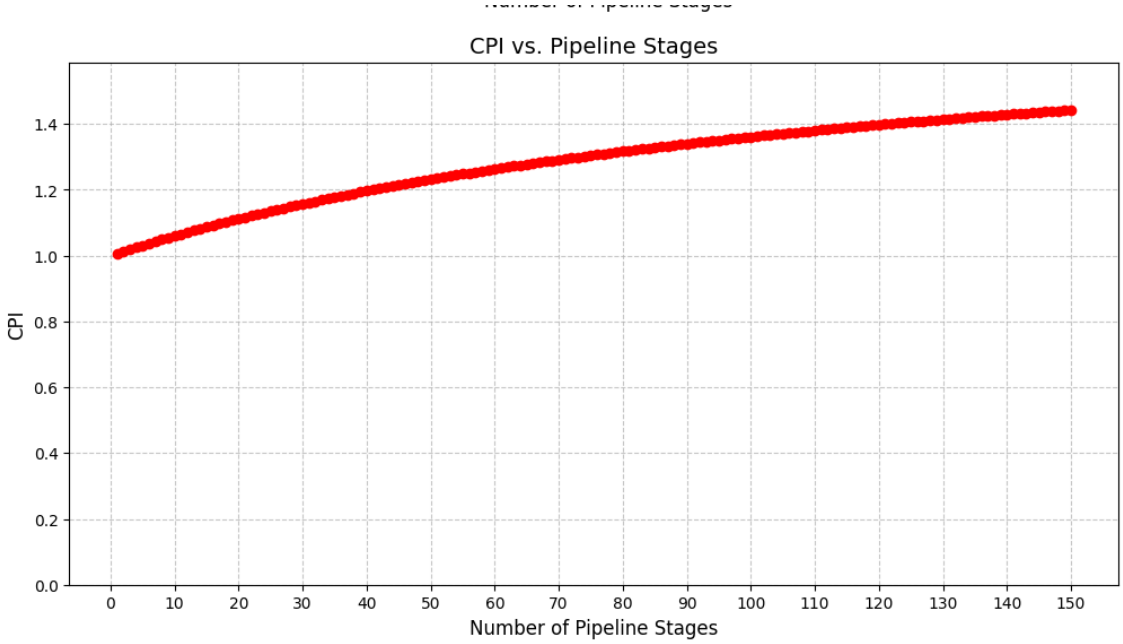
The Maximum Theoretical frequency would be 12.5 GHz

Question 3:

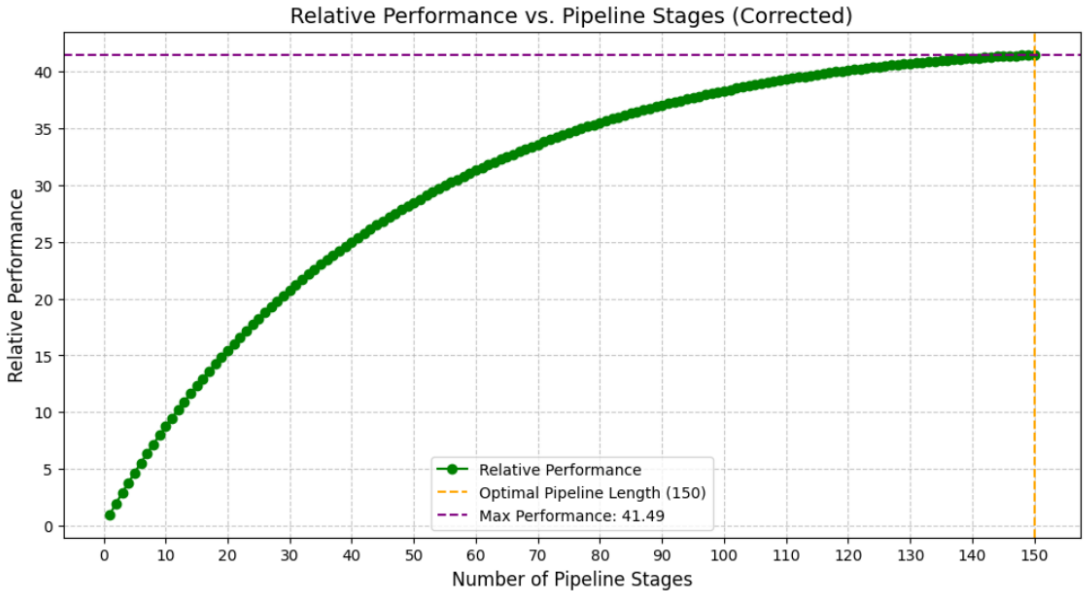
i. Maximum Clock Frequency vs Pipeline Stages



ii. CPI vs Pipeline stages

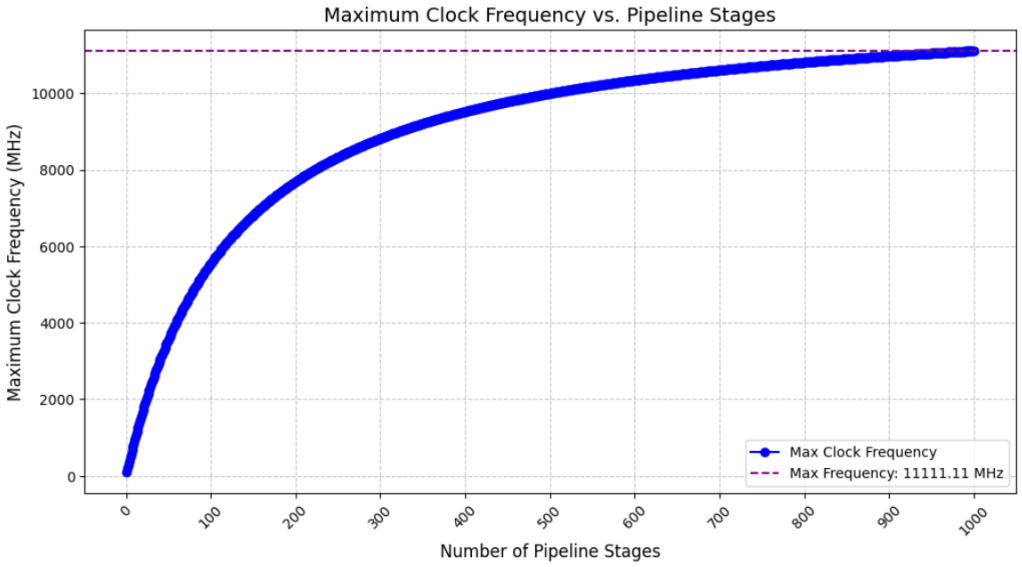


iii. Relative Performance vs Pipeline Stages

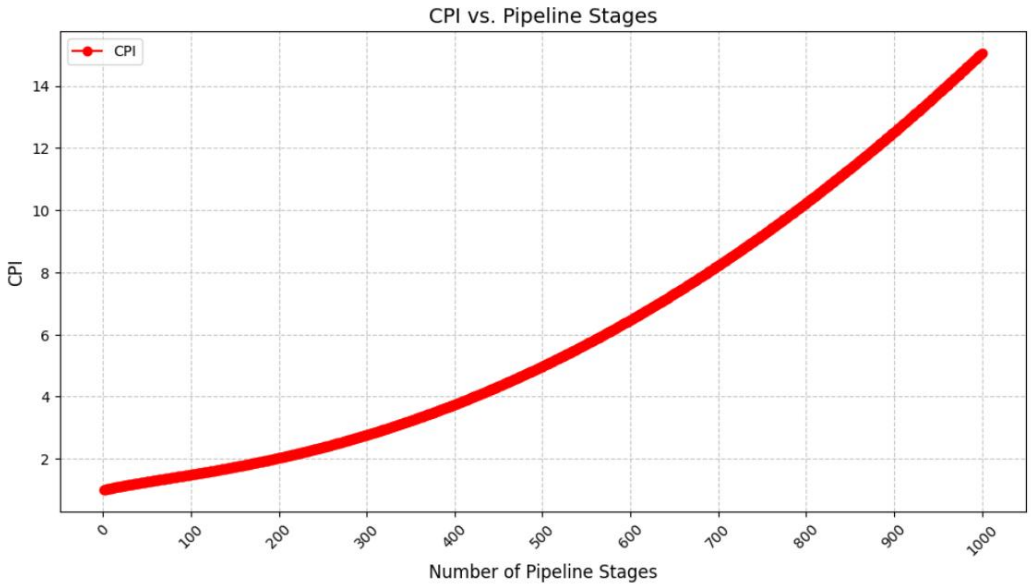


Question 4:

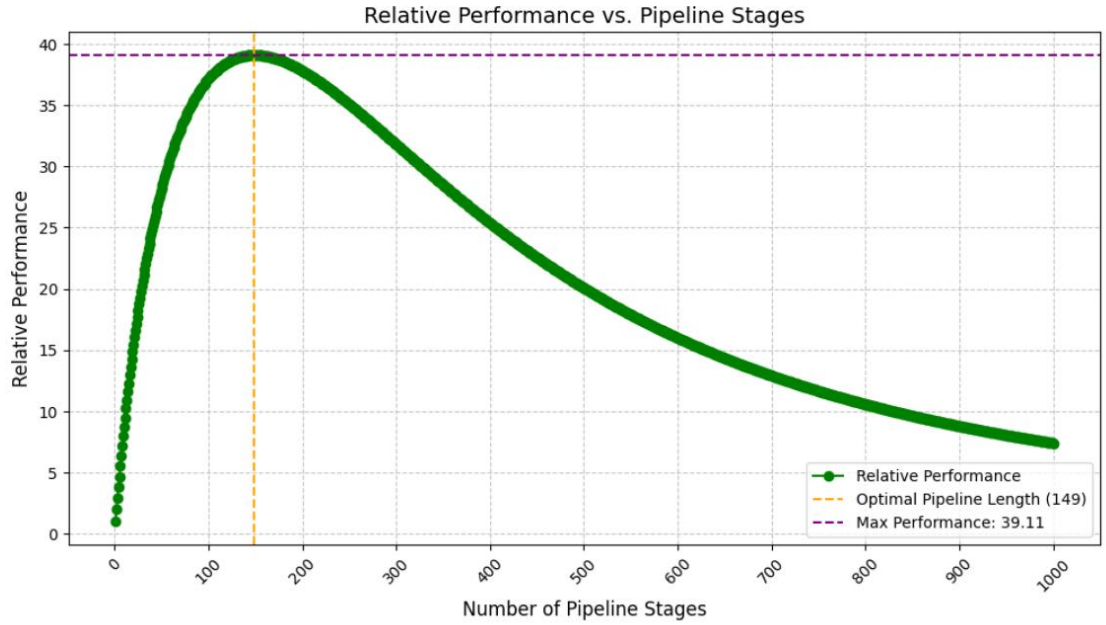
i. Maximum clock frequency vs Pipeline stages:



ii. CPI vs Pipeline stages

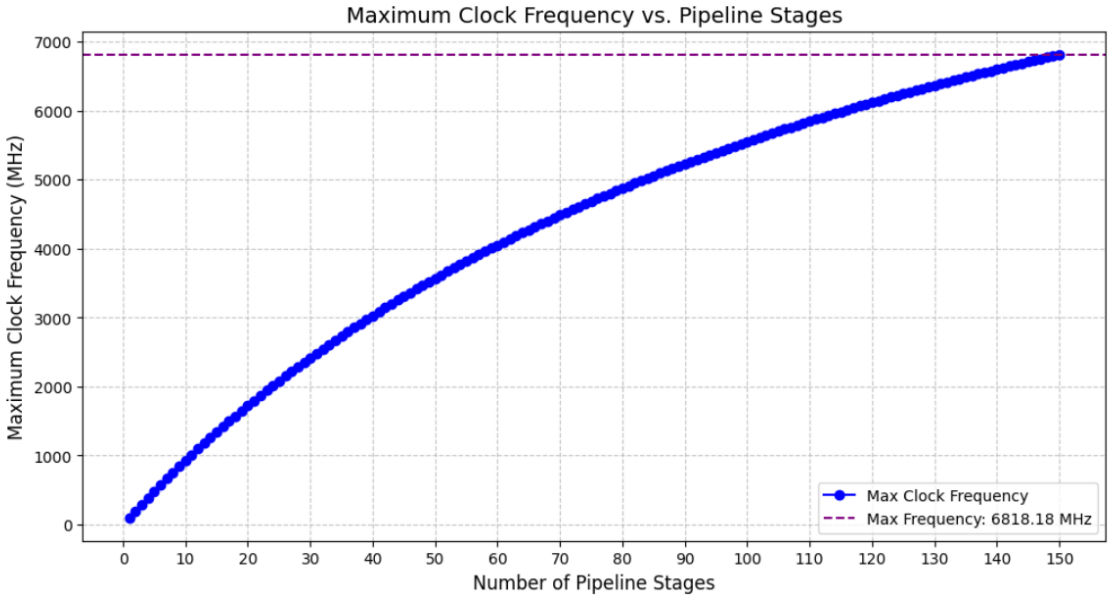


iii. Relative performance vs Pipeline stages:

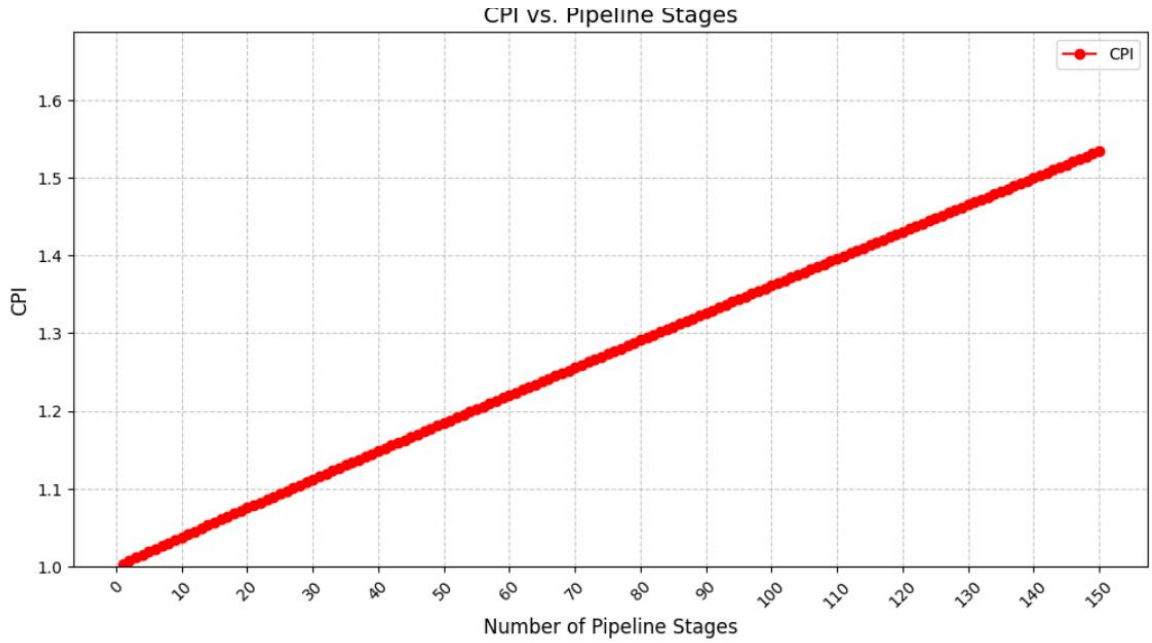


Question 5:

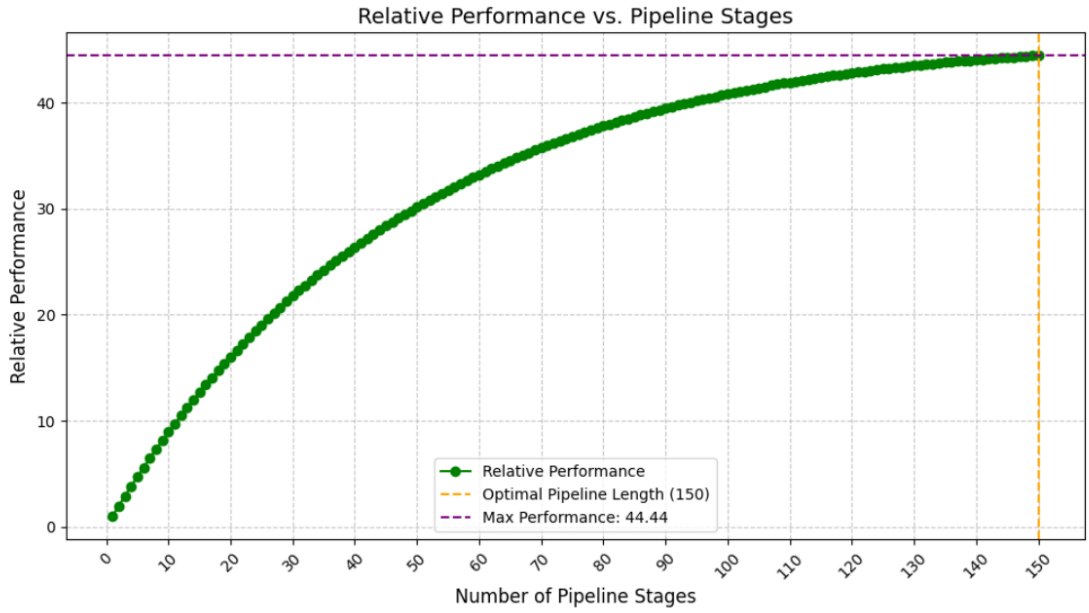
i. Maximum clock frequency vs Pipeline stages



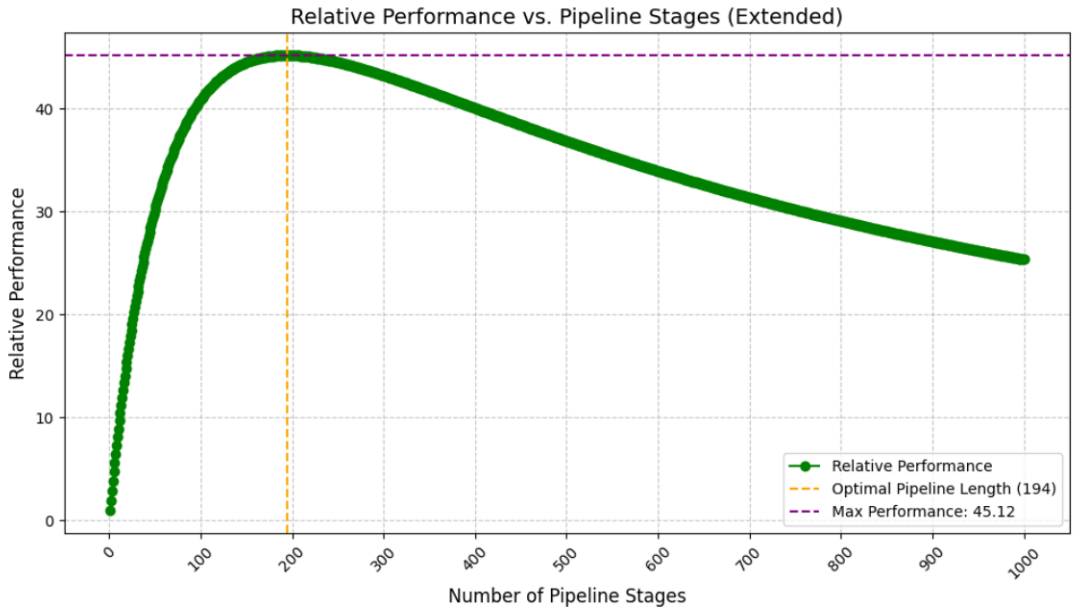
ii. CPI vs Pipeline stages



iii. Relative performance vs Pipeline stages



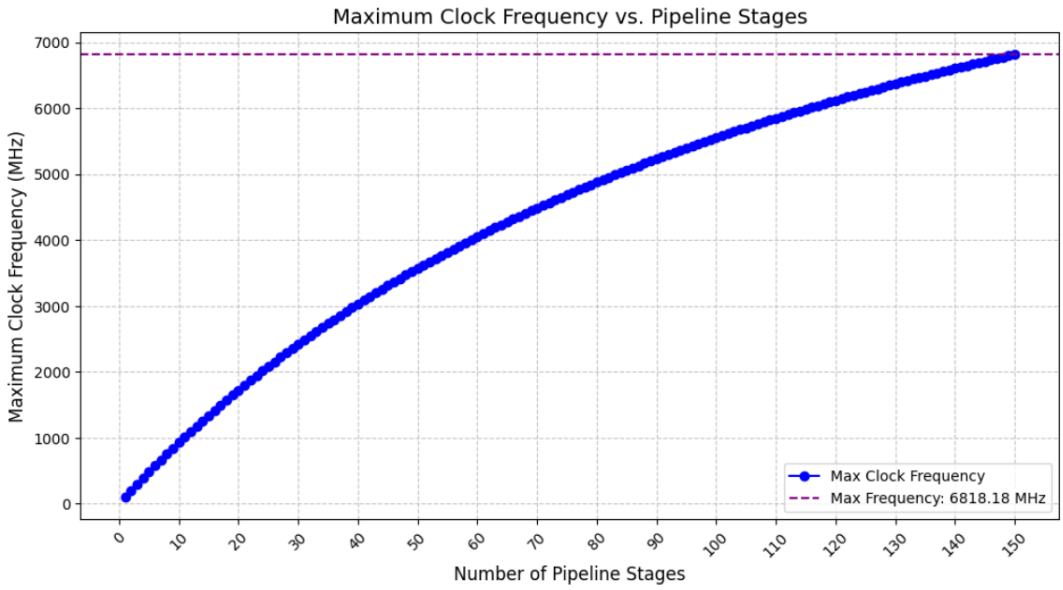
Question 6:



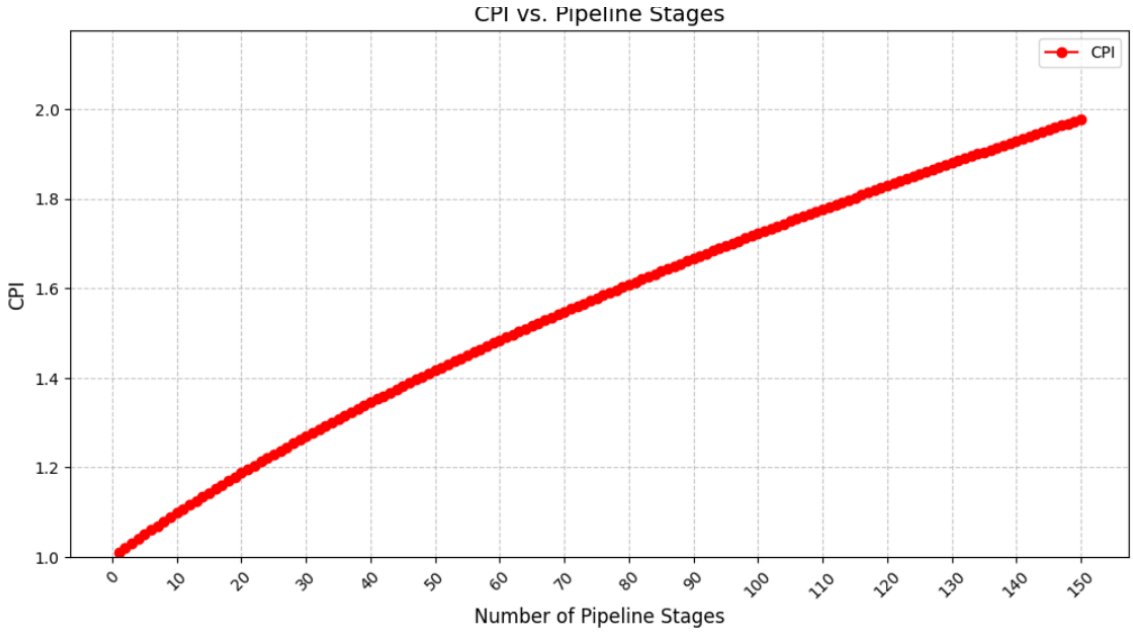

```
Performance-Optimal Pipeline Length: 194 stages
Maximum Relative Performance: 45.12× compared to non-pipelined implementation
```

Question 7:

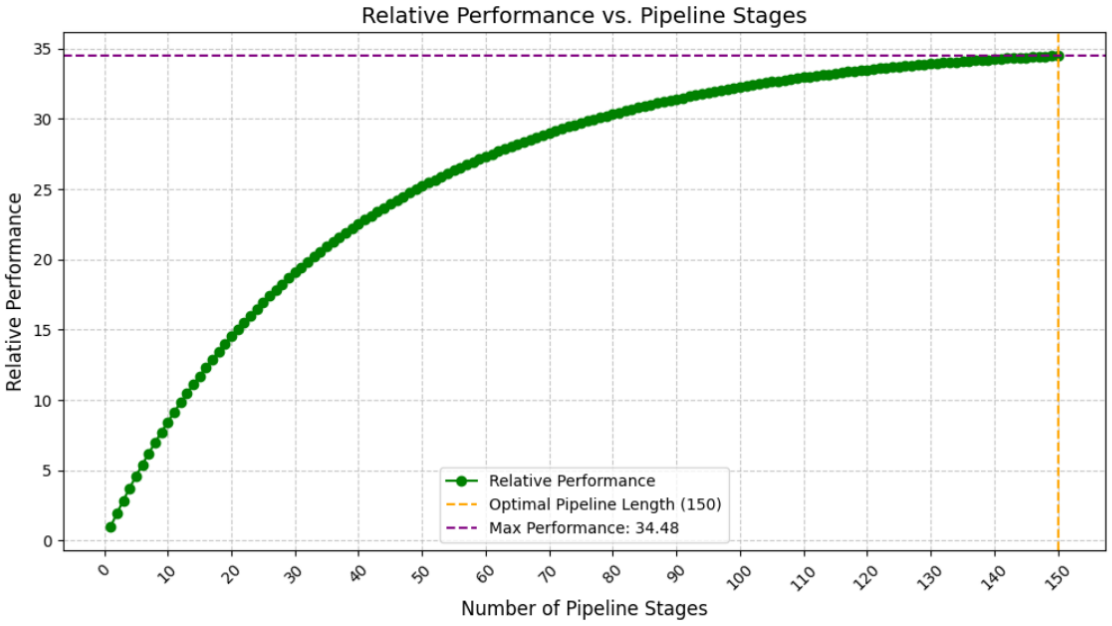
i. Maximum clock frequency vs Pipeline stages



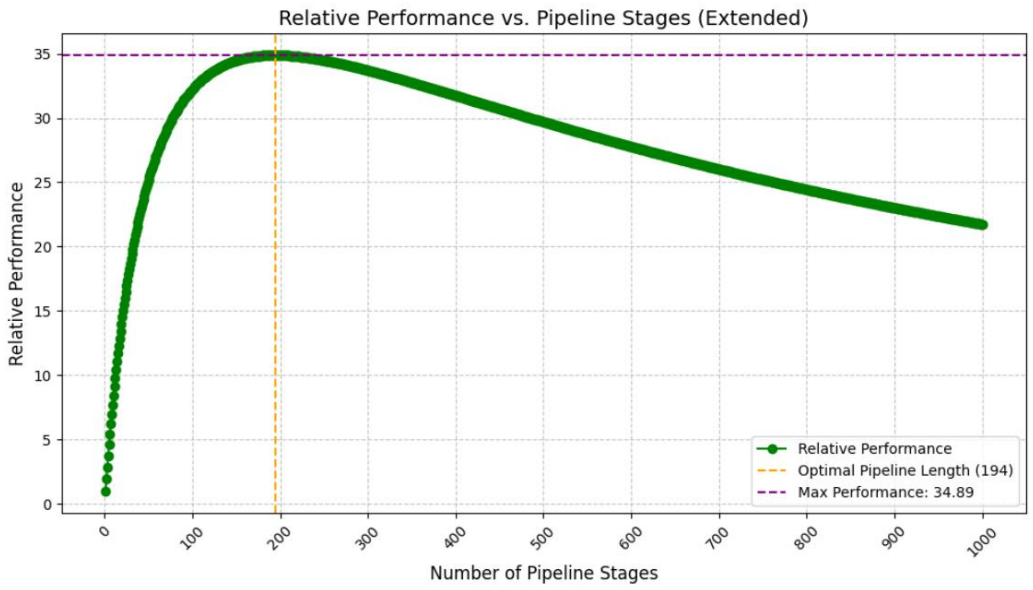
ii. CPI vs Pipeline Stages



iii. Relative performance vs Stages



Question 8:



[53]: (np.int64(194), np.float64(34.89024559855355))

Question 9:

i. Dynamic Power Consumption:

Given $P=c \cdot f \cdot V_{dd}^2$

given c = 12.75 nF and V_{dd} = 1.1V

Single-cycle Datapath critical path = 10 ns

Latch Latency: 80 ps.

Cycle Time $T = \frac{10\ ns}{N} + 80\ ps$

Max Frequency → Min Latency or Cycle Time

$$f = \frac{1}{\frac{T_{critical\ path}}{k} + T_{lat\ latency}}$$

Minimal Cycle Time: $T_{min} = 80\ ps$

$$T = \frac{10 * 10^{-9}}{150} + 80 * 10^{-12} = 1.4667 \times 10^{-10}\ seconds$$

$$f = \frac{1}{1.4667 \times 10^{-10}}$$

$$f = 6.818\,GHz$$

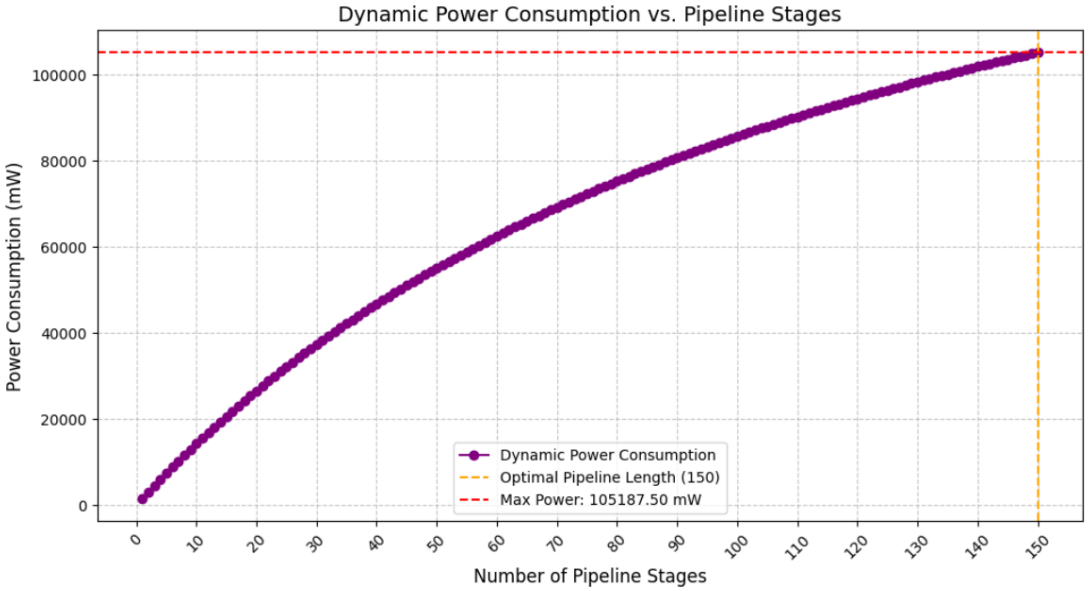
Substitution in Power equation:

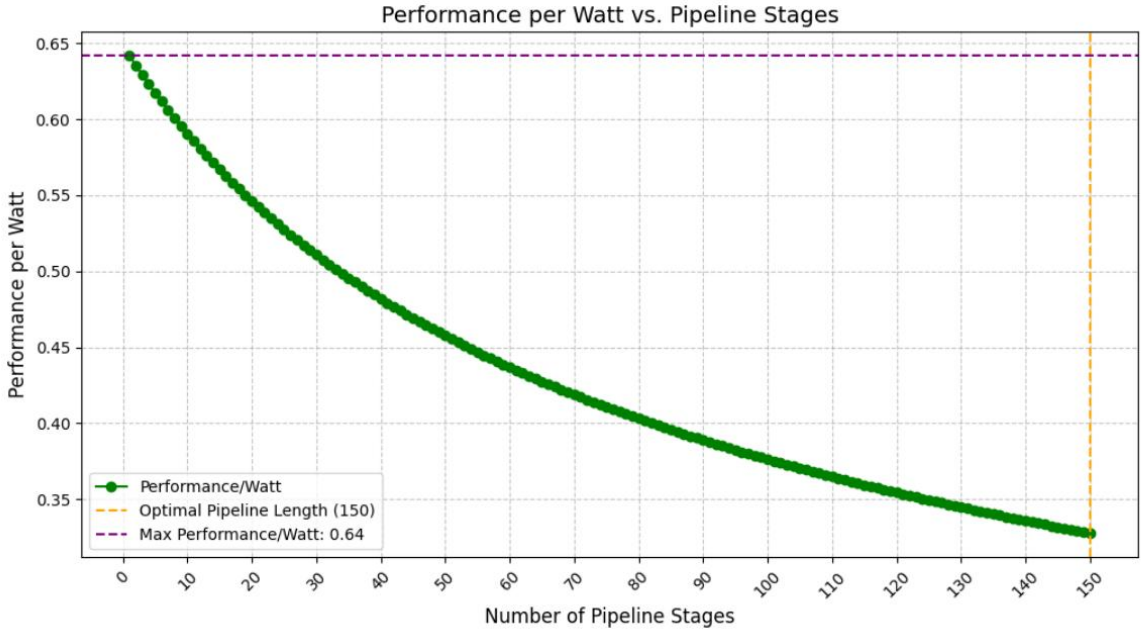
$$P = (12.75 * 10^{-9}) . (6.818 * 10^{9}). (1.1)^2$$

$$P = 12.75 . 6.818 . 1.21$$

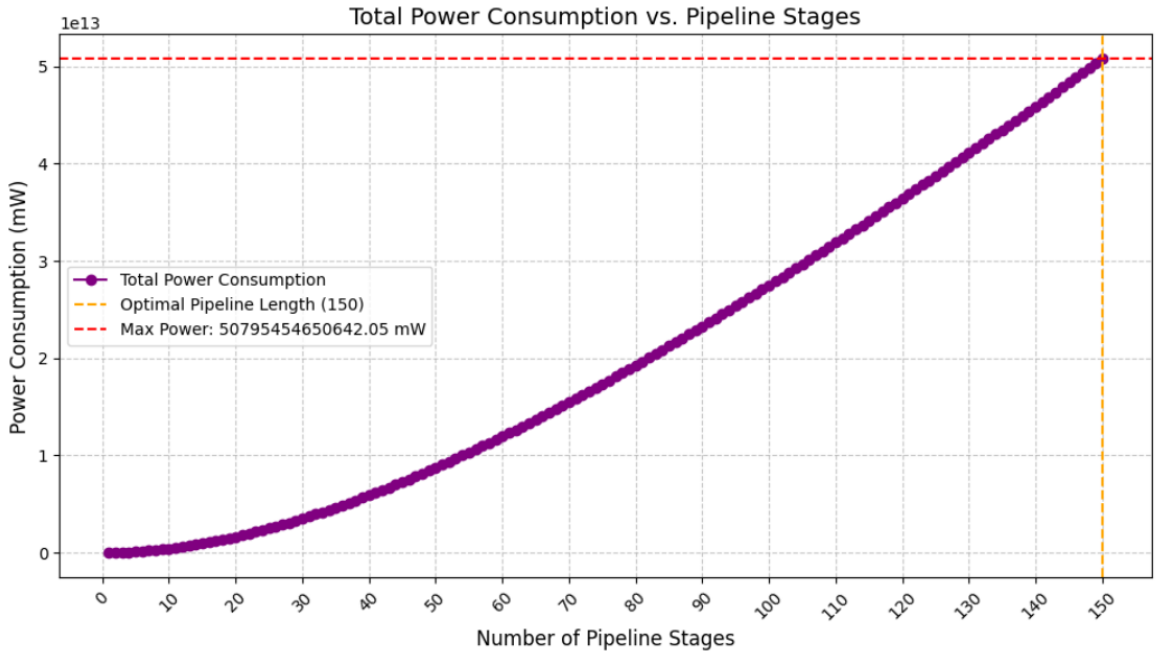
$$Power\ P = 105.19\,W$$

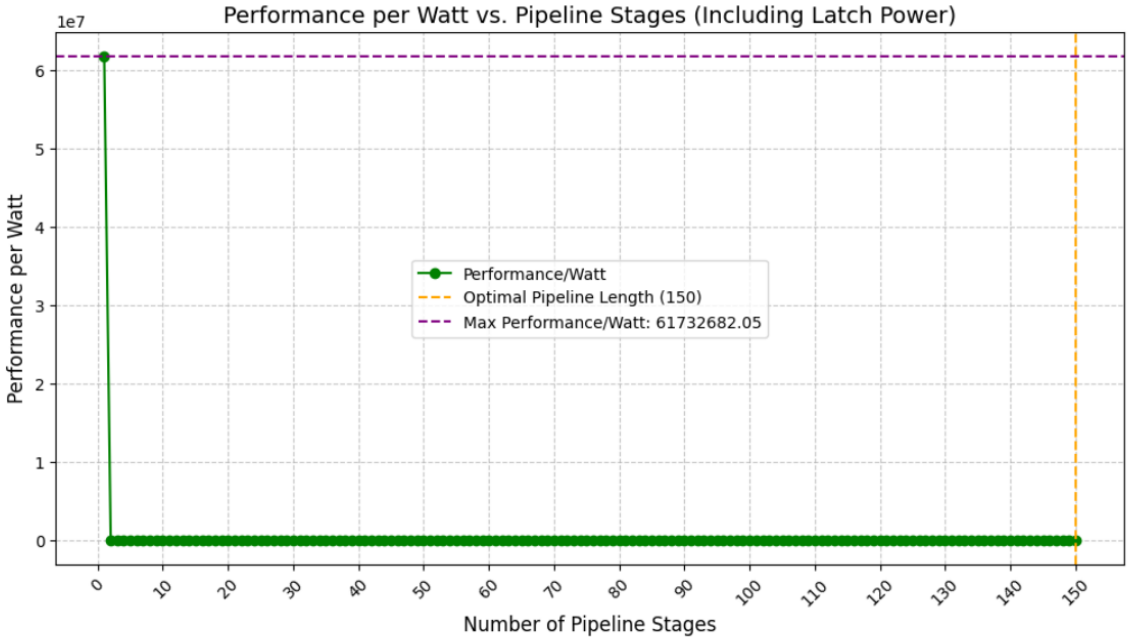
ii. Plot Power consumption and Performance / Watt



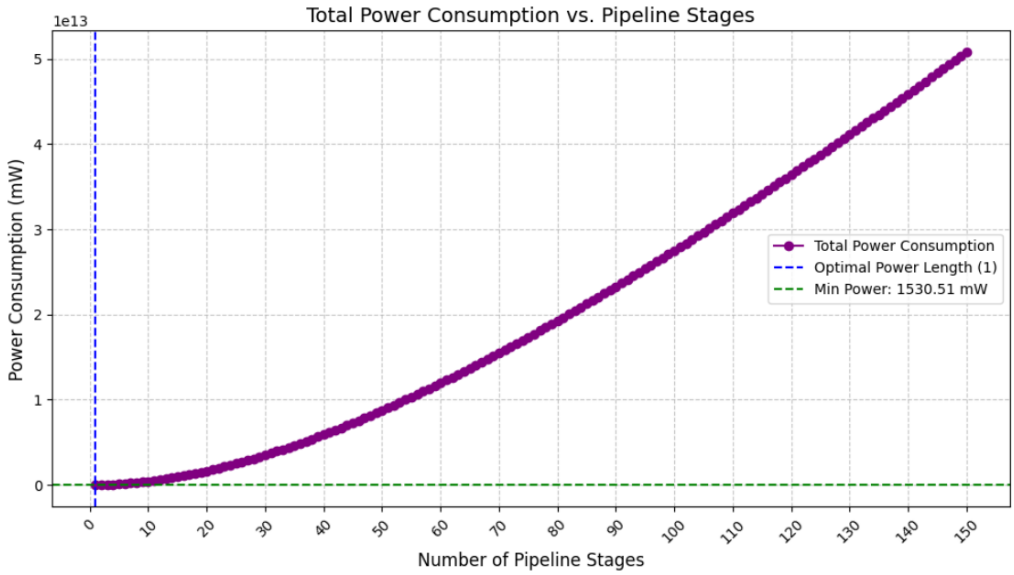


iii. Power Consumption and Performance/ Watt

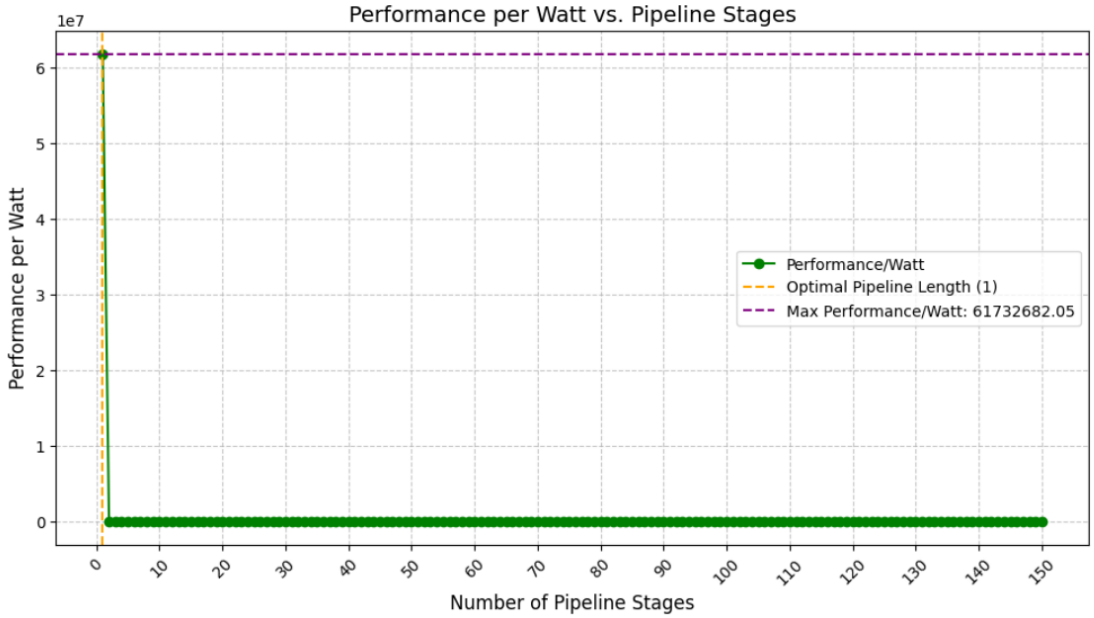




iv. Optimal Power Length for Minimal Power Consumption:



v. Optimal Pipeline Length for Maximum Performance:



vi. Maximum Clock Frequency

$$\boldsymbol{P_{total} = P_{datapath} + P_{latches}}$$

Substitution of values as given:

$$P_{latches} = 0.05 \times f$$

K stage pipeline would have (k-1) latches

Power given = 50 W

$$P_{total} = P_{datapath} + 0.05 \times f$$

$$50 = P_{datapath} + 0.05 \times f$$

$$50 = (12.75 \times 10^{-9} * f * 1.21) + (k - 1) * 0.05$$

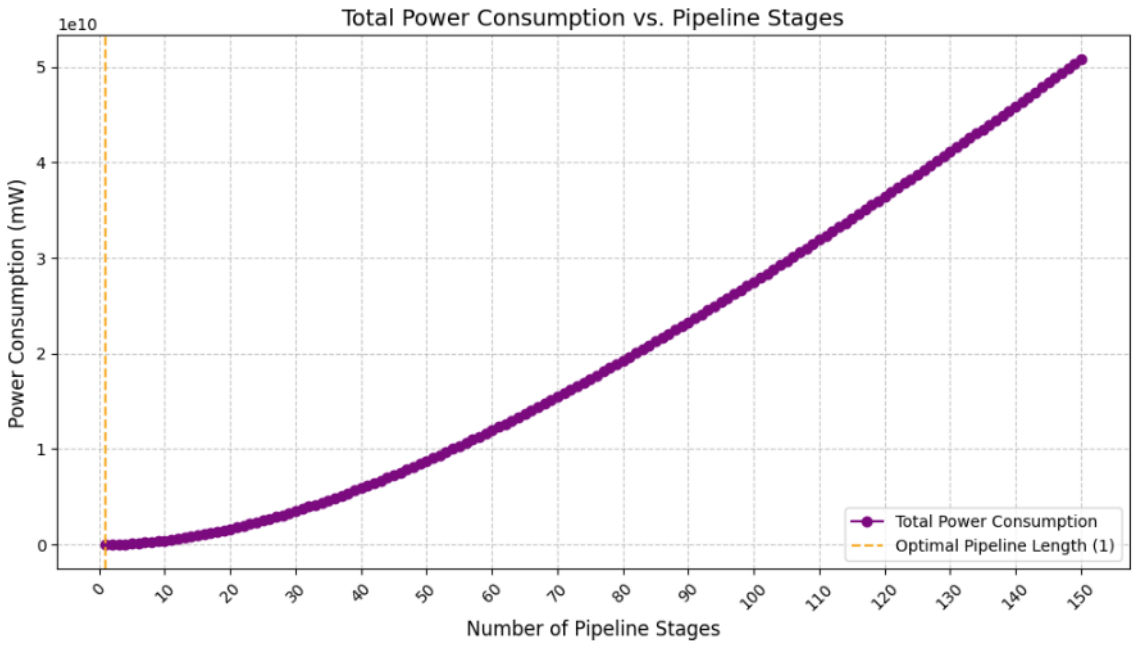
$$f = \frac{50}{(12.75 \times 10^{-9} \times 1.21) + (k - 1) * 0.05}$$

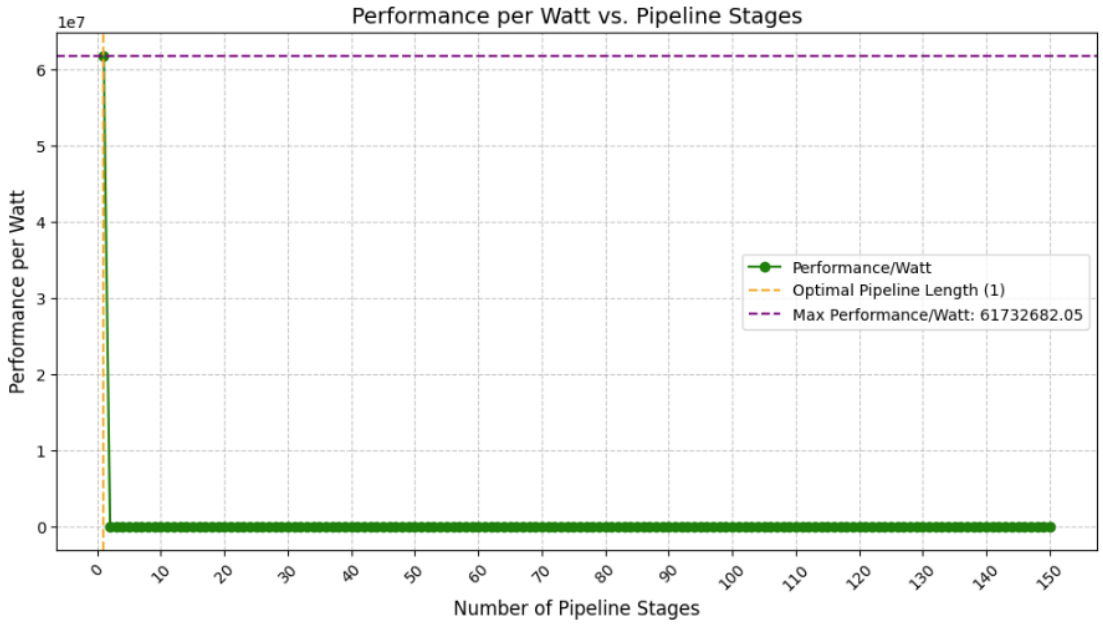
As per given condition; k =150

$$f = \frac{50}{(12.75 \times 10^{-9} \times 1.21) + (149) * 0.05}$$

$$f = 99.21\ MHz$$

Question 10:




Performance per Watt vs. Pipeline Stages
1e7
Performance per Watt
Number of Pipeline Stages
Performance/Watt
Optimal Pipeline Length (1)
Max Performance/Watt: 61732682.05