**Question 1**

1. Maximum Clock Frequency:

A graph showing a curve

Description automatically generated

1. Percentage Overhead VS Pipeline Stages

A graph with a red line

Description automatically generated

**Question 2:**

The maximum theoretical frequency would be:

Formula:



A close up of text

Description automatically generated

Given

Latency = 80 ps = 80 \* 10-12 seconds

Therefore

12.5 GHz

The Maximum Theoretical frequency would be 12.5 GHz

**Question 3:**

1. **Maximum Clock Frequency vs Pipeline Stages**

**A graph showing a curve

Description automatically generated**

1. **CPI vs Pipeline stages**

**A graph with a red line

Description automatically generated**

1. **Relative Performance vs Pipeline Stages**

**A graph of a number of pipeline stages

Description automatically generated**

**Question 4:**

1. **Maximum clock frequency vs Pipeline stages:**

**A graph of a curve

Description automatically generated**

1. **CPI vs Pipeline stages**

**A graph with a red line

Description automatically generated**

1. **Relative performance vs Pipeline stages:**

**A graph of a number of pipeline stages

Description automatically generated**

**Question 5:**

1. **Maximum clock frequency vs Pipeline stages**

**A graph of a curve

Description automatically generated**

1. **CPI vs Pipeline stages**

**A graph with a red line

Description automatically generated**

1. **Relative performance vs Pipeline stages**

**A graph showing a curve

Description automatically generated**

**Question 6:**

**A graph with a green line

Description automatically generated**

**Question 7:**

1. **Maximum clock frequency vs Pipeline stages**

**A graph showing a curve

Description automatically generated**

1. **CPI vs Pipeline Stages**

**A graph with a red line

Description automatically generated**

1. **Relative performance vs Stages**

**A graph showing a curve

Description automatically generated**

**Question 8:**

**A graph with a green line

Description automatically generated**

**Question 9:**

1. **Dynamic Power Consumption:**

Given *P*=*c*⋅*f*⋅*Vdd2*​  
given c = 12.75 nF and Vdd = 1.1V

Single-cycle Datapath critical path = 10 ns

Latch Latency: 80 ps.

Cycle Time

Max Frequency 🡪 Min Latency or Cycle Time

Minimal Cycle Time:

Substitution in Power equation:

1. **Plot Power consumption and Performance / Watt**

**A graph of a graph showing a curve

Description automatically generated with medium confidence**

**A graph showing a curve

Description automatically generated**

1. **Power Consumption and Performance/ Watt**

**A graph showing a number of pipeline stages

Description automatically generated**

**A graph with numbers and a line

Description automatically generated with medium confidence**

1. **Optimal Power Length for Minimal Power Consumption:**

**A graph with a purple line

Description automatically generated**

1. **Optimal Pipeline Length for Maximum Performance:**

**A graph with green lines and numbers

Description automatically generated**

1. **Maximum Clock Frequency**

Substitution of values as given:

K stage pipeline would have (k-1) latches

Power given = 50 W

As per given condition; k =150

**Question 10:**

A graph with a purple line

Description automatically generated

A graph showing performance and performance

Description automatically generated