Simulink Design Verifier Report

Vehicle_Speedometer_Module

jamesbond

19-Mar-2023 02:44:45

Table of Contents

Chapter 1. Summary

Analysis Information

Model:	Vehicle_Speedometer_Module
Release:	R2022a Update 2
Checksum:	379700363 2376830566 2080933560 886107326
Mode:	Design error detection
Model Representation:	Built on 19-Mar-2023 02:43:15
Status:	Completed normally
PreProcessing Time:	16s
Analysis Time:	19s

Objectives Status

Number of Objectives:	**26**	
Objectives Valid:	10	(38%)
Dead Logic:	0	(0%)

Chapter 2. Analysis Information

Table of Contents

2.1. Model Information

File:	Vehicle_Speedometer_Module
Version:	1.29
Time Stamp:	Sun Mar 19 02:09:56 2023
Author:	jamesbond

2.2. Analysis Options

Mode:	DesignErrorDetection
Rebuild Model Representation:	IfChangeIsDetected
Detect dead logic (partial):	on
Run exhaustive analysis for dead logic:	off
Coverage objectives analyzed for dead logic:	ConditionDecision
Detect integer overflow:	on
Detect division by zero:	on
Detect specified minimum and maximum value violations:	off
Detect out of bound array access:	on
Detect non-finite and NaN floating-point values:	off
Detect subnormal floating-point values:	off
Detect data store access violations:	off
Detect specified block input range violations:	off
Detect usage of remainder and reciprocal operations (hisl_0002):	off
Detect usage of square root operations (hisl_0003):	off
Detect usage of log and log10 operations (hisl_0004):	off
Detect usage of Reciprocal Square Root blocks (hisl_0028):	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on

Save Data:	on
Save Harness:	off
Save Report:	off

2.3. Constraints

Table of Contents

2.3.1. Design Min Max Constraints

Name	Design Min Max Constraint
Avg_VehicleSpeed	[0..280]
In_MainFilt_SpeedValue	[1..3]
In_AuxFilt_SpeedValue	[1..3]

Chapter 3. Dead Logic

Simulink Design Verifier proved these objectives to be unreachable or dead logic. This can be a side effect of parameter configurations or minimum and maximum constraints specified on inputs. Simulink Design Verifier ran a partial check for dead logic. Consider enabling the 'Dead logic > Run exhaustive analysis' configuration option in order to perform an exhaustive analysis.

Chapter 4. Design Error Detection Objectives Status

Table of Contents

4.1. Objectives Valid

#	Type	Model Item	Description	Analysis Time (sec)
17	Integer overflow	Speedometer_Module/Main_Data_Filtering/Gain	Overflow	12
22	Division by zero	Speedometer_Module/Main_Data_Filtering/Divide	Division by zero	12
23	Integer overflow	Speedometer_Module/Main_Data_Filtering/Divide	Overflow	12
26	Integer overflow	Speedometer_Module/Auxilliary_Data_Filtering/Gain	Overflow	12
28	Integer overflow	Speedometer_Module/Main_Data_Filtering/Add	Overflow	12
30	Integer overflow	Speedometer_Module/Display_Speed_Output/Add	Overflow	12
33	Division by zero	Speedometer_Module/Auxilliary_Data_Filtering/Divide	Division by zero	12
34	Integer overflow	Speedometer_Module/Auxilliary_Data_Filtering/Divide	Overflow	12
38	Integer overflow	Speedometer_Module/Display_Speed_Output/Abs	Overflow	12
40	Integer overflow	Speedometer_Module/Auxilliary_Data_Filtering/Add	Overflow	16

Chapter 5. Derived Ranges

Signal	Derived Ranges
Speedometer_Module/Compare To Zero/Constant- Outport 1	0
Speedometer_Module/Constant- Outport 1	10
Speedometer_Module/Display_Speed_Output/Constant- Outport 1	1.5
Avg_VehicleSpeed- Outport 1	[0..280]
Speedometer_Module/Input_Processing/Saturation- Outport 1	[2..250]
Speedometer_Module/Rem- Outport 1	[0..9]
Speedometer_Module/Compare To Zero/Compare- Outport 1	[F..T]
Speedometer_Module/Main_Data_Filtering/Constant- Outport 1	0.05000000000000000027755575615628913510590791702270507812 5
Speedometer_Module/Main_Data_Filtering/Gain- Outport 1	[1.29000000000000003552713678800500929355621337890625..162.490000000000009094947017729 28
In_MainFilt_SpeedValue- Outport 1	[1..3]
Speedometer_Module/Main_Data_Filtering/Divide- Outport 1	[0.42999999999999999333866185224906075745820999145507812 5..162.49000000000000909494701 77
Speedometer_Module/Auxilliary_Data_Filtering/Constant- Outport 1	0.02999999999999999888977697537484345957636833190917968 75
Speedometer_Module/Auxilliary_Data_Filtering/Gain- Outport 1	[0.28999999999999998001598555674718227237462997436523437 5..126.68999999999999772626324 55
Speedometer_Module/Main_Data_Filtering/Add- Outport 1	[0.38000000000000000444089209850062616169452667236328125..162.43999999999999772626324 556
Speedometer_Module/Display_Speed_Output/Add- Outport 1	[-250..124.65999999999999658939486835151910781860351562 5]
In_AuxFilt_SpeedValue- Outport 1	[1..3]

Signal	Derived Ranges
Speedometer_Module/Auxilliary_Data_Filtering/Divide-Outport 1	[0.089999999999999996669330926124530378729104995727539062 5..126.68999999999999772626324 5
Speedometer_Module/Display_Speed_Output/Abs-Outport 1	[0..250]
Speedometer_Module/Auxilliary_Data_Filtering/Add-Outport 1	[0.059999999999999997779553950749686919152736663818359375..126.65999999999999658939486 83
Speedometer_Module/Display_Speed_Output/Relational Operator- Outport 1	[F..T]
Speedometer_Module/Display_Speed_Output/Switch-Outport 1	[0.5..250]
Out_VehicleSpeed_Display- Outport 1	[0.5..250]