1. Description

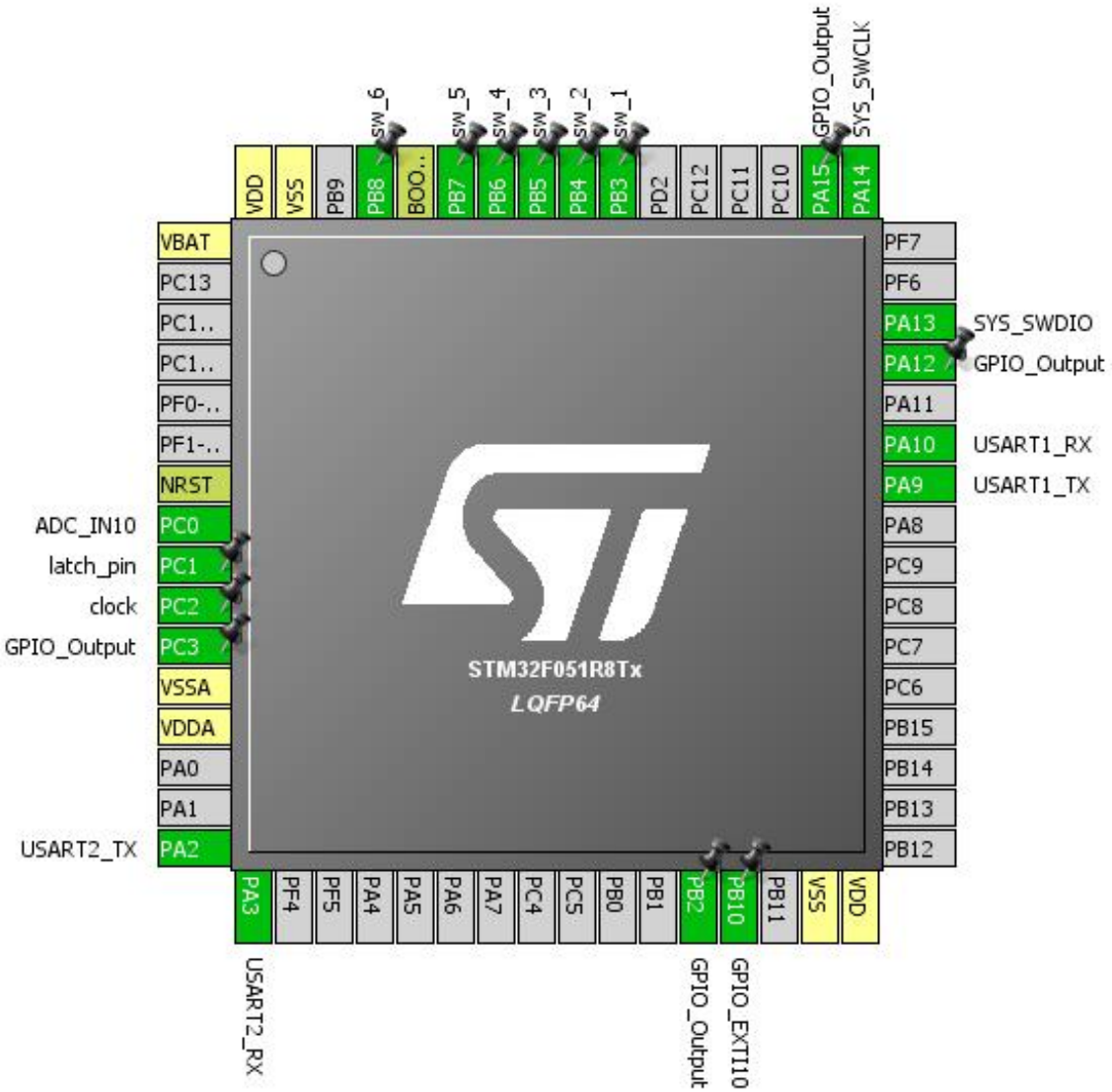
1.1. Project

Project Name	STM32F0_BRAILLE_V1
Board Name	STM32F0_BRAILLE_V1.0
Generated with:	STM32CubeMX 4.14.0
Date	09/14/2016

1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x1
MCU name	STM32F051R8Tx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration

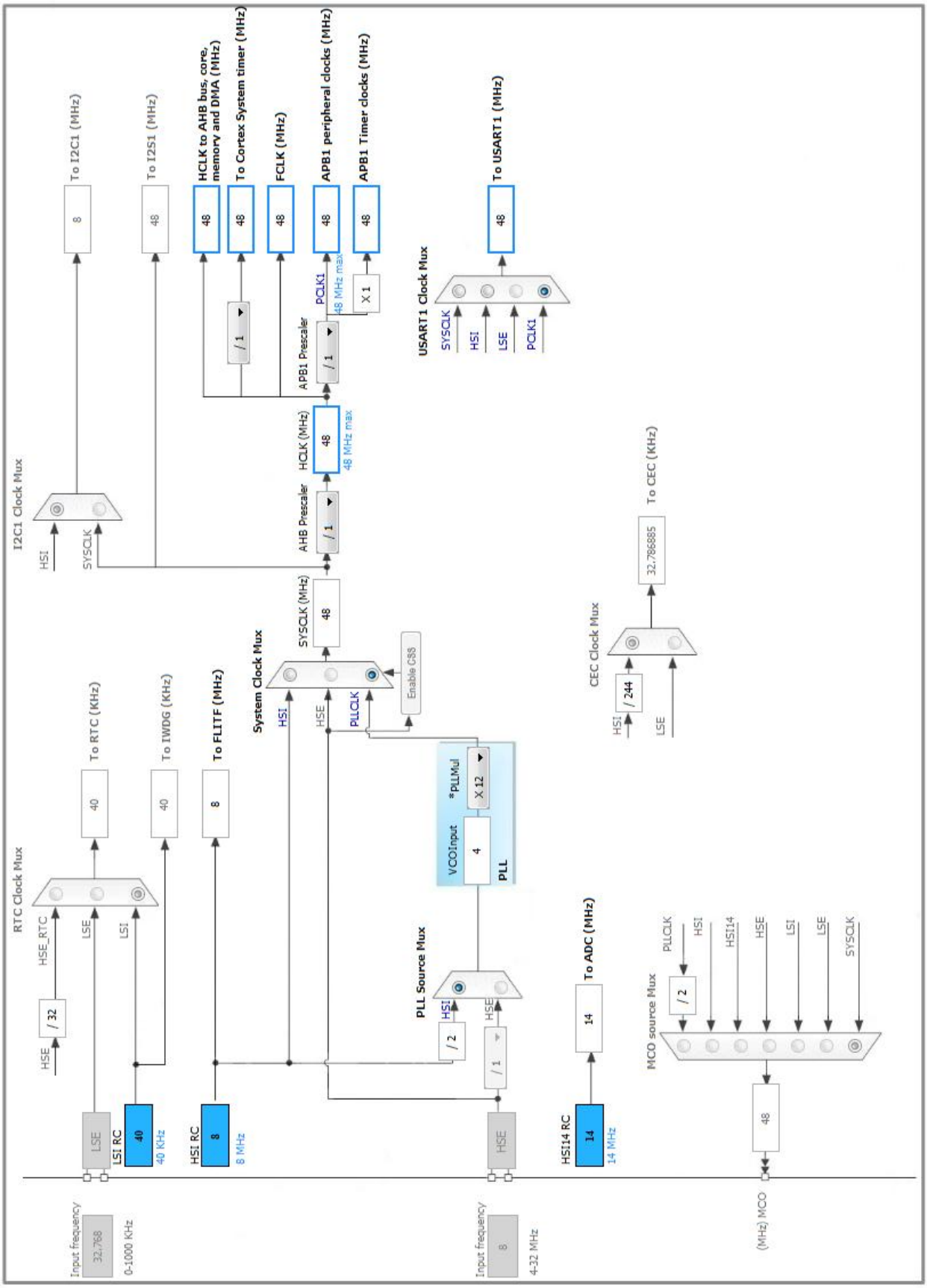


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
8	PC0	I/O	ADC_IN10	
9	PC1 *	I/O	GPIO_Output	latch_pin
10	PC2 *	I/O	GPIO_Output	clock
11	PC3 *	I/O	GPIO_Output	
12	VSSA	Power		
13	VDDA	Power		
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
28	PB2 *	I/O	GPIO_Output	
29	PB10	I/O	GPIO_EXTI10	
31	VSS	Power		
32	VDD	Power		
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
45	PA12 *	I/O	GPIO_Output	
46	PA13	I/O	SYS_SWDIO	
49	PA14	I/O	SYS_SWCLK	
50	PA15 *	I/O	GPIO_Output	
55	PB3	I/O	GPIO_EXTI3	sw_1
56	PB4	I/O	GPIO_EXTI4	sw_2
57	PB5	I/O	GPIO_EXTI5	sw_3
58	PB6	I/O	GPIO_EXTI6	sw_4
59	PB7	I/O	GPIO_EXTI7	sw_5
60	BOOT0	Boot		
61	PB8	I/O	GPIO_EXTI8	sw_6
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC

mode: IN10

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Forward
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled
Low Power Auto Power Off	Disabled

ADC_Regular_ConversionMode:

Sampling Time	1.5 Cycles
External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false

5.2. SYS

mode: Serial-WireDebug

Timebase Source: SysTick

5.3. TIM3

Clock Source : Internal Clock

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.4. USART1

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.5. USART2

Mode: Asynchronous

5.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PC0	ADC_IN10	Analog mode	No pull-up and no pull-down	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**High ***	
GPIO	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	latch_pin
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	clock
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB10	GPIO_EXTI10	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB3	GPIO_EXTI3	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	sw_1
	PB4	GPIO_EXTI4	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	sw_2
	PB5	GPIO_EXTI5	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	sw_3
	PB6	GPIO_EXTI6	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	sw_4
	PB7	GPIO_EXTI7	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	sw_5
	PB8	GPIO_EXTI8	**External Interrupt**	No pull-up and no pull-down	n/a	sw_6

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			Mode with Falling edge trigger detection			

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System tick timer	true	0	0
EXTI line 2 and 3 interrupts	true	0	0
EXTI line 4 to 15 interrupts	true	0	0
ADC and COMP interrupts (COMP interrupts through EXTI lines 21 and 22)	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
USART2 global interrupt	true	0	0
PVD interrupt through EXTI Line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x1
MCU	STM32F051R8Tx
Datasheet	022265_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F0_BRAILLE_V1.0
Project Folder	C:\Data\Project-Docs\Braille\STM32F0_BRAILLE_V1.0
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F0 V1.5.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No