1. Description

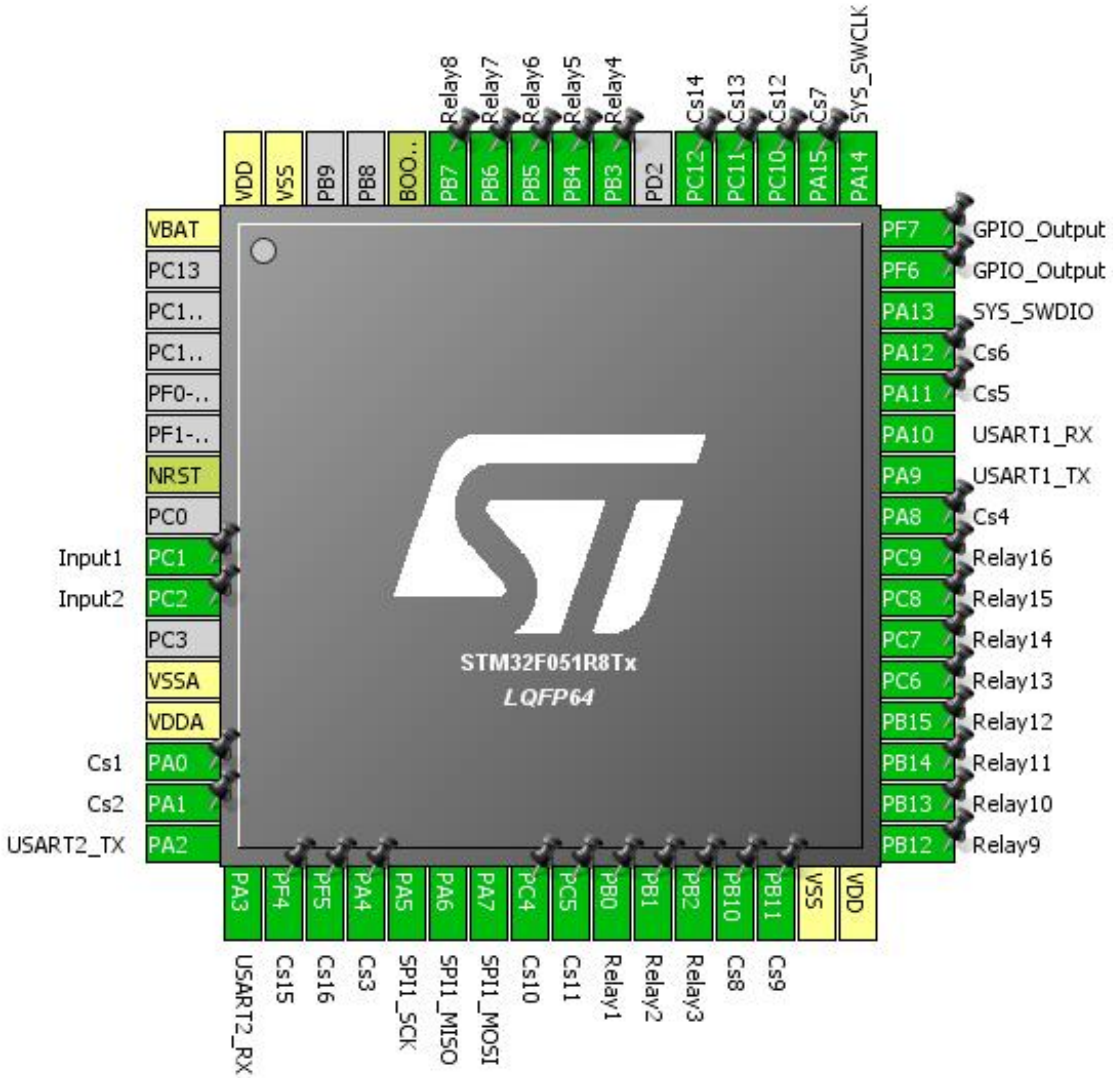
1.1. Project

Project Name	STM32F0-Superloop-V1
Board Name	STM32F0-Superloop-V1.0
Generated with:	STM32CubeMX 4.14.0
Date	08/17/2016

1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x1
MCU name	STM32F051R8Tx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



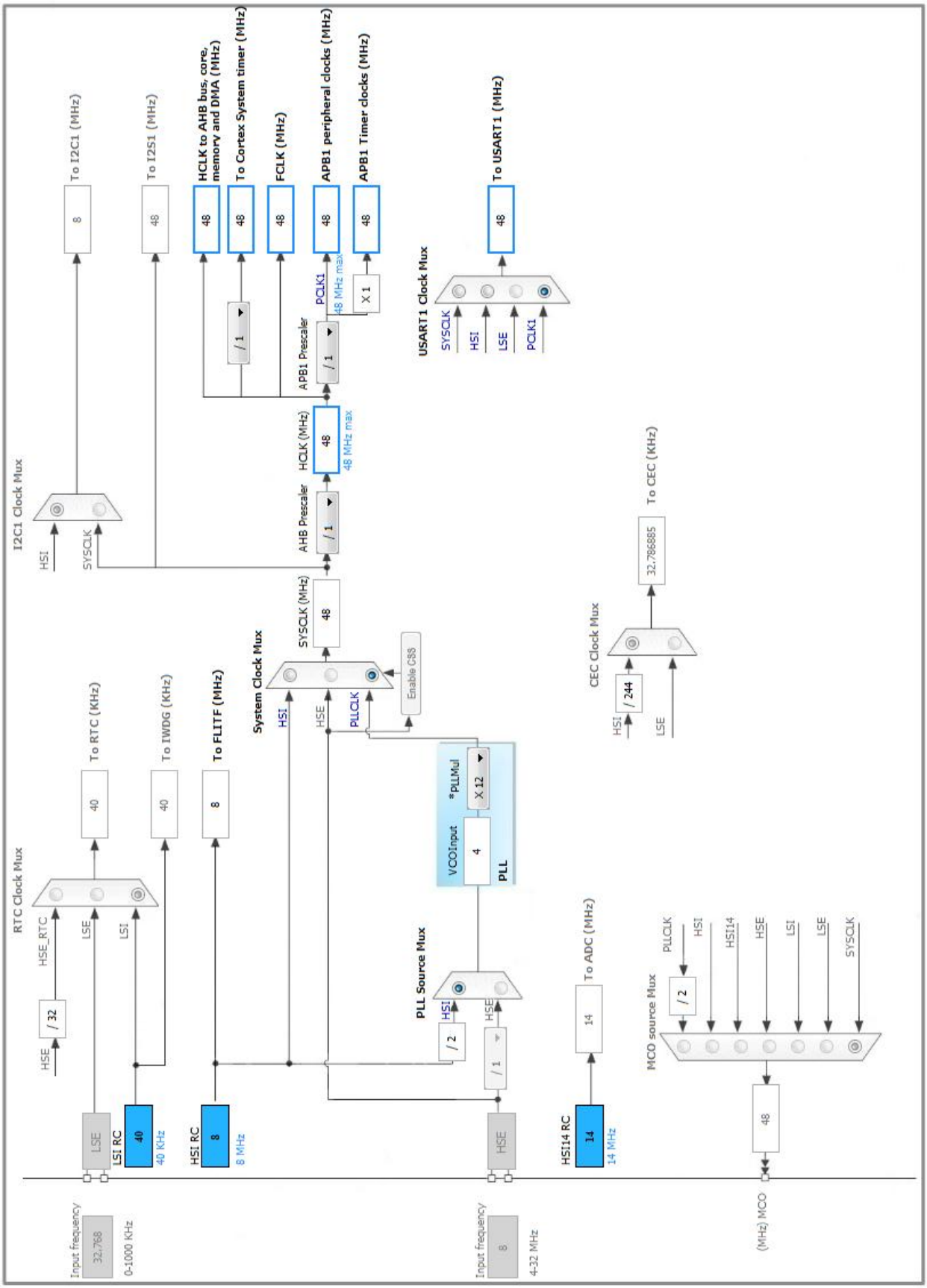
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
9	PC1 *	I/O	GPIO_Input	Input1
10	PC2 *	I/O	GPIO_Input	Input2
12	VSSA	Power		
13	VDDA	Power		
14	PA0 *	I/O	GPIO_Output	Cs1
15	PA1 *	I/O	GPIO_Output	Cs2
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	PF4 *	I/O	GPIO_Output	Cs15
19	PF5 *	I/O	GPIO_Output	Cs16
20	PA4 *	I/O	GPIO_Output	Cs3
21	PA5	I/O	SPI1_SCK	
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
24	PC4 *	I/O	GPIO_Output	Cs10
25	PC5 *	I/O	GPIO_Output	Cs11
26	PB0 *	I/O	GPIO_Output	Relay1
27	PB1 *	I/O	GPIO_Output	Relay2
28	PB2 *	I/O	GPIO_Output	Relay3
29	PB10 *	I/O	GPIO_Output	Cs8
30	PB11 *	I/O	GPIO_Output	Cs9
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	Relay9
34	PB13 *	I/O	GPIO_Output	Relay10
35	PB14 *	I/O	GPIO_Output	Relay11
36	PB15 *	I/O	GPIO_Output	Relay12
37	PC6 *	I/O	GPIO_Output	Relay13
38	PC7 *	I/O	GPIO_Output	Relay14
39	PC8 *	I/O	GPIO_Output	Relay15
40	PC9 *	I/O	GPIO_Output	Relay16
41	PA8 *	I/O	GPIO_Output	Cs4
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
44	PA11 *	I/O	GPIO_Output	Cs5
45	PA12 *	I/O	GPIO_Output	Cs6
46	PA13	I/O	SYS_SWDIO	
47	PF6 *	I/O	GPIO_Output	
48	PF7 *	I/O	GPIO_Output	
49	PA14	I/O	SYS_SWCLK	
50	PA15 *	I/O	GPIO_Output	Cs7
51	PC10 *	I/O	GPIO_Output	Cs12
52	PC11 *	I/O	GPIO_Output	Cs13
53	PC12 *	I/O	GPIO_Output	Cs14
55	PB3 *	I/O	GPIO_Output	Relay4
56	PB4 *	I/O	GPIO_Output	Relay5
57	PB5 *	I/O	GPIO_Output	Relay6
58	PB6 *	I/O	GPIO_Output	Relay7
59	PB7 *	I/O	GPIO_Output	Relay8
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. SPI1

Mode: Full-Duplex Master

5.1.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**12.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.2. SYS

mode: Serial-WireDebug

Timebase Source: SysTick

5.3. USART1

Mode: Asynchronous

5.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.4. USART2

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

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6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**High ***	
GPIO	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Input1
	PC2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Input2
	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs1
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs2
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs15
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs16
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs3
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs10
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs11
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay1
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay2
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay3
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs8
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs9
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay9
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay10
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay11
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay12
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay13
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay14
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay15
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay16
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs4
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs5

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs6
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs7
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs12
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs13
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Cs14
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay4
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay5
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay6
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay7
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Relay8

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System tick timer	true	0	0
SPI1 global interrupt	true	0	0
PVD interrupt through EXTI Line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
USART2 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x1
MCU	STM32F051R8Tx
Datasheet	022265_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F0-Superloop-V1.0
Project Folder	Y:\hardware\STM32\STM32F0\STM32F0-Superloop-V1.0
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F0 V1.5.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No