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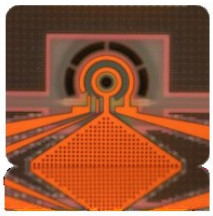
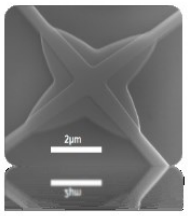
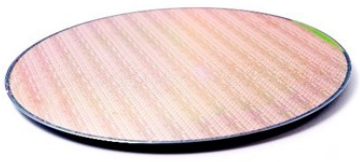
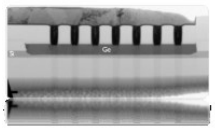
Technology Handbook

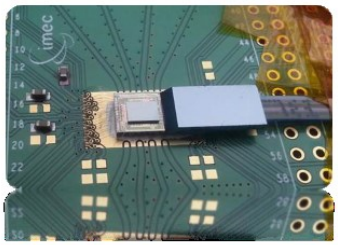
ISIPP50G 2.3.0











Changes

Version	Change
X.Y.Z	See changelog document
1.0.1	Bug fixes
1.0.0	Initial release

Contents

1 Document information

1.1 Purpose

The purpose of this document is to describe imec's silicon photonics ISIPP50G technology and specifications to take into account when designing into ISIPP50G technology. The imec Silicon Photonics platform consists of predefined fixed process modules. For customized processes, customers should contact imec directly.

1.2 Scope

The process modules in ISIPP50G are intended to be useful for prototyping and manufacturing of devices for a wide range of applications, but with a focus on communication devices. The process is fixed and cannot be altered by the customer, except for a number of options that are clearly described. The process described is applicable to every design submitted to Imec. The process details are the intellectual property of imec and are not shared with the customer.

1.3 Responsibility

Each device submitted to imec designed for the imec Silicon Photonics ISIPP50G technology will be processed according to the description here. It is the responsibility of the designer to make sure that their design is compatible with the processing. The design rules that have to be followed are described in the ISIPP50G Layout handbook. Imec cannot provide any guarantee that the circuit will have the functionality it was designed for.

2 Technology overview

The ISIPP50G technology offers a range of building blocks supporting various applications but with a focus on devices based on 50Gbit/s modulator and detector components and to enable fiber edge coupling. The technology is run on a 200mm wafer and uses a 220nm SOI layer. It features:

- A SOI layer to pattern waveguide devices such a splitters, couplers, polarization splitters and rotators, fiber couplers.
- A poly-silicon overlay layer for higher-efficiency grating couplers, polarization splitters/rotators and waveguides.
- High-speed modulators based on depletion-mode PN junction phase shifters, both in Mach-Zehnder and ring resonator configurations.
- High-speed germanium photodiodes.
- Edge fiber couplers.

A library of building blocks is provided with validated devices. Designers can also design custom components, following the design rules outlined in the ISIPP50G Layout Handbook.

A cross-section indicating the various possible types of devices is shown in Figure 1.

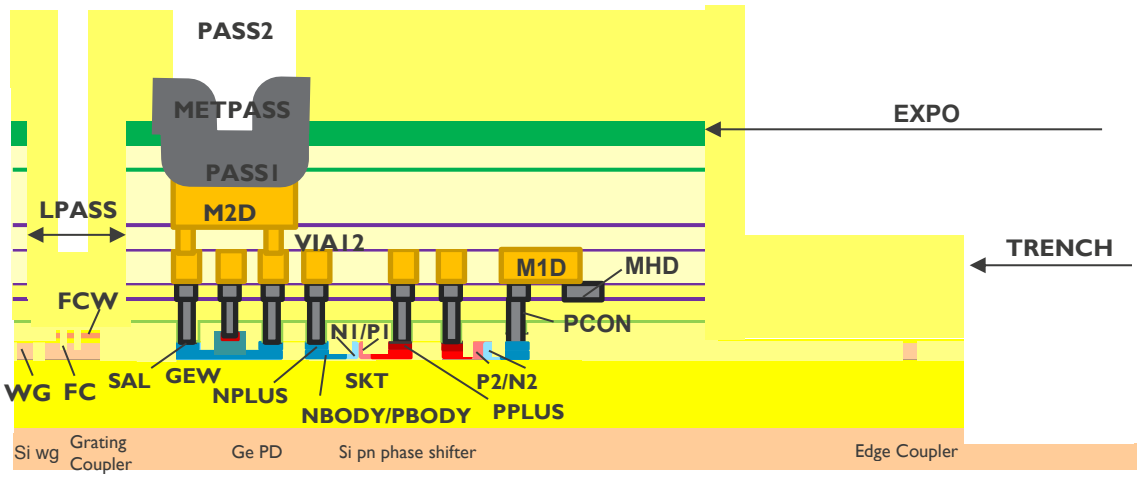


Figure 1: Schematic of the "final" cross-section

2.1 Process modules

The ISIPP50G technology consist of the following process modules:

Module name	Description	Devices
WG	Full etch (220nm) of SOI	Strip waveguides, couplers, MMIs, WDM devices, interferometers,…
FC	Partial 70nm etch of SOI	Rib waveguides, couplers, MMIs, with lower refractive index contrast, modulators
SKT	Partial 150nm etch of SOI	Rib waveguides, couplers, MMIs, .. with intermediate refractive index contrast, high-speed modulators

FCW	160nm poly-Si areas	Raised fiber couplers, thick rib waveguides. A separate design layer may not be offered in all runs.
NBODY/PBODY	Body well implants N, P	High-speed MZM (N1/P1), high speed ring modulators (N2/P2) and doped silicon heaters
N1/P1	Junction implants, lower dose	
N2/P2	Junction implants, higher dose	
NPLUS/PPLUS	Contact implant	
GEW	Germanium or SiGe	• Ge option: high-speed Ge photodiodes in O- and C- band • SiGe option: high-speed C-band EAM and photodiode
GN1/GP1	N and P implants in Ge or SiGe	• Ge option: high-speed Ge photodiodes in O- and C- band • SiGe option: high-speed C-band EAM and photodiode
SAL	Silicidation	
PCON	Contact plugs to SOI, poly and Ge	
MHD	Tungsten heaters	
M1D	Cu metal 1	Metal Routing
VIA12	Via metal-1 to metal-2	Metal Routing
M2D	Cu metal 2	Metal routing
PASS1/METPASS	Nitride passivation opening and AlCu metal pads	Standard wire-bondable Al pads
LPASS	Clears high refractive layers above grating couplers	Grating couplers
EXPO	Back-end opening down to silicon waveguide	Sensors, infiltration, edge coupler
PASS2	Dielectric opening to access METPASS	
TRENCH	Deep trench	End-fire fiber attachment

2.2 Process flow schematic

A schematic representation of the process flow is given below, from , to visualize the different process modules.

Figure 2: After WG, FC and SKT etchings, filling, planarization and NBODY and PBODY implants

Figure 3: After poly deposition and patterning (FCW), N1, P1, N2, P2, NPLUS and PPLUS implants, filling and planarization.

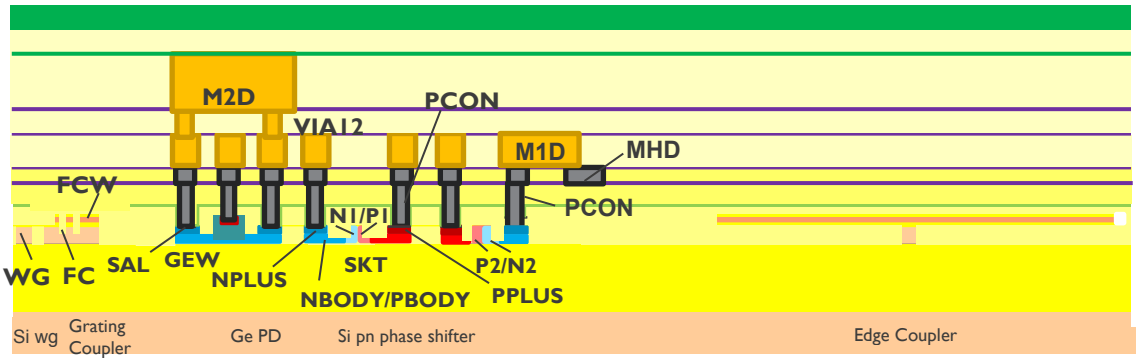


Figure 4: After growing Ge, implanting and planarizing the metal layers are built: SAL, PCON, MHD, M1D, VIA12, M2D and passivation.

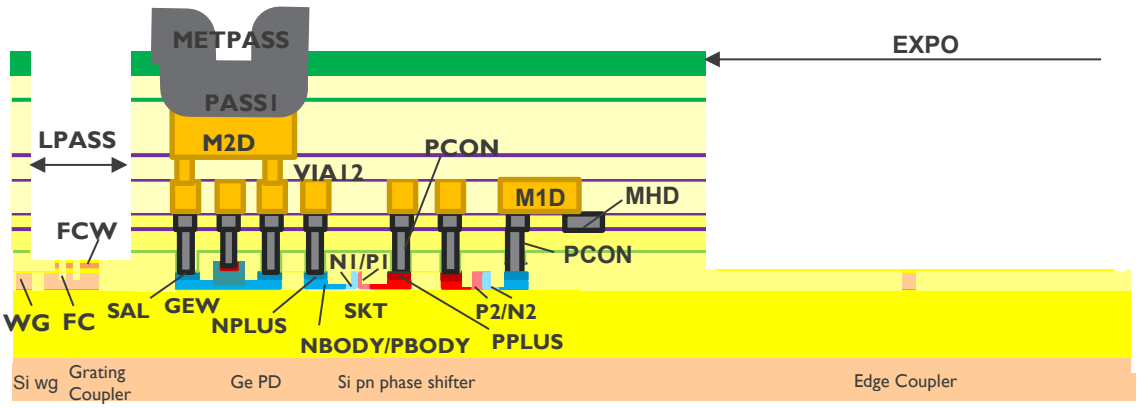


Figure 5: After PASS1 opening, AlCu deposition and patterning (METPASS), removal of the stack over gratings (LPASS) and etch down to top surface of SOI (EXPO).

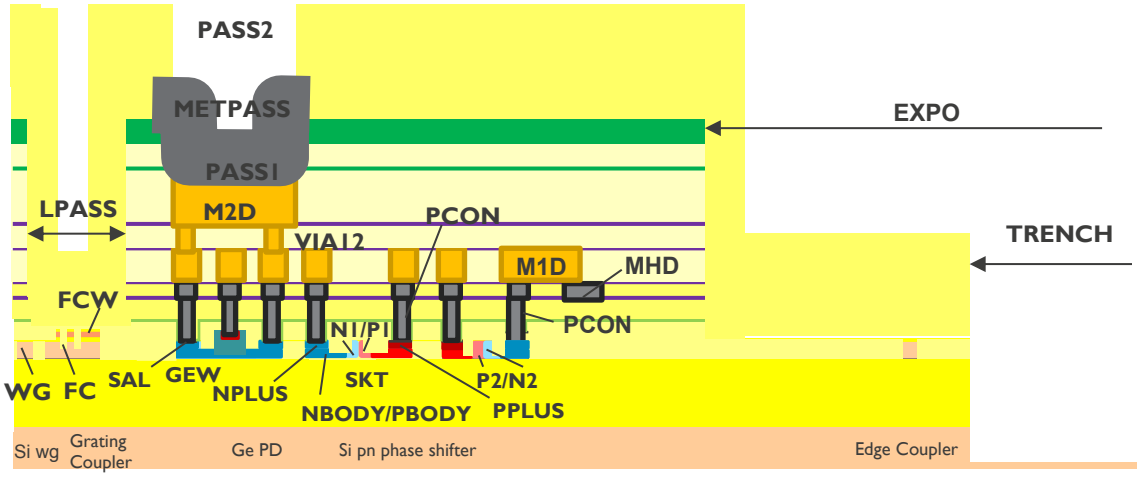


Figure 6: After oxide deposition, opening over bond pads (PASS2) and TRENCH etch, the final stack is complete.

3 Masks

The main masks are listed below. Some auxiliary masks and the one needed for Ge devices are not listed. For details on preparing the masks data see the Layout Handbook.

Mask	Description	Dummy filling	Perforation	Field type
WG	Full etch on 220nm SOI	X		DF
FC	70nm etch on 220nm SOI	X		DF
SKT	160nm etch on 220nm SOI	X		DF
NBODY	Body N implant			DF
PBODY	Body P implant			DF
FCW	160nm poly patterning	X		LF
N1	Phase modulator junction N implant			DF
P1	Phase modulator junction P implant			DF
N2	Ring modulator junction N implant			DF
P2	Ring modulator junction P implant			DF
NPLUS	N implant for contact			DF
PPLUS	P implant for contact			DF
SAL	Silicide			DF
PCON	Contacts to SOI and Ge			DF
MHD	Metal heater			DF
M1D	First level of metal	X	X	DF
VIA12	Via between M1D and M2D			DF
M2D	Second level of metal	X	X	DF
PASS1	Passivation layer opening for Bond Pad			DF
METPASS	Aluminium bond pad definiton			LF
LPASS	Open BEOL over gratings			DF
EXPO	BEOL opening			DF
PASS2	Passivation layer opening			DF
TRENCH	Deep trench			DF

4 Process modules specifications

In this section, the specifications of the different process modules are detailed for custom designs.

4.1 Starting wafers

	Parameter	Unit	Min	Typ	Max
Handle wafer (Si substrate)	Thickness	um	710	725	740
	Resistivity (Regular)	Ohm.cm	12		20
	Warp		0	20	80
Buried oxide	Thickness	nm	1950	2000	2050
SOI	Thickness t_{SOI}	nm	215	225	235
	Resistivity (unprocessed)	Ohm.cm	8.5		11.5

Table 1: Starting wafers specifications.

Device (SOI) and handle layers are p-type.

4.2 SOI patterning: WG, FC, SKT

The following tables are provided as design guidelines.

No bias is applied by imec during mask preparation.

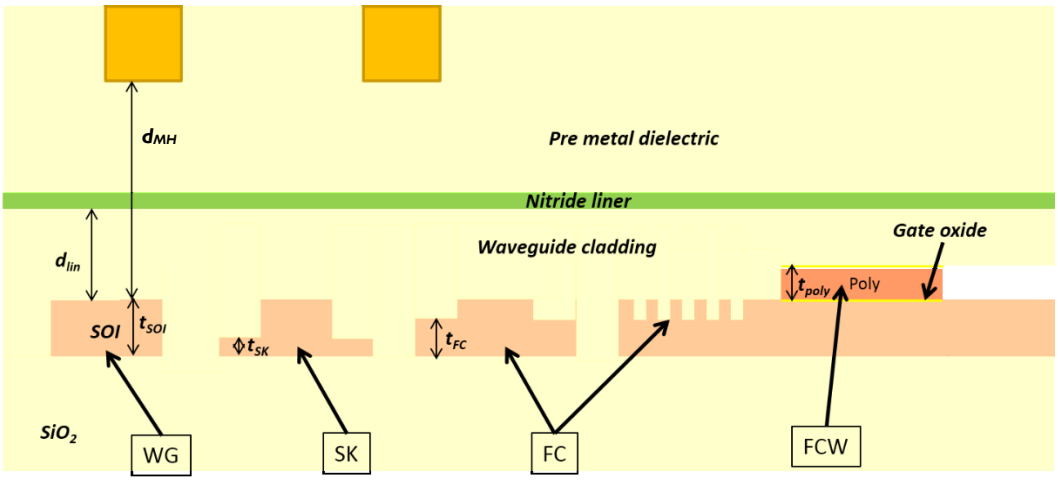


Figure 7: FEOL SOI patterning layers, detail view. See the following tables for values of the t and d parameters.

4.2.1 Methodology

The values of the structural characteristics of the fabricated features are provided based on in-line metrology (thickness measurement, CD-SEM, optical overlay).

The thickness is measured by an ellipsometer in an 80 µm x 80 µm uniform pad in one slip-box location per die, nine dies per wafer organized in a map that covers approximately the 200 mm wafer surface minus an edge exclusion of ~1.0 cm.

The CD is measured automatically by a CD-SEM in one slip-box location per die, five dies per wafer, organized in a map that covers approximately the 200 mm wafer surface minus an edge exclusion of ~2.0 cm. The exact measurement location will depend on the die size and the location of the measurement structure that may vary from one reticle set to another.

The process performance is typically monitored on five wafers per lot. The process performance statistical data below is provided for information purpose only and is not a guarantee for the control of structures present in the delivered dies or wafers. The Min. & Max. limits are defined to describe a process capability "cpk" of 1.0 except for the waveguide silicon thickness that is determined by the incoming wafer material specifications.

The structure widths in the table below corresponds to the "drawn" dimensions as present in the GDS-II design. For more aggressive dimensions please contact imec or Europractice.

4.2.2 WG specifications

Design parameter	Value	Unit
Minimum width	130	nm
Recommended minimum width	150	nm
Minimum space	130	nm
Recommended minimum space	150	nm
Minimum pitch	260	nm
Sidewall angle	>85	°

All dimensions in the table below are in nanometres. They are representative of the **final dimensions** after fabrication.

Specification (drawn dimensions)	target	LSL	USL	Median	Mean	StdDev	Q10	Q90	Withinin wafer stddev
Line/space 450nm /180nm: 180nm trench	165	150	187	170.2	171.3	5.2	165.4	179	2.74
450nm iso waveguide	470	445	495	478.7	478.6	8.6	468	489	5.3
150nm iso waveguide	165	145	185	173	173.5	5.9	166	182	4.6
130nm iso waveguide	145	120	170	152	152.2	6.1	144	160	4.3
Waveguide thickness t_{SOI}	215	200	230	209.9	210.1	1.33	208.7	212	0.7

4.2.3 FC specifications

Design parameter	Value	Unit
Minimum width	180	nm
Minimum space	180	nm
Minimum pitch	360	nm
Sidewall angle	>80	°

All dimensions in the table below are in nanometres. They are representative of the **final dimensions** after fabrication.

Specification (drawn dimensions)	target	LSL	USL	Median	Mean	StdDev	Q10	Q90	Withinin wafer stddev
Line/space 315nm/315nm: 315nm etched trench	300	280	350	300.3	300.6	5.1	293.9	307	4
FC-WG overlay X (mean + 3sigma)	25	0	50	16		10.5	37	37	
FC-WG overlay Y (mean + 3sigma)	25	0	50	17		8	10	29	
FC remaining thickness t_{FC}	140	125	155	146	145.8	3.1	142	149	1.7

4.2.4 SKT specifications

Design parameter	Value	Unit
Minimum width	180	nm
Minimum space	180	nm
Minimum pitch	360	nm
Sidewall angle	>80	°

All dimensions in the table below are in nanometres. They are representative of the **final dimensions** after fabrication.

Specification (drawn dimensions)	target	LSL	USL	Median	Mean	StdDev	Q10	Q90	Withinin wafer stddev
Line/space 450nm/180nm:	175	160	190	173.6	174	5.9	167	182	4

180nm etched trench									
450nm iso waveguide	495	465	525	501.7	500.7	11.8	484.9	516	
SKT remaining thickness t_{SKT}	60	45	75	62	62.7	4.7	57	69	1.7

The SKT-WG overlay statistics are the same than for the FC-WG overlay.

4.3 Poly patterning: FCW

Design parameter	Value	Unit
Minimum width	170	nm
Minimum space	170	nm
Minimum pitch	340	nm
Gate oxide thickness t_{GATE}	5	nm

All dimensions in the table below are in nanometres. They are representative of the **final dimensions** after fabrication.

Specification (drawn dimensions)	target	LSL	USL	Median	Mean	StdDev	Q10	Q90	Withinin wafer stddev
280nm iso waveguide	280	250	310	282	281.5	8.8	270	292	6.8
FC-WG overlay X (mean + 3sigma)	25	0	50	38		10	16	48	
FC-WG overlay Y (mean + 3sigma)	25	0	50	38		10	16	48	
Poly silicon remaining thickness t_{FC}	160	150	170	163	161.7	3.3	157	165	2.0

4.4 Implants in silicon N1, P1, N2, P2, NBODY, PBODY, NPLUS, PPLUS

4xP and 4xN implant levels are available for implementing diodes and resistors in the (patterned) SOI layer:

- N1 and P1 are typically used to define the PN junctions of MZM.
- N2 and P2 are typically used to define the PN junctions of ring modulators.
- PBODY and NBODY are typically used serve to create low-resistivity paths in SKT etched slabs (avg. 60nm thick).
- PPLUS and NPLUS are used to create low-resistance ohmic contacts to silicide.

The implant conditions are not shared as part of ISIPP50G.

4.4.1 Sheet Resistance specifications

The sheet resistance for doped silicon and metal layers are measured at the end of the process using fully automated wafer parametric testers. The measurement map is performed using a wafer map of typical 11 to 14 dies per wafer.

The location of the measured dies is done to establish a distribution that is representative as if the full 200mm wafer would be measured, minus a 1-cm edge exclusion. Figure 8 shows an example of wafer map used for the electro-optical characterization.

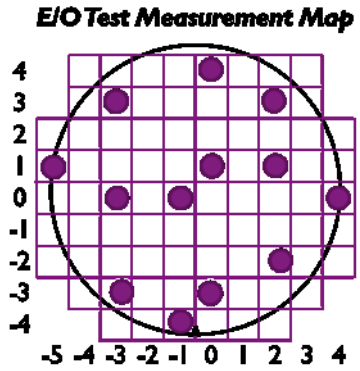


Figure 8: Typical wafer map used for electro-optical characterization.

Values for the sheet resistance measurements are given in Table 2 and Table 3 below:

		N R_s		P R_s	
	Unit	**Median**	**Stdev**	**Median**	**Stdev**
N1/P1	Ω/sq	2005	82.4	6672	793
N2/P2 target	Ω/sq	638		1020	

Table 2: N1, P1, N2, P2 sheet resistance specifications (WG slab).

NBODY/PBODY		NBODY R_s in WG slab		PBODY R_s in WG slab		NBODY Rs in SKT slab		PBODY Rs in SKT slab	
	Unit	**Mean**	**Stdev**	**Mean**	**Stdev**	**Mean**	**Stdev**	**Mean**	**Stdev**
Sheet resistance (Rs)	Ω/sq	215	10	307	21	711	110	982	126

Table 3: NBODY/PBODY sheet resistance specifications.

Module	Sheet resistance [**Ω/sq**]	Stddev
NPLUS	45.5	0.9
PPLUS	93.0	3.4

Table 4: NPLUS/PPLUS sheet resistance specifications.

4.4.2 Patterning specifications

All dimensions in the table below are in nanometres. They are representative of the **final dimensions** after fabrication.

Specification (drawn dimensions)	target	LSL	USL	Median	Mean	StdDev	Q10	Q90	Withinin wafer stddev
N1/N2 300nm iso waveguide	300	265	335	293	296.5	15.3	280.4	320	9.2
N1/N2-SKT overlay X (mean + 3sigma)	50	0	80	40		21	17	65	
N1/N2-SKT overlay Y (mean + 3sigma)	50	0	80	31		11	16	41	
P1/P2 300nm iso waveguide	300	265	335	300	300.9	16.5	280.1	323	
P1/P2-SKT overlay X (mean + 3sigma)	50	0	80	46		14	18	46	11.3
P1/P2-SKT overlay Y (mean + 3sigma)	50	0	80	27		10	19	42	

4.5 BEOL: SAL, PCON, MHD, M1D, VIA12, M2D

The back-end-of-line (BEOL) stack regroup all the modules used to electrically contact the devices.

Parameter	Min	Typ	Max	Unit
Distance from SOI d_{MH}	1.0 µm			nm
SiN thickness t_{lin}		50 nm		nm
Distance from SOI d_{lin}		390 nm		nm

Table 5: BEOL stack specifications (see Figure 7 for related drawing).

Layer	Min	Typ	Max	Stddev	Unit
NiSi contact (SAL)		7.1	20		Ω/sq
MHD (W heater)		500	650		mΩ/sq
M1D, isolated line in high metal density region		40.7		2.4	mΩ/sq
M1D, large area in high metal density region		50.5		2.3	mΩ/sq
M2D, isolated line in high metal density region		24.4		2.4	mΩ/sq

Table 6: Backend sheet resistance specifications

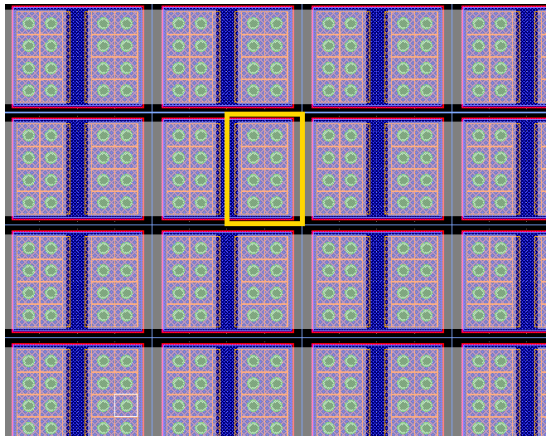


Figure 9: M1D to PPLUS 8 contacts contact chain. A unit is framed in yellow.

Structure	Median	Mean	Stddev	Q10	Q90	Unit
M1D to PPLUS 8 contacts unit (see Figure 9)	17.3	17.3	0.6	16.7	18.0	Ω
M1D to NPLUS 8 contacts unit	11.4	11.5	0.4	11.0	12.1	Ω
M1D to SAL 8 contacts unit	7	7.3	1.4	6.3	8.9	Ω

Table 7: Contact resistance specifications

4.5.1 SAL

The Si body is locally silicided where SAL is drawn. This is only allowed on non-etched Si layers.

4.5.2 PCON

4.5.2.1 Description

250 nm diameter contact vias, to be drawn using the cell provided by imec (see Library Handbook). Minimum contact pitch is 600 nm. It is recommended to provide redundancy by drawing more than one via for any given contact.

4.5.2.2 Maximum current density

No precise data is available, but comparing with imec's recommendations for its standard 130nm CMOS process, we recommend 0.6 mA/plug max current density when operating at 100°C max temperature. Higher currents should be possible at lower temperature.

4.5.3 MHD

4.5.3.1 Description

A 300nm thick tungsten layer is deposited and patterned on top of PCON to make heaters. The minimum distance to waveguides is 1 µm. The linewidth is fixed to 600nm.

All PCON vias have a 310nm MHD via on top to connect to M1D. MHD vias are added automatically during mask preparation.

4.5.3.2 Reliability

The reliability of the tungsten heaters is limited by their absolute operating temperature. We recommend 180°C as the maximum operating temperature for 1000ppm on 10 years.

4.5.4 M1D

4.5.4.1 Description

A 500 nm thick Cu layer is available as the first metal routing layer. Minimum M1D line width and space are 300nm. M1D lines wider than 10 µm are perforated with 0.6 µm oxide slots on a 1.7 µm pitch unless a M1_NOPERF region is defined. Lines wider than 30 µm will be perforated. Avoid using M1_NOPERF as it affects processing, at your own risk.

4.5.4.2 Maximum current density

Data is available from a reliability study on the smallest metal line dimensions in imec's 130nm CMOS process (300 nm x 200 nm Cu cross-section). Based on it Table 8 gives some guidance for the upper limit for the maximum current density that M1D in the silicon photonics platform can support. Furthermore, to take into account the impact of Joule heating, it is advised to half these maximum current values. At 105°C top temperature, the recommended maximum current is then 5.4mA/µm (of metal width).

Top temperature [°C]	Jmax [MA/cm^2]
70	11.6
80	6.0
105	2.6
125	1.2

Table 8: For 10 years lifetime, as function of temperature

4.5.5 VIA12

A VIA12 is a square of 0.6 µm side. Minimum spacing between vias is 600 nm. The via thickness target is 500 nm.

4.5.6 M2D

Minimum width and spacing must not be less than 900 nm. A M2D line should not be wider than 50 µm. M2 lines wider than 10 µm are perforated unless a M2_NOPERF region is

defined. Lines wider than 30 µm will be perforated. Avoid using M2_NOPERF as it affects processing, at your own risk.

The targeted thickness is 700nm. Using the same model than for M1, it is advised to limit the maximum current to 9.1mA/um (of metal width) at a maximal operating temperature of 105°C.

4.6 Passivation module and bond pads: PASS1 and METPASS

PASS1 is used to open the passivation before the AlCu layer is deposited and pattern with METPASS. Standard pads are provided in the Library which adhere to design rules. Use them.

4.7 Optical BEOL: LPASS, EXPO, PASS2, TRENCH

4.7.1 LPASS

LPASS (for Light Pass) is used to remove the dielectric stack (nitride liner, BEOL dielectric stack). It has been designed to be used over grating couplers.

4.7.2 EXPO

EXPO is used to etch the BEOL stack to access FEOL layers. For depth control the etch stops on the polysilicon (etch stop layer) before removing it.

4.7.3 PASS2

After deposition of the silicon oxide used for the edge coupler, PASS2 is used to open it above the bond pads to allow contacting and wire bonding.

4.7.4 TRENCH

TRENCH is used to define the deep etch through the full stack and down 60 µm into the silicon. Facets of edge couplers are created by this etch.

5 Summary of possible options

The customer can choose between the following mutually exclusive options:

- Optimized process for Ge photodetectors (O-band and C-band photodetectors).
- Optimized process for SiGe devices (C-band EAM and photodetectors).