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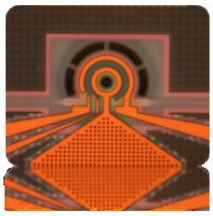
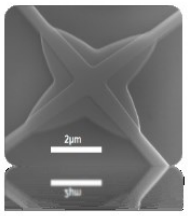
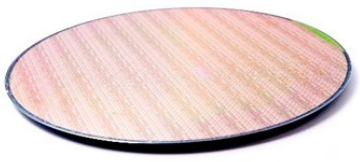
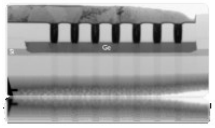
# Layout Handbook

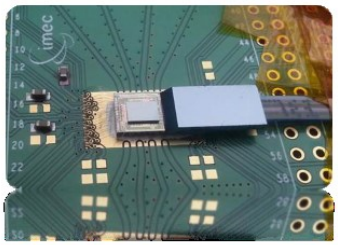
# ISIPP50G 2.3.0









# Changes

| Version | Change |
|---|---|
| | |
| **X.Y.Z** | See changelog document |
| **1.0.1** | Bug fixes release |
| **1.0.0** | Initial release |

# Contents

# 1 Document information

## 1.1 Purpose

The purpose of this document is to describe the layout rules to be followed when designing into imec silicon photonics ISIPP50G technology. The imec silicon photonics platform consists of predefined fixed process modules. This Layout Handbook documents the ISIPP50G technology only. For customized processes, contact imec directly.

## 1.2 Scope

The layout rules presented here have to be followed when doing a full custom design in the imec ISIPP50G technology. The rules are applicable for every design submitted to imec.

## 1.3 Responsibility

Every customer submitting a design in the imec ISIPP50G technology has to follow the rules as stated in this document. It is their responsibility to check whether or not these rules have been used, prior to submitting a design. The rules have to be followed for every design. Any deviation from the design rules gives imec the right to refuse the design for processing. Imec cannot provide any guarantee that the circuit will have the functionality it was designed for.

# 2 Data preparation overview

After a design file has been submitted to imec for fabrication it enters a mask data preparation flow before the reticules can be manufactured. A simplified view of flow is:

1. Verification of conformance of incoming design:
    - GDSII file structure.
    - DRC free layout.
    - PDK cells.
2. The cells from the PDK library present in the design are force replaced by their golden version.
3. All the designs belonging to the same masks set are assembled together with the optical and electrical process control module (PCM). The result then goes through tiling (optical and metal layers) and perforation (metal layers).
4. Boolean operations are then performed on the design data.
5. The frame around the design data is assembled with the structures needed for processing. They are alignment marks and, for in-line measurements: overlay control structures, dimension control (CD) structures and thickness measurement structures.
6. Design data and frame are assembled.
7. Mask level rule checks (MRC) are performed to verify the masks can be manufactured and the masks set is compatible with a safe processing (no cross-contamination etc).
8. The masks set is signed-off and tape out to the masks shop.

# 3 Layout data exchange format

The file format for layout submission is Calma GDSII. This format is supported by all major design automation software tools and is the de facto data standard.

The following restrictions apply:

- Library and structure names must start by a letter (a to z, A to Z) and then be composed of letters (a to z, A to Z), numbers (0 to 9) or underscore "_". They must not include dot `.`, slash `/`, backslash `\`, equal sign `=`, asterisk `*`, percent `%`, `#`, `@`, `!`, parenthesis `()` etc.
- The hierarchy of the submitted design must not exceed 28 levels.
- Shapes that self-intersect are not allowed.
- Shapes with zero data (no vertices) are not allowed.
- GDSII Elements must be limited to the following types:
    - BOUNDARY (filled, closed polygon),
    - PATH (open line with a certain centerline and width),
    - SREF (singular reference to a structure, also called instance),
    - AREF (array reference to a structure).
- Rotated SREF or AREF (instances) are only allowed under 90° angles (0, 90, 180, 270). Any other rotation angle is not allowed.
- Shapes with acute angles <85° are not allowed on any layer/datatype, except on DOC.
- Do not use magnification with magnification factor different from 1.

- *The database unit of the GDSII file must be set to 1 nm* (1E-9) while the user unit should be set to 1 um (1E-6). Files with a different grid will be converted. The resulting grid snapping can lead to unintended variations of the structure and design rule violations.

# 4 Layout guidelines

- For every layer, the design grid to be used is indicated later in this document if different from 1 nm. This design grid can be equal to or larger than the grid of the GDSII file but the designers are required to stick to the specified design grid for each layer.
- Avoid the coincidence of edges on different layers.
- While GDSII PATH elements are supported, GDSII BOUNDARY elements are preferred to avoid unpredictable grid snapping for photonics front-end layers.
- Text labels and logos to be included in the design data should be defined as polygons (BOUNDARY) on layer LOGOTXT, not as GDSII LABELS. GDSII LABELS will be ignored by imec.
- No data should introduce layout rule violation. If layout rule violations cannot be avoided, the designer shall always notify imec prior to the design submission, the cell name of the structure not complying and the layout rule which is violated. It is imec's decision whether or not to accept the design for fabrication.
- The current PDK library is not DRC free. Imec will waive any error in the PDK library automatically.

# 5 CAD and mask layers

## 5.1 Nomenclature

CAD layers are the layers a designer draws on. Each layer has unique name (mnemonic) and a unique pair of GDSII layer and GDSII datatype.

Mask layers are the actual masks as used in the fabrication process. The mask layer data is derived from the CAD layers and other information using Boolean operations.

## 5.2 CAD layers

| mnemonic | purpose | for designer | description | gdsii layer | gdsii data type |
|---|---|---|---|---|---|
| **WG_COR** | drawing | yes | Fully etched Si body: waveguide core | 37 | 4 |
| **WG_CLD** | drawing | yes | Fully etched Si body: waveguide cladding | 37 | 5 |
| **WG_TRE** | drawing | yes | Fully etched Si body: trenches | 37 | 6 |
| **WG_HOL** | drawing | yes | Fully etched Si body: regular hole lattice | 37 | 2 |

| | | | | | |
|---|---|---|---|---|---|
| **FC_COR** | drawing | yes | 70nm etched Si body: waveguide core | 35 | 4 |
| **FC_CLD** | drawing | yes | 70nm etched Si body: waveguide cladding | 35 | 5 |
| **FC_TRE** | drawing | yes | 70nm etched Si body: trenches | 35 | 6 |
| **FC_HOL** | drawing | yes | 70nm etched Si body: regular hole lattice | 35 | 2 |
| **SKT_COR** | drawing | yes | 160nm etched Si body: waveguide core | 43 | 4 |
| **SKT_CLD** | drawing | yes | 160nm etched Si body: waveguide cladding | 43 | 5 |
| **SKT_TRE** | drawing | yes | 160nm etched Si body: trenches | 43 | 6 |
| **SKT_HOL** | drawing | yes | 160nm etched Si body: regular hole lattice | 43 | 2 |
| **NBODY** | drawing | yes | N-type Body implant | 25 | 0 |
| **PBODY** | drawing | yes | P-type Body implant | 26 | 0 |
| **FCW_COR** | drawing | yes | Poly silicon (islands and lines) | 31 | 6 |
| **FCW_TRE** | drawing | yes | Etched poly, must be on FCW_INV | 31 | 4 |
| **FCW_INV** | drawing | yes | Poly area with FCW_TRE | 31 | 5 |
| **N1** | drawing | yes | N-type implant - dose 1 | 2 | 0 |
| **P1** | drawing | yes | P-type implant - dose 1 | 3 | 0 |
| **N2** | drawing | yes | N-type implant - dose 2 | 6 | 0 |
| **P2** | drawing | yes | P-type implant - dose 2 | 7 | 0 |
| **NPLUS** | drawing | yes | N-type contact implant | 4 | 0 |
| **PPLUS** | drawing | yes | P-type contact implant | 5 | 0 |
| **SAL** | drawing | yes | Local Silicide | 8 | 0 |
| **PCON** | drawing | yes | Tungsten Contact Plugs | 10 | 0 |
| **MH_DRW** | drawing | yes | Metal heater | 14 | 6 |
| **M1_DRW** | drawing | yes | Metal 1 (Cu damascene): drawing | 11 | 1 |
| **M1_NOFILL** | drawing | yes | Metal 1 (Cu damascene): dummy fill exclusion zone | 11 | 9 |
| **M1_PERF** | drawing | yes | Metal 1 (Cu damascene): perforation | 11 | 11 |
| **M1_NOPERF** | drawing | yes | Metal 1 (Cu damascene): perforation exclusion zone | 11 | 12 |
| **VIA12** | drawing | yes | M1 to M2 Via | 12 | 0 |
| **M2_DRW** | drawing | yes | Metal 2 (Cu damascene): drawing | 13 | 1 |
| **M2_NOFILL** | drawing | yes | Metal 2 (Cu damascene): dummy fill exclusion zone | 13 | 9 |
| **M2_PERF** | drawing | yes | Metal 2 (Cu damascene): perforation | 13 | 11 |
| **M2_NOPERF** | drawing | yes | Metal 2 (Cu damascene): perforation exclusion zone | 13 | 12 |
| **PASS1** | drawing | yes | Windows in passivation nitride | 16 | 0 |
| **METPASS** | drawing | yes | AlCu bond pads | 18 | 0 |
| **EXPO** | drawing | yes | BEOL etch for waveguide exposure | 83 | 0 |
| **LPASS** | drawing | yes | BEOL etch for grating couplers and edge couplers | 91 | 0 |

| | | | | | |
|---|---|---|---|---|---|
| **PASS2** | drawing | yes | Open passivation on bond pads | 17 | 0 |
| **TRENCH** | drawing | yes | Deep Trench | 88 | 0 |
| **OPT_DUM** | drawing | yes | Placement of dummy cells in optical layers (WG, FC, SKT, FCW) | 101 | 0 |
| **LOGOTXT** | drawing | yes | Text and logo on WG, M1 and M2 | 100 | 0 |
| **NOMET** | drawing | yes | No metal | 102 | 0 |
| **NOFILL** | drawing | yes | No dummy of any sort | 1158 | 0 |
| **VERTBX** | documentation | yes | Vertical port indication | 1000 | 0 |
| **DICING** | drawing | yes | Dicing street | 1111 | 0 |
| **DOC** | documentation | yes | Other documentation information | 1152 | 0 |
| **IP** | documentation | no | IP box | 129 | 0 |
| **LABEL** | text | internal | Device label | 1002 | 0 |
| **PIN** | marking | internal | PIN recognition layer | 1003 | 0 |
| **PAYLOAD_DRW** | marking | yes | Outline of design block | 1110 | 1 |

## 5.3 Remarks

### 5.3.1 Text labels and logos

Text labels and logos which should be visible on the chip need to be drawn in the LOGOTXT layer. This layer needs to adhere to design rules. The LOGOTXT layer will automatically be placed on the WG layer and on the metal layers M1 and M2.

Text should NOT be put on the regular drawing layers (WG_COR, M1_DRW, etc).

When possible, a tile free zone will automatically be added around LOGOTXT for better legibility.

### 5.3.2 Dummy tiling

For uniform processing of some layers (for example WG, FC, SKT, FCW, M1, M2) the features density should be as uniform as possible. Therefore dummy structures are added to compensate the features density variations across the design area of the full mask. A designer can influence the tiling process in the following way:

- Provide hints where tiles for optical layers (WG, FC, SKT, FCW) should be added by drawing squares in OPT_DUM with a side width of exactly 2.800 µm and sides parallel to grid axis. Notice that they are only hint and only for local usage. Hints further than 2 dummies away from design will be automatically ignored.
- Use M1_NOFILL or M2_NOFILL to define areas where no metal dummy should be added on M1 or M2 respectively.
- Use NOFILL where no dummy (optical or M1 or M2) should be added.

SOI area that must not be covered by optical dummies but where metal dummies are acceptable (ex: slab waveguide) should be defined with a WG_COR, FC_COR or SKT_COR layer plus the associated _CLD layer.

### 5.3.3 Perforation

On the metal layers M1 and M2, large area with width >10 µm will be automatically perforated by small dielectric area to control the local density as required by the CMP process. A designer can use M1_NOPERF or M2_NOPERF to give hints where perforation should be avoided. Use them very sparingly as it can adversely influence processing.

## 5.4 Mask generation formulas

To help understand how CAD layers should be used, some Boolean formulas used to generate the mask data are given on Table 1 below. The tone of the mask is either Dark Field (DF) or Light Field (LF). Since only positive resist is used in the process flow, for DF masks the polygons define a clear area on the mask and therefore an area that will be etch away on the wafer. For LF masks the polygon define an opaque area on the mask that will *not* be etched on the wafer.

| Mask | Boolean formula | Mask tone |
|---|---|---|
| **WG** | (WG_CLD not WG_COR) or WG_TRE or WG_HOL or LOGOTXT | DF |
| **FC** | (FC_CLD not FC_COR) or FC_TRE or FC_HOL | DF |
| **SKT** | (SKT_CLD not SKT_COR) or SKT_TRE or SKT_HOL | DF |
| **FCW** | (FCW_INV not FCW_TRE) or FCW_COR | LF |
| **M1D** | (M1_DRW not M1_PERF) or LOGOTXT | DF |
| **M2D** | (M2_DRW not M2_PERF) or LOGOTXT | DF |

*Table 1: Mask Boolean formula for design data.*

# 6 Drawing guidelines

## 6.1 Layers use

The figures below clarify the relation between mask layers and process modules:

- SOI patterning (WG, FC, SKT): Figure 1, Figure 2, Figure 3 and Figure 4.
- Poly-Si patterning (FCW): Figure 5 and Figure 6.
- SOI doping (NBODY, PBODY, N1, P1, N2, P2, NPLUS, PPLUS): Figure 7, Figure 8 and Figure 9.
- Contacting (SAL, PCON): Figure 10.

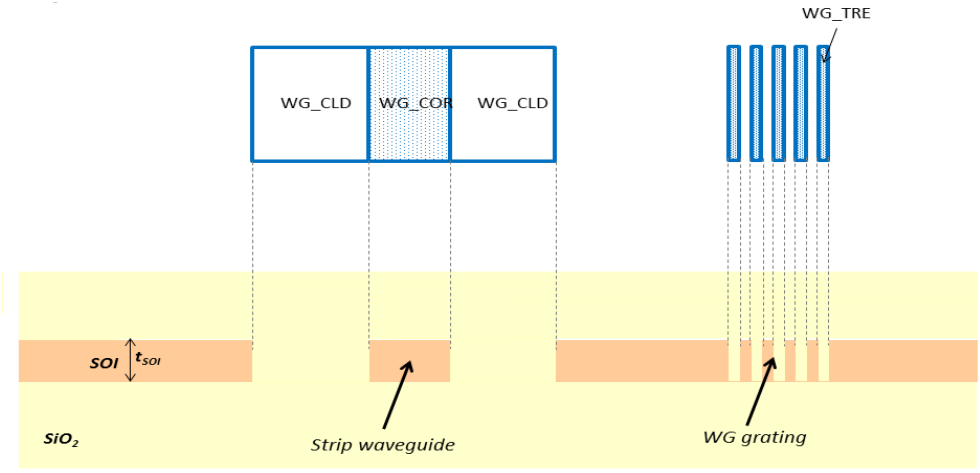



*Figure 1: SOI patterning - WG cross-section and mask layers*

All waveguide lines (WG_COR) have to be drawn on a cladding (WG_CLD) area. Other trenches filled with cladding material should be drawn on WG_TRE. These can be drawn on top of WG_COR lines to draw a grating in a waveguide. Similarly, one can draw holes inside a waveguide by drawing WG_HOL on WG_COR. WG_HOL is for drawing photonic crystals and allows to draw smaller holes or thinner hole separations than normal WG patterning but with no warranty of being printed properly. WG_HOL must be drawn on WG_COR and not overlap with trenches WG_TRE. It is *strongly* recommended to draw WG_COR where a slab is expected and not default to the implicit behavior of the technology (DF mask + positive resist).

The same applies for FC_ and SKT_ layers on Figure 2 and Figure 4.

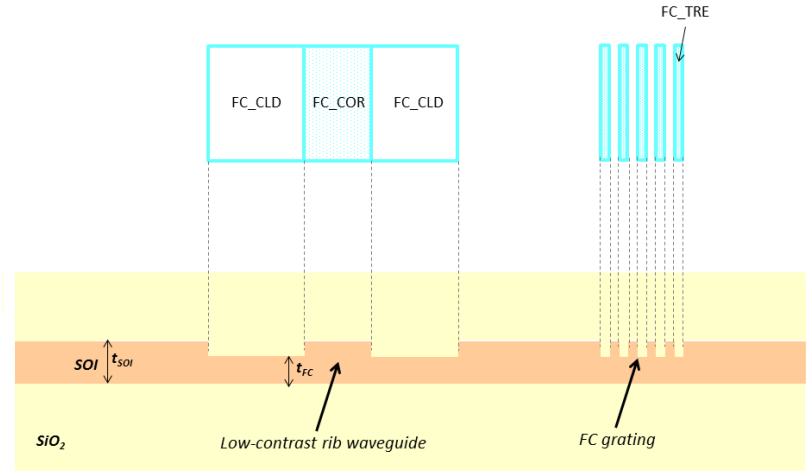



*Figure 2: SOI patterning, FC cross-section and mask layers.*

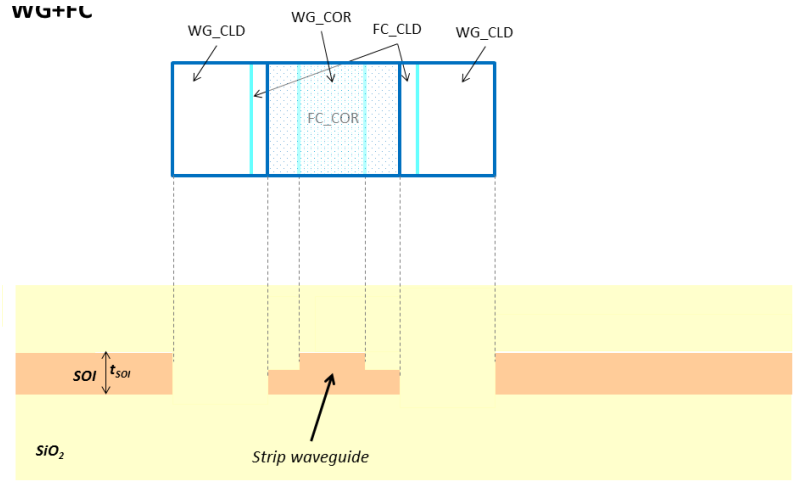



*Figure 3: SOI patterning: combination of WG and FC cross-section and mask layers.*

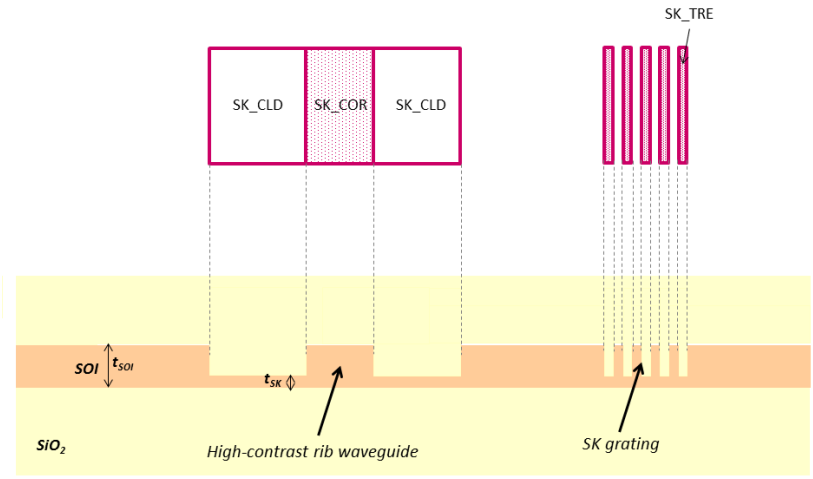



*Figure 4: SOI patterning, SKT cross-section and mask layers.*

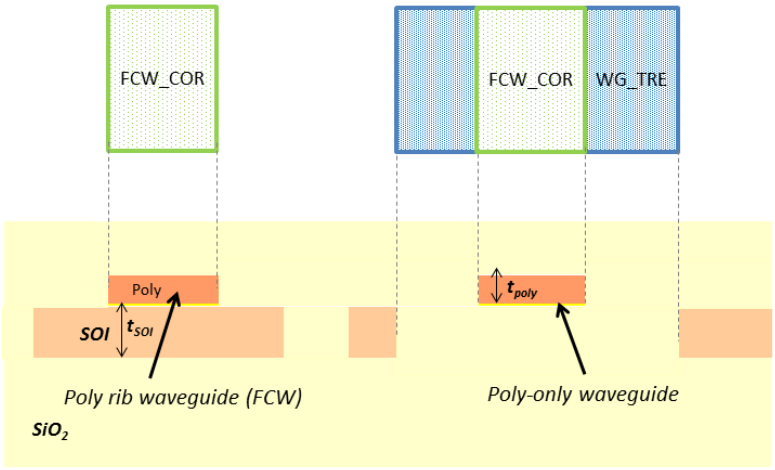



*Figure 5: Poly patterning: FCW cross-section and mask layers.*

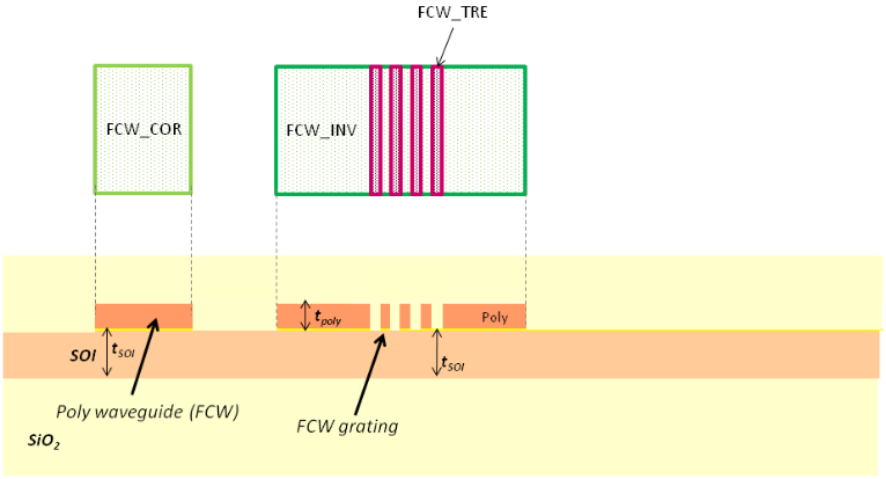



*Figure 6: Poly patterning: FCW cross-section and mask layers.*

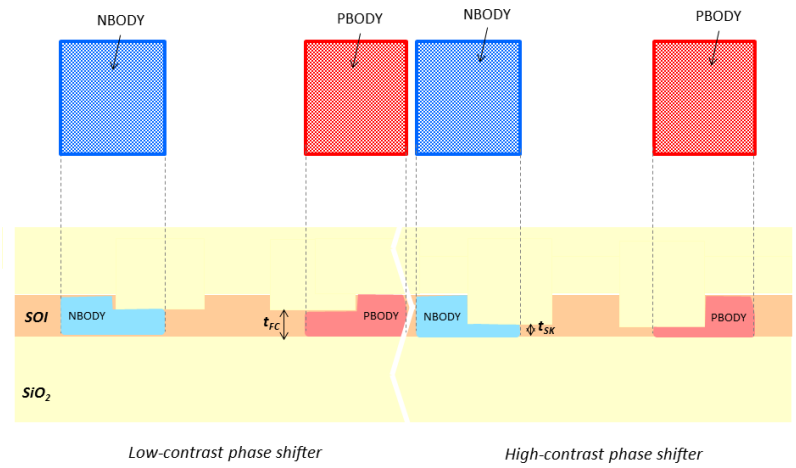



*Figure 7: SOI doping: NBODY and PBODY implants for low-resistance paths, cross-section and mask layers.*

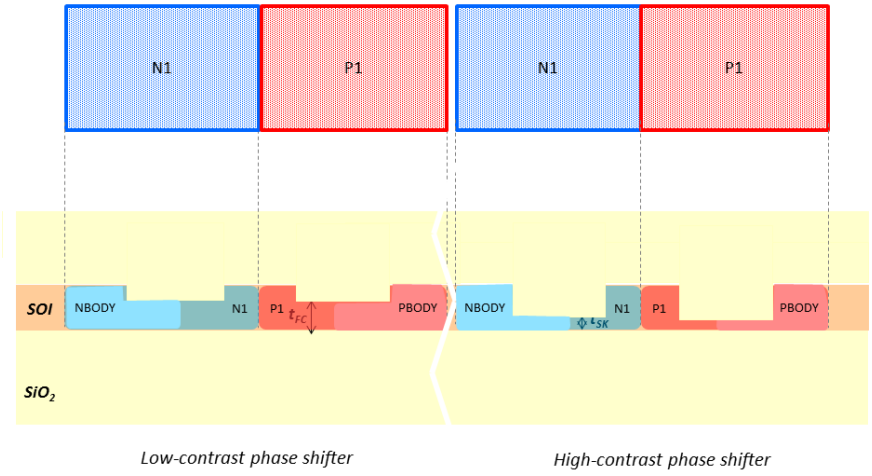



*Figure 8: SOI doping: Cross-section and mask layers for N1 and P1, implants for modulator junctions. N2 and P2 implants (high doping) should be used in a similar fashion.*

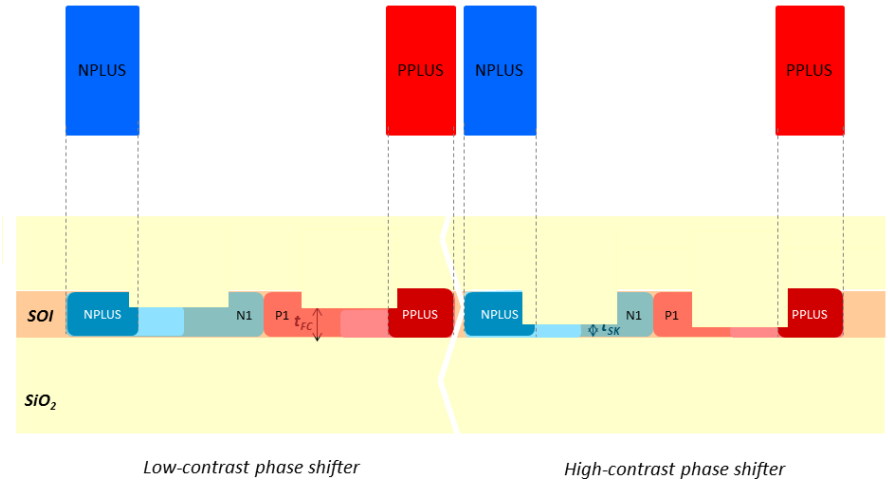



*Figure 9: SOI doping: Cross-section and mask layers for NPLUS and PPLUS, implants for contacting.*

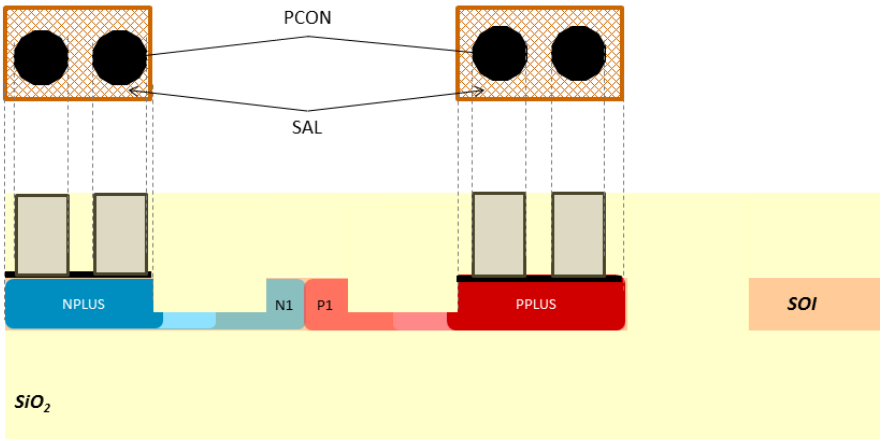



*Figure 10: Cross-section and mask layers for silicide (SAL) and contacts (PCON) contact modules.*

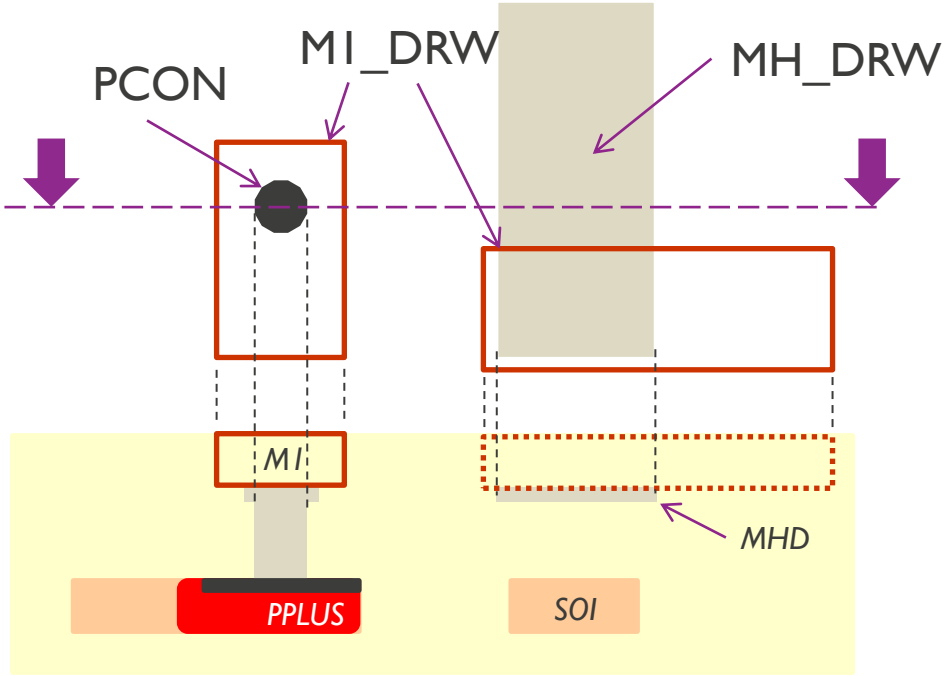



*Figure 11: (top) Layout example of PCON, MH_DRW and M1_DRW (bottom) Corresponding cross section.*

## 6.2 Layout templates

A user layout should be done on top of one of the template provided in the library. See the library handbook for details on how to use it in conjunction with edge couplers.

### 6.3 Using Library Cells

The devices from the library are provided as fixed GDSII cells. After a design has been accepted, the design will be automatically inspected. *All cells recognized as belonging to imec's devices library will be force-replaced by the reference cells* ('golden cells') to ensure the correct version is used. The tool recognize that a cell belong to the library based on the following criteria:

- The name of the cell.
- The presence of 3 labels (GDSII text) in the LABEL layer: cell name, imec name and PDK version.

To ensure cells are correctly recognized, all criteria (name of the cell and labels) are checked. It is therefore an error when:

- A cell has been renamed.
- Any of the labels is missing or has been modified.

Notice also that library cells contain sub-cells whose name is constructed as `<device_name>_<integer>`. For example the cell M12CTE_FC_5000_25400 contains one sub-cell, M12CTE_FC_5000_25400_1.

Users must not modify library cells in any way. You cannot:

- Modify the origin.
- Modify the content (shapes, subcells, layers etc).
- Rename the cell or its subcells.
- Alter the labels.
- Flatten the hierarchy.
- Etc.

## 7 Layer rules

### 7.1 Rules check tool

The DRC deck included in the PDK is written for Calibre from Mentor Graphics. It has been tested with Calibre 2015.4_16.11 . Older versions are known to be incompatible.

### 7.2 DRC deck usage

An example driver file, `isipp50g_batch.cal` is provided. It can be used without modification to run DRC jobs. For that set the following environment variables:

| Environment variable | Meaning |
|---|---|
| **$layout_path** | Path to the GDSII layout to verify |
| **$results** | Path to write the result database (ASCII format) to |
| **$summary_report** | Path to write the summary report to |

| | |
|---|---|
| **$ISIPP_DRC_INCLUDE_DIR** | Path to the directory containing the DRC deck files. Default to "." |

## 7.3 Rules: warnings and errors

There are 2 categories of rules:

- Rules with a 'WARNING' prefix in the mnemonic are warnings. They are to provide information to the designer and should be followed when possible. If a designer choose to ignore a warning, she does so at her own risk.
- All the other rules were written to catch errors. If you have a good reason, you may ask imec for a waiver for a specific error flagged by a rule. A waiver will be refused if it deemed necessary for processing. The layout submitted for fabrication MUST be error free or with all errors waived.

## 7.4 Rules list

### 7.4.1 WG rules

| Mnemonic | Description |
|---|---|
| **WG.W.130** | Minimum WG width=0.130 micron |
| **WARNING.WG.W.150** | WG width < 0.150 and >= 0.130 allowed but out of process window |
| **WG.S.130** | Minimum WG spacing=0.130 micron |
| **WARNING.WG.S.150** | WG spacing < 0.150 and >= 0.130 allowed but out of process window |
| **WG.SHARPANGLE** | Angle < 85 degrees |
| **WARNING.WG.SMALLNOTCH** | Small notch (<=50nm) on WG |
| **WG_COR.I.WG_CLD** | WG_COR outside WG_CLD |

### 7.4.2 WG_HOL rules

| Mnemonic | Description |
|---|---|
| **WARNING.WG_HOL.S.1** | WG_HOL spacing between 0.20um and 0.120um is allowed but will not print accurately. Use at your own risks. |
| **WARNING.WG_HOL.S.2** | The distance between WG_HOL and the rest of the WG etch pattern is between 0.20um and 0.120um. This is allowed but will not print accurately. Use at your own risks. |
| **WARNING.WG_HOL.W.1** | WG_HOL width between 0.20um and 0.120um is allowed but will not print accurately. Use at your own risks. |
| **WARNING.WG_HOL.MinArea** | WG_HOL between area between 0.0314 um**2 and 0.0113 um**2 is allowed but will not print accurately. Use at your own risks. |
| **WG_HOL.S.1** | Absolute minimum WG_HOL spacing is 0.120um |
| **WG_HOL.S.2** | Absolute minimum distance between WG_HOL and the rest of the WG etch pattern is 0.120um. |
| **WG_HOL.W.1** | Absolute minimum WG_HOL width is 0.120um |

| | |
|---|---|
| **WG_HOL.MinArea** | Absolute minimum area of WG_HOL region is 0.0113 um**2 |
| **WG_HOL.CONCAV** | Illegal concave WG_HOL shape |
| **WG_HOL.I.WG_COR** | WG holes must be defined on WG_COR |
| **WG_HOL.IO.WG_TRE** | Illegal overlap between WG holes and trenches |
| **WG_HOL.IO.WG_CLD** | No overlap between WG holes and cladding outside of WG_COR |

### 7.4.3 FC rules

| Mnemonic | Description |
|---|---|
| **FC.W.180** | Minimum FC width=0.180 micron |
| **FC.S.180** | Minimum FC spacing=0.180 micron |
| **FC.SHARPANGLE** | Angle < 85 degrees |
| **WARNING.FC.SMALLNOTCH** | Small notch (<=50nm) on FC |
| **FC_COR.I.FC_CLD** | FC_COR outside FC_CLD |

### 7.4.4 FC_HOL rules

| Mnemonic | Description |
|---|---|
| **WARNING.FC_HOL.S.1** | FC_HOL spacing between 0.20um and 0.120um is allowed but will not print accurately. Use at your own risks. |
| **WARNING.FC_HOL.S.2** | The distance between FC_HOL and the rest of the FC etch pattern is between 0.20um and 0.120um. This is allowed but will not print accurately. Use at your own risks. |
| **WARNING.FC_HOL.W.1** | FC_HOL width between 0.20um and 0.120um is allowed but will not print accurately. Use at your own risks. |
| **WARNING.FC_HOL.MinArea** | FC_HOL between area between 0.0314 um**2 and 0.0113 um**2 is allowed but will not print accurately. Use at your own risks. |
| **FC_HOL.S.1** | Absolute minimum FC_HOL spacing is 0.120um |
| **FC_HOL.S.2** | Absolute minimum distance between FC_HOL and the rest of the FC etch pattern is 0.120um. |
| **FC_HOL.W.1** | Absolute minimum FC_HOL width is 0.120um |
| **FC_HOL.MinArea** | Absolute minimum area of FC_HOL region is 0.0113 um**2 |
| **FC_HOL.CONCAV** | Illegal concave FC_HOL shape |
| **FC_HOL.IO.FC_TRE** | Illegal overlap between FC holes and trenches |
| **FC_HOL.IO.FC_CLD** | No overlap between FC holes and cladding |

### 7.4.5 SKT rules

| Mnemonic | Description |
|---|---|
| **SKT.W.180** | Minimum SKT width=0.180 micron |
| **SKT.S.180** | Minimum SKT spacing=0.180 micron |
| **SKT.SHARPANGLE** | Angle < 85 degrees |
| **WARNING.SKT.SMALLNOTCH** | Small notch (<=50nm) on SKT |
| **SKT_COR.I.SKT_CLD** | SKT_COR outside SKT_CLD |

### 7.4.6 SKT_HOL

| Mnemonic | Description |
|---|---|
| **WARNING.SKT_HOL.S.1** | SKT_HOL spacing between 0.20um and 0.120um is allowed but will not print accurately. Use at your own risks. |
| **WARNING.SKT_HOL.S.2** | The distance between SKT_HOL and the rest of the SKT etch pattern is between 0.20um and 0.120um. This is allowed but will not print accurately. Use at your own risks. |
| **WARNING.SKT_HOL.W.1** | SKT_HOL width between 0.20um and 0.120um is allowed but will not print accurately. Use at your own risks. |
| **WARNING.SKT_HOL.MinArea** | SKT_HOL between area between 0.0314 um**2 and 0.0113 um**2 is allowed but will not print accurately. Use at your own risks. |
| **SKT_HOL.S.1** | Absolute minimum SKT_HOL spacing is 0.120um |
| **SKT_HOL.S.2** | Absolute minimum distance between SKT_HOL and the rest of the SKT etch pattern is 0.120um. |
| **SKT_HOL.W.1** | Absolute minimum SKT_HOL width is 0.120um |
| **SKT_HOL.MinArea** | Absolute minimum area of SKT_HOL region is 0.0113 um**2 |
| **SKT_HOL.CONCAV** | Illegal concave SKT_HOL shape |
| **SKT_HOL.I.SKT_COR** | SKT holes must be defined on SKT_COR |
| **SKT_HOL.IO.SKT_TRE** | Illegal overlap between SKT holes and trenches |
| **SKT_HOL.IO.SKT_CLD** | No overlap between SKT holes and cladding |

### 7.4.7 NBODY and PBODY rules

| Mnemonic | Description |
|---|---|
| **NBODY.W.300** | Minimum NBODY width=0.300 micron |
| **NBODY.S.300** | Minimum NBODY spacing=0.300 micron |
| **NBODY.SHARPANGLE** | Angle < 85 degrees |
| **NBODY.MinArea** | Minimum area of NBODY region is 0.25 sq um |
| **PBODY.W.300** | Minimum PBODY width=0.300 micron |
| **PBODY.S.300** | Minimum PBODY spacing=0.300 micron |
| **PBODY.SHARPANGLE** | Angle < 85 degrees |
| **PBODY.MinArea** | Minimum area of PBODY region is 0.25 sq um |

### 7.4.8 FCW rules

| Mnemonic | Description |
|---|---|
| **FCW.W.170** | Minimum FCW width=0.170 micron |
| **FCW.S.170** | Minimum FCW spacing=0.170 micron |
| **FCW.SHARPANGLE** | Angle < 85 degrees |
| **FCW_COR.IO.FCW_INV** | Illegal overlap between FCW_COR and FCW_INV |
| **FCW_TRE.O.FCW_INV** | FCW_TRE must overlay FCW_INV |

### 7.4.9 N1 and P1 rules

| Mnemonic | Description |
|---|---|
| **N1.W.300** | Minimum N1 width=0.300 micron |
| **N1.S.300** | Minimum N1 spacing=0.300 micron |
| **N1.SHARPANGLE** | Angle < 85 degrees |
| **N1.MinArea** | Minimum area of N1 region is 0.25 sq um |
| **N1.IO.FCW** | Illegal overlap between N1 and FCW layers |
| **P1.W.300** | Minimum P1 width=0.300 micron |
| **P1.S.300** | Minimum P1 spacing=0.300 micron |
| **P1.SHARPANGLE** | Angle < 85 degrees |
| **P1.MinArea** | Minimum area of P1 region is 0.25 sq um |
| **P1.IO.FCW** | Illegal overlap between P1 and FCW layers |

### 7.4.10 N2 and P2 rules

| Mnemonic | Description |
|---|---|
| **N2.W.300** | Minimum N2 width=0.300 micron |
| **N2.S.300** | Minimum N2 spacing=0.300 micron |
| **N2.SHARPANGLE** | Angle < 85 degrees |
| **N2.MinArea** | Minimum area of N2 region is 0.25 sq um |
| **N2.IO.FCW** | Illegal overlap between N2 and FCW layers |
| **P2.W.300** | Minimum P2 width=0.300 micron |
| **P2.S.300** | Minimum P2 spacing=0.300 micron |
| **P2.SHARPANGLE** | Angle < 85 degrees |
| **P2.MinArea** | Minimum area of P2 region is 0.25 sq um |
| **P2.IO.FCW** | Illegal overlap between P2 and FCW layers |

### 7.4.11 NPLUS and PPLUS rules

| Mnemonic | Description |
|---|---|
| **NPLUS.W.300** | Minimum NPLUS width=0.300 micron |
| **NPLUS.S.300** | Minimum NPLUS spacing=0.300 micron |
| **NPLUS.SHARPANGLE** | Angle < 85 degrees |
| **NPLUS.MinArea** | Minimum area of NPLUS region is 0.25 sq um |
| **WARNING.NPLUS.S.FC_COR** | NPLUS and FC_COR distance <= 1um : potential for higher loss device |
| **WARNING.NPLUS.S.SKT_COR** | NPLUS and SKT_COR distance < 0.75um : potential for higher loss device |
| **WARNING.NPLUS.overlap.WG_ETCH** | Overlap between NPLUS and WG etch layers |
| **WARNING.NPLUS.overlap.FC_ETCH** | Overlap between NPLUS and FC etch layers |
| **WARNING.NPLUS.overlap.SKT_ETCH** | Overlap between NPLUS and SKT etch layers |
| **NPLUS.IO.FCW** | Illegal overlap between NPLUS and FCW layers |
| **PPLUS.W.300** | Minimum PPLUS width=0.300 micron |
| **PPLUS.S.300** | Minimum PPLUS spacing=0.300 micron |

| | |
|---|---|
| **PPLUS.SHARPANGLE** | Angle < 85 degrees |
| **PPLUS.MinArea** | Minimum area of PPLUS region is 0.25 sq um |
| **WARNING.PPLUS.S.FC_COR** | PPLUS and FC_COR distance <= 1um : potential for higher loss device |
| **WARNING.PPLUS.S.SKT_COR** | PPLUS and SKT_COR distance < 0.75um : potential for higher loss device |
| **WARNING.PPLUS.overlap.WG_ETCH** | Overlap between PPLUS and WG etch layers |
| **WARNING.PPLUS.overlap.FC_ETCH** | Overlap between PPLUS and FC etch layers |
| **WARNING.PPLUS.overlap.SKT_ETCH** | Overlap between PPLUS and SKT etch layers |
| **PPLUS.IO.FCW** | Illegal overlap between PPLUS and FCW layers |

### 7.4.12 SAL rules

| Mnemonic | Description |
|---|---|
| **SAL.W.600** | Minimum SAL width=0.600 micron |
| **SAL.S.600** | Minimum SAL spacing=0.600 micron |
| **SAL.SHARPANGLE** | Angle < 85 degrees |
| **SAL.MinArea** | Minimum area of SAL region is 0.36 sq um |
| **SAL.IO.WG_CLD** | Illegal overlap between SAL and WG_CLD (when not on FCW or WG_COR) |
| **SAL.IO.WG_TRE** | Illegal overlap between SAL and WG_TRE (when not on FCW) |
| **SAL.IO.WG_HOL** | Illegal overlap between SAL and WG_HOL (when not FCW) |
| **SAL.IO.FC_CLD** | Illegal overlap between SAL and FC_CLD (when not on FCW or FC_COR) |
| **SAL.IO.FC_TRE** | Illegal overlap between SAL and FC_TRE (when not on FCW) |
| **SAL.IO.FC_HOL** | Illegal overlap between SAL and FC_HOL (when not FC_HOL) |
| **SAL.IO.SKT_CLD** | Illegal overlap between SAL and SKT_CLD (when not on FCW or SKT_COR) |
| **SAL.IO.SKT_TRE** | Illegal overlap between SAL and SKT_TRE (when not on FCW) |
| **SAL.IO.SKT_HOL** | Illegal overlap between SAL and SKT_HOL (when not SKT_HOL) |
| **WARNING.SAL.S.FC_COR** | Salicide and FC_COR distance <= 1um : potential for higher loss device |
| **WARNING.SAL.S.SKT_COR** | Salicide and SKT_COR distance < 0.75um : potential for higher loss device |
| **SAL.S.ETCH** | Spacing between SAL and SOI etch must be >= 0.100 um |
| **WARNING.SAL.O.IMP** | Silicide should overlap with NPLUS or PPLUS |
| **NPLUS.E.SAL** | NPLUS enclose SAL with 0.075 um margin |
| **SAL.EXT.NPLUS** | NPLUS must enclose SAL |
| **NPLUS.SAL.COINCIDENTEDGES** | NPLUS and SAL coincident edges are not allowed |
| **PPLUS.E.SAL** | PPLUS enclose SAL with 0.075 um margin |

| | |
|---|---|
| **SAL.EXT.PPLUS** | PPLUS must enclose SAL |
| **PPLUS.SAL.COINCIDENTEDGES** | PPLUS and SAL coincident edges are not allowed |
| **FCW.E.SAL** | FCW enclose SAL with 0.100 um margin |

### 7.4.13 PCON rules

| Mnemonic | Description |
|---|---|
| **PCON.S.1_1** | Minimum PCON spacing=0.35um |
| **PCON.Area** | Area of PCON region is 0.048012 +-0.0006 sq um |
| **PCON.VERTEX** | Number of vertices for PCON < 20 |
| **PCON.CONCAV** | Illegal concave contact shape |
| **PCON.IO.WG_CLD** | Illegal overlap between PCON and WG_CLD (when not on WG_COR) |
| **PCON.IO.WG_TRE** | Illegal overlap between PCON and WG_TRE (when not on FCW) |
| **PCON.IO.WGHOL** | Illegal overlap between PCON and WG_HOL (when not on FCW) |
| **PCON.IO.FC_CLD** | Illegal overlap between PCON and FC_CLD (when not on FC_COR or FCW) |
| **PCON.IO.FC_TRE** | Illegal overlap between PCON and FC_TRE (when not on FCW) |
| **PCON.IO.FC_HOL** | Illegal overlap between PCON and FC_HOL (when not on FCW) |
| **PCON.IO.SKT_CLD** | Illegal overlap between PCON and SKT_CLD (when not on FC_COR or FCW) |
| **PCON.IO.SKT_TRE** | Illegal overlap between PCON and SKT_TRE (when not on FCW) |
| **PCON.IO.SKT_HOL** | Illegal overlap between PCON and SKT_HOL (when not on FCW) |
| **PCON.I.SAL** | PCON not allowed outside of SAL |
| **SAL.E.PCON** | Minimum enclosure of PCON by salicide of 0.150 um |

### 7.4.14 MH rules

| Mnemonic | Description |
|---|---|
| **MH_DRW.W.1** | Minimum MH_DRW width is 0.3 um |
| **MH_DRW.W.2** | Maximum MH_DRW width is 1um |
| **MH_DRW.S.300** | Minimum MH_DRW spacing=0.300 micron |

### 7.4.15 M1 rules

| Mnemonic | Description |
|---|---|
| **M1.W.300** | Minimum M1 width=0.300 micron |
| **M1.maxW.50um** | Maximum M1 width=50.0um |
| **M1.S.1** | Minimum M1 spacing = 0.300 um for spacing <= 1.7 um |

| | |
|---|---|
| **M1.S.2** | Minimum M1 spacing = 0.5um for 1.7 < M1 width < 5 um |
| **M1.S.3** | Minimum M1 spacing = 1.1um for 5 um <= M1 width and < 10 um |
| **M1.S.4** | Minimum M1 spacing = 2.0 um for 10 um <= M1 width |
| **M1.SHARPANGLE** | Angle < 85 degrees |
| **PCON.I.M1** | PCON not allowed outside of M1 |
| **M1.E.PCON** | Minimum enclosure of PCON by M1 of 0.080 um |
| **WARNING.MH.O.M1** | MH_DRW should be connected to M1 |

### 7.4.16 VIA12 rules

| Mnemonic | Description |
|---|---|
| **VIA12.outdim** | Vias are squares with a 0.600 um side |
| **VIA12.spacing** | Minimum space between two vias is 0.600 um |
| **VIA12.I.M1** | VIA12 must be inside M1 |
| **M1.E.VIA12** | M1 must enclose VIA12 with a minimum margin of 0.14 um |

### 7.4.17 M2 rules

| Mnemonic | Description |
|---|---|
| **M2.W.900** | Minimum M2 width=0.900 micron |
| **M2.maxW.50um** | Maximum M2 width=50.0um |
| **M2.S.1** | Minimum M2 spacing = 0.900 um |
| **M2.SHARPANGLE** | Angle < 85 degrees |
| **VIA12.I.M2** | M2 must lie over VIA12 |
| **M2.E.VIA12** | M2 must enclose VIA12 with a minimum margin of 0.14 um |

### 7.4.18 PASS1 rules

| Mnemonic | Description |
|---|---|
| **PASS1.W.1** | Minimum PASS1 width = 5.0um |
| **PASS1.S.1** | Minimum PASS1 spacing = 5.0um |
| **PASS1.O.M2** | PASS1 must lie over M2_DRW |
| **M2.E.PASS1** | Minimum enclosure of PASS1 by M2_DRW is 2.5 um |
| **PASS1.O.M2** | M2 must be solid under PASS1 with a 2.5um margin |

### 7.4.19 METPASS rules

| Mnemonic | Description |
|---|---|

| | |
|---|---|
| **METPASS.W.1** | Minimum METPASS width = 11.0um |
| **METPASS.S.1** | Minimum METPASS spacing = 20.0um |
| **METPASS.O.PASS1** | PASS1 must be covered by METPASS |
| **METPASS.O.PASS2** | PASS2 must be covered by METPASS |
| **METPASS.E.PASS1** | Minimum enclosure of PASS1 by METPASS is 2.5 um |

### 7.4.20 EXPO rules

| Mnemonic | Description |
|---|---|
| **EXPO.W.2** | Minimum EXPO width = 2.0 micron |
| **EXPO.S.2** | Minimum EXPO spacing = 2.0 micron |
| **EXPO.SHARPANGLE** | Angle < 85 degrees |
| **EXPO.I.FCW** | EXPO must be on top of poly (FCW) |
| **FCW.E.EXPO** | Minimum enclosure of EXPO by FCW of 0.2 um |
| **EXPO.IO.SAL** | Illegal overlap EXPO and SAL, margin 5um |
| **EXPO.IO.PCON** | Illegal overlap EXPO and PCON, margin 5um |
| **EXPO.IO.MH** | Illegal overlap EXPO and MH_DRW, margin 5um |
| **EXPO.IO.M1** | Illegal overlap EXPO and M1, margin 5um |
| **EXPO.IO.VIA12** | Illegal overlap EXPO and VIA12, margin 5um |
| **EXPO.IO.M2** | Illegal overlap EXPO and M2, margin 5um |
| **EXPO.IO.METPASS** | Illegal overlap EXPO and METPASS, margin 30um |

### 7.4.21 LPASS rules

| Mnemonic | Description |
|---|---|
| **LPASS.W.5** | Minimum LPASS width = 5.0 micron |
| **LPASS.S.5** | Minimum LPASS spacing = 5.0 micron |
| **LPASS.SHARPANGLE** | Angle < 85 degrees |
| **LPASS.IO.SAL** | Illegal overlap LPASS and SAL, margin 5um |
| **LPASS.IO.PCON** | Illegal overlap LPASS and PCON, margin 5um |
| **LPASS.IO.MH** | Illegal overlap LPASS and MH_DRW, margin 5um |
| **LPASS.IO.M1** | Illegal overlap LPASS and M1, margin 5um |
| **LPASS.IO.VIA12** | Illegal overlap LPASS and VIA12, margin 5um |
| **LPASS.IO.M2** | Illegal overlap LPASS and M2, margin 5um |
| **LPASS.IO.METPASS** | Illegal overlap LPASS and METPASS, margin 30um |
| **LPASS.IO.EXPO** | Illegal overlap LPASS and EXPO, margin 20um |

### 7.4.22 PASS2 rules

| Mnemonic | Description |
|---|---|
| **PASS2.W.1** | Minimum PASS2 width = 5.0um |
| **PASS2.S.1** | Minimum PASS2 spacing = 5.0um |
| **PASS2.O.PASS1** | PASS2 must lie over PASS1 |
| **PASS2.NOHOLE** | PASS2 should not have any hole |
| **METPASS.E.PASS2** | Minimum enclosure of PASS2 by METPASS is 2.5 um |

| | |
|---|---|
| **PASS2.IO.LPASS** | No overlap allowed between PASS2 and LPASS, with a 5um margin |
| **PASS2.IO.EXPO** | No overlap allowed between PASS2 and EXPO, with a 5um margin |

### 7.4.23 TRENCH rules

| Mnemonic | Description |
|---|---|
| **TRENCH.O.EXPO** | TRENCH must be inside EXPO |
| **TRENCH.EXPO.W1** | EXPO W1 must be >= 150um |
| **TRENCH.EXPO.W2** | EXPO area around trench has a minimal external distance of 25um |
| **TRENCH.EXPO.W3** | EXPO area around trench has a minimal internal distance of 30um |
| **TRENCH.W4** | WG_COR to TRENCH must be >= 3um |
| **TRENCH.EXPO.W5** | Minimum enclosure of TRENCH by EXPO is 15.0 um |
| **TRENCH.W.150** | TRENCH is made of rectangles of 150um width and >= 330 um long |
| **TRENCH.EXPO.W7** | Minimum distance between 2 EXPO polygons enclosing a trench is 100um |
| **TRENCH.E.EXPO.2** | Only one TRENCH enclosed per EXPO polygon |
| **TRENCH.IO.SOI** | No overlap allowed between Si (body and poly) patterning and TRENCH with a margin of 1um |
| **WG_CLD.E.TRENCH** | Minimum enclosure of TRENCH by WG_CLD is 1um |

### 7.4.24 OPT_DUM

| Mnemonic | Description |
|---|---|
| **OPT_DUM.outdim** | Optical layers dummy place holders are squares with a 2.800 um side |
| **OPT_DUM.spacing** | Minimum space between two dummy place holders is exactly 0.200um or >= 0.400um |
| **OPT_DUM.IO.WG** | No overlap between OPT_DUM and WG, margin 0.2um |
| **OPT_DUM.IO.FC** | No overlap between OPT_DUM and FC, margin 0.2um |
| **OPT_DUM.IO.SKT** | No overlap between OPT_DUM and SKT, margin 0.2um |
| **OPT_DUM.IO.FCW** | No overlap between OPT_DUM and FCW, margin 0.2um |
| **OPT_DUM.IO.SAL** | No overlap between OPT_DUM and SAL, margin 0.2um |
| **OPT_DUM.IO.PCON** | No overlap between OPT_DUM and PCON, margin 0.2um |
| **OPT_DUM.IO.EXPO** | No overlap between OPT_DUM and EXPO, margin 0.5um |

| | |
|---|---|
| **OPT_DUM.IO.LPASS** | No overlap between OPT_DUM and LPASS, margin 2um |
| **OPT_DUM.IO.TRENCH** | No overlap between OPT_DUM and TRENCH, margin 0.5um |

### 7.4.25 LOGOTXT rules

| Mnemonic | Description |
|---|---|
| **LOGOTXT.IO.WG** | Illegal overlap between LOGOTXT and WG_ layers |
| **LOGOTXT.IO.FC** | Illegal overlap between LOGOTXT and FC_ layers |
| **LOGOTXT.IO.SKT** | Illegal overlap between LOGOTXT and SKT_ layers |
| **LOGOTXT.IO.FCW** | Illegal overlap between LOGOTXT and FCW_ layers |
| **LOGOTXT.IO.MH** | Illegal overlap between LOGOTXT and MH_DRW |
| **LOGOTXT.S.MH** | LOGOTXT minimum spacing to MH_DRW is 0.5 um |
| **LOGOTXT.IO.M1** | Illegal overlap between LOGOTXT and (M1_DRW not M1_PERF) layers |
| **LOGOTXT.S.M1** | LOGOTXT minimum spacing to M1 is 0.5 um |
| **LOGOTXT.IO.M2** | Illegal overlap between LOGOTXT and (M2_DRW not M2_PERF) layers |
| **LOGOTXT.S.M2** | LOGOTXT minimum spacing to M2 is 0.5 um |
| **LOGOTXT.IO.METPASS** | Illegal overlap between LOGOTXT and METPASS layers |
| **LOGOTXT.IO.EXPO** | Illegal overlap LOGOTXT and EXPO |
| **LOGOTXT.IO.LPASS** | Illegal overlap LPASS and LOGOTXT |

### 7.4.26 NOMET rules

| Mnemonic | Description |
|---|---|
| **NOMET.IO.PCON** | PCON not allowed in NOMET |
| **NOMET.IO.MH** | MH_DRW not allowed in NOMET |
| **NOMET.IO.M1** | M1 not allowed in NOMET |
| **NOMET.IO.VIA12** | VIA12 not allowed in NOMET |
| **NOMET.IO.M2** | M2 not allowed in NOMET |
| **NOMET.IO.METPASS** | METPASS not allowed in NOMET |

### 7.4.27 NOFILL rules

| Mnemonic | Description |
|---|---|
| **NOFILL.IO.OPT_DUM** | OPT_DUM not allowed in NOFILL |

### 7.4.28 DICING rules

| Mnemonic | Description |
|---|---|

| | |
|---|---|
| **WARNING.DICING.IO.SOI** | SOI pattern in DICING line |
| **DICING.IO.METALS** | Illegal overlap between DICING and metals pattern layers |

### 7.4.29 IP rules

| Mnemonic | Description |
|---|---|
| **IP.IO.WG** | No overlap between IP and WG |
| **IP.IO.FC** | No overlap between IP and FC |
| **IP.IO.SKT** | No overlap between IP and SKT |
| **IP.IO.FCW** | No overlap between IP and FCW |
| **IP.IO.OPT_DUM** | No overlap between IP and OPT_DUM, margin 0.2um |

### 7.4.30 PAYLOAD rules

| Mnemonic | Description |
|---|---|
| **data.in.PAYLOAD** | All the data must be drawn inside PAYLOAD_DRW |

## 7.5 Density rules

For process control reasons, the density of structures needs to adhere to the rules outlined below. This is after dummy filling (see 5.3.2). Both the dummy filling and density check will be done by imec, not by the user. However, the user needs to ensure that no structures are intrinsically violating these rules, for instance large continues areas of SOI drawn on the WG layer.

Please note that today no rule is implemented in the deck for checking the density on the layout. Users should take care to respect the density rules themselves.

| Layer | Rule | Value |
|---|---|---|
| **WG.DENSITY.GLOBAL** | Average density on full mask (density of fully etched areas) | 36-44% |
| **WG.DENSITY.LOCAL** | Average density within any 500umx500um window, with 250um overlap step size (density of fully etched areas) | 10-70% |
| **FCW.DENSITY.GLOBAL** | Average density on full mask | 15-25% |
| **FCW.DENSITY.LOCAL** | Average density within any 500umx500um window, with 250um overlap step size | 10-40% |
| **M1.DENSITY.GLOBAL** | Average density on full mask | >15% |
| **M1.DENSITY.LOCAL** | Average density within any 50umx50um window, with 10um overlap step size | 15-85% |
| **M2.DENSITY.GLOBAL** | Average density on full mask | >15% |
| **M2.DENSITY.LOCAL** | Average density within any 50umx50um window, with 10um overlap step size | 15-85% |

*Table 2: Density rules.*

## 7.6 Other advices, not encoded in the DRC deck

### 7.6.1 Contacts layout

When adding contacts to a device we recommend to use 2 sets of 2 rows of contacts separated by > 3.75um. Increasing the number of rows or decreasing the distance is likely to cause leakage current.