AN14354

Multimode Bidirectional AC-DC Converter Design using MC56F83783

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Document information

Information	Content
Keywords	AN14354, MC56F83783, AC-DC converter, totem-pole PFC, standalone inverter, grid-connected inverter, LCL
Abstract	This document presents the design of a multimode bidirectional AC-DC converter using the 32-bit NXP microcontroller MC56F83783.

1 Overview

This document presents the design of a multimode bidirectional AC-DC converter using the 32-bit NXP microcontroller MC56F83783. The DC-to-AC mode can be either the grid-connected mode or the standalone mode, with seamless mode switching between the two modes.

1.1 Introduction

Bidirectional AC-DC converters are used in applications where bidirectional power flow is required, such as energy storage systems and bidirectional onboard charger (OBC). In the DC-to-AC mode, the converter can operate in either the grid-connected mode or the standalone mode. The converter switches smoothly between the two modes as required in many application scenarios.

Figure 1 shows the simplified block diagram for the multimode bidirectional AC-DC converter design. In the PFC mode, a totem-pole power factor correction (PFC) circuit controls the power flow from the AC side to the DC bus. In the inverter mode, a 2-level H-bridge inverter controls the reverse active power transfer from the DC bus to the AC side. An inductor-capacitor-inductor (LCL) filter is used to achieve the desired filtering effect with a minimum filter volume. It contains a grid-side inductor L_g, a filter capacitor C_f, and a converter-side inductor L_r.

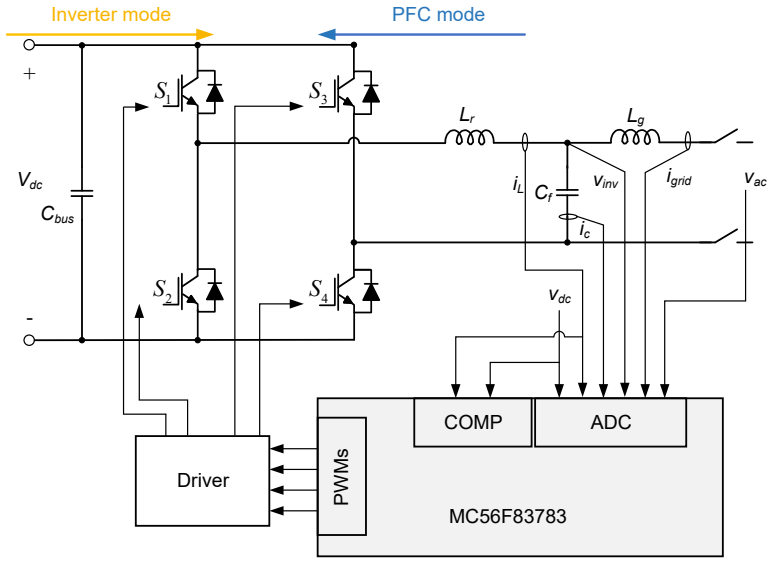

Figure 1. Simplified block diagram

1.2 Application features and components

The system is designed to drive a multimode bidirectional AC-DC converter. The key features of the system are as follows:

- A bridgeless totem-pole PFC circuit controls power flow from AC side to DC side.
- A 2-level H-bridge inverter controls power flow from DC side to AC side. It can operate in either grid-connected mode or standalone mode.
- Seamless transition between the PFC mode and the inverter mode
- Seamless transition between the grid-connected and standalone inverter modes without a voltage/current surge
- 85 V_{rms} to 265 V_{rms} AC voltage range in the PFC mode
- Typical 380 V DC voltage
- 800 W rated power at 220 V_{ac} and 400 W rated power at 110 V_{ac} in either direction

- 20 kHz switching frequency
- Remote Serial Communication Interface (SCI) control through FreeMASTER

The following are the main application components available for users:

- Software: The software is written in C code using some library algorithms from NXP real-time control embedded software libraries (RTCESL). The project is developed in CodeWarrior for Microcontrollers v11.1 and MCUXpresso Config Tools v13.1.
- Hardware: The hardware includes a dedicated main power board and NXP HVP-56F83783 controller card.
- Documentation: Apart from this document, the documents listed in Section 6 are available.

1.3 NXP DSC advantages and features

The NXP MC56F837xx digital signal controllers (DSCs) are well suited for digital power conversion and motor control applications. They combine the features of microcontroller units (MCUs) and digital signal processors (DSPs) on a single chip. The DSCs offer dedicated peripherals to facilitate application design.

The MC56F83783 DSC contains the following blocks:

- The core operates at frequencies of up to 100 MHz
- Up to two 128 KB dual-partition flash memories with error correcting code (ECC) protection and partition swap function
- Up to 64 KB data / program RAM
- Both on-chip flash memory and RAM can be mapped into both program and data memory spaces
- The 32 KB boot ROM supports boot from SCI, I2C, and controller area network (CAN)
- Two high-resolution eFlexPWM modules, each with up to eight PWM outputs of 312 ps resolution
- 2x4 16-bit timers
- Two high-speed 12-bit ADCs with 16 external channels
- Four analog comparators with integrated 8-bit DAC references
- Two 12-bit DACs with automatic waveform generation function
- EVTG and crossbar for flexible signal routing
- Two SCI modules with Local Interconnect Network (LIN) slave functionality
- One SPI module
- Two I2C / System Management Bus (SMBus) ports
- One FlexCAN module with CAN flexible data rate (FD) support

2 System description

This section contains the following subsections:

- Section 2.1 "Block diagram"
- Section 2.2 "PFC mode"
- Section 2.3 "Inverter mode"

2.1 Block diagram

Figure 2 shows the block diagram of the implementation of the multimode bidirectional AC-DC converter.

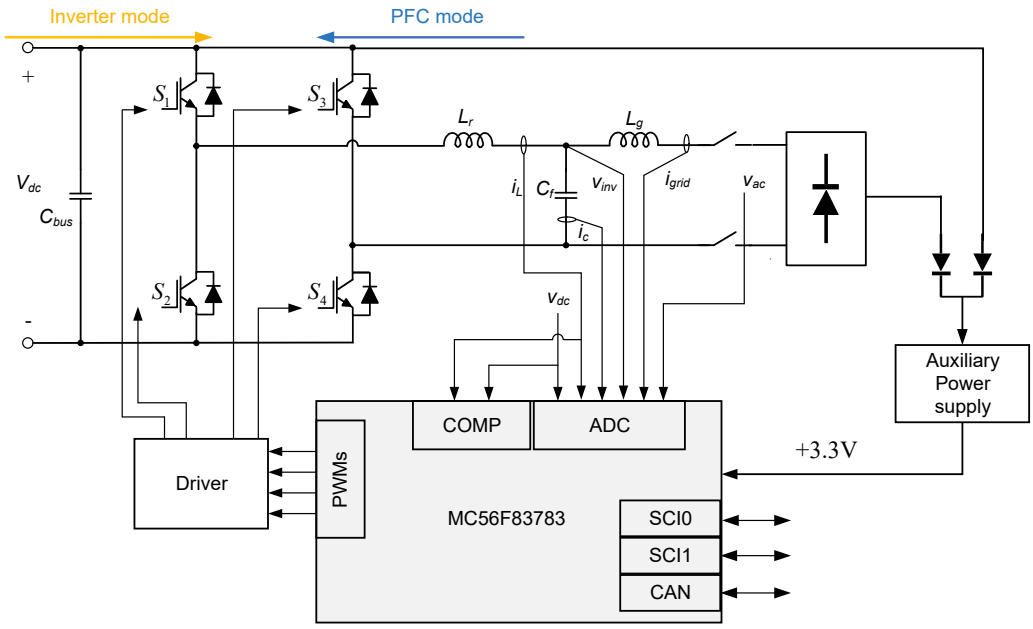

Figure 2. System block diagram

The block diagram contains:

- A full bridge constructed with four insulated-gate bipolar transistor (IGBT) switches
- An inductor-capacitor-inductor (LCL) filter for the high-frequency harmonics. The LCL filter helps achieve the desired filter effect with minimum filter volume.

The auxiliary power supply takes power from the AC or DC side, depending on whose voltage is higher. Then, it generates the desired voltages with a flyback converter and a low dropout (LDO) regulator.

The MC56F83783 DSC acts as the brain of the application as it receives the feedback signals, executes the control algorithm, and then outputs the drive signals. To handle the control of the system in all modes, the following voltage and current components must be sampled:

- DC bus voltage v_{dc}
- Inverter output voltage v_{inv}
- Grid voltage v_{grid}
- Grid-side current i_{grid}
- Inductor current i_L

The capacitor current i_c is used to dampen LCL resonance spike. It can also be obtained through i_{grid} and i_L.

The DSC is also used to communicate with other equipments and boards:

- One Universal Asynchronous Receiver / Transmitter (UART) port is used to communicate with the backward DC-DC stage.
- One UART-to-USB bridge using another UART port is employed to communicate with the host computer for FreeMASTER or firmware updating.
- One CAN port is reserved for parallel operation communication.

2.2 PFC mode

This section contains the following subsections:

2.2.1 Modulation scheme

In the PFC mode, a totem-pole PFC converter controls the power flow from the AC side to the DC bus. As compared to a traditional boost PFC converter, a totem-pole PFC converter requires fewer power switches to reduce the power loss in the conduction path. A totem-pole PFC converter contains:

- A pair of fast switches (S1 and S2) operating at PWM frequency
- A pair of slow switches (S3 and S4) operating at power frequency

In a low frequency band, an LCL filter produces the same frequency response as a single L filter with the same inductance does. In addition, the PFC fundamental frequency is lower than the LCL resonant frequency. Therefore, a totem-pole PFC converter based on an LCL filter works similar to a single inductor filter. To track the AC voltage waveform, the current flow at different points is shown in Figure 3.

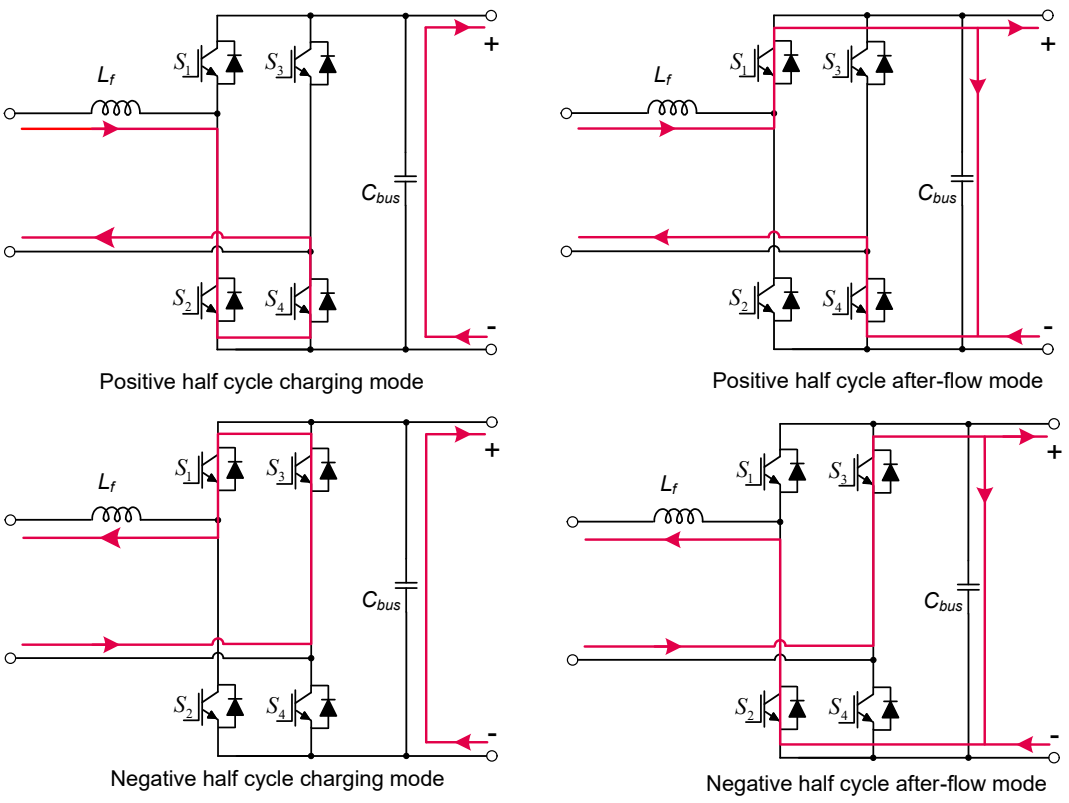

Figure 3. Totem-pole PFC converter working principle

The current flow is explained below:

- In the positive half cycle of the AC voltage:
  - S2 acts as the master switch to increase the current of the boost inductor. Its duty cycle determines the boost ratio.
  - S1 works complementarily to S2, allowing the energy to flow to the DC output.

– During this period, S4 is always ON and S3 is always OFF.
- In the negative half cycle of the AC voltage:
  – S1 acts as the master switch to increase the current of the boost inductor. Its duty cycle determines the boost ratio.
  – S2 works complementarily to S1, allowing the energy to flow to the DC output.
  – During this period, S3 is always ON and S4 is always OFF.

2.2.2 Control scheme

A totem-pole PFC converter adopts dual loop control, as shown in Figure 4.

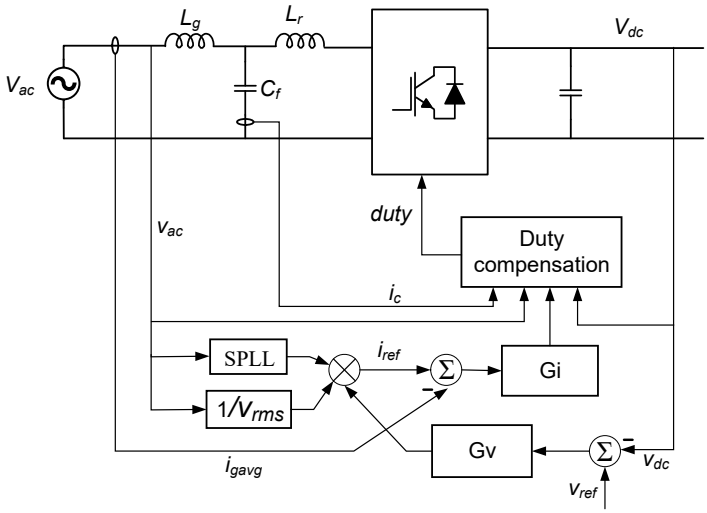

Figure 4. Totem-pole PFC converter control scheme

The sensed DC bus voltage v_{dc} is compared against the reference bus voltage v_{ref}. To regulate the bus voltage at the reference level, the error is supplied as an input to the voltage regulator *Gv*. To eliminate the influence of the input voltage fluctuation, the AC input root mean square (RMS) voltage v_{rms} compensates the current reference. A software PLL algorithm is used to compute the angle and phase of the grid. To generate the current reference i_{ref}, the PLL output is multiplied with the voltage regulator output and the inverse of v_{rms}. To control the shape of the current, the current reference is compared against the sensed average grid-side current i_{gavg}. The error is supplied as input to the current regulator *Gi*.

To improve the performance of the system under all working conditions and to enhance the system stability, dedicated duty cycle ratio compensators are added.

2.2.2.1 Voltage feedforward duty compensation for different converter dynamics

Depending on whether the inductor current is continuous or not, a PFC converter can operate in one of the following modes:

- Continuous current mode (CCM)
- Critical current mode (CRM)
- Discontinuous current mode (DCM)

The totem-pole PFC converter in the current design operates mostly in the CCM mode. However, it operates in the DCM mode near the zero crossing of the input voltage, especially at light loads. The change in the converter dynamics leads to input current distortion. Because the converter dynamics change abruptly between CCM and DCM, the following problems occur when the same DSC controller is used for both modes:

- Poor inductor current tracking
- Significant input current distortion

One method to suppress current distortion without increasing the complexity of the controller design is to add the duty cycle ratio feedforward. In this method, the ideal value of the duty cycle ratio is calculated and is added to the output of the current controller to generate the final duty cycle ratio. As a result, the current controller only compensates small values of input current error and a high gain loop is not required. A PI controller designed for converter in the CCM mode can be used for the entire operation with low current distortion.

In the CCM mode, the ideal value of the duty cycle ratio d_{CCM} can be derived as follows:

$$d_{CCM} = 1 - \frac{v_{ac}}{v_{dc}} \tag{1}$$

where v_{ac} is the sampled input voltage.

In the DCM mode, the input current is directly related to the duty cycle. The average current in the DCM mode is:

$$i_{gavg} = \frac{1}{2} * \frac{v_{ac} d_{DCM} T_s}{L} * \frac{v_{dc} d_{DCM}}{v_{dc} - v_{ac}} \tag{2}$$

According to the control scheme, the required average current i_{ref} is:

$$i_{ref} = \frac{v_{pi\_out} v_{ac}}{v_{rms}^2} \tag{3}$$

where v_{pi_out} is the output of the voltage regulator.

Based on Equation (1), Equation (2), and Equation (3), the ideal DCM duty cycle ratio can be calculated as given in Equation (4), assuming that the ideal current waveform $i_{lavg} = i_{ref}$:

$$d_{DCM} = \sqrt{\frac{2L}{T_s} \frac{v_{pi\_out}}{v_{rms}^2} d_{CCM}} \tag{4}$$

The two calculated ideal duty cycle ratios, d_{CCM} and d_{DCM}, are equal when the converter operates in the CRM mode.

When the converter operates in the CCM mode, the calculated d_{DCM} value is bigger than the d_{CCM} value. On the other hand, in the DCM mode, the calculated d_{DCM} value is smaller than the d_{CCM} value. Therefore, the required feedforward value of the duty cycle ratio for operation in the mixed mode is a combination of d_{CCM} and d_{DCM}. The correct value is obtained by taking the smaller value of the two duty cycle ratios.

2.2.2.2 Capacitor current feedback for LCL resonance suppression

Figure 5 shows the current loop control block diagram of an LCL-based rectifier with no duty cycle compensation, where:

- i_g is the grid-side current to be controlled.
- Gi represents the current regulator.
- v_{ac} is the input AC voltage.
- v_i is the bridge-side input voltage.
- v_r is the output of the current regulator.

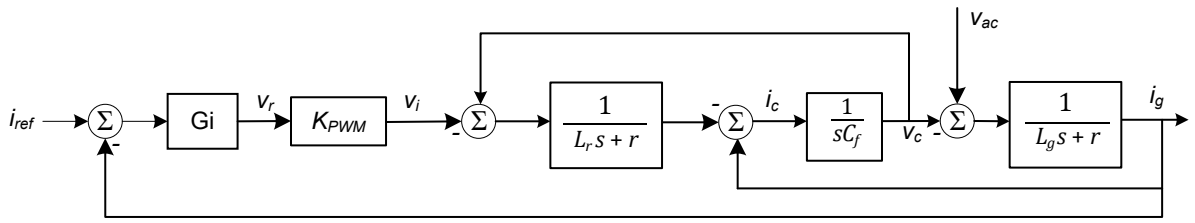

Figure 5. Undamped current control loop

Ignoring the internal resistance of the filter inductor, the transfer function between i_g and v_r is given below:

$$\frac{i_g(s)}{v_r(s)} = \frac{K_{PWM}}{L_g L_r C_f s^3 + (L_g + L_r)s} \tag{5}$$

Assuming that $\omega_{res} = \sqrt{(L_g + L_r) / L_g L_r C_f}$, the transfer function can be changed into:

$$\frac{i_g(s)}{v_r(s)} = \frac{K_{PWM}}{L_g + L_r} \frac{\omega_{res}}{s(s^2 + \omega_{res}^2)} \tag{6}$$

It is a third-order system contained within the current loop. It resonates when the angular frequency is equal to ω_{res}. If not designed and controlled properly, it may harm the stability of the system.

To eliminate the resonance, the most direct way is to add some resistors in the filter. However, power loss on the resistor leads to reduced system efficiency. The filter capacitor current feedback control is added as the active damping in this design. It is physically equivalent to the passive damping control of the capacitor in parallel with a resistor, ignoring the control delay. The current loop control block diagram with filter capacitor current feedback is shown in Figure 6.

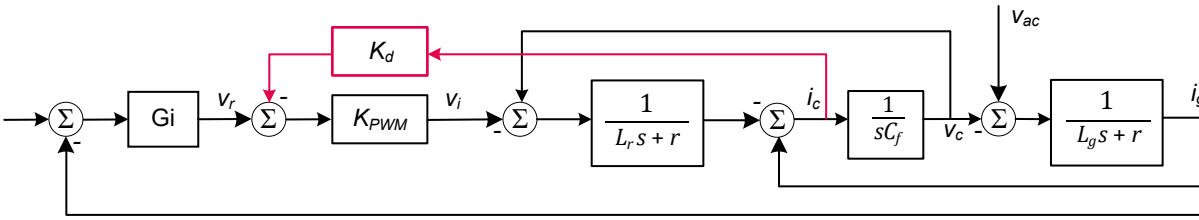

Figure 6. Capacitor current feedback active damping current control loop

As shown in Figure 6, the transfer function between i_g and i_c can be derived as:

$$\frac{i_c(s)}{i_g(s)} = -L_g C_f s^2 \tag{7}$$

When using capacitor current feedback, the transfer function between i_g and v_r based on Equation (5) and Equation (7) can be calculated as given below:

$$\frac{i_g(s)}{v_r(s)} = \frac{K_{PWM}}{L_g L_r C_f s^3 + K_{PWM} K_d L_g C_f s^2 + (L_g + L_r)s} \tag{8}$$

An s^2 term is introduced in the denominator, which can damp the resonance spike by properly adjusting the K_d value.

Figure 7 shows the bode plots of the transfer function between i_g and v_r for different K_d values.

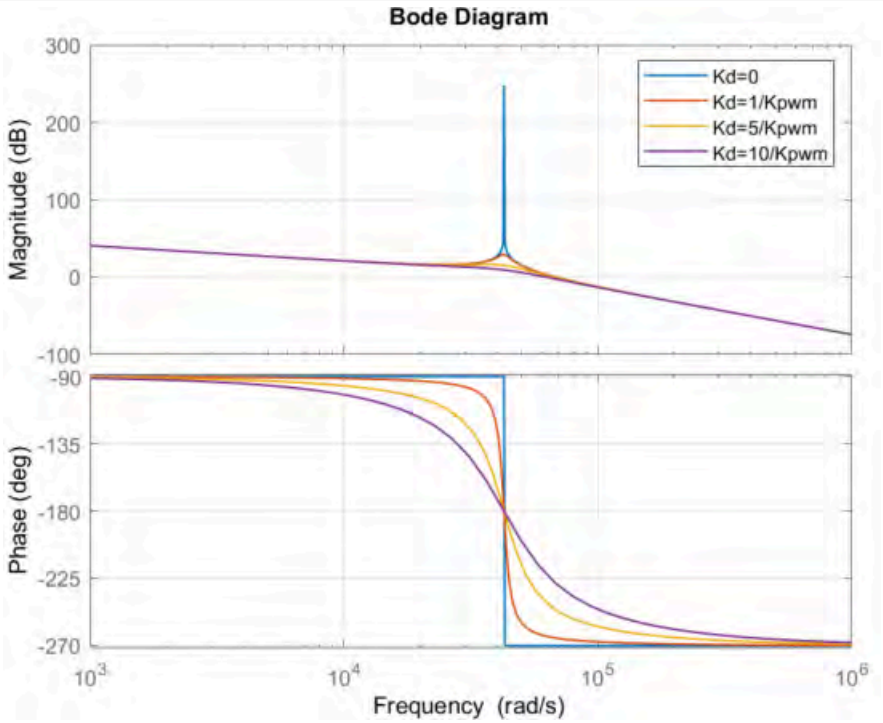

Figure 7. Bode plots for different K_d values

By adding the filter capacitor current feedback, the resonance spike is effectively suppressed with little impact on other frequencies. With an increase in the K_d value, the resonance peak suppression becomes more obvious. However, this change also has an impact on the phase-frequency response.

For the current design, the K_d value is calculated as $K_d = 5 / K_{PWM}$. This value is selected considering both the amplitude and phase effects and ensuring the stability of the closed loop system.

2.2.3 Precharging strategy

Generally, the PFC converter requires huge filter capacitance to reduce the DC bus voltage ripple. However, the filter capacitor is first charged from the AC input through the diodes of the IGBT bridge. To avoid the charging current becoming too high, implement a proper method to limit the current.

The current limiting resistors and relays are commonly used in the PFC converters, as shown in Figure 8. Unfortunately, the contact resistors of the relays and the current limiting resistors degrade the efficiency and power density of the converter.

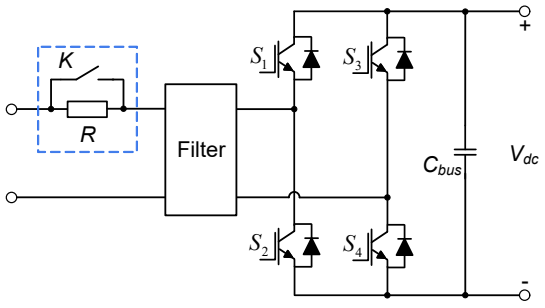

Figure 8. Precharging with a current limiting resistor

In this multimode bidirectional AC-DC converter, controllable switches are present between the grid and the converter as grid-connected switches. In the PFC mode, the progressive phase control of the TRIACs (see Figure 9) can also serve the purpose of limiting the current in the precharging stage. Therefore, relay and resistor are not needed anymore.

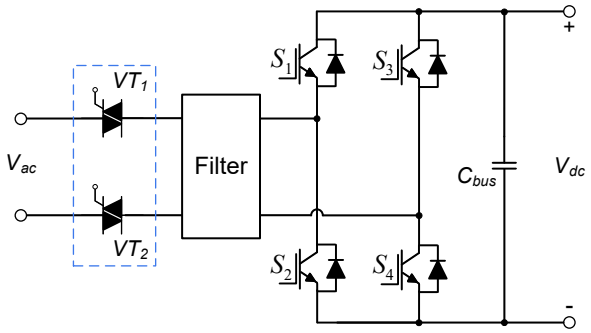

Figure 9. Precharging with TRIACs

If a TRIAC is OFF, it remains OFF until it gets a trigger signal. If the TRIAC is ON, it remains ON until the current through it reduces to zero, even though no trigger signal is present. Based on the characteristics of a TRIAC, the bus capacitor can be charged in stages by controlling the conduction phase of the TRIAC. Therefore, the charging current can be limited in the allowable range.

As shown in Figure 10, the TRIAC is only triggered in the second quarter of a positive half cycle of the grid voltage V_{ac}.

In the first grid voltage cycle, the TRIAC is turned on when the grid voltage is relatively low. Therefore, the charging current is relatively small. When the current reduces to zero, the bus voltage V_{dc} is charged from the instantaneous value of V_{ac}. This value is a little smaller than the V_{ac} when the TRIAC is turned on.

In the next grid voltage cycle, the new TRIAC trigger point is obtained by adding a fixed voltage step to the V_{ac}, where the TRIAC is turned on in the previous grid cycle. Therefore, the V_{dc} is charged to a higher level. By increasing V_{ac} cycle-by-cycle at which the trigger point is, you charge the bus capacitor step-by-step to near the peak value of V_{ac}, with allowable charging current. After the precharging is done, V_{driver} is high constantly.

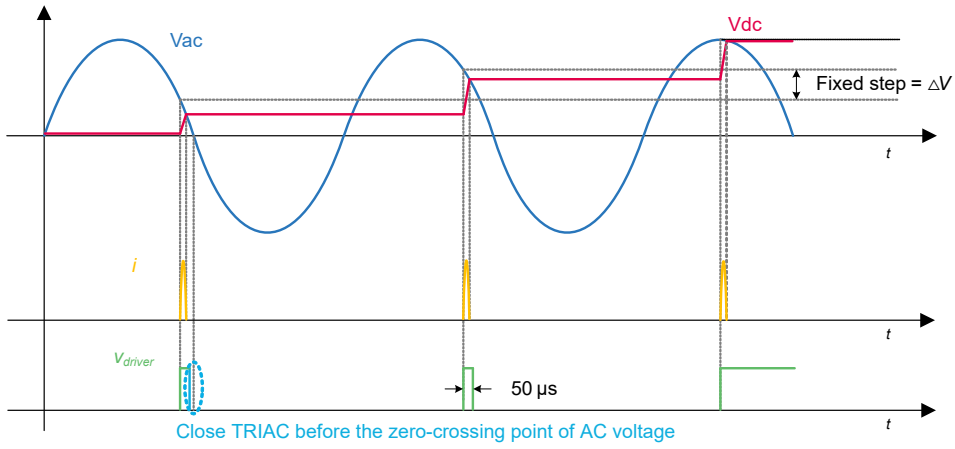

Figure 10. Precharging strategy with TRIACs

Because the voltage step is fixed in the previously mentioned process, the peak value of the charging current is almost the same in the precharging process. Therefore, the bus capacitor can be charged with the maximum allowed current with this strategy, which helps speed up the precharging process.

2.2.4 Working mode

To improve the efficiency and current quality at light loads, the burst mode is implemented in this design. As shown in Figure 11, when the light load condition is detected, the PWM drive signals are blocked periodically according to the output voltage peak-valley detection. When PWM is ON in the burst mode, the constant reference current is used. As the load increases, the converter switches back to the normal mode smoothly.

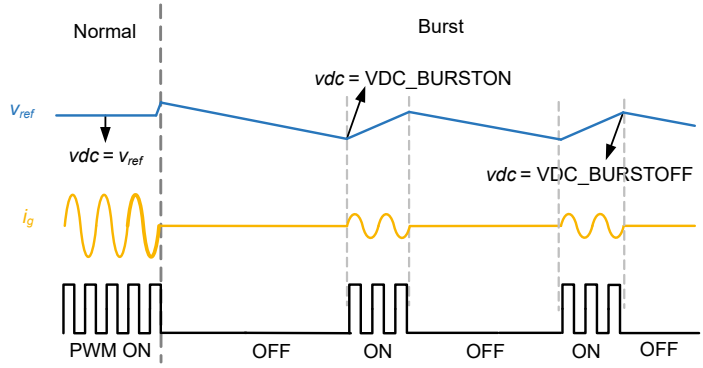

Figure 11. Illustration of different working modes

2.3 Inverter mode

This section contains the following subsections:

- Section 2.3.1 "Modulation scheme"
- Section 2.3.2 "Control scheme"
- Section 2.3.3 "Presynchronization of inverter output and grid voltage"

2.3.1 Modulation scheme

Unipolar sinusoidal pulse width modulation (SPWM) is used when working in the inverter mode. Figure 12 shows the basic working principle of the unipolar modulation, where u_m is the modulation wave and u_c is the carrier.

By comparing the amplitudes of u_m and u_c, the driver signals u_{g1} and u_{g2} are generated for the high-frequency bridge composed of *S1* and *S2*. u_{g3} and u_{g4} are the driver signals for the low-frequency bridge composed of *S3* and *S4* working at line frequency. Due to the flexible PWM module, the SPWM driver signals can be generated easily on the DSC.

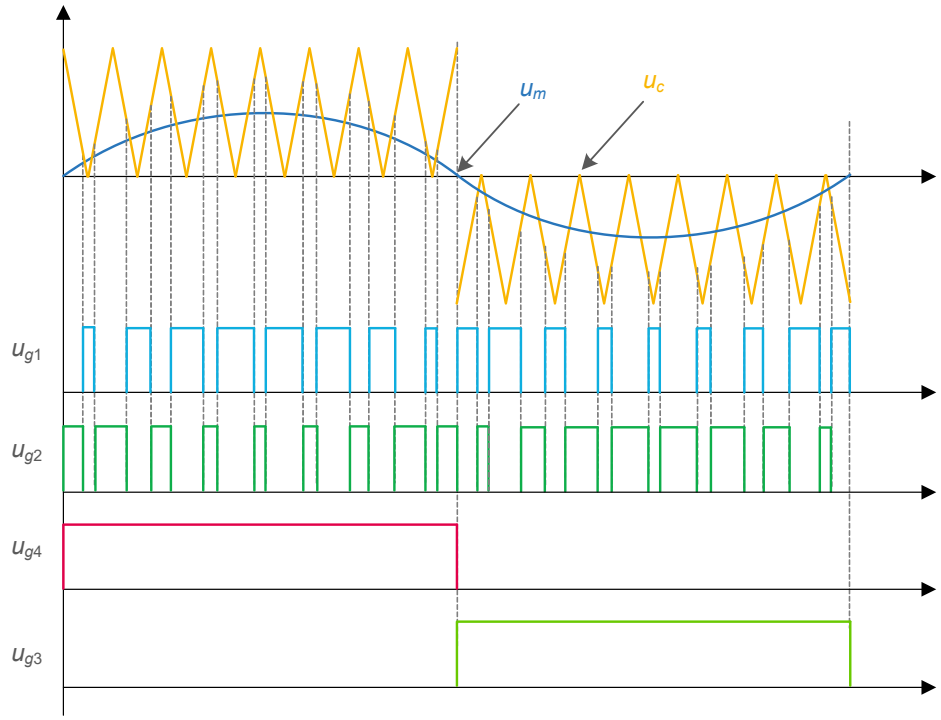

Figure 12. Basic working principle of unipolar modulation

The basic operating mode of the converter is the same in different inverter modes, as shown in Figure 13.

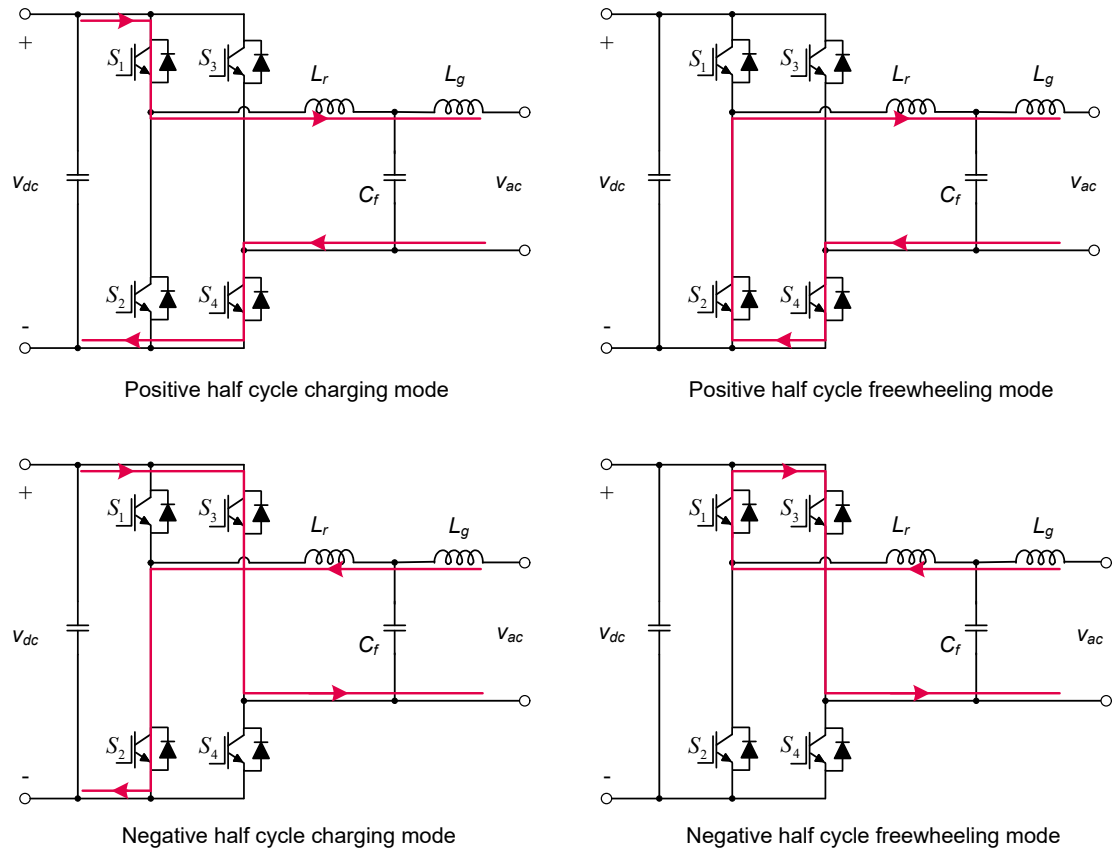

Figure 13. Operating modes at inverter mode

2.3.2 Control scheme

In this design, the inverter can operate in either the grid-connected mode or the standalone mode with seamless transition control. Different control strategies are used for different modes:

- In the grid-connected mode, the inverter works as a current source because the grid governs the voltage. Therefore, grid current is controlled in this mode.
- In the standalone mode, the inverter works as a voltage source. Therefore, the filter capacitor voltage is controlled in this mode.

The subsections that follow describe the two inverter modes in detail.

2.3.2.1 Standalone mode

Figure 14 shows the control scheme when operating in the standalone inverter mode. A dual-loop control strategy of voltage outer loop and current inner loop is adopted in this mode.

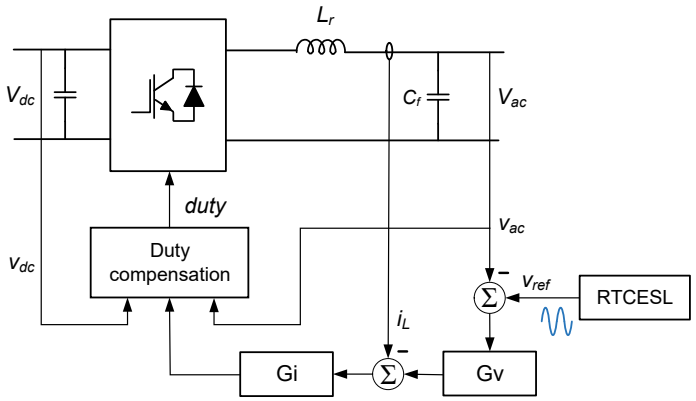

Figure 14. Standalone inverter control scheme

First, the sinusoidal reference voltage is generated by calling the NXP RTCESL library function. The error between the reference voltage and the sensed inverter output is input to the voltage compensator *Gv* to achieve error-free control. The output of the voltage compensator is used as a reference for the inner current loop in which a current compensator G_i is used. In addition, the output voltage feedforward compensation is added to decouple the inner current loop and the outer voltage loop. It facilitates the design of the inner current loop controller and improves the output dynamic performance further.

Figure 15 shows the bode plots for both the proportional integral (PI) and proportional resonant (PR) regulators. With an increase in the frequency, the gain of the PI regulator decreases dramatically. Therefore, the PI regulator cannot be used to track the periodical signals without error. However, the PR regulator can provide a large gain at a specific frequency, which can be used to zeroize the error at the AC frequency. To ensure adaptability to the grid frequency, the quasi-PR regulator is used in the voltage outer loop.

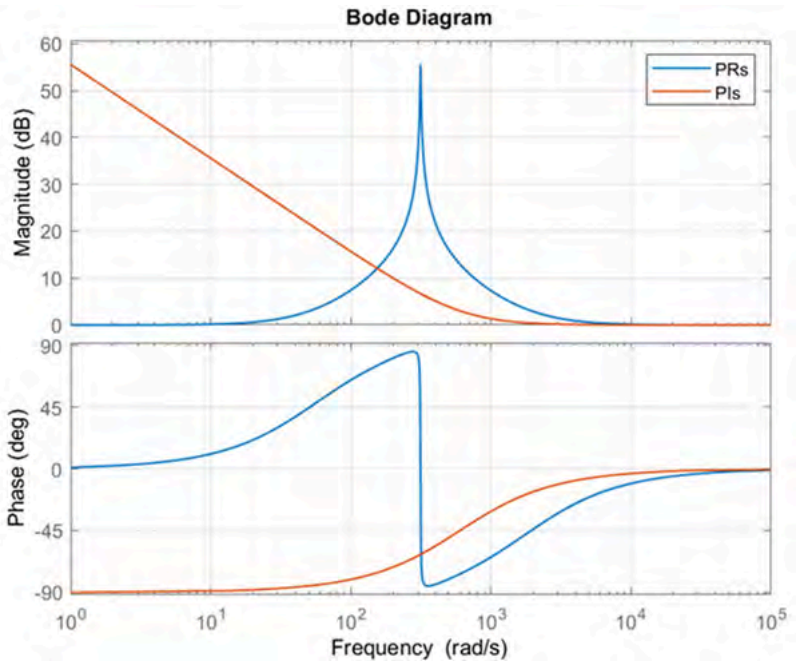

Figure 15. Bode plots of PI and PR regulators

In addition to the fundamental quasi-PR regulator (G_{PR_1st}), the harmonic compensators (G_{PR_3rd}, G_{PR_5th}, and G_{PR_7th}) are also added to eliminate the corresponding harmonics. The expression of the voltage compensator is given below:

$$G_v(s) = K_{P\_1H} + \sum_{n=1,3,5,7} \frac{2K_{R\_nH}\omega_c s}{s^2 + 2\omega_c s + \omega_{0\_nH}^2} \quad (9)$$

Figure 16 shows the detailed control block diagram in the standalone inverter mode. Because the filter capacitor voltage is selected as the inverter output to be controlled. Therefore, no LCL resonance problem occurs.

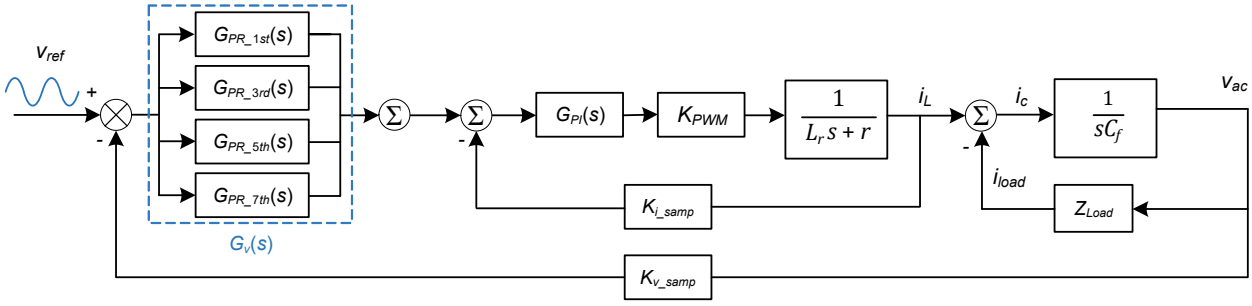

Figure 16. Control block diagram in standalone inverter mode

Figure 17 shows the simplified control block diagram to illustrate the harmonic compensation mechanism.

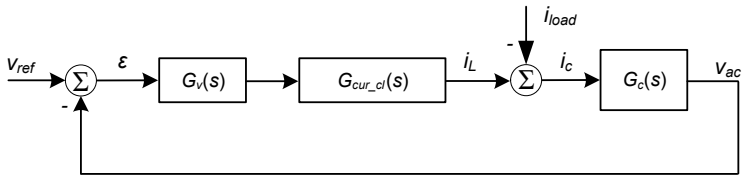

Figure 17. Simplified control block diagram

The $G_{cur\_cl}(s)$ represents the closed loop transfer function for the current loop. Load current i_{load} is considered a disturbance. Especially, when the inverter is loaded with a nonlinear load, i_{load} has many harmonics. The voltage error disturbance ratio rejection capability at null reference is defined as:

$$\left.\frac{\varepsilon(s)}{i_{load}(s)}\right|_{v_{ref}=0} = \frac{G_C(s)}{1 + G_C(s)*G_v(s)*G_{cur\_cl}(s)} \quad (10)$$

where ε is the voltage error and $G_C(s)$ is the transfer function of the filter capacitor.

The bode plot of the disturbance rejection transfer function is shown in Figure 18. By introducing the harmonic regulators, about 60 dB attenuation is achieved for the third, fifth, and seventh harmonics.

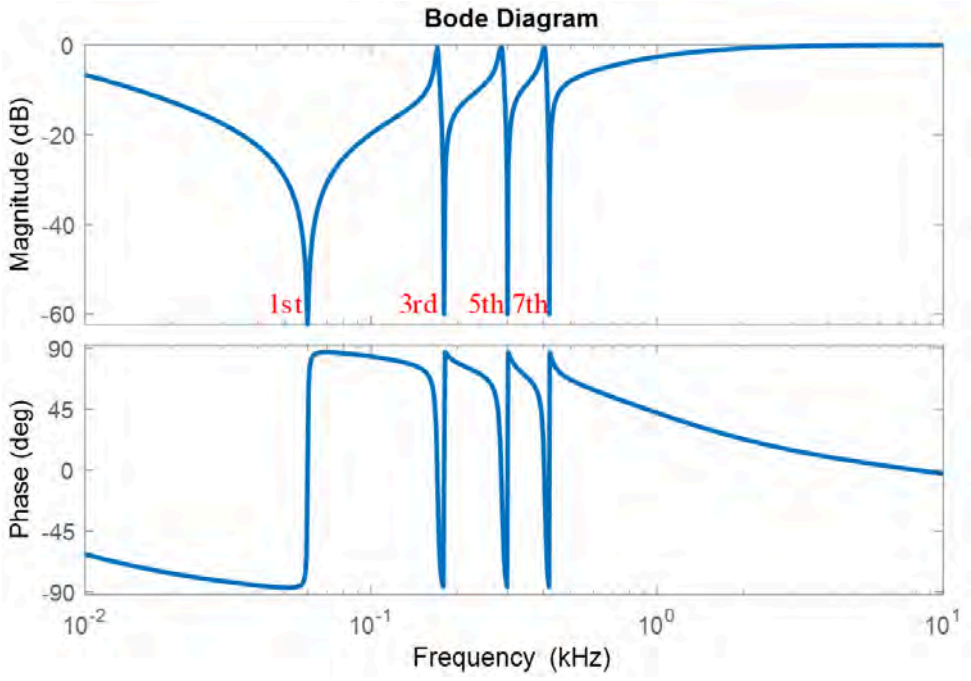

Figure 18. Bode plot of disturbance rejection

2.3.2.2 Grid-connected mode

Figure 19 shows the block diagram of the grid-connected inverter system, operating in the current-controlled mode.

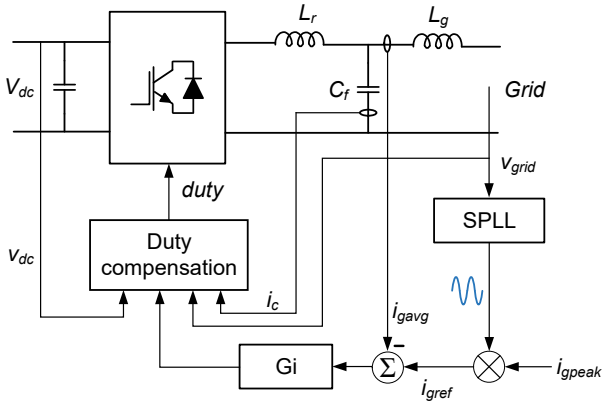

Figure 19. Grid-connected inverter control scheme

A software phase-locked loop (PLL) algorithm is used to calculate the phase of the grid. Then, the phase is multiplied with the peak current command i_{gpeak} to generate the current reference. The error between the current reference and the sensed grid-side average current i_{gavg} is input to the current compensator Gi to achieve error-free control. For periodical signal control, the quasi-PR regulator is used as part of the current compensator to improve the steady-state control accuracy.

In addition to the fundamental quasi-PR compensator (G_{PR_1st}), the harmonic compensators (G_{PR_3rd}, G_{PR_5th}, and G_{PR_7th}) are also added to eliminate the corresponding harmonics. Besides, a PI controller is added to improve the dynamic performance. The expression of the current compensator is given below:

$$G_i(s) = K_P + \frac{K_I}{s} + K_{P\_1H} + \sum_{n=1,3,5,7} \frac{2K_{R\_nH}\omega_c s}{s^2 + 2\omega_c s + \omega_{0\_nH}^2} \quad (11)$$

As in the PFC mode, the third-order LCL network is included in the current control loop. Among the basic passive damping methods, adding a parallel resistor to the filter capacitor method provides the best damping effect. It can effectively damp the resonance spike with little impact on other frequencies.

As shown in Figure 20 (ignoring the control delay), the filter capacitor current feedback is equivalent to the passive suppressor that adds a parallel resistor to the capacitor. Therefore, also in the grid-connected inverter mode, the filter capacitor current feedback can be used to suppress the resonance spike effectively.

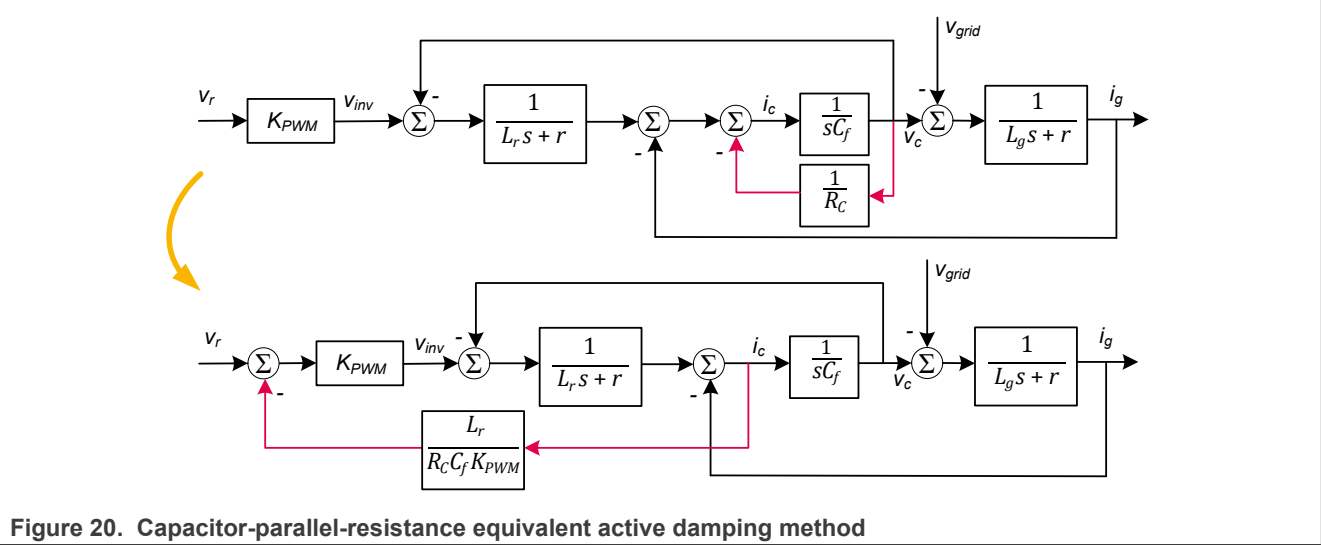

Figure 20. Capacitor-parallel-resistance equivalent active damping method

Also, due to the influence of nonlinear loads, background harmonics are always present in the grid voltage. It leads to obvious distortion of the grid current. To improve the grid current quality, you must suppress the influence of the grid voltage on the grid current. The grid current compensator mentioned above only covers the main harmonics. Due to the influence of digital control delay, achieving the best dynamic performance while ensuring stability is difficult. The grid voltage feedback control strategy can suppress multiple harmonics at the same time without affecting the grid current loop gain, and can maintain good dynamic performance. Therefore, the grid voltage feedforward is added to suppress the influence of grid voltage on grid current.

Figure 21 shows the detailed control block diagram of the grid-connected inverter mode. To cover more harmonics, the grid voltage feedforward includes three terms: proportional, first differential, and second differential.

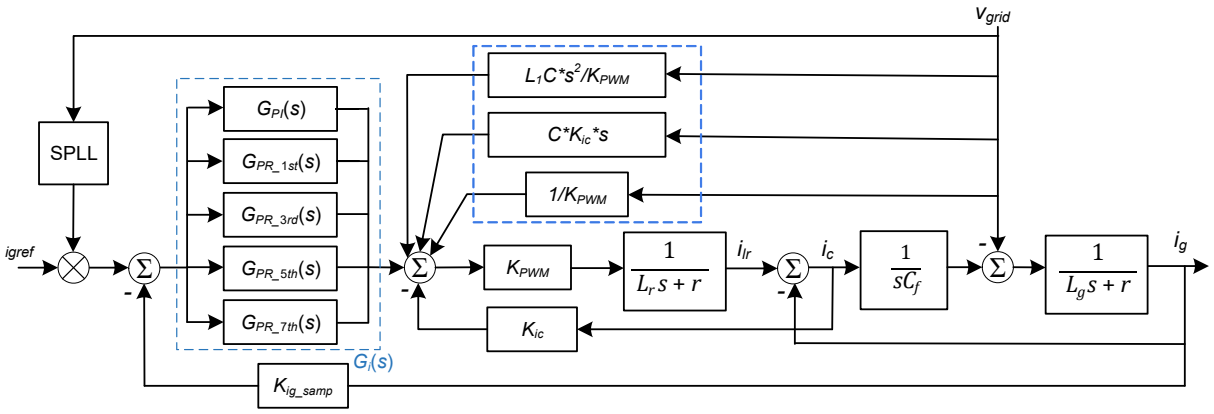

Figure 21. Control block diagram in grid-connected inverter mode

2.3.3 Presynchronization of inverter output and grid voltage

In the standalone inverter mode with the TRIAC open, the inverter output voltage may differ from the grid voltage in terms of phase and amplitude. Now, if the TRIAC is closed suddenly, the huge voltage difference may cause serious consequences. Therefore, before turning on the TRIAC to connect the inverter to the grid, the phases and magnitudes of the two voltages must be matched.

The amplitude can be matched easily by adjusting the inverter reference voltage amplitude according to the current grid voltage. To match the phase, increase or decrease the frequency of the inverter output voltage gradually. To minimize the synchronization time, the correct frequency adjustment direction must be determined based on the current phase difference θ_{diff}. The software PLL calculates the phase of the power grid θ_{PLL}. Under good control conditions, the inverter output voltage tracks its reference without error. Therefore, the reference phase θ_{ref} can be used directly as the inverter output voltage phase. Assuming $\theta_{diff} = \theta_{PLL} - \theta_{ref}$, Figure 22 shows the basic principle of frequency adjustment.

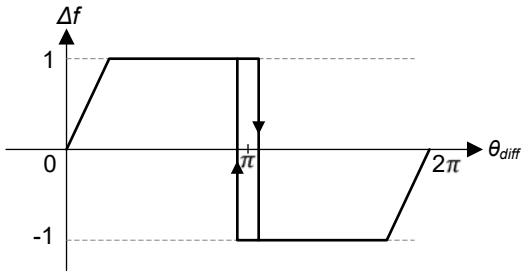

Figure 22. Frequency adjustment principle

When $0 < \theta_{diff} < \pi$, that is, the power grid voltage is ahead of the inverter output voltage; increase the inverter reference voltage frequency. Otherwise, decrease the inverter reference voltage frequency.

To ensure that the inverter output voltage meets the load requirements, the frequency change Δf is limited to 1 Hz. When θ_{diff} is around π, Δf may jitter between 1 and -1 due to some measurement error. To avoid this issue, a hysteresis is added. Figure 23 shows the phase synchronization implementation block diagram.

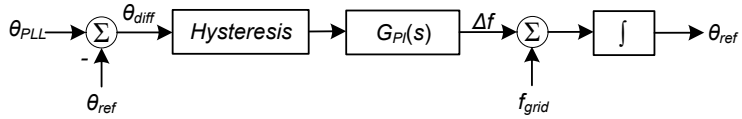

Figure 23. Phase synchronization implementation

When θ_{diff} equals 0 or 2π, it means that the power grid voltage and the inverter output voltage are in phase. Because Δf is zero when θ_{diff} equals 0 or 2π, the two voltages stay in phase after the phase match is obtained. Then, the TRIAC can be closed to connect the inverter to the grid.

3 Hardware

This section describes the hardware design and layout considerations for the multimode bidirectional AC-DC converter.

3.1 Specifications

Table 1 shows the specifications of the multimode bidirectional AC-DC converter.

Table 1. Multimode bidirectional AC-DC converter specifications

Mode		Item	Symbol	Parameter
/		Maximum power	P	800/400 W
		Switching frequency	f_{sw}	20 kHz
AC-to-DC		Input voltage	V_{ac_rms}	85-265 V, 50/60 Hz
		Output voltage	V_{dc}	380 V
		Peak efficiency	η	93% at 110 V, 96% at 220 V
		Power factor	PF	> 0.95
		Total harmonic distortion in current (iTHD)	iTHD	< 5%
DC-to-AC	/	Maximum input voltage	V_{dc_max}	400 V
		Nominal input voltage	V_{dc_nom}	380 V
	Standalone	Output voltage	V_{ac}	220 V / 50 Hz, 110 V / 60 Hz
		Peak efficiency	η	95%
		iTHD for linear load	iTHD	< 3%

3.2 Converter-side inductor design

Calculate the converter-side inductor value according to the tolerable inductor current ripple. For this design, the maximum inductor current ripple is calculated using the formula $\Delta I_{Lmax} = 30\% * I_{Lpk}$. Here, I_{Lpk} is the peak value of the inductor current. The steps to calculate the converter-side inductor value are as follows:

1. Calculate the inductor RMS current I_{Lrms}:

$$I_{Lrms} = \frac{P}{V_{ac_{rms}}} = \frac{800W}{220V} = 3.636A \tag{12}$$

2. Calculate the maximum inductor current ripple ΔI_{Lmax}:

$$\Delta I_{Lmax} = 30\% * \sqrt{2} * I_{Lrms} = 1.54A \tag{13}$$

3. Calculate the minimum inductor value L_{min}:

$$L_{fmin} = \frac{V_{dc}}{4 f_{sw} \Delta I_{Lmax}} = \frac{380V}{4 * 20kHz * 1.54A} = 3.08mH \tag{14}$$

Based on the calculation result, two standard inductors (L201204-162MHF from ITG Electronics) are used as the grid-side inductors. The total inductance value is 3.268 mH at 0 A. You can configure the two inductors in one of the following ways:

- Connect both inductors to a single IGBT bridge leg in series by performing the following resistor reconfiguration:
  - Solder R35, R36, and R41.
  - Remove R24, R38, and R39.
- Connect each inductor to a separate IGBT bridge by performing the following resistor reconfiguration:
  - Remove R35, R36, and R41.
  - Solder R24, R38, and R39.

3.3 Filter capacitor and grid-side inductor selection

Because the circuit of this design is compatible with both the standalone and grid-connected inverter modes, the capacitor is designed based on the reactive power it introduces. The maximum capacitor value is calculated as follows:

$$C_f = \lambda_c \frac{P}{\omega_0 V_g^2} = \frac{5\%*800W}{2*\pi*50Hz*220V*220V} = 2.6\mu F \quad (15)$$

where:

- λ_c is the maximum tolerable ratio of the reactive power introduced by the filter capacitor to the inverter active power.
- ω_0 is the angular frequency of the grid voltage.
- V_g is the RMS value of the grid voltage.

Finally, an electromagnetic interference (EMI) suppression capacitor B32923C3225+ (2.2 µF, 305 V_{ac}) from TDK Electronics is used as the filter capacitor.

Combined with the converter-side inductor design result, the cut-off frequency of the LC filter is about 1896 Hz, which is about 1/10 of the switching frequency. In addition, select the grid-side inductor that meets both filtering and system stability requirements. Usually, the grid-side inductor is selected such that the LCL resonant frequency is greater than $f_{sw}/6$.

3.4 Schematic overview

This section contains the following subsections:

3.4.1 Power circuit

Figure 24 shows the power circuit of the converter.

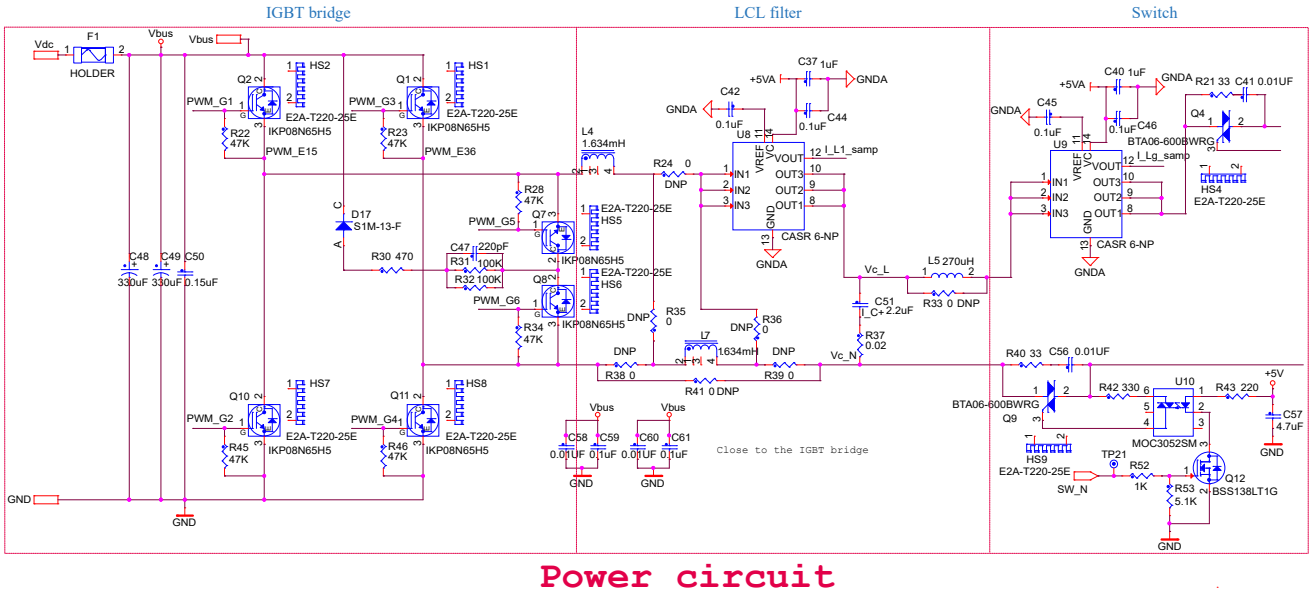

Figure 24. Power circuit

As shown in Figure 24, the following four insulated-gate bipolar transistors (IGBTs) are used to form a complete IGBT bridge circuit:

- Q1
- Q2
- Q10
- Q11

Q1 and Q2 form an IGBT sub-bridge. Similarly, Q10 and Q11 form another IGBT sub-bridge.

Additionally, two IGBTs Q_7 and Q_8 are used at the center of the two sub-bridges as bidirectional switches. For the current design, these two IGBTs are disabled.

The design also uses TRIACs as load and grid switches. For more details, see Section 3.4.2.

3.4.2 TRIAC and its driver circuit

Figure 25 shows the TRIAC and its driver circuit.

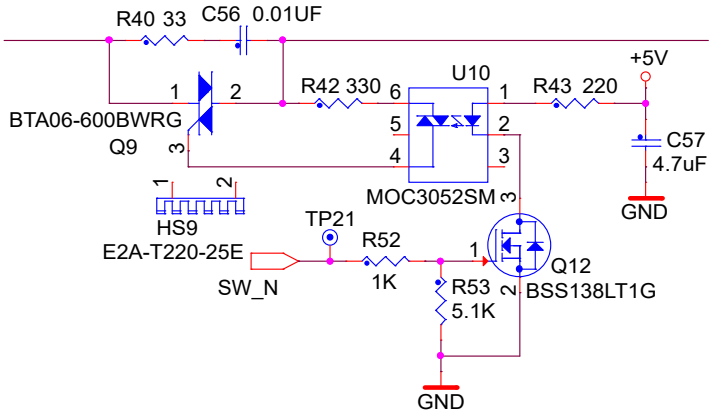

Figure 25. TRIAC and its driver circuit

To handle the insulated driver, an optocoupler is used for the TRIAC driver with few components. No isolated power is needed.

When working in the inverter mode, the TRIAC is used as a load or grid-connected switch. In the PFC mode, the bus capacitor can be precharged smoothly without the current limiting resistor and the relay. The precharging is done by controlling the conduction angle of the TRIAC.

3.4.3 Sensing circuits

Figure 26 shows an AC voltage sensing circuit. The 1.65 V offset voltage generated by the resistor divider is added for AC voltage sensing with single supply OpAmp. In addition, the offset voltage can be removed in the DSC ADC by the hardware.

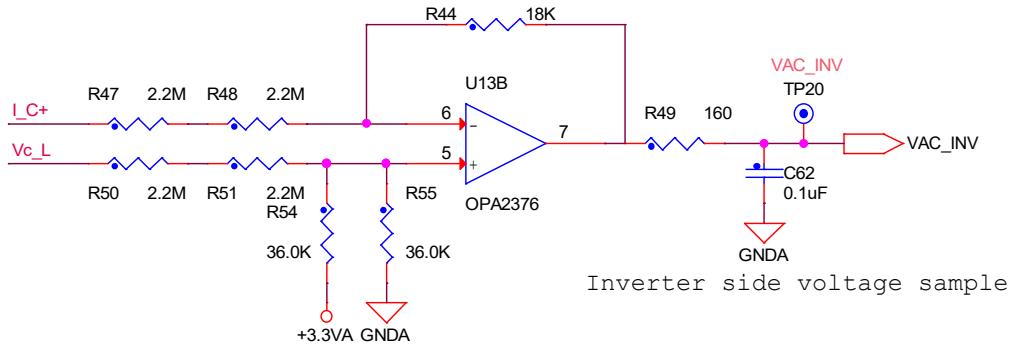

Figure 26. AC voltage sensing circuit

Figure 27 shows a DC bus voltage sensing circuit. The resistor divider circuit is used to detect the DC bus voltage. Due to the high resistance of the DSC ADC input port, OpAmp is not needed in this voltage sensing circuit.

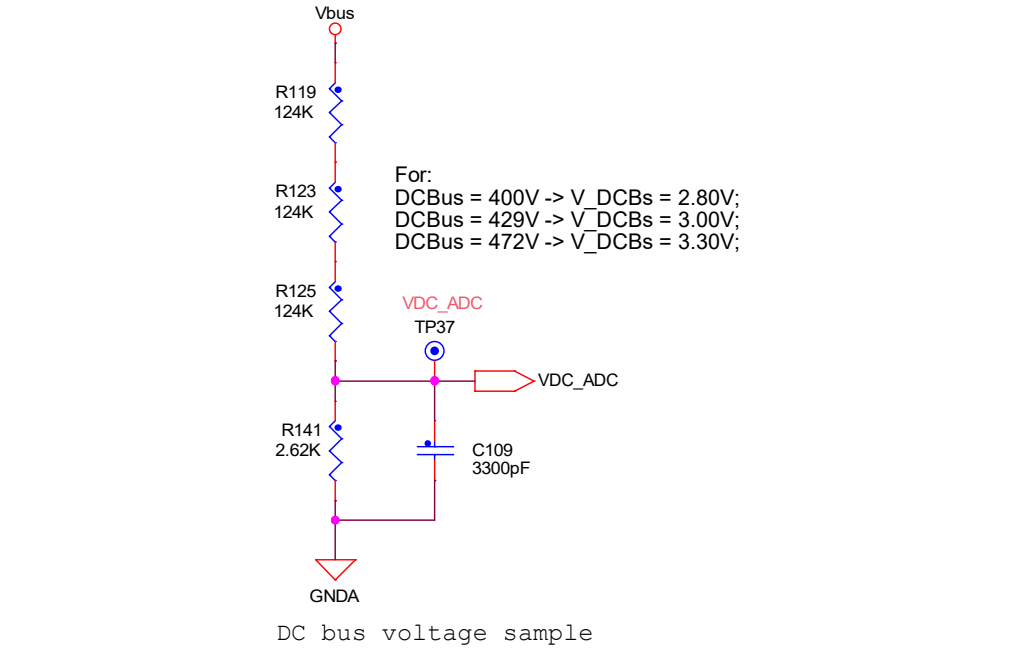

Figure 27. DC bus voltage sensing circuit

Figure 28 shows the current sensing circuit. A CASR 6-NP current transducer is used for the current sensing. The output signal of the current transducer is connected with the differential OpAmp circuit.

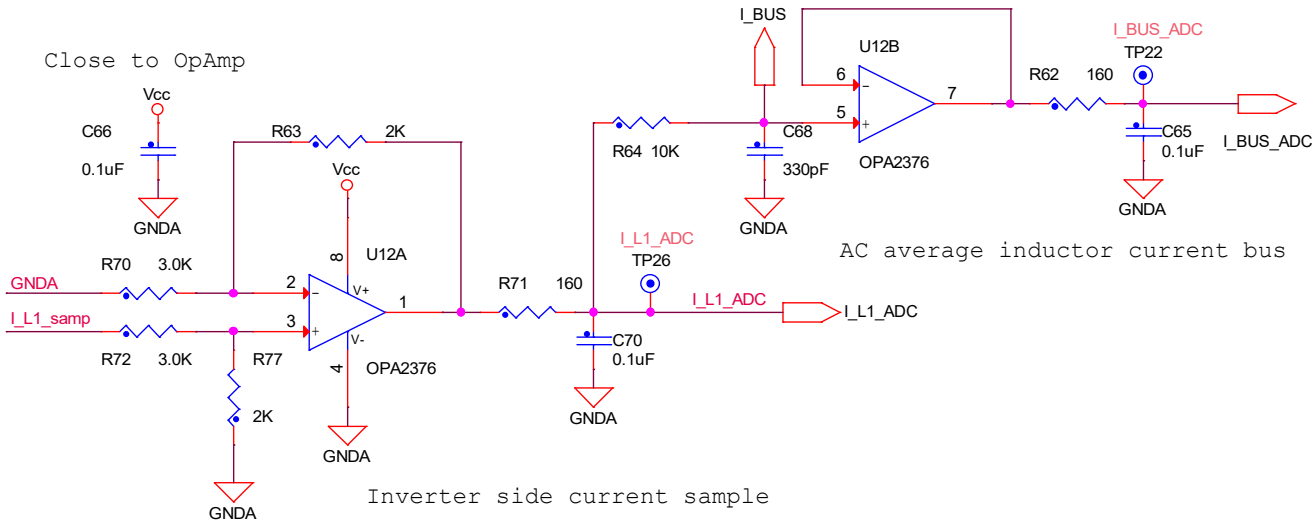

Figure 28. Current sensing circuit

3.4.4 Auxiliary power circuits

Figure 29 shows the circuit diagrams of the auxiliary power circuits.

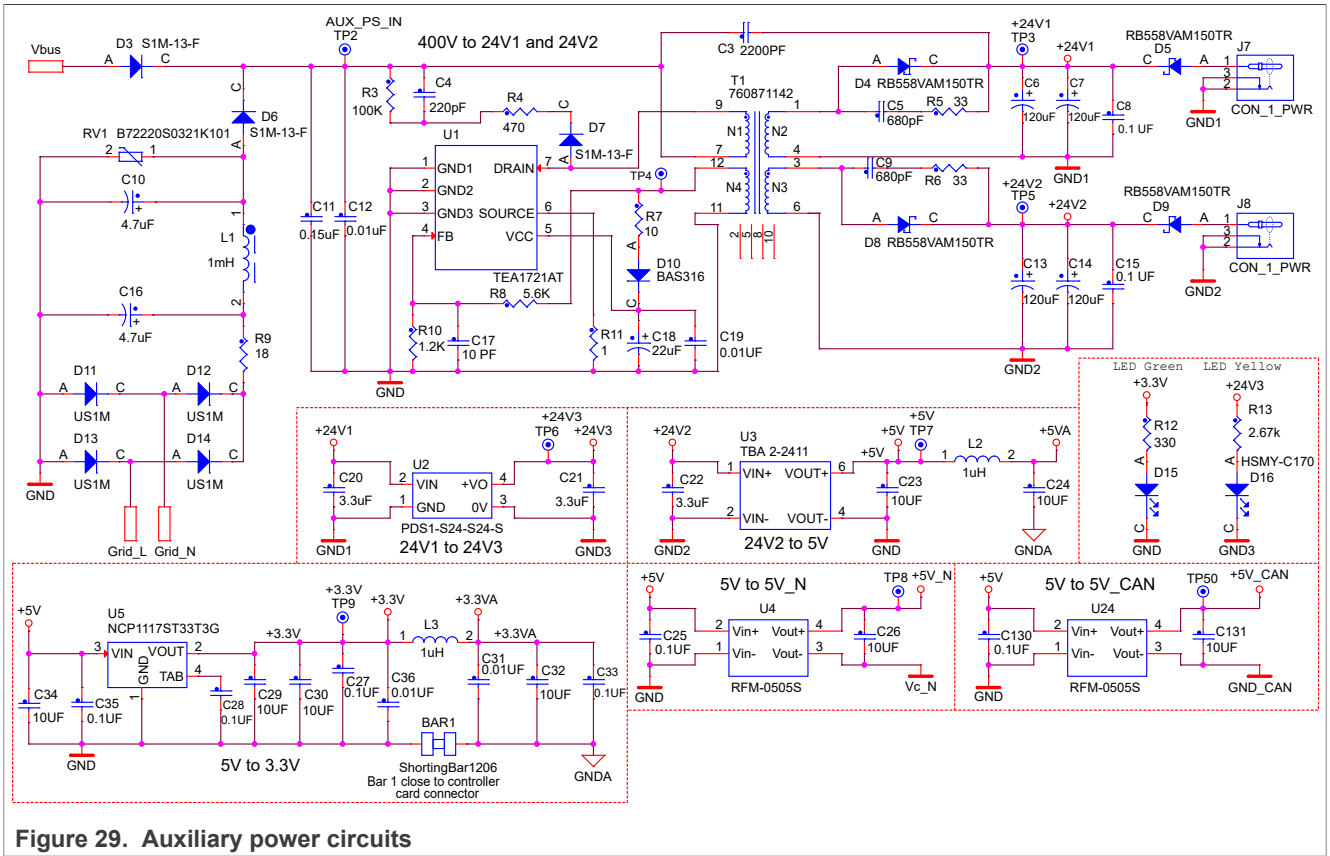

Figure 29. Auxiliary power circuits

Both the AC side and the DC bus can supply power to the flyback converter. The converter converts the high-voltage input to two isolated 24 V power supplies, namely +24V1 and +24V2. An NXP TEA1721 device having a good control performance is used as the controller for the flyback converter. Alternatively, the +24V1 and +24V2 supplies can also be powered from an external power supply or adapter, in the absence of the high-voltage

input. It is more convenient for debugging. An isolated power module with the +24V1 input generates one more power supply, +24V3. The +24V1, +24V2, and +24V3 supplies are used to power up the IGBT driver circuits.

Another isolated power module with the +24V2 input generates the +5V supply. In addition, an LDO regulator with the +5V input generates the +3.3V supply. The isolated +5V_N and +5V_CAN supplies are used for powering up the isolated OpAmp and the isolated controller area network (CAN) transceiver, respectively.

3.5 PCB layout considerations

In this multimode bidirectional AC-DC converter reference design, both the AC port voltage and the DC bus voltage are high voltages. Also, the system works in the high switching frequency mode with high dv/dt and di/dt. Therefore, the PCB layout must be well considered, especially for the following points:

- The current loop routing in the power circuit
- Power ground copper pouring to avoid influence by high frequency and high current signal
- Heat dissipation for power components
- Distance consideration for high-voltage circuits

Figure 30 shows the component placement strategy for the power board.

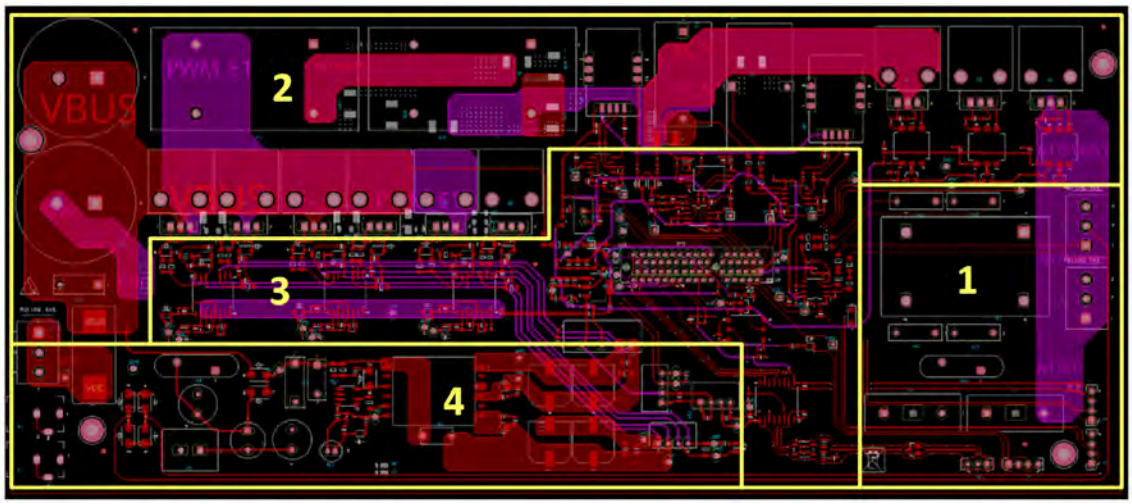

Figure 30. Power board component placement strategy

The PCB can be divided into the following four regions:

- Region 1: EMI filter circuit
- Region 2: Power circuit
- Region 3: Signal and DSC control board circuit
- Region 4: Auxiliary power circuit

The following are some recommendations for component placement on the PCB:

- Keep the power loop as small as possible.
- Ensure that the output current flows through the filter circuits first, before reaching at the output port.
- To prevent the high-frequency power circuit from interfering with the control signals, separate the control circuits from the power components.

The GND strategy is important because the converter is a switch-mode power supply. Figure 31 shows the GND routing strategy for the power board.

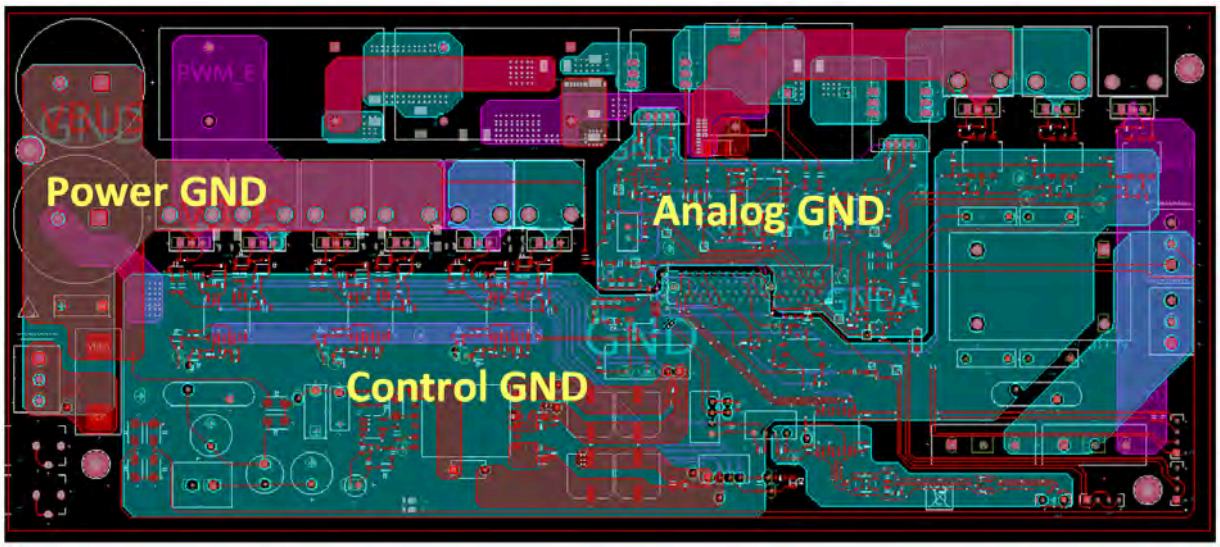

Figure 31. Power board GND strategy

The following are some recommendations for GND routing strategy:

- Power GND, control GND, and analog AGND must be separated.
- Connect the power GND and the control GND at the DC bus eCAP pin.
- Ground the analog ground and the control ground at a single point.

4 Software design

This section contains the following subsections:

4.1 Scaling

This section contains the following subsections:

4.1.1 Fractional number representation

The current application uses fractional representations for most of the quantities. The NXP DSCs support the fractional arithmetic. It benefits the application and the algorithm library.

The N-bit signed fractional format is represented using the 1.[N-1] format (one signed bit, N-1 fractional bits). Signed fractional (SF) numbers lie in the following range:

$$-1.0 \leq SF \leq +1.0 - 2^{[N-1]} \tag{16}$$

For word and long-word signed fractions:

- The most negative word is 0x8000, which equals to -1.0.

- The most negative long-word is 0x80000000, which equals to -1.0.
- The most positive word is 0x7FFF, which equals to 1.0 - 2^{-15}.
- The most positive long-word is 0x7FFFFFFF, which equals to 1.0 - 2^{-31}.

In short, the fractional value that a signed N bit integer represents for the 1.[N-1] format is:

$$\frac{integer}{2^{N-1}} \tag{17}$$

4.1.2 Scaling of analog quantities

Equation (18) shows the relationship between a real representation and a fractional representation of an analog quantity:

$$Fractional\ \ Value = \frac{Real\ \ Value}{Real\ \ Quantity\ \ Range} \tag{18}$$

- Fractional Value = Fractional representation of a quantity
- Real Value = Real quantity in physical units
- Real Quantity Range = Maximum defined quantity value (in physical units) used for scaling

The ADC module performs a ratio metric conversion. For single-ended measurements, the digital result is proportional to the ratio of the analog input to the reference voltage. The ADC result register value is calculated as follows:

$$ADC\ \ result\ \ register = round\left(\left(\frac{V_{in} - V_{REFL}}{V_{REFH} - V_{REFL}}\right) * 4096\right) * 8 \tag{19}$$

where V_{in} is the ADC pin voltage and V_{REFH} and V_{REFL} are reference voltages ($V_{REFH} = 3.3V$ and $V_{REFL} = 0$).

In the current design, all ADC channels are configured to work in the single-ended mode. Therefore, the ADC result can be interpreted directly as the fractional expression of the analog quantity.

4.1.2.1 DC bus voltage scale

The ADC module measures the voltage on the voltage resistor divider. Therefore, the maximum voltage scale is proportional to the maximum ADC input voltage range. In this application, the DC bus voltage is 472 V, when the ADC pin voltage is 3.3 V. Figure 32 shows the DC bus voltage scaling process.

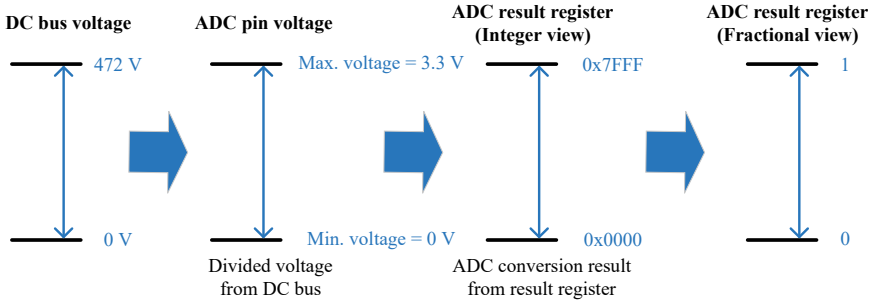

Figure 32. DC bus voltage scaling process

4.1.2.2 AC current scale

The current transducer senses the AC current. Because the current is an AC current, the current transducer adds to it a 2.5 V voltage offset. Therefore, the output of the current transducer is always positive. An OpAmp amplifies the transducer output with a gain of 2/3, adding approximately 1.65 V offset to the ADC input pin. The

AC current scale is proportional to the ADC input voltage range. The current range <-24 A, 24 A> corresponds to the voltage range <0 V, 3.3 V> at the input of the ADC channel. It implies that the current range <-24 A, 24 A> corresponds to a fractional value in the range <-0.5, 0.5> in the code, as shown in Figure 33. Therefore, the AC current scale is 48 A in this case.

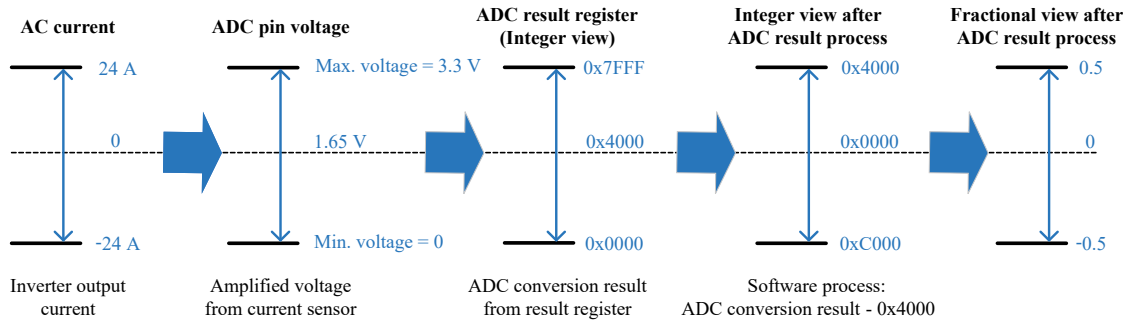

Figure 33. AC current scaling process

4.1.2.3 AC voltage scale

A differential amplifier circuit senses the AC voltage. Because the voltage is an AC voltage, a resistor divider adds to it a 1.65 V offset, ensuring that the OpAmp output is always positive. The AC voltage scale is proportional to the ADC input voltage range. The voltage range <-404 V, 404 V> corresponds to the voltage range <0 V, 3.3 V> at the input of the ADC channel. It implies that the voltage range <-404 V, 404 V> corresponds to a fractional value in the range <-0.5, 0.5> in the code, as shown in Figure 34. Therefore, the AC voltage scale is 808 V in this case.

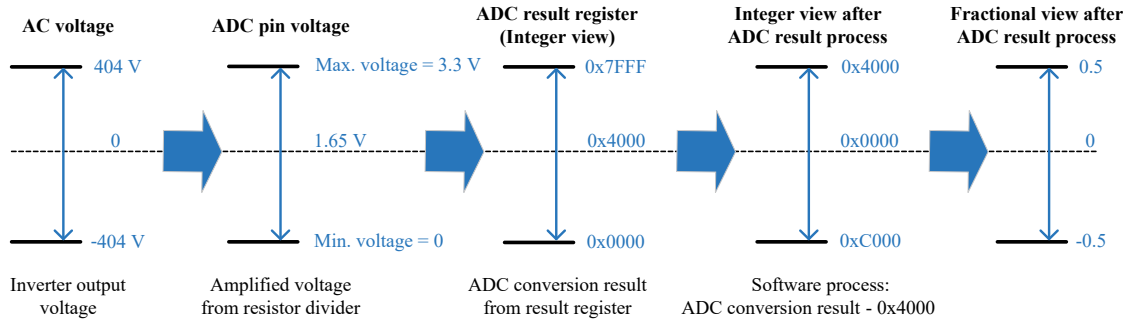

Figure 34. AC voltage scaling process

4.2 Software control flow

This section contains the following subsections:

- Section 4.2.1 "Mode selection and switching"
- Section 4.2.2 "Interrupts"
- Section 4.2.3 "Main state machine"
- Section 4.2.4 "PFC substate machine"

4.2.1 Mode selection and switching

The AC-DC converter operates in one of the following modes:

- PFC mode
- Standalone inverter mode

- Grid-connected inverter mode

The converter can switch modes smoothly according to the instructions provided or based on the grid and DC-side conditions. Due to the limitations of the test conditions, remote control is used in this design to simulate mode selection and switching.

4.2.1.1 Switching between PFC and inverter modes

Figure 35 shows the selection and switching logic between the PFC and inverter modes.

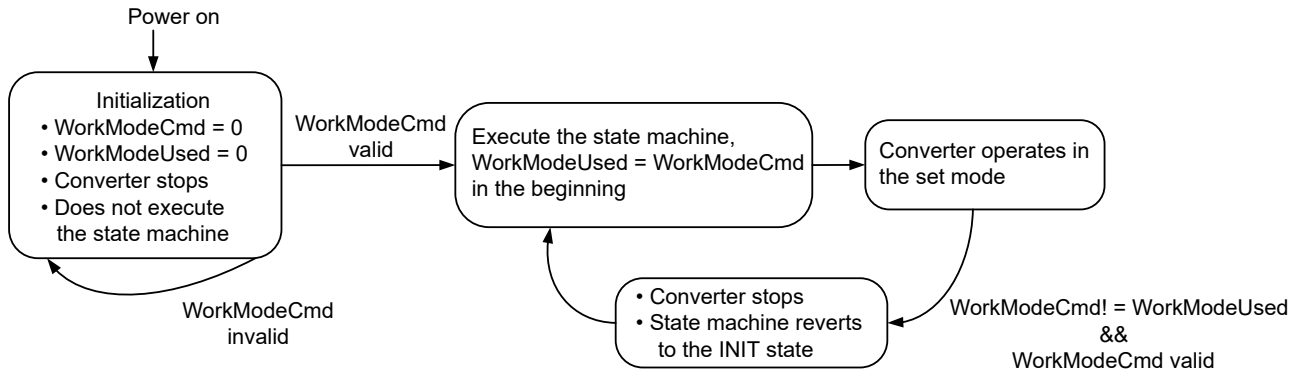

Figure 35. PFC and inverter mode switching flow

For mode control, the following two variables are defined:

- WorkModeCmd: It represents a work mode command. The value of this variable can be changed via a remote control (FreeMASTER).
- WorkModeUsed: It represents the current work mode. The code logic can determine the value of this variable.

For the above two variables, value 1 represents inverter mode, value 2 represents PFC mode, and other values are invalid.

After reset, both variables have the invalid value 0. The converter is idle until a valid WorkModeCmd is detected. When WorkModeCmd = 1, a valid inverter mode should be configured. After that, WorkModeUsed is assigned to the value of WorkModeCmd in the beginning of the INIT state. Then, the converter operates in the set mode. During the operation of the converter, if a valid change is detected in WorkModeCmd:

- The converter stops immediately.
- The state machine reverts to the INIT state, and all variables are reinitialized.

Note: *Remove the DC source before the PFC mode starts working, and remove the AC source before the inverter mode starts working.*

4.2.1.2 Switching between standalone and grid-connected inverter modes

Figure 36 shows the selection and switching logic between the standalone and grid-connected inverter modes.

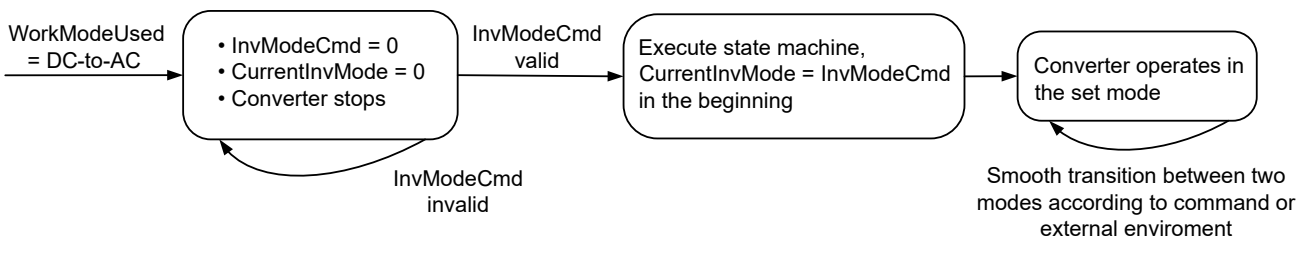

Figure 36. Selection and switching logic between two inverter modes

In the inverter mode, selection between the standalone and grid-connected modes can be done using the following two variables:

- InvModeCmd: It represents the inverter mode command. The value of this variable can be changed via a remote control (FreeMASTER).
- CurrentInvMode: It represents the current inverter mode. The code logic can determine the value of this variable.

For the above two variables, value 1 represents the grid-connected inverter mode, value 2 represents the standalone inverter mode, and other values are invalid.

When no valid inverter mode is selected, the converter does not start. When a valid InvModeCmd is detected, CurrentInvMode is assigned to the value of InvModeCmd and the converter operates in the set mode.

During the operation of the converter, if a valid change is detected in InvModeCmd, the system must follow a specific switching process to ensure system safety.

Figure 37 shows two flows explaining the switching process between the two inverter modes: grid-connected mode and standalone mode. In this process, the converter is always working, no need to pause it.

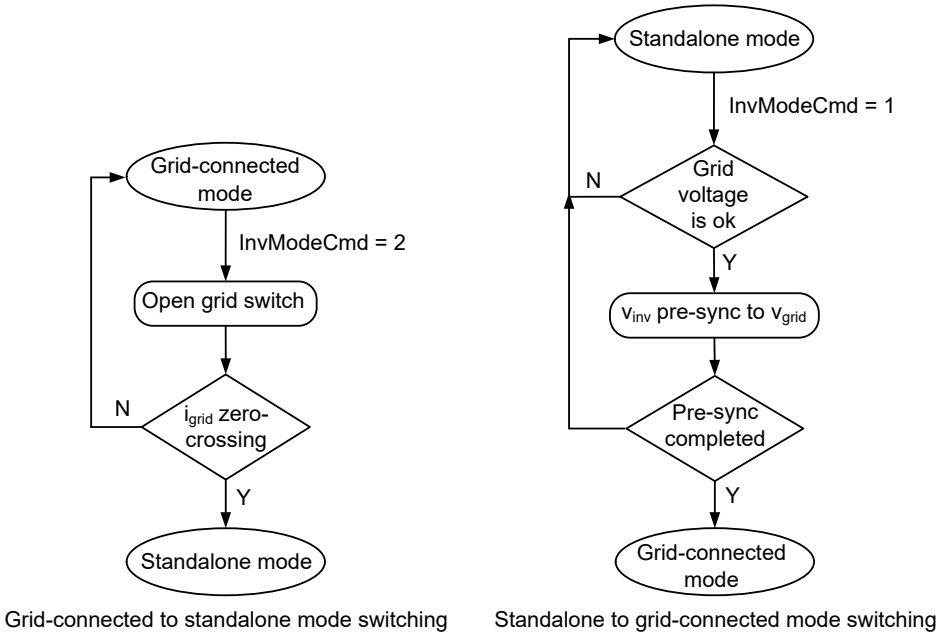

Figure 37. Detailed switching process between two inverter modes

When the inverter is operating in the grid-connected mode and InvModeCmd is changed to 2, the grid-connected switch drivers are immediately turned OFF. However, due to the characteristic of the TRIAC, the line remains ON until the current reaches zero, keeping the converter operating in the grid-connected mode. When the current reaches zero, switch the inverter to the standalone mode.

When the inverter is operating in the standalone mode and InvModeCmd is changed to 1, the grid voltage detection is executed first. The inverter output voltage and grid voltage synchronization logic is started after determining that the grid voltage is normal. When the inverter output voltage is synchronized with the grid voltage, close the grid-connected switches and switch the inverter to the grid-connected mode.

4.2.2 Interrupts

The multimode bidirectional AC-DC converter control is interrupt driven. The system provides the following interrupt service routines (ISRs):

- Fast_Ctrl_ISR: The Enhanced Flexible Pulse Width Modulator A (eFlexPWMA) submodule 0 VAL5 compare match signal generates Fast_Ctrl_ISR. This ISR has a higher priority (priority 2) and a frequency of 20 kHz. All control loops in the inverter mode and the current loop in the PFC mode are handled in this ISR. The state machine and the power metering calculations are also handled in this ISR.
- PFC_VolCtrl_ISR: The periodic interrupt PIT0 generates PFC_VolCtrl_ISR. This ISR has a lower priority (priority 1) and a frequency of 2 kHz. It is only enabled in the PFC mode to handle the voltage loop.
- CUR_CBCPro_Cnt_ISR: eFlexPWMA fault 0 and fault 1, which are connected to CMPA and CMPB for hardware current protection, generate CUR_CBCPro_Cnt_ISR. This ISR has a lower priority (priority 1). In the standalone inverter mode, fault automatic clearing is enabled and only the fault counting is performed in this ISR. In the PFC and grid-connected inverter modes, the fault flag is set directly in this ISR.

4.2.3 Main state machine

Both the PFC and inverter modes use the same main state machine (see Figure 38). A conditional statement based on the WorkModeUsed and CurrentInvMode variables is used for selecting the code to be used in a mode. The state machine is implemented in Fast_Ctrl_ISR with a frequency of 20 kHz.

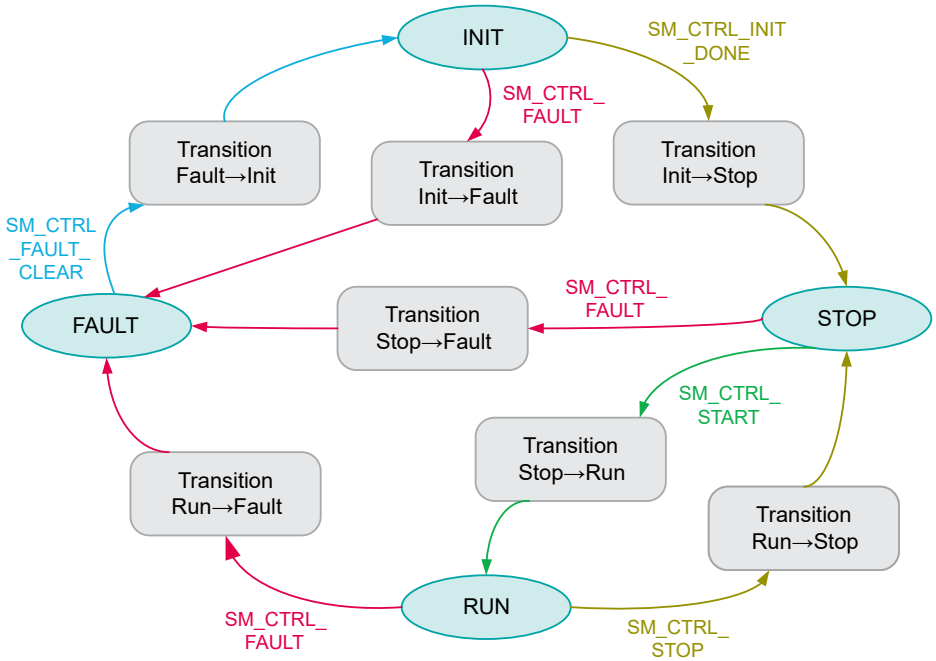

Figure 38. Main state machine

After reset, the state machine always stops in the INIT state. It starts executing after detecting a valid WorkModeCmd. A valid inverter mode should be configured when WorkModeCmd = 1. After starting, the state machine does not stop even if WorkModeCmd and InvModeCmd become invalid. During the operation, if a valid WorkModeCmd is detected that is different from the current WorkModeUsed, the state machine reverts to the INIT state and starts again.

The main state machine can be in one of the following states:

- INIT: All variables are initialized. The AC voltage and current offsets are calibrated. After calibration, the state machine goes to the STOP state.
- STOP: The converter is stopped and it waits for all startup conditions to be met. After the startup conditions are met, the state machine enters the RUN state. The startup conditions for different modes are as follows:
  - PFC mode:
    - AC input satisfies the requirements.

  - The precharge is done.
  - `bACDC_Run` = 1
- Standalone inverter mode:
  - DC bus voltage satisfies the requirements.
  - `bACDC_Run` = 1
- Grid-connected inverter mode:
  - Grid voltage and DC bus voltage satisfy the requirements.
  - `bACDC_Run` = 1

- RUN: The converter starts running. Both the voltage and current control loops are only executed in this state. In addition, the `bACDC_Run` command is checked regularly in this state. When the command is cleared, the state machine goes back to the STOP state.
- FAULT: The state machine goes to the FAULT state in these conditions:
  - Over/under voltage on the DC or AC side
  - Over current
  - Over/under AC frequency
  - Over temperature

  After the faults disappear, the state machine goes to the INIT state. The protection of the DC bus voltage in the PFC mode or AC voltage in the inverter mode is not enabled until the converter has been started.

4.2.4 PFC substate machine

To achieve soft-start and improve light load efficiency, a substate machine is adopted in the PFC mode, as shown in Figure 39. The substate machine is enabled only in the RUN state of the main state machine.

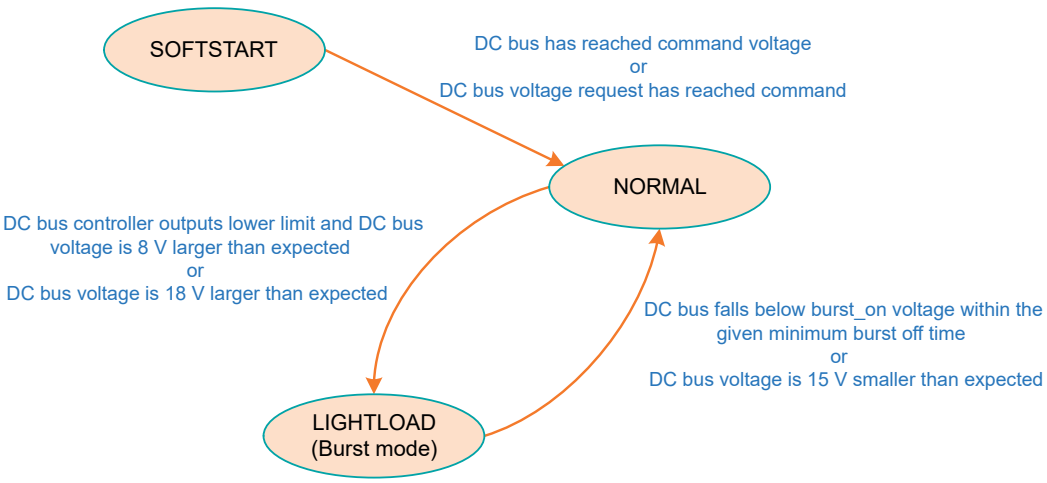

Figure 39. PFC substate machine

The PFC substate machine can be in one of the following states:

- SOFTSTART: PFC control has just started. The voltage reference starts from the current DC bus voltage value and it follows a ramp to make the DC bus voltage rise smoothly. Considering that the initial voltage value is not fixed, the DC bus undervoltage protection value for this period is 0. The substate machine goes to the NORMAL state when one of the following conditions is met:
  - The actual DC bus voltage has reached the command voltage during reference voltage ramping (loading is light).
  - The reference voltage has reached the command voltage but the actual DC bus voltage has not reached the command voltage yet (loading is heavy).

The voltage controller output is used as a current amplitude reference for the current loop. The soft-start algorithm is implemented in PFC_VolCtrl_ISR with a frequency of 2 kHz.

- NORMAL: DC bus loading is relatively heavy. The voltage controller output is used as a current amplitude reference for the current loop. Considering the impact of input voltage feedforward, the output limits of the voltage controller change according to the input voltage RMS. It ensures that the current reference limit remains unchanged.
- LIGHTLOAD: DC bus loading is relatively light. This state is also referred to as the burst mode. A peak-to-valley controller replaces the voltage PI controller, which:
  - Disables the PWM output when the DC bus voltage is higher than the peak value.
  - Enables the PWM output when the DC bus voltage is lower than the valley value.

  A fixed current amplitude reference is used in this state.

Because the DC bus current is not sampled, the following parameters are used to analyze the load condition:

- Output voltage
- Voltage controller output

The outcome of this analysis is used to determine whether switching is required from the NORMAL state to the LIGHTLOAD state or vice versa. For more details, see Figure 39. The switching logic between the NORMAL and LIGHTLOAD states is implemented in the RUN main state. The RUN main state is implemented in Fast_Ctrl_ISR with a frequency of 20 kHz.

4.3 Control timing

To simplify peripheral operations during mode switching, the PFC and inverter modes share the same ADC trigger signal, sampling slot, and interrupt. The ADC trigger point is configured to sample the average current. A PIT interrupt is enabled in the PFC mode for voltage control. It is disabled in the inverter mode.

Figure 40 shows a detailed system timing with ADC configuration, ISR setting, drive signals, and possible current waveform.

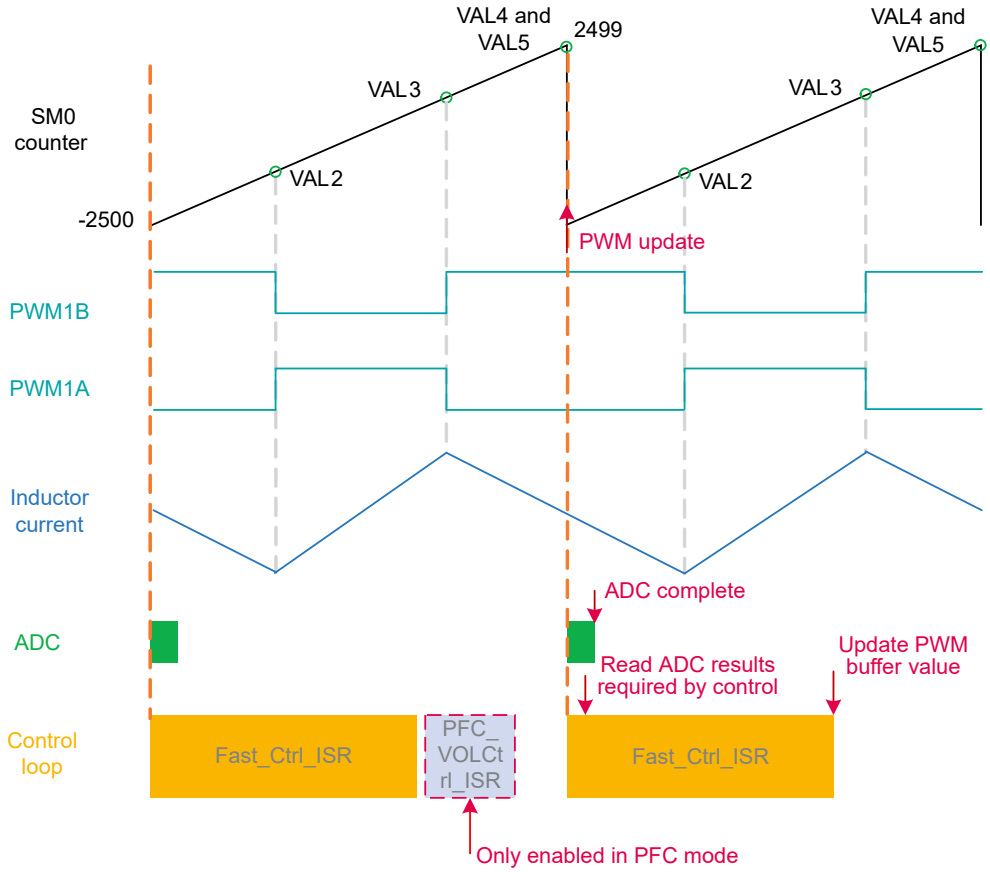

Figure 40. System timing

4.3.1 PFC mode process

Figure 41 shows the PFC mode control diagram.

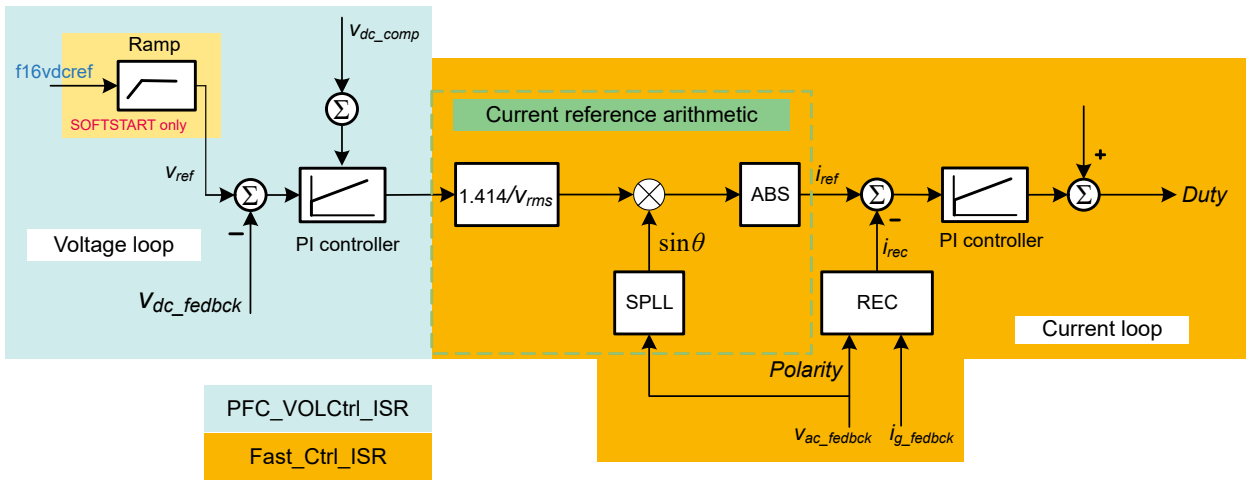

Figure 41. Control diagram of PFC mode

Two control loops are used for PFC mode control:

- The outer loop controls DC bus voltage.
- The inner loop controls the inductor current. It makes the inductor current sinusoidal and ensures that the current has the same phase as the input voltage.

4.3.2 Inverter mode process

Figure 42 shows the standalone inverter mode control diagram.

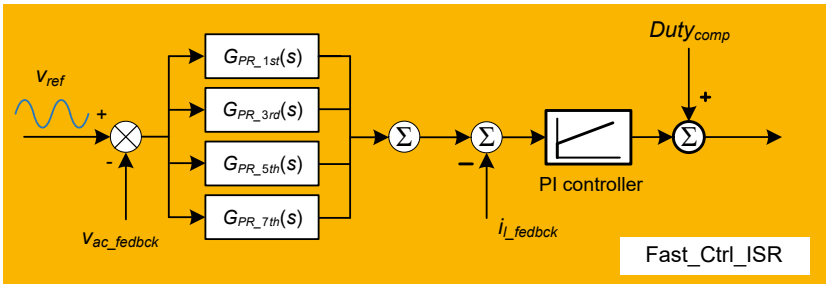

Figure 42. Control diagram of standalone inverter mode

Two control loops are used for standalone inverter mode control:

- The outer loop controls the AC output voltage. A PR regulator is used for eliminating the steady state error. Harmonic compensators are added to reduce the total harmonic distortion (THD).
- The inner current loop improves the dynamic response performance of the system.

Figure 43 shows the grid-connected inverter mode control diagram. Only one control loop is used for this mode control.

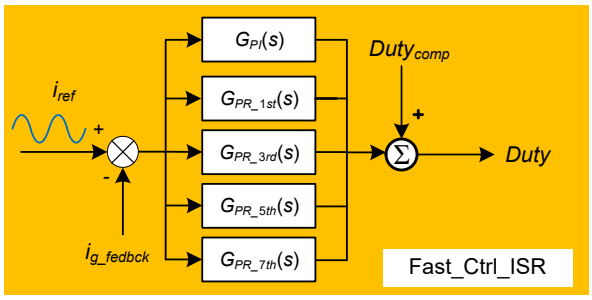

Figure 43. Control diagram of grid-connected inverter mode

Figure 44 shows the detailed implementation of presynchronization of inverter output and grid voltage, when the converter switches from the standalone mode to the grid-connected mode.

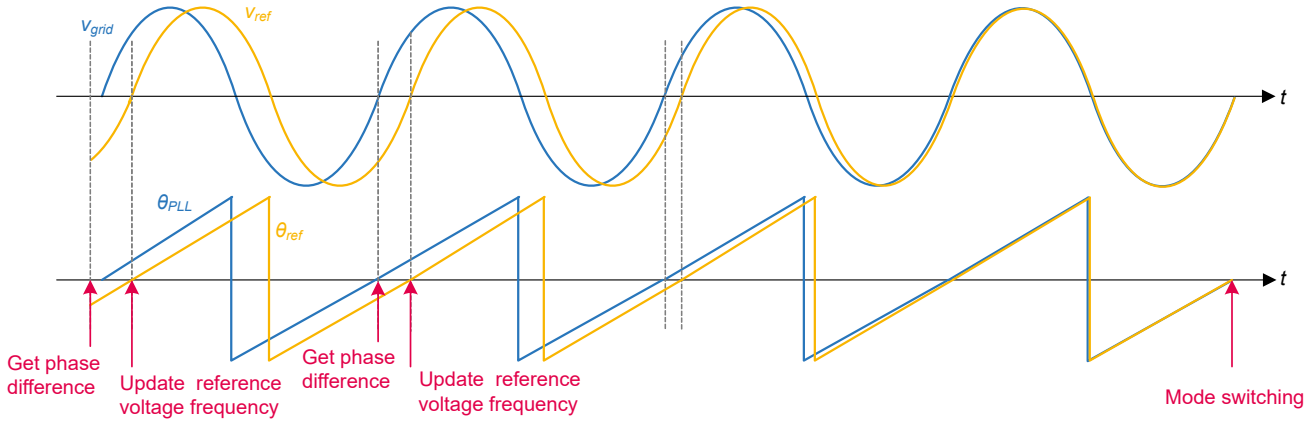

Figure 44. Presynchronization implementation

The inverter output reference voltage frequency is updated once every cycle. The phase difference θ_{diff}, is obtained at the zero-crossing point of the grid voltage from negative to positive. The desired reference voltage frequency is calculated based on this phase difference. Then, the inverter reference voltage frequency is updated at its subsequent negative-to-positive zero-crossing point.

As shown in Figure 44, in the first cycle $0 < \theta_{diff} < \pi$, the desired inverter reference voltage frequency is increased. Therefore, the phase difference θ_{diff} becomes smaller in the second cycle. This process is repeated until the negative-to-positive zero-crossing points of the grid voltage and the inverter voltage coincide. Then, mode switching can be performed.

4.4 Key peripheral configuration

To simplify peripheral operations during mode switching, the configuration of peripherals is similar in all modes. The configuration of key peripherals for control and protection is described below:

- eFlexPWMA: eFlexPWMA submodule 0 generates two complementary PWM outputs for high frequency switches in both the PFC and inverter modes. The PWM output has a constant frequency of 20 kHz and a variable duty cycle. The VAL5 compare event of submodule 0 generates an interrupt routine Fast_Ctrl_ISR. To obtain a more accurate average current, VAL4 is placed at the midpoint of the switch.
  Note: *In the inverter mode, the GPIO outputs control the slow switches. In the PFC mode, because IGBTs are used, synchronous rectification has no efficiency advantage. The slow switches are always OFF and the current flows through the antiparallel diode.*
- ADC: The VAL4 compare event of eFlexPWMA submodule 0 triggers ADC, which is configured in the simultaneous parallel mode.
- PIT0: PIT0 is used to generate a 2 kHz periodic interrupt routine PFC_VolCtrl_ISR. The priority of this ISR is lower than the priority of the eFlexPWMA compare event ISR.
- HSCMP: Three high-speed comparators (HSCMPs) are used. They can be grouped into the following two categories:
  - HSCMPA and HSCMPB: The inductor current is an alternating current. Therefore, for overcurrent protection, two comparators (HSCMPA and HSCMPB) are used. The built-in 8-bit DAC sets the fault threshold.
  - HSCMPC: The built-in high-speed comparator C is used to detect the overvoltage condition of the DC bus voltage.

Figure 45 shows the connections between different peripherals. eFlexPWMA fault 0 and fault 1 from CMPA and CMPB, respectively, are configured in the automatic recovery mode for the cycle-by-cycle current limit in the standalone inverter mode. In addition, the interrupt for fault 0 and fault 1 is enabled for fault recording. eFlexPWMA fault 2 from CMPC is configured in the manual recovery mode.

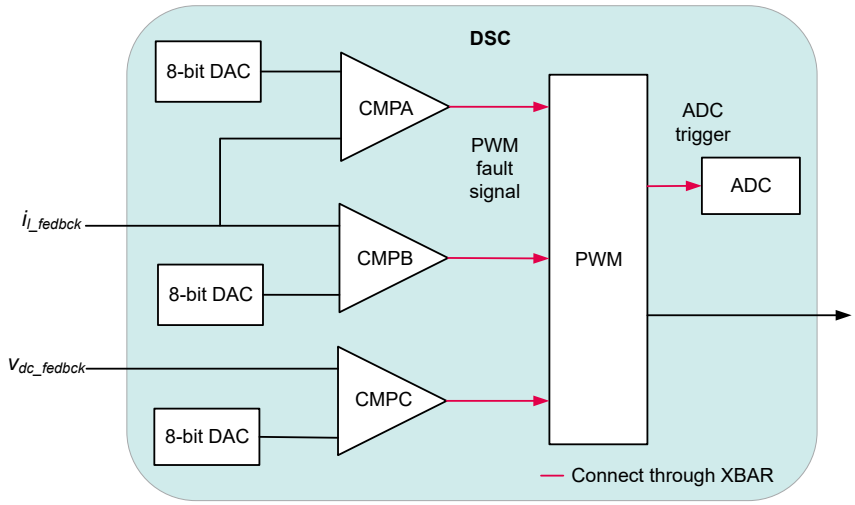

Figure 45. Peripheral connections

5 Testing and results

Figure 46 shows the power board of the multimode bidirectional AC-DC converter and the HVP-56F83783 daughter card. The major interfaces used are highlighted.

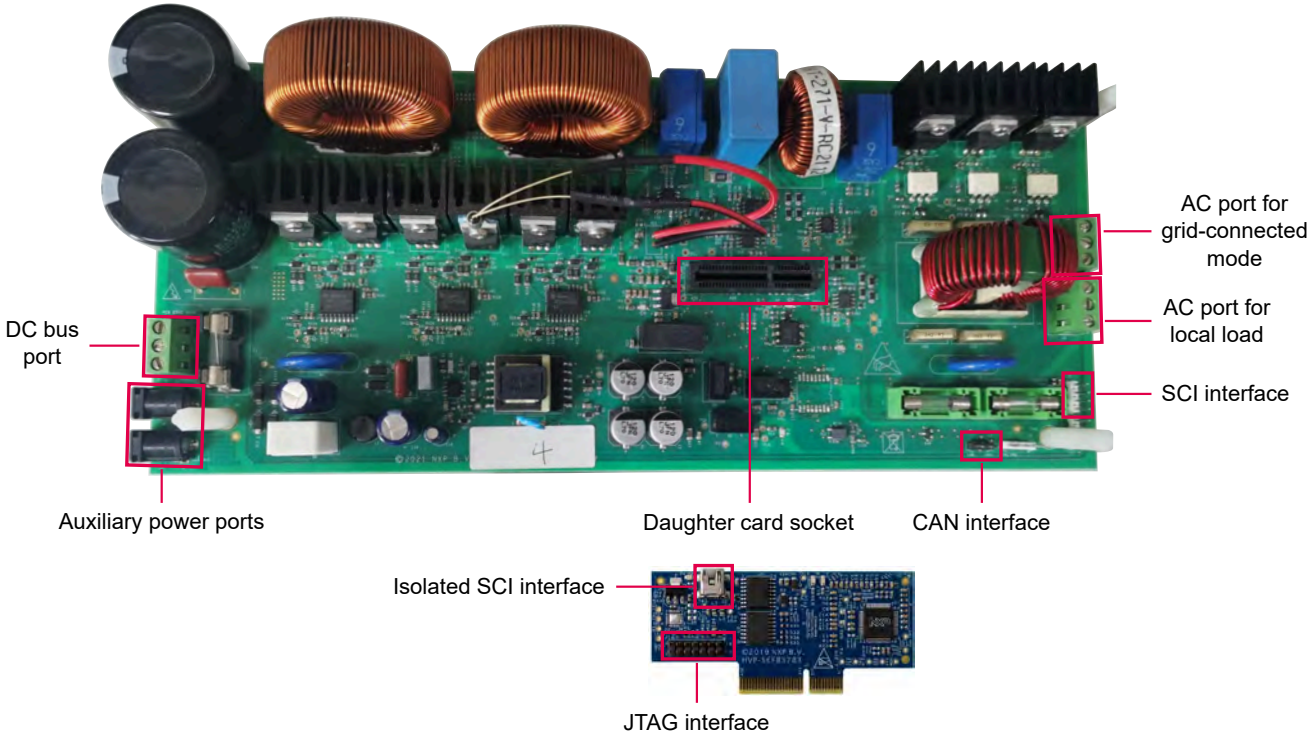

Figure 46. Hardware platform of multimode bidirectional AC-DC converter

To download the program into the DSC, connect the JTAG interface of the daughter card to the host computer through a debugger, such as a Multilink debug probe from PEmicro. The daughter card can be powered using its USB interface or from the main power board.

To control and monitor the working status of the converter, follow these steps:

1. Connect the isolated SCI interface on the daughter card to the host computer through a USB cable.
2. Open the `Multimode_Bidir_DCAC_LCL_MC56F83783.pmpx` file with the latest FreeMASTER version.
3. Go to the Bidirectional ACDC converter block and activate it.

5.1 PFC mode

This section contains the following subsections:

5.1.1 Test setup

The programmable AC power source model 61704 from Chroma is used as the AC voltage input for the PFC mode tests. To create the PFC mode test setup, follow these steps:

1. Connect the AC power source to the grid-connected AC port and connect the DC port to the load.
2. Power up the AC source.
3. Start FreeMASTER, open the `Multimode_Bidir_DCAC_LCL_MC56F83783.pmpx` file, and click the **Connect** button.
4. Go to the Bidirectional ACDC converter block. In the Variable Watch window, choose `AC_TO_DC` from the Value drop-down menu of the `gsACDC_Drive.u16WorkModeCmd` command, as shown in Figure 47.

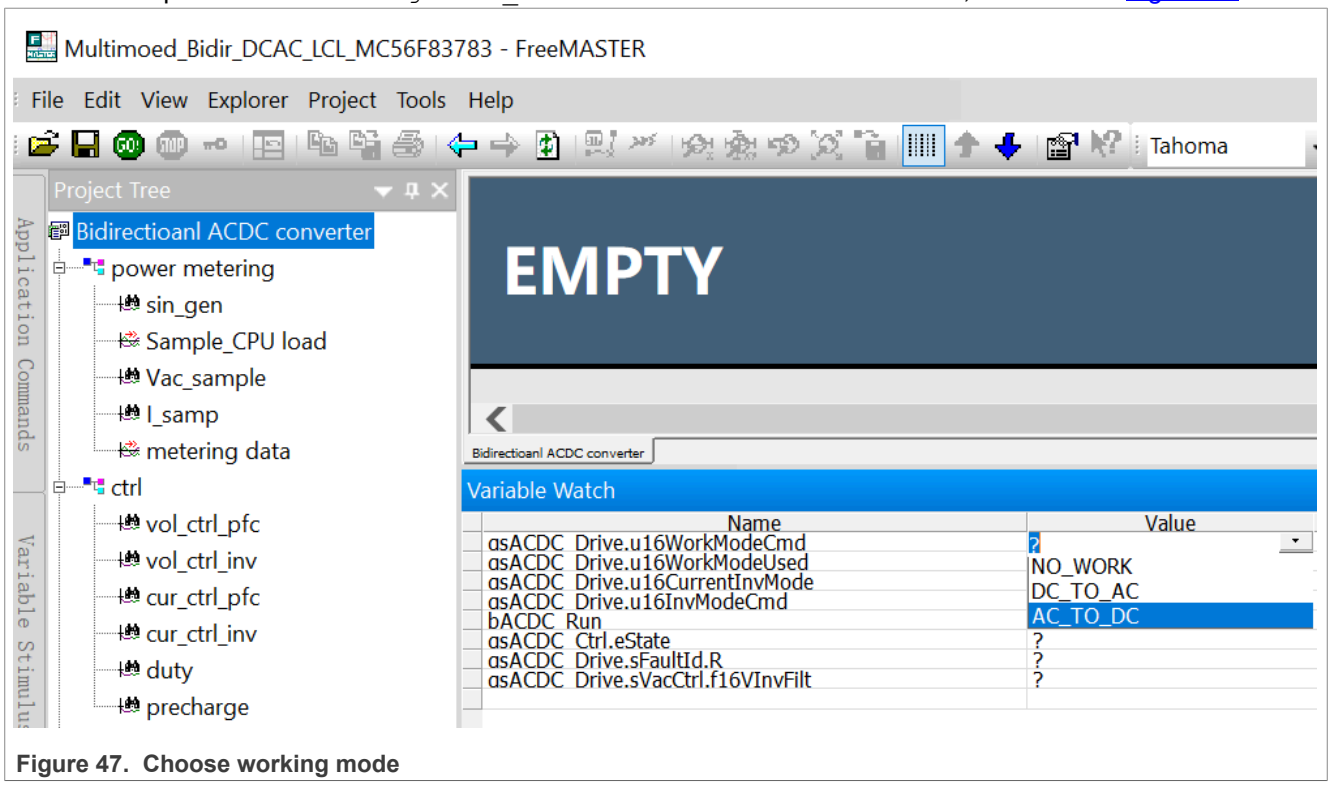

Figure 47. Choose working mode

5. To start/stop the converter, use the Value drop-down menu of the `bACDC_Run` command, as shown in Figure 48.

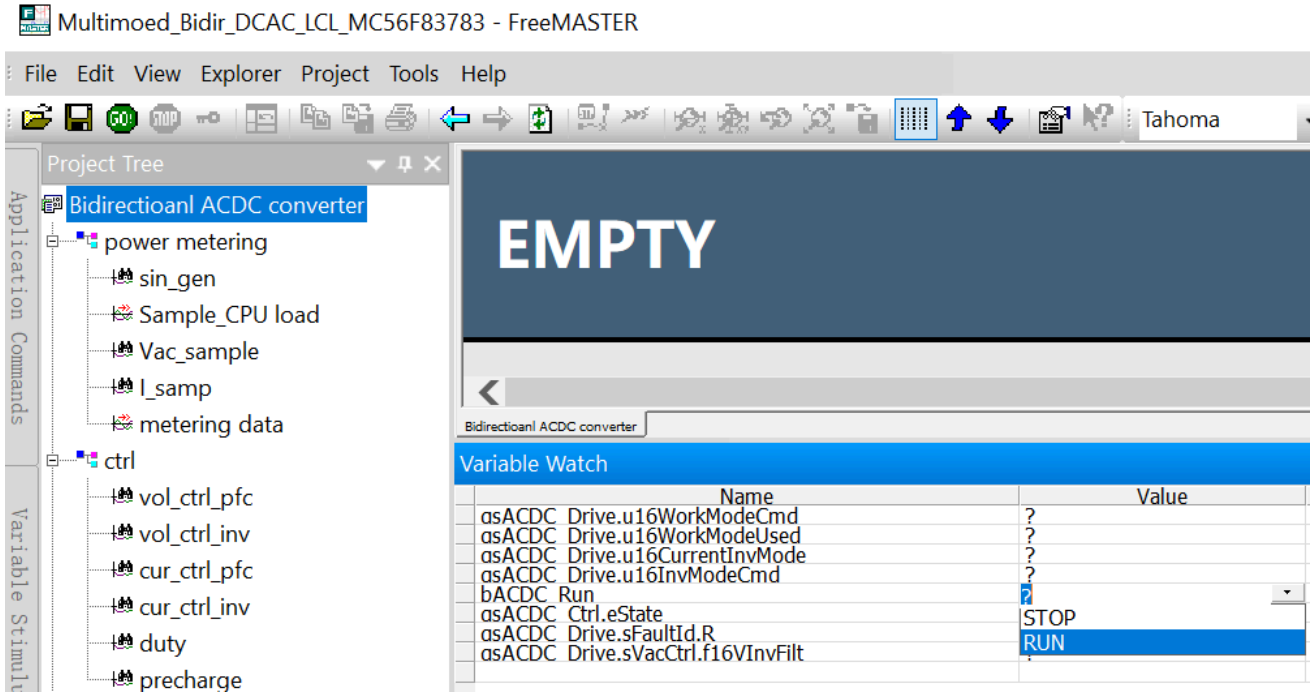

Figure 48. Start/stop converter

5.1.2 Power factor and efficiency

Figure 49 shows the power factor graph for the PFC mode at 110 V_{rms} and 220 V_{rms}.

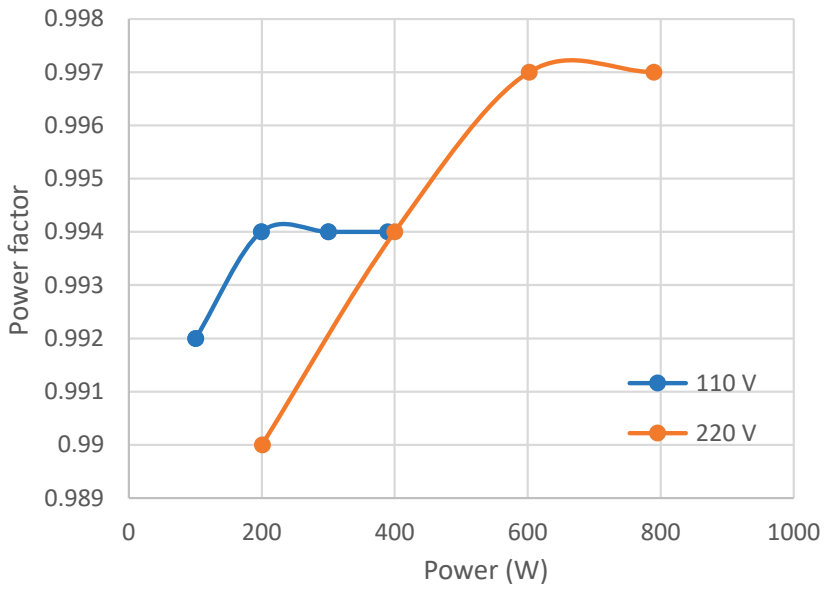

Figure 49. Power factor

The efficiency is calculated from the power displayed on the electronic load and the AC source. Figure 50 shows the efficiency graph for the PFC mode at 110 V_{rms} and 220 V_{rms}.

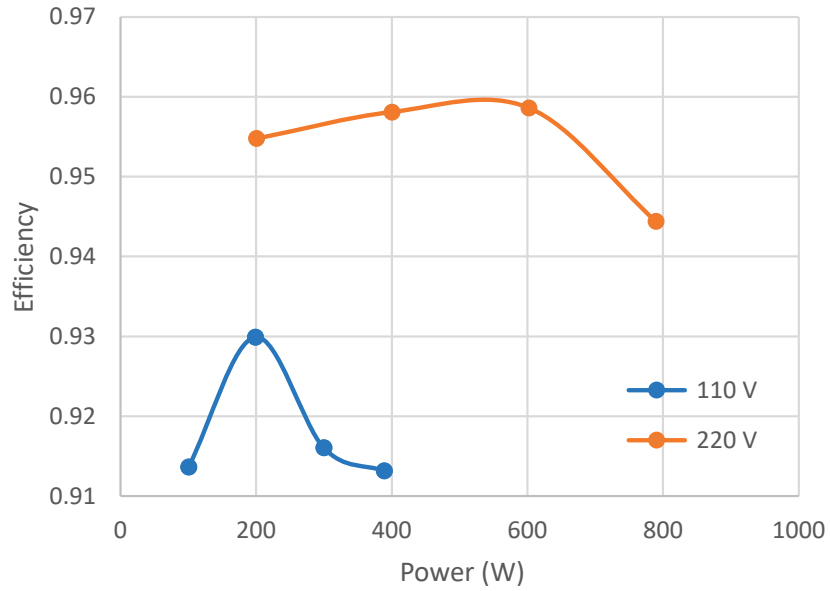

Figure 50. Efficiency at 110 V_{rms} and 220 V_{rms}

5.1.3 Startup

Figure 51 shows the startup waveform of the output DC bus voltage. The waveform is explained below:

1. The TRIAC precharges the output DC voltage to the input peak voltage.
2. The output DC voltage is soft-started to the desired voltage.
3. The output DC voltage enters the normal mode. Because the load is light, the PFC converter works in the burst mode.

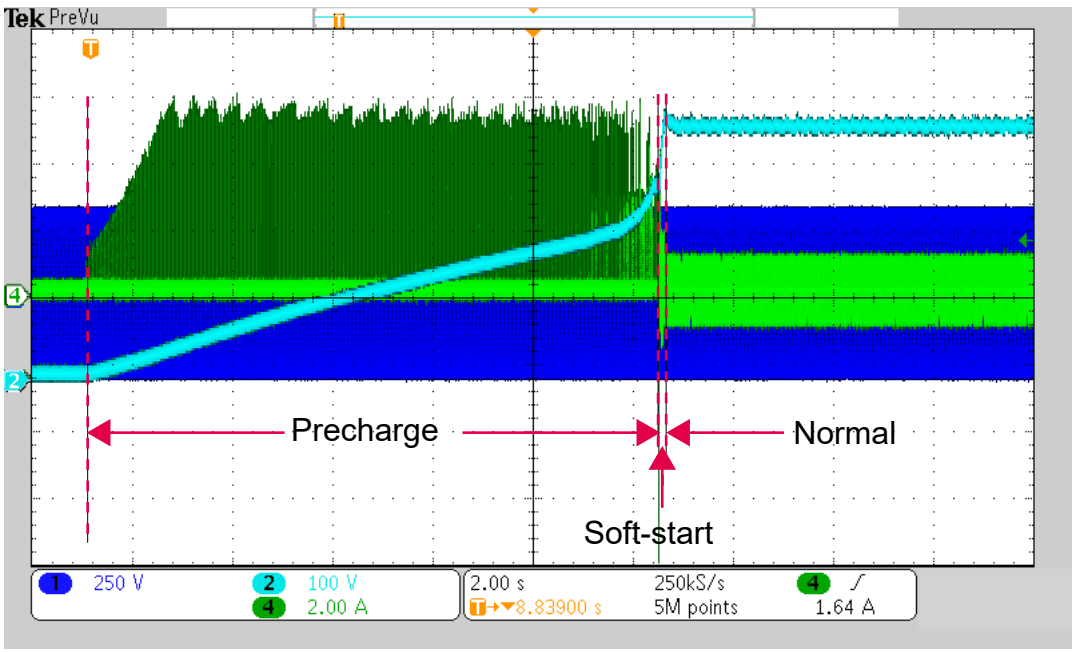

Figure 51. Startup waveform (CH1: Input AC voltage; CH2: Output DC voltage; CH4: Input current)

5.1.4 Steady state

Figure 52 shows the output voltage and input current waveforms under a steady state condition with a 389 W output power at a 110 V_{rms} input.

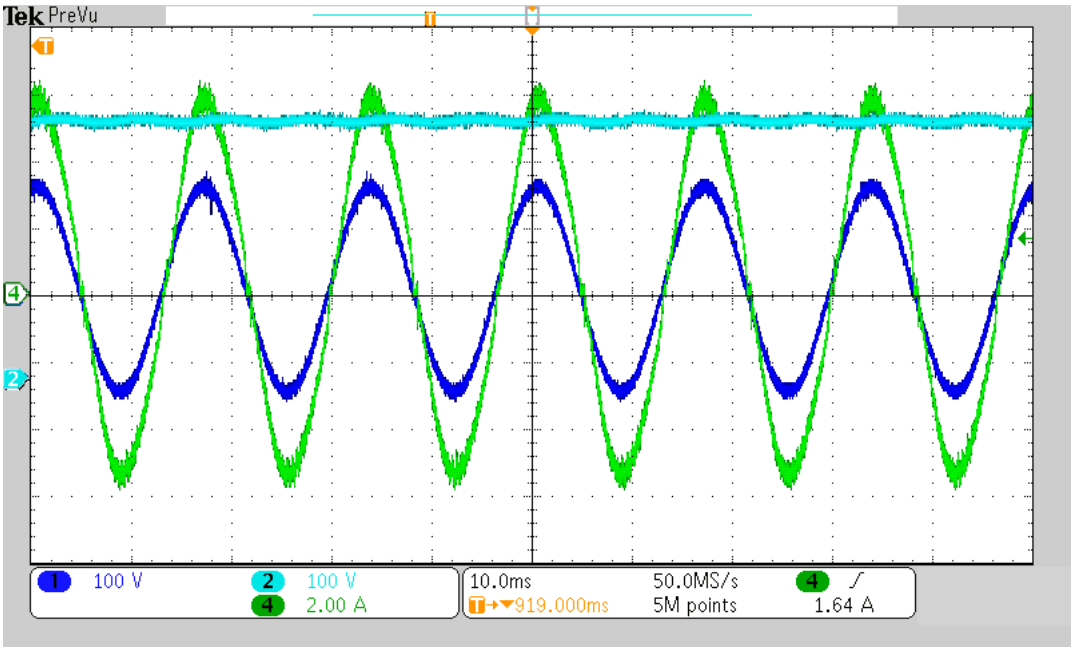

Figure 52. Steady state waveform at 110 V_{rms}

Figure 53 shows the output voltage and input current waveforms under a steady state condition with a 790 W output power at a 220 V_{rms} input.

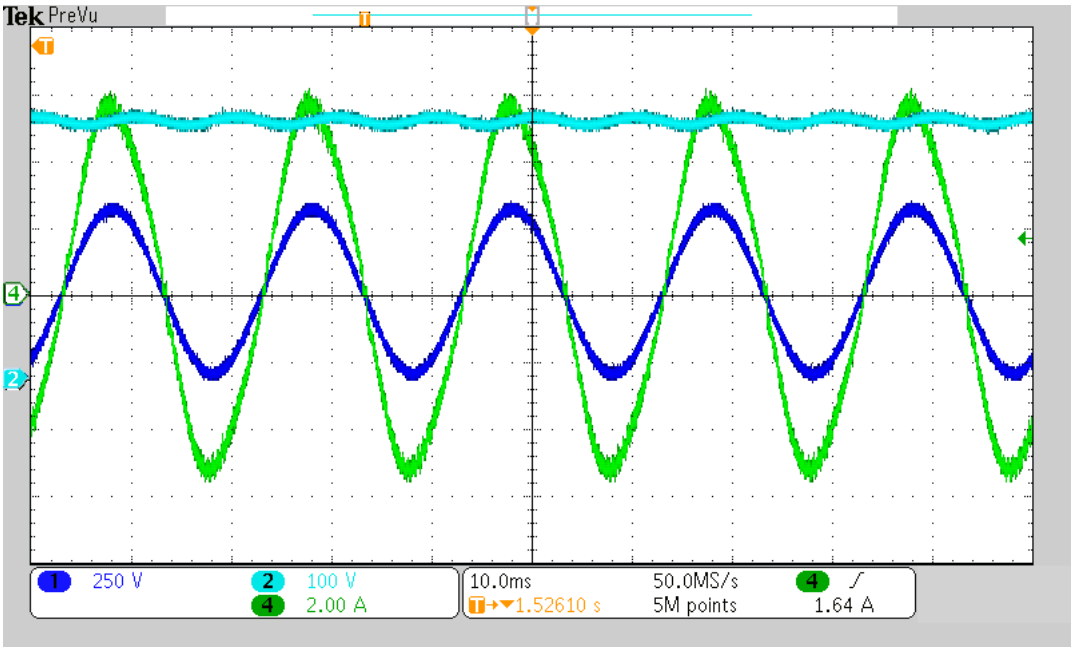

Figure 53. Steady state waveform at 220 V_{rms}

5.1.5 Dynamic performance with load change

Figure 54 shows the dynamic performance when load changes from 0 W to 800 W at a 220 V_{rms} input. The PFC converter goes from the burst mode to the normal mode immediately.

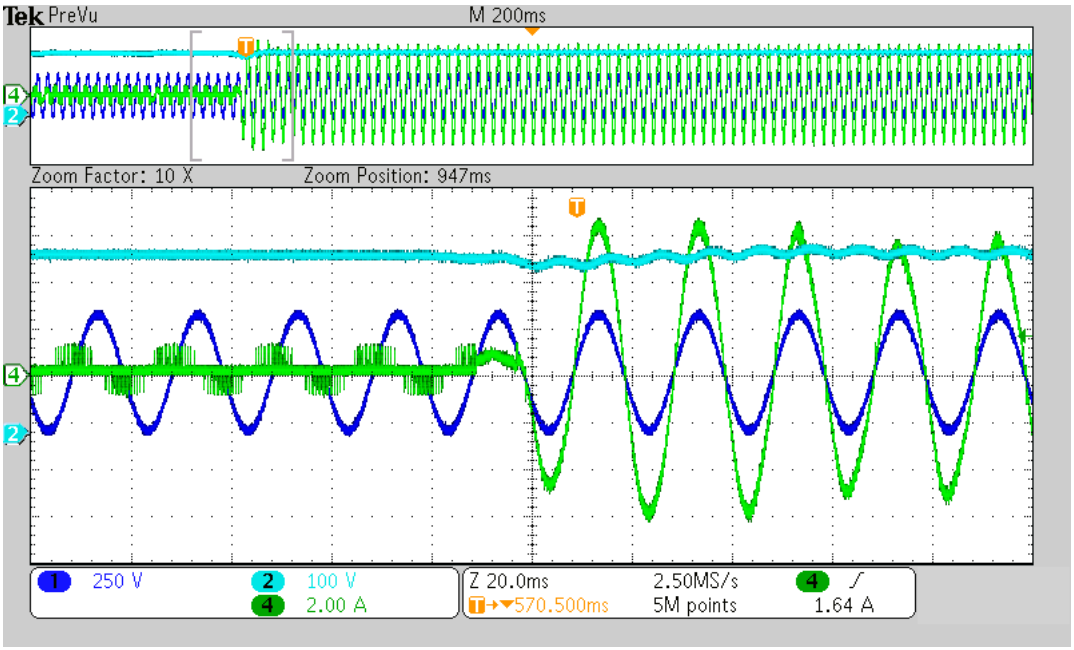

Figure 54. Waveform with load changing from 0 W to 800 W

Figure 55 shows the dynamic performance when load changes from 800 W to 0 W at a 220 V_{rms} input. The PFC converter goes from the normal mode to the burst mode immediately.

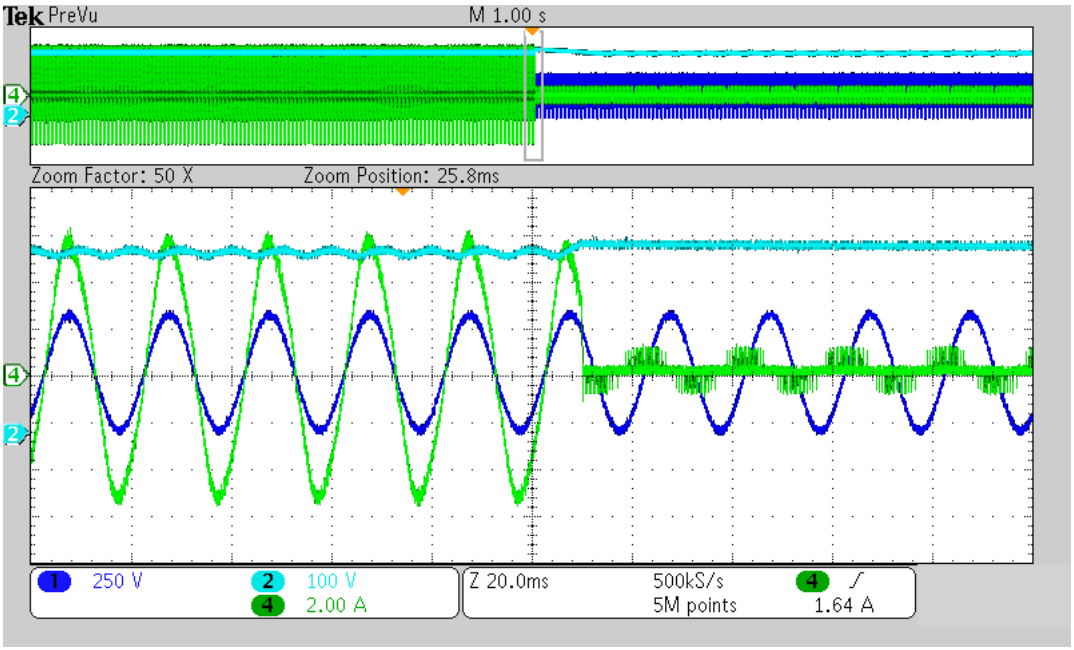

Figure 55. Waveform with load changing from 800 W to 0 W

5.1.6 Dynamic performance when input voltage is dropping

Figure 56 shows a waveform when the AC input voltage is powered down for a short period. The converter stops working after detecting that the input AC voltage has been powered off. If the input voltage recovers before the output voltage drops to the lowest limit, the converter resumes working immediately.

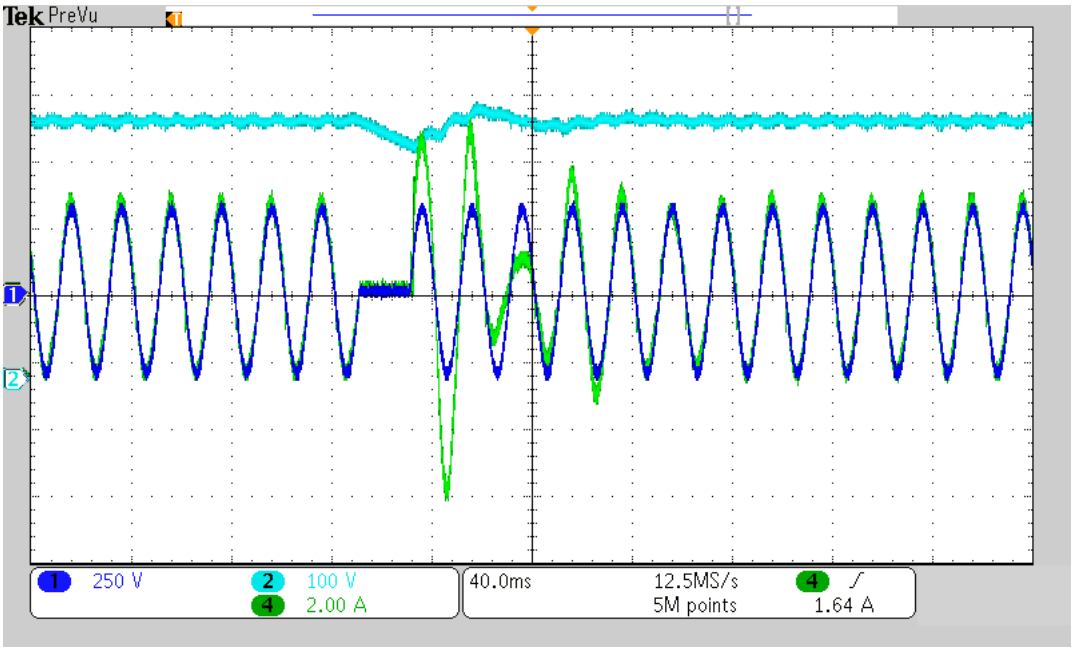

Figure 56. Waveform when AC input voltage is short-term power down

5.2 Standalone inverter mode

This section contains the following subsections:

- Section 5.2.1 "Test setup"
- Section 5.2.2 "Efficiency and THD"
- Section 5.2.3 "Steady State"
- Section 5.2.4 "Dynamic performance with load change"

5.2.1 Test setup

A programmable DC power source is used as the DC voltage input for the standalone inverter mode tests. To create the standalone inverter mode test setup, follow these steps:

1. Connect the DC power source to the DC port.
2. To enable load connection, uncomment the `CLOSE_SW_LOAD()` command in the `ACDC_TransStopRun` function.
3. Connect the load to the local load AC port.
4. Power up the DC source.
5. Start FreeMASTER, open the `Multimode_Bidir_DCAC_LCL_MC56F83783.pmpx` file, and click the **Connect** button.
6. Go to the Bidirectional ACDC converter block. In the Variable Watch window, choose `DC_TO_AC` from the Value drop-down menu of the `gsACDC_Drive.u16WorkModeCmd` command.
7. Choose `OFFGRID` from the Value drop-down menu of the `gsACDC_Drive.u16InvModeCmd` command.

8. To start/stop the converter, use the Value drop-down menu of the `bACDC_Run` command.

5.2.2 Efficiency and THD

The efficiency is calculated from the power displayed on the electronic load and the voltage source. Figure 57 shows the efficiency graph for the standalone inverter mode at 110 V_{rms} and 220 V_{rms}.

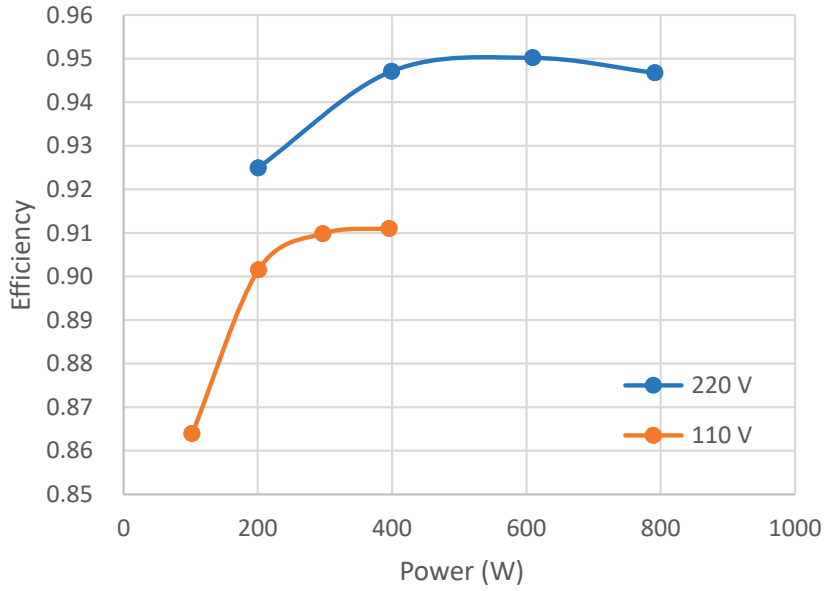

Figure 57. Efficiency at 110 V_{rms} and 220 V_{rms} with linear load

Figure 58 shows the total harmonic distortion (THD) graph for the standalone inverter mode.

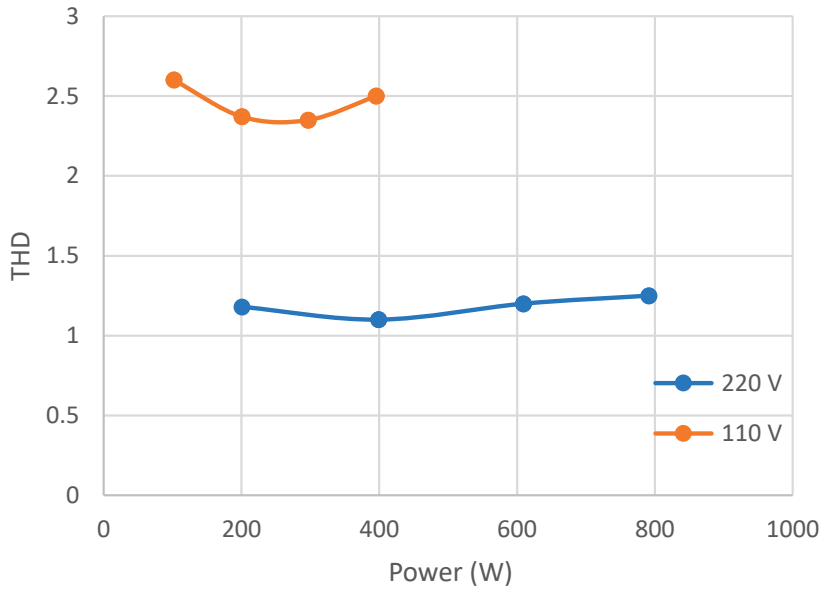

Figure 58. Total harmonic distortion with linear load

5.2.3 Steady State

Figure 59 shows the output voltage and current waveforms with a linear load under a steady state condition at a 110 V_{rms} input.

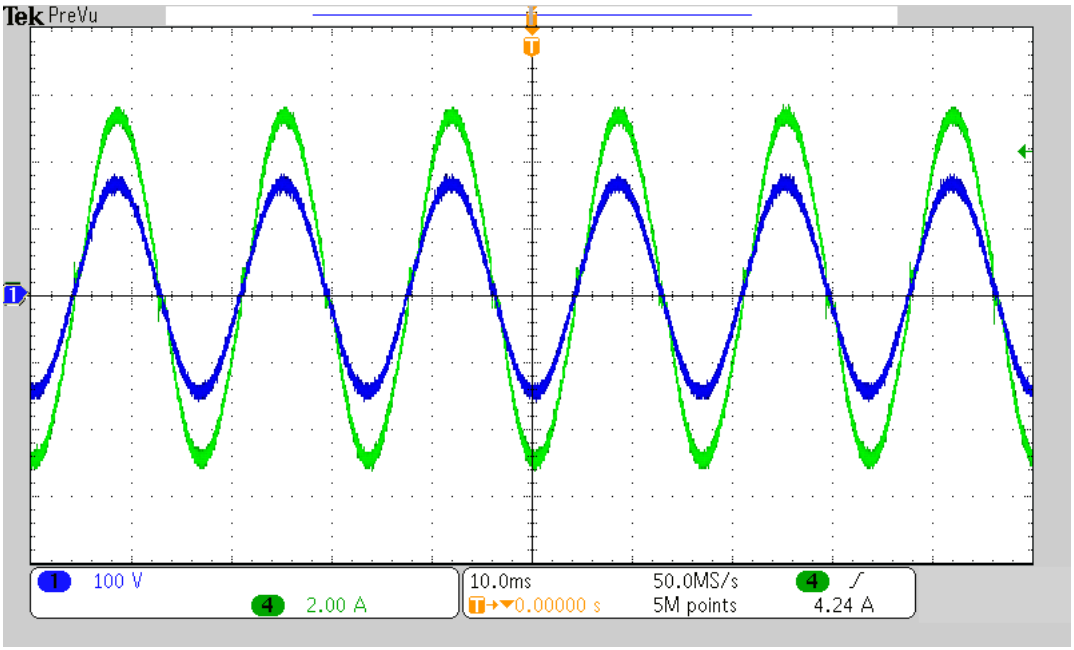

Figure 59. AC output voltage and current with linear load at 110 V_{rms} (CH1: Output voltage, CH4: Output current)

Figure 60 shows the output voltage and current waveforms with a linear load under a steady state condition at a 220 V_{rms} input.

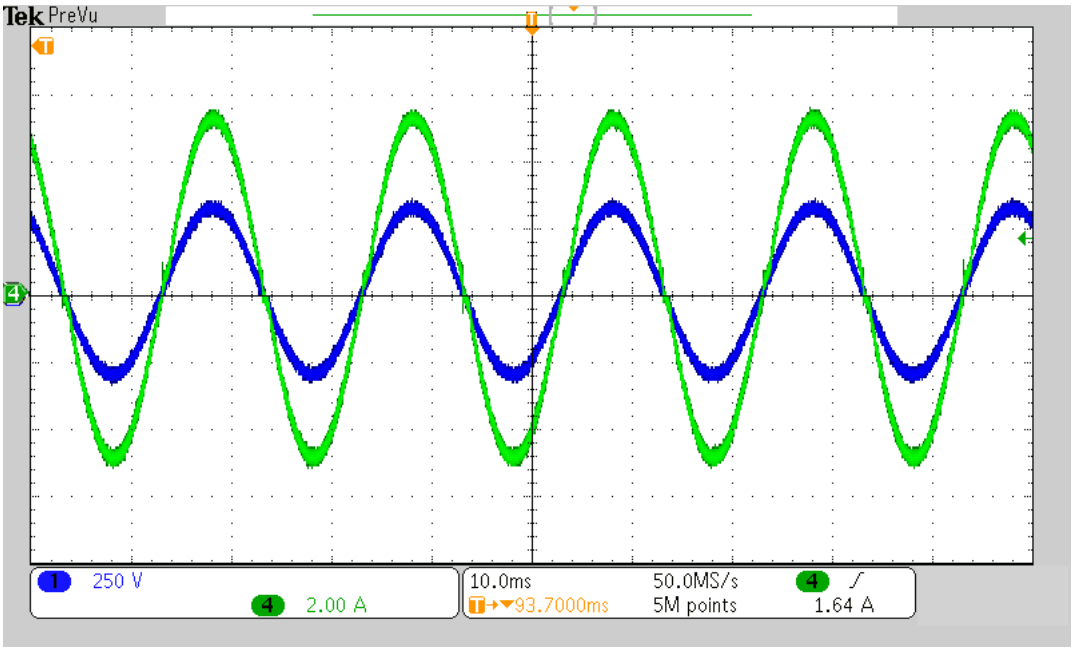

Figure 60. AC output voltage and current with linear load at 220 V_{rms}

5.2.4 Dynamic performance with load change

Figure 61 shows the dynamic performance when the load is added abruptly at a 220 V_{rms} input.

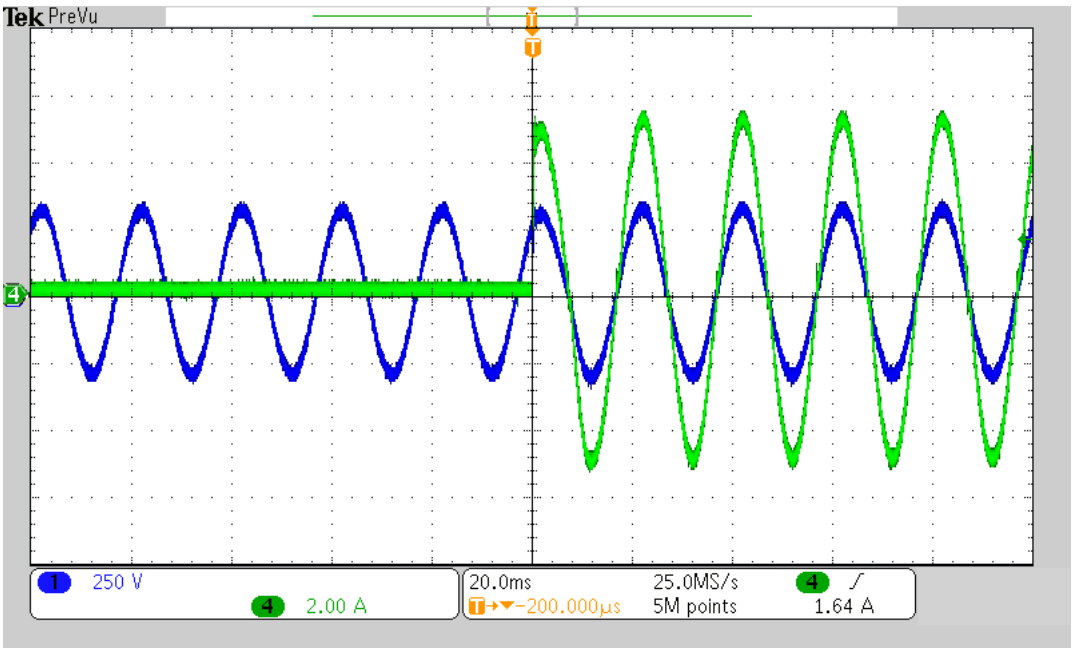

Figure 61. Waveform with load change at 220 V_{rms}

5.3 Grid-connected inverter mode

This section contains the following subsections:

- Section 5.3.1 "Test setup"
- Section 5.3.2 "Steady state"

5.3.1 Test setup

A programmable DC power source is used as the DC voltage input for the grid-connected inverter mode tests. To create the grid-connected inverter mode test setup, follow these steps:

1. Connect the DC power source to the DC port.
2. Connect the grid-connected AC port to a power frequency transformer. The other side of the transformer is connected to the power grid with a transformation ratio of 1:1.
3. Power up the DC source.
4. Start FreeMASTER, open the `Multimode_Bidir_DCAC_LCL_MC56F83783.pmpx` file, and click the **Connect** button.
5. Go to the Bidirectional ACDC converter block. In the Variable Watch window, choose `DC_TO_AC` from the Value drop-down menu of the `gsACDC_Drive.u16WorkModeCmd` command.
6. Choose `GRIDCONNECTED` from the Value drop-down menu of the `gsACDC_Drive.u16InvModeCmd` command.
7. To start/stop the converter, use the Value drop-down menu of the `bACDC_Run` command.

5.3.2 Steady state

Figure 62 shows the steady-state grid voltage and grid current with a 400 W output power at a 220 V_{rms} input.

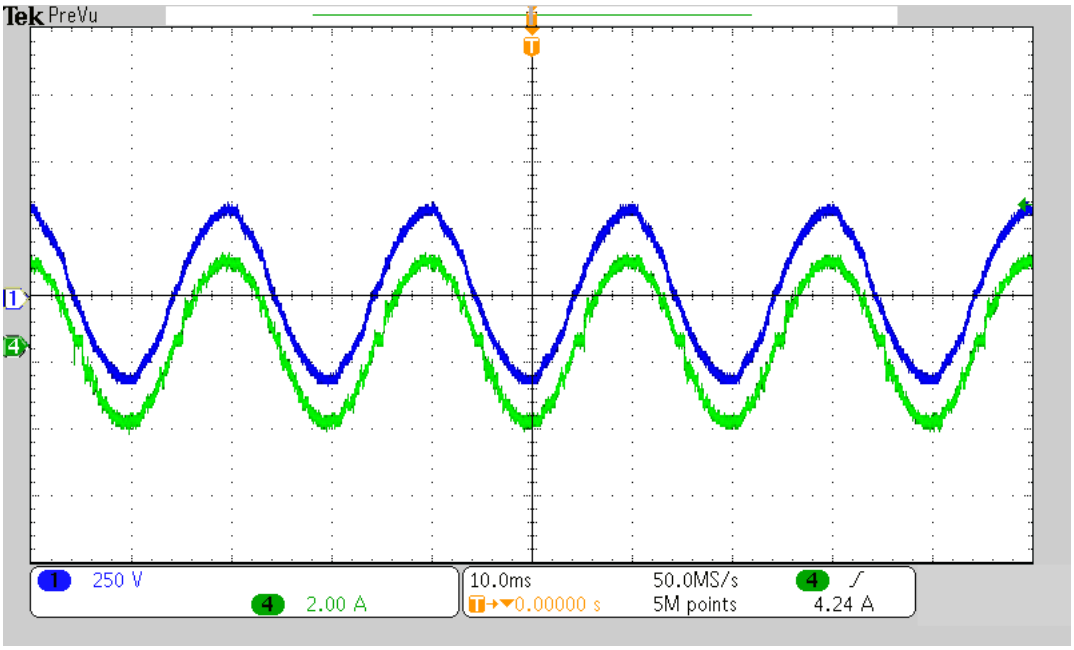

Figure 62. Steady-state waveform with 400 W output (CH1: Grid voltage, CH4: Grid current)

Figure 63 shows the steady-state grid voltage and grid current with an 800 W output power at a 220 V_{rms} input.

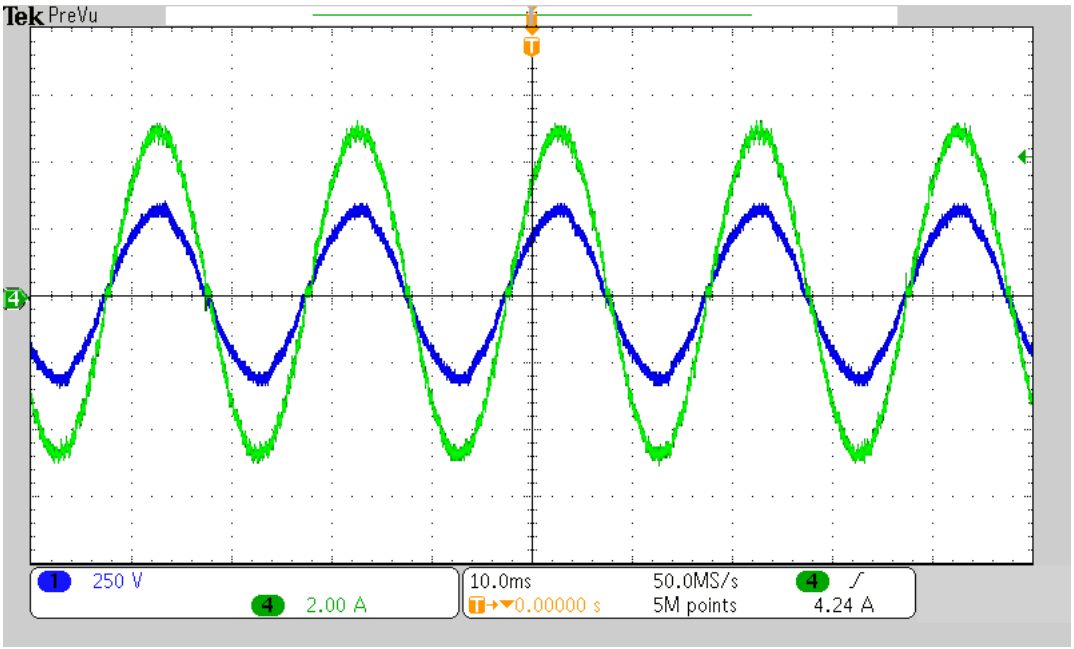

Figure 63. Steady-state waveform with 800 W output

5.4 Mode switching

Note: *When the converter operates in the standalone inverter mode and the grid-connected AC port is connected to the grid, there is a risk that the hardware may get damaged. To avoid the hardware damage, comment out the* `CLOSE_SW_LOAD()` *command in the* `ACDC_TransStopRun` *function.*

5.4.1 Mode switching between PFC and inverter modes

Assuming that the converter first operates in the PFC mode, mode switching can be done as follows:

1. To start the converter in the PFC mode, follow the steps provided in Section 5.1.1.
2. Change the value of the `gsACDC_Drive.u16WorkModeCmd` command in FreeMASTER from `AC_TO_DC` to `DC_TO_AC`. After making this change, the converter stops.
3. Power down the AC power source.
4. Disconnect the AC source from the AC port, and remove the load from the DC port.
5. Connect the DC power source to the DC port and power up the DC source.
   Note: *During this process, the DSC remains powered from the host computer through the USB port.*
6. To choose the desired inverter mode, use the Value drop-down menu of the `gsACDC_Drive.u16InvModeCmd` command in the Variable Watch window of the Bidirectional ACDC converter block.
7. To start the converter, use the Value drop-down menu of the `bACDC_Run` command.

5.4.2 Mode switching between standalone and grid-connected inverter modes

Assuming that the converter first operates in the standalone inverter mode, mode switching to the grid-connected inverter mode can be done as follows:

1. Connect the DC power source to the DC port.
2. Connect the grid-connected AC port to a power frequency transformer. Connect the other side of the transformer to a power grid with a transformation ratio of 1:1.
3. Power up the DC source.
4. Start FreeMASTER.
5. Choose `DC-TO-AC` from the Value drop-down menu of the `gsACDC_Drive.u16WorkModeCmd` command. Also, choose `OFFGRID` from the Value drop-down menu of the `gsACDC_Drive.u16InvModeCmd` command.
6. Start the converter.
7. When the converter is working, choose `GRIDCONNECTED` from the Value drop-down menu of the `gsACDC_Drive.u16InvModeCmd` command. The converter mode changes automatically from the standalone inverter mode to the grid-connected inverter mode. Figure 64 shows the waveform of the mode switching.

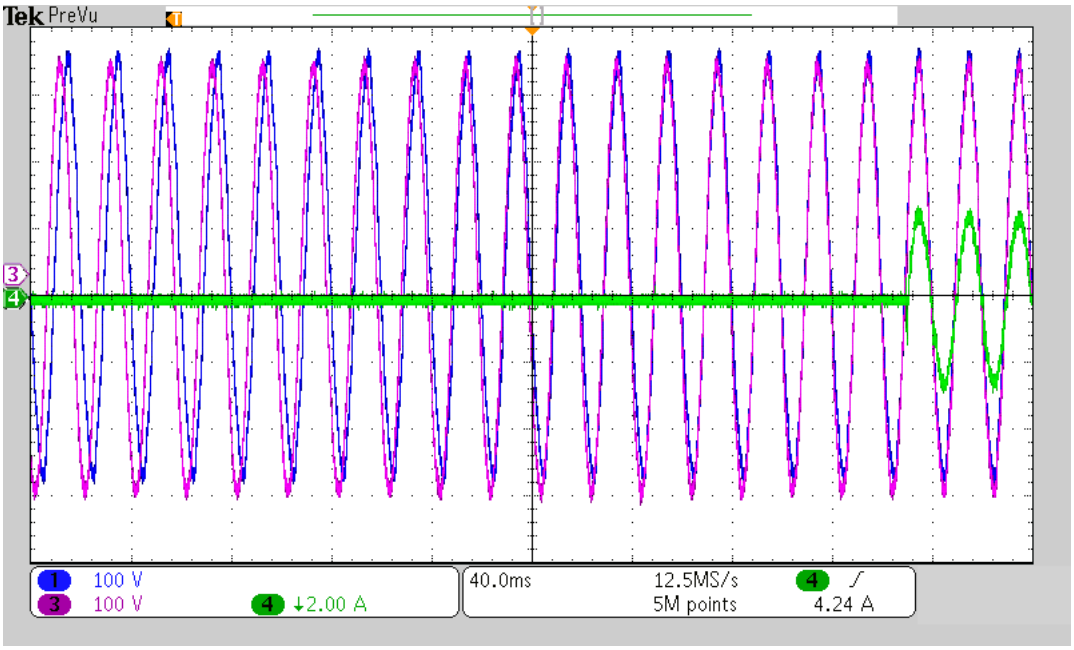

Figure 64. Switching waveform of standalone to grid-connected inverter mode (CH1: Grid voltage, CH3: Inverter output voltage, CH4: Grid current)

8. When the converter is working, choose `OFFGRID` from the Value drop-down menu of the `gsACDC_Drive.u16InvModeCmd` command. The converter mode changes automatically from the grid-connected inverter mode to the standalone inverter mode. Figure 65 shows the waveform of the mode switching.

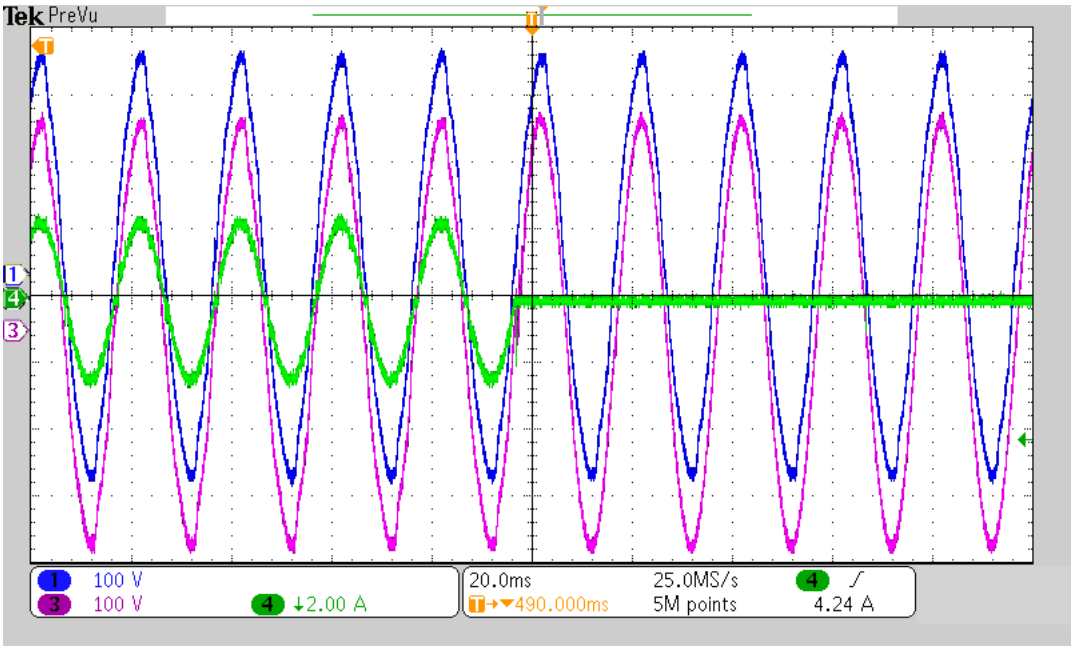

Figure 65. Switching waveform of grid-connected to standalone inverter mode

6 References

For more information on the AC-DC converter design using MC56F83783, refer to the following documents:

- *DSP56800E and DSP56800EX Reference Manual* (DSP56800ERM)
- *MC56F83xxx Reference Manual* (MC56F83XXXRM)
- *Bidirectional AC-DC Converter Design using MC56F83783* (AN14061)

7 Acronyms

Table 2 lists the acronyms used in this document.

Table 2. Acronyms

Acronym	Description
AC	Alternating current
ADC	Analog-to-Digital Converter
CAN	Controller area network
CCM	Continuous current mode
CRM	Critical current mode
DAC	Digital-to-Analog Converter
DC	Direct current
DCM	Discontinuous current mode
DMA	Direct memory access
DSC	Digital signal controller
DSP	Digital signal processor/processing
ECC	Error correcting code
eFlexPWMA	Enhanced Flexible Pulse Width Modulator A
EMI	Electromagnetic interference
EVTG	Event Generator
FD	Flexible data rate
HSCMP	High-Speed Comparator
I2C	Inter-Integrated Circuit
IGBT	Insulated-gate bipolar transistor
ISR	Interrupt service routine
iTHD	Total harmonic distortion in current
LCL	Inductor-capacitor-inductor
LDO	Low dropout
LIN	Local Interconnect Network
MCU	Microcontroller unit
OBC	Onboard charger
OpAmp	Operational amplifier

Table 2. Acronyms...*continued*

Acronym	Description
PFC	Power factor correction
PI	Proportional integral
PLL	Phase-locked loop
PR	Proportional resonant
PWM	Pulse width modulation/modulator
RAM	Random-access memory
RMS	Root mean square
ROM	Read-only memory
RTCESL	Real-time control embedded software libraries
SCI	Serial Communication Interface
SF	Signed fractional
SMBus	System Management Bus
SPI	Serial Peripheral Interface
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion
TRIAC	Triode for alternating current
UART	Universal Asynchronous Receiver / Transmitter
USB	Universal Serial Bus
XBAR	Crossbar switch

8 Revision history

Table 3 summarizes the revisions to this document.

Table 3. Revision history

Document ID	Release date	Description
AN14354 v.1.0	30 August 2024	Initial public release

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