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Revisions			
Rev	Description	Date	Approved
A	Initial release	AUG 24 2024	Jonson Chen
A1	1.Change PFC Current Sample isolation using HCNR201-500E replace AMC1351DWVR 2.Fix Connection of ENC_IND	SEP 10 2024	Jonson Chen
A2	1.AGND Link to GND by L5, Remove C48 For ISP 2.Fix Net Lable P3_7/PWM0_B3-PFC_BT 3.Delete D3, Add MCU Power LED,ADD L6, D2, J12 4.Exchange PFC Sample Pin with Temp_IPM and U_DCB, Exchange P2_3 and P2_6 for MC3_I_DCB 5.Exchange P3_21/SMART_P21-MC3_PWM_BT P3_22/SMART_P22-MC3_PWM_BB PIN On J8 6.Exchange Function of P1_4 P1_5 For CMBD	March 10 2025	Jonson Chen

X-MCXA34X-3MC

High-Voltage Development Platform Controller Card, MCXA346 MCU



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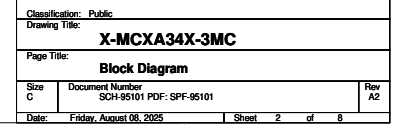
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Rev
A2

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Friday, August 08, 2025

Sheet
1 of 8

The diagram illustrates the functional block architecture of the MCXA346VLL system. It features a central blue block labeled **MCXA346VLL**. Above this block is a green **MCULink** block, connected via **SWD** and **McULink VCOM** lines. To the left of the MCXA346VLL block are four external interfaces: **I2C/Uart**, **Digital IO**, **Lvpmsm motor2 2X10 2.0MM Interface**, and **Lvpmsm motor3 2X10 2.0MM Interface**, each connected to the MCXA346VLL block via bidirectional blue arrows. The MCXA346VLL block contains internal components: **LPUART1 LPI2C0**, **PWM1/ADC1**, and **PWM1/ADC1/CTIME**. To the right of the MCXA346VLL block is a yellow **Isolation** block, which is connected to the MCXA346VLL block via bidirectional yellow arrows for **PWM0**, **ADC0**, and **LPUART3**. The Isolation block is also connected to a **FreeMaster** block via bidirectional yellow arrows. Above the Isolation block is a red **V_ISO** block, which is connected to the MCXA346VLL block via a **3.3V_ISO** line and to the Isolation block via a **5V_ISO** line. The V_ISO block is also connected to a **5V_PCI** line. The Isolation block is connected to a **FreeMaster** block via bidirectional yellow arrows. The entire system is connected to a **PCI** block via a **PFC/PWM Interface**.



ISO Power

Galvanic isolated part. Isolation = 8mm
Creepage and clearance (5kV)

Galvanic non-isolated part. Isolation = 8mm
Creepage and clearance (5kV)

Galvanic non-isolated part. Isolation = 8mm
Creepage and clearance (5kV)

The diagram illustrates the power distribution and isolation for a system. Key components and connections include:

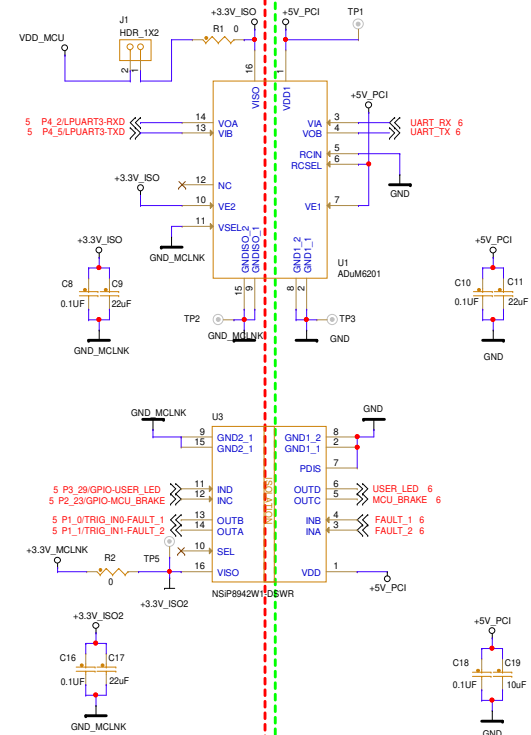
- Galvanic Isolated Part:**
 - VDD_MCU connected to +3.3V_LVPM5M via L7 (220 Ohm).
 - GND_MCLNK connected to +3.3V_ISO via J1 (HDR_1X2) and R1.
 - +3.3V_ISO connected to +3.3V_LVPM5M via L6 (220 Ohm).
 - Capacitors C8 (0.1uF) and C9 (22uF) are connected to +3.3V_ISO and GND_MCLNK.
- Galvanic Non-Isolated Part (Left):**
 - U1 (ADuM201) is connected to +3.3V_ISO, GND_MCLNK, and +5V_PCI.
 - Capacitors C10 (0.1uF) and C11 (22uF) are connected to +5V_PCI and GND.
- Galvanic Non-Isolated Part (Right):**
 - U3 (NSIP8942W1D5WR) is connected to GND_MCLNK, +3.3V_ISO2, +3.3V_ISO2, and +5V_PCI.
 - Capacitors C16 (0.1uF) and C17 (22uF) are connected to +3.3V_ISO2 and GND_MCLNK.
 - Capacitors C18 (0.1uF) and C19 (10uF) are connected to +5V_PCI and GND.

Galvanic isolated part. Isolation = 8mm
Creepage and clearance (5kV)

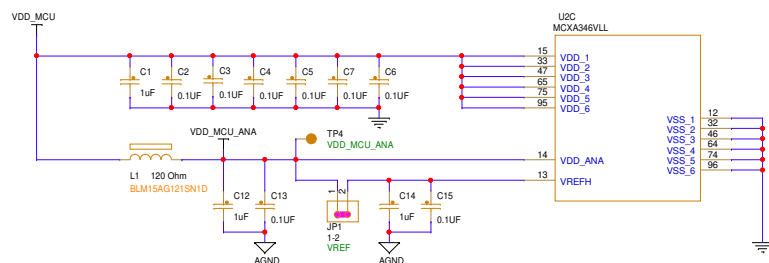


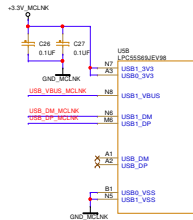
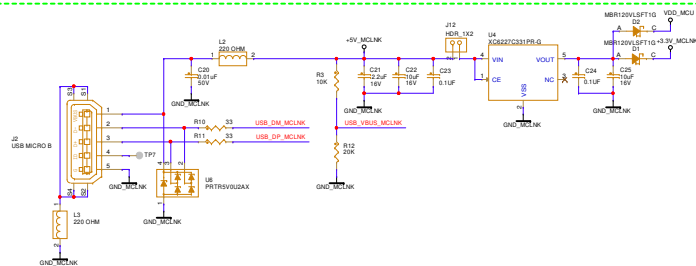
Galvanic non-isolated part. Isolation = 8mm
Creepage and clearance (5kV)

Galvanic non-isolated part. Isolation = 8mm
Creepage and clearance (5kV)



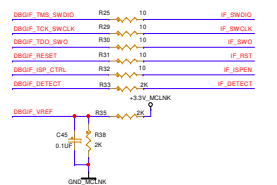
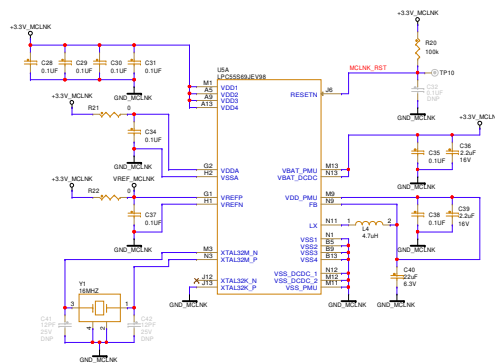
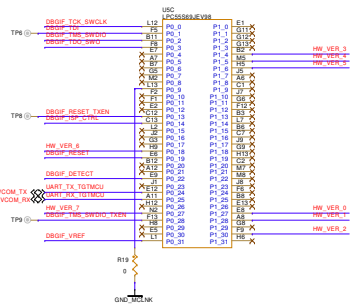
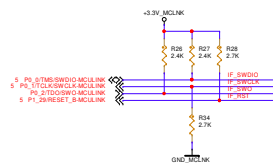
VDD_MCU  +3.3V_LVPM5V



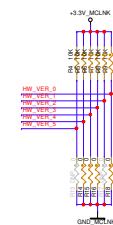


Galvanic isolated part. Isolation = 8mm
Creepage and clearance (5kV)

Galvanic non-isolated part. Isolation = 8mm
Creepage and clearance (5kV)



Items	Description	OB setting
HW_VER_0	Power negotiation when low	0
HW_VER_1	Reserved	1
HW_VER_2	USARTIO bridge disabled / not present when 0	0
HW_VER_3	OB (0) / Pro (1) type select	0
HW_VER_4	Board identity code used (when low)	0
HW_VER_5	Power measurement enabled/present when low	1
HW_VER_6	VCOM disabled when low	1
HW_VER_7	SWD debug disabled when low	1

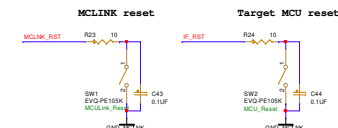
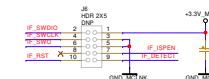


HW_VER_6 1 VCOM disabled

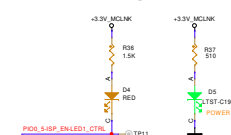
HW_VER_7 1 SWD disabled

POB_S-ISP_ENABLED1_CTRL 1 MCLK Enable ISP mode
Open: Boot from internal FLASH
Closed: Enable ISP mode (USB or UART)

Target MCU SWD interface



LED: SWD activity



IN CIRCUIT TEST GND PROBING



4 P0_0TMS/SWDIO-MCULINK
4 P0_1TCLK/SWCLK-MCULINK
4 P0_2TDO-MCULINK_VCOM_B
4 P0_3TDMCULINK_VCOM_TX
5 P0_6ISPMODE-N-MCULINK
8 P0_16LP2C0_SDA
8 P0_17LP2C0_SCL
7 P0_18ADC0_A8-PFC - L_pfc1
7 P0_18ADC0_A8-PFC - L_pfc2
6 P0_20ADC0_A10-MC1 - L_pfcA
6 P0_21ADC0_A11-MC1 - L_pfcB
6 P0_22ADC0_A12-MC1 - L_pfcC
6 P0_23ADC0_A13-MC1_CURD_C0
3 P1_0TRIG_IN0-FAULT_1
3 P1_1TRIG_IN1-FAULT_2
8 P1_2GPIO_Digital0
7 P1_3ADC0_A19-V_in
8 P1_4CMP0_IN2-MC2-FAULT
6 P1_5ADC0_A21-MC1_VOLT_DCB
6 P1_6ADC0_A22-MC1_Temp_IPM
7 P1_7AD01_A23-MC1-TA
8 P1_8LPUART1_RXD
8 P1_9LPUART1_TXD
8 P1_10ADC0_A8-MC2 - L_pfcA
8 P1_11ADC0_A9-MC2 - L_pfcB
8 P1_12ADC0_A10-MC2 - L_pfcC
8 P1_13ADC0_A11-MC2_VOLT_DCB
8 P1_14ADC0_A12-MC2_CURD_C0
8 P1_15ADC0_A13-MC3 - L_pfcA
4 P1_26RESET_B-MCULINK
5 P1_30XTAL48M-CLOCK
5 P1_31XTAL48M-CLOCK
8 P2_0TRIG_IN6-MC2_ENC_I
8 P2_1ADC1_A4-MC3 - L_pfcB
8 P2_2DAC_OUT
8 P2_3ADC1_A4-MC3_CURD_C0
8 P2_4GPIO_Digital0
8 P2_5ADC1_A1-MC3 - L_pfcC
8 P2_6GPIO_Digital0
8 P2_7VFE1
8 P2_10GPIO_Digital0
8 P2_11GPIO_Digital0
35.57 AGND
6 P2_13OPAMP0_INN
6 P2_15OPAMP0_OUT
35.57 AGND
6 P2_17OPAMP1_INN
6 P2_19OPAMP1_OUT
7 P2_20TRIG_IN6-MC1_ENC_A
7 P2_21TRIG_IN6-MC1_ENC_B
3 P2_23GPIO4MCU_BRAKE
8 P2_24GPIO_Digital0
5 P2_25GPIO-RED
8 P2_26GPIO_Digital0

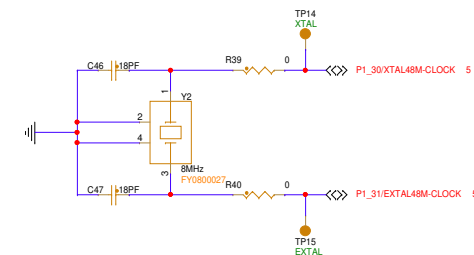
U2A
MCXA346VLL

P0_0TMS/SWDIO-LPUART0_CTS_BLPSP0_PCS2CT0_INP0
P0_1TCLK/SWCLK-LPUART0_CTS_BLPSP0_SDVCT_INP1
P2_0ADC0_A8/TDO/SWOL-LPUART0_RXD-LPSP0_SCK/CT0_MAT0UTICK_CAP0
P0_3CMP1_INV-ADC0_A14/LPUART0_TXD-LPSP0_SDO/CT0_MAT1UTICK_CAP1CMP1_OUT
P0_6ISPMODE_N-ADC0_A15/ISPMODE_N-LP2C0_HREQ-LPSP0_PCS1CT_INP2-SMARTDMA_PIO2CMP1_OUT/CLKOUT-ADC1_CONV_CLK
P1_14ADC2_A14CT_INP2UTICK_CAP0SMARTDMA_PIO4
P1_15ADC2_A15CT_INP3UTICK_CAP1SMARTDMA_PIO5
P1_16NVMM_TMO-LP2C0_SDA-LPSP0_PCS2CT0_MAT0UTICK_CAP2SMARTDMA_PIO6ADC1_CONV_DATA0_WU00_IN2
P1_17NVMM_TMO-LP2C0_SCL-LPSP0_PCS3CT0_MAT1UTICK_CAP3SMARTDMA_PIO7ADC1_CONV_DATA1
P1_18ADC0_A8/LP2C0_SCL-SCT0_MAT2SMARTDMA_PIO8CMP2_OUT
P1_19ADC0_A9/LP2C0_SDA-SCT0_MAT3SMARTDMA_PIO9CMP1_OUT_WU00_IN3
P1_20ADC0_A10/LPUART0_RXD/CT_INP0SMARTDMA_PIO10CMP2_OUT_WU00_IN4
P1_21ADC0_A11/LPUART0_TXD/CT_INP1SMARTDMA_PIO11
P1_22ADC0_A12/LPUART0_RTS_B/CT_INP2CT0_MAT0SMARTDMA_PIO12
P1_23ADC0_A13CMP2_IN2/LPUART0_CTS_B/CT_INP3CT0_MAT1SMARTDMA_PIO13WU00_IN5
P1_0SPI_SDO-ADC0_A16CMP0_IN3TRIG_IN0-LPSP0_SDO-LP2C1_SDACT_INP4CT0_MAT2PLL0_CLKOUT/TP_DATA0_WU00_IN6LPTMR0_ALT3
P1_1SPI_SCK-ADC0_A17CMP1_IN3TRIG_IN1-LPSP0_SCK-LP2C1_SCLCT_INP5CT0_MAT3FRO12M_CLKOUT/TP_DATA1
P1_2SPI_SDA-ADC0_A18CMP2_IN3TRIG_OUT0-LPSP0_SDA-LP2C1_SDA-SCT1_MAT0CT_NPVCAN0_TXD/TP_DATA2
P1_3SPI_PCS-ADC0_A19CMP0_IN1TRIG_OUT1-LPSP0_PCS0-LP2C1_SCL-SCT1_MAT1CT_INP1CAN0_RXD/FRO18M_CLKOUT/TP_DATA3_WU00_IN7
P1_4ADC0_A20CMP0_IN2FREQME_CLK_IN-LPSP0_PCS3/LPUART2_TXD/CT1_MAT2SMARTDMA_PIO0ADC1_CONV_DATA5_WU00_IN8
P1_5ADC0_A21CMP1_IN2FREQME_CLK_IN-LPSP0_PCS0/LPUART2_TXD/CT1_MAT3SMARTDMA_PIO1ADC1_CONV_DATA3
P1_6ADC0_A22NVMM_TMO2TRIG_OUT2-LPSP0_PCS1/LPUART2_RTS_B/CT_INP6CT4_MAT0SMARTDMA_PIO2ADC1_CONV_DATA4
P1_7ADC0_A23NVMM_TMO3TRIG_OUT2-LPUART2_CTS_B/CT_INP7CT4_MAT1SMARTDMA_PIO3ADC1_CONV_DATA5_WU00_IN9
P1_8I2C_SDA-FREQME_CLK_IN-LPUART1_RXD-LP2C2_SDA/CT_INP8CT0_MAT2SMARTDMA_PIO4TP_HTRANS_WU00_IN10
P1_9I2C_SCL-FREQME_CLK_IN-LPUART1_TXD-LP2C2_SCL/CT_INP9CT0_MAT3SMARTDMA_PIO5TP_HWRITE
P1_10ADC1_A8/LPUART1_RTS_BLP2C2_SDA-SCT2_MAT0SMARTDMA_PIO6/LPUART5_TXD/CAN0_TXD/ADC1_CONV_DATA7_WU00_IN11
P1_11ADC1_A9/TRIG_OUT0-LPUART1_CTS_BLP2C2_SCL-SCT2_MAT1SMARTDMA_PIO7/LPUART5_RXD/CAN0_RXD/ADC1_CONV_DATA7_WU00_IN11
P1_12ADC1_A10/LP2C1_SDA-LPUART2_RXD/CT2_MAT2SMARTDMA_PIO8/LPUART5_CTS_B_WU00_IN12
P1_13ADC1_A11/LP2C1_SDA-LPUART2_TXD/CT2_MAT3SMARTDMA_PIO9/LPUART5_RTS_B
P1_14ADC1_A12/LP2C1_SCL-S/LPUART2_RTS_B/CT3_MAT0SMARTDMA_PIO10
P1_15ADC1_A13/LP2C1_SDA-S/LPUART2_CTS_B/CT3_MAT1SMARTDMA_PIO11/WU00_IN13
P1_26RESET_B/SPI_LPTMR0
P1_30XTAL48M/TRIG_OUT3-LP2C0_SDA/CT_INP16
P1_31XTAL48M/TRIG_IN4-LP2C0_SCL/CT_INP17
P2_0ADC0_A0/OPAMP2_INP/TRIG_IN6/LPUART0_RXD/LPUART4_CTS_B/CT_INP16/CT2_MAT0SMARTDMA_PIO24WU00_IN18
P2_1ADC1_A0/OPAMP2_INN/TRIG_IN7/LPUART0_TXD/LPUART4_RTS_B/CT_INP17/CT2_MAT1SMARTDMA_PIO25
P2_2UART_RXD-ADC0_A4/CMP0_IN0/ADC2_INN/TRIG_IN8/LPUART0_RTS_B/LPUART2_TXD/CT_INP12/CT2_MAT2SMARTDMA_PIO26
P2_3UART_RXD-ADC0_A3/CMP1_IN0/ADC1_A4/TRIG_IN7/LPUART0_CTS_B/LPUART2_RXD/CT_INP13/CT2_MAT3SMARTDMA_PIO27NVMM_SDO/WU00_IN19
P2_4ADC0_A1/ADC2_A0/CMP2_IN0/LPUART2_CTS_B/CT_INP14CT1_MAT0SMARTDMA_PIO28
P2_5ADC1_A1/ADC3_A0/LPUART2_RTS_B/CT_INP15CT1_MAT1SMARTDMA_PIO29
P2_6ADC1_A3/ADC2_A0/OPAMP2_OUT/CMP2_INP4/TRIG_OUT4-LPSP1_PCS1/LPUART4_RXD/CT_INP18/CT1_MAT2SMARTDMA_PIO30
P2_7VREF-ADC0_A7/ADC1_A7/ADC2_A7/ADC3_A7/TRIG_IN5/LPUART4_TXD/CT_INP19CT1_MAT3SMARTDMA_PIO31TP_HREADY
P2_10ADC2_A1/TRIG_OUT5-LPUART2_TXD/CT3_MAT2SMARTDMA_PIO14
P2_11ADC3_A1/TRIG_IN4/LPUART2_RXD/CT3_MAT3SMARTDMA_PIO15
P2_12ADC0_A5/ADC2_A0/OPAMP0_INP/LPSP1_SCK/LPUART1_RXD/CT1_MAT0SMARTDMA_PIO16/CAN0_RXD/WU00_IN20
P2_13ADC1_A5/ADC3_A0/CMP0_INN/TRIG_IN5/LPSP1_SCK/LPUART1_TXD/CT1_MAT1CT0_MAT1SMARTDMA_PIO17/CAN0_TXD
P2_15OPAMP0_OUT/ADC0_A2/CMP0_INP4/TRIG_OUT4-LPSP1_SDA/LPUART1_RTS_B/CT4_MAT3CT0_MAT2SMARTDMA_PIO18WU00_IN21
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P2_21ADC3_A6/OPAMP3_INN/TRIG_IN5/LPSP1_PCS3/CT2_MAT1SMARTDMA_PIO23
P2_23ADC3_A2/OPAMP3_OUT/CMP0_INN4/TRIG_OUT5/CT2_MAT3
P2_24ADC2_A3/TRIG_OUT/CT_INP6
P2_25ADC3_A3/TRIG_OUT/CT_INP9
P2_26/TRIG_IN5/CT_INP10

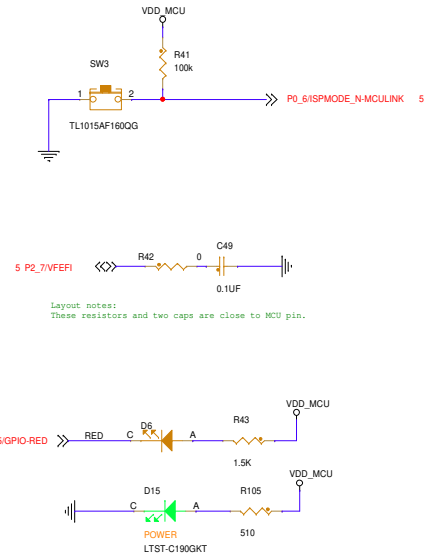
U2B
MCXA346VLL


7 P3_0PWM0_A0-MC1_PWM_AT
7 P3_1PWM0_B0-MC1_PWM_AB
7 P3_3PWM0_A3-PFC_AT
7 P3_3PWM0_B3-PFC_BT
7 P3_3PWM0_A1-MC1_PWM_BT
7 P3_3PWM0_B1-MC1_PWM_BB
7 P3_3PWM0_A2-MC1_PWM_CT
7 P3_11PWM0_B2-MC1_PWM_CB
8 P3_12PWM1_A2-MC2_PWM_CT
8 P3_13PWM1_B2-MC2_PWM_CB
8 P3_14PWM1_A1-MC2_PWM_BT
8 P3_15PWM1_B1-MC2_PWM_BB
8 P3_16PWM1_A2-MC2_PWM_AT
8 P3_17PWM1_B2-MC2_PWM_AB
7 P3_18GPIO-RALY
8 P3_19SMART_P16-MC3_PWM_CT
8 P3_20SMART_P20-MC3_PWM_CB
8 P3_21SMART_P21-MC3_PWM_BT
8 P3_22SMART_P22-MC3_PWM_BB
8 P3_27PWM1_A3-MC3_PWM_AT
8 P3_28PWM1_B3-MC3_PWM_AB
3 P3_29GPIO-USER_LED
8 P3_30ADC1_A21-MC3_VOLT_DCB
7 P3_31TRIG_IN10-MC1_ENC_I
P4_2/ADC2_A18/CLKOUT-LP2C2_SDA-S/LPUART3_RXD/CT4_MAT0PWM0_A2SMARTDMA_PIO22WU00_IN16
P4_3/ADC2_A19/LP2C2_SCL-LPUART4_TXD/CT4_MAT1PWM0_B2SMARTDMA_PIO23
P4_4/ADC2_A20/LP2C2_SDA-LPUART4_RXD/CT4_MAT2PWM0_A1SMARTDMA_PIO24WU00_IN17
P4_5/ADC2_A21/TRIG_OUT3-LP2C2_SCL-S/LPUART3_TXD/CT4_MAT3PWM0_B1SMARTDMA_PIO25
P4_6/ADC2_A22/TRIG_IN4-LP2C2_HREQ-LPUART3_CTS_B/CT_INP6PWM0_A0SMARTDMA_PIO26
P4_7/ADC2_A23/TRIG_IN5-LPUART3_RTS_B/CT_INP7PWM0_B0SMARTDMA_PIO27

MCU CLOCK

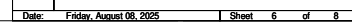


ISP

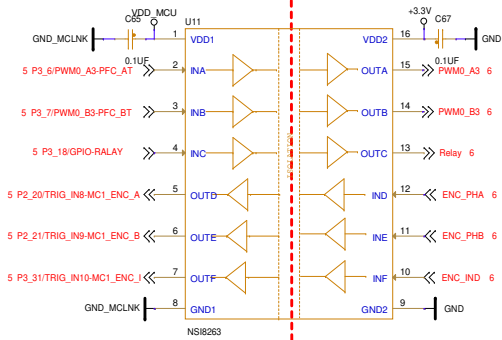
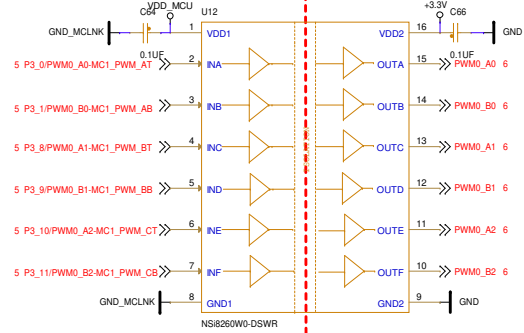




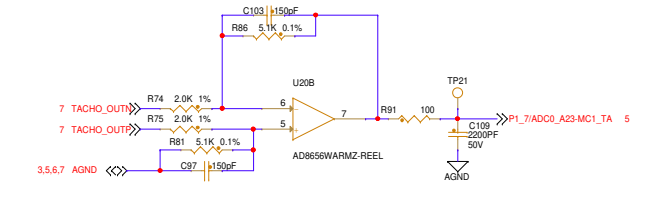
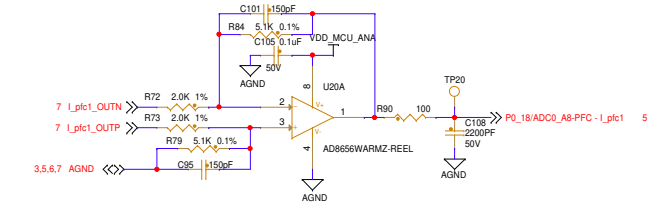
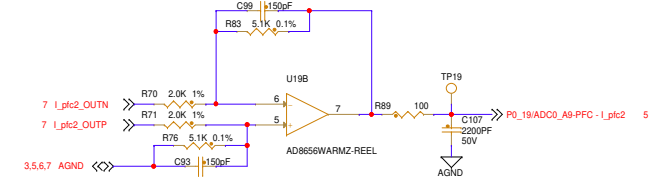
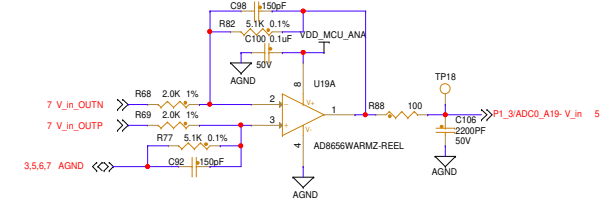
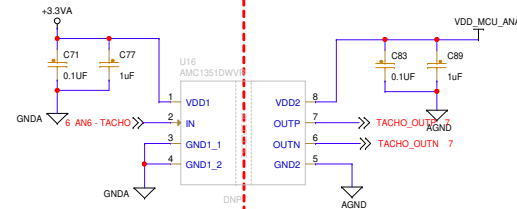
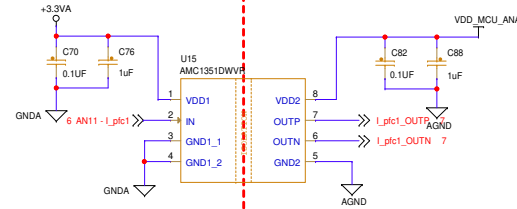
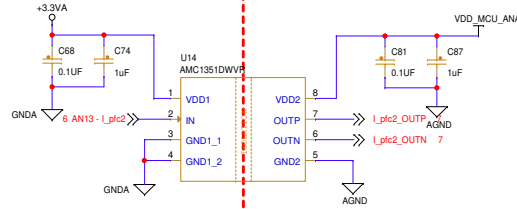
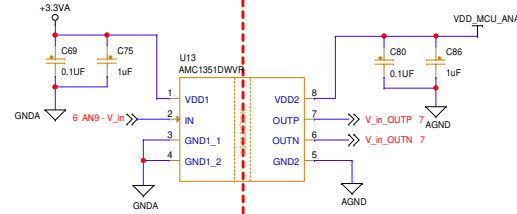
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Size C Document Number SCH-95101 PDF: SPF-95101
Date: Friday, August 08, 2025 Sheet 5 of 8



DIGITAL ISOLATION

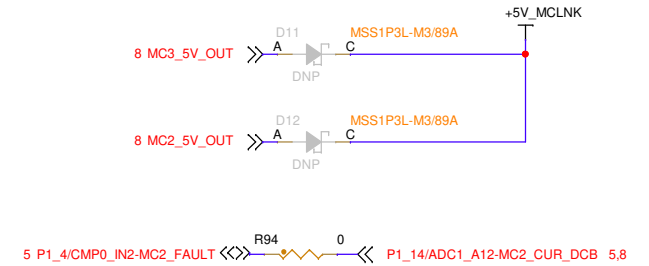
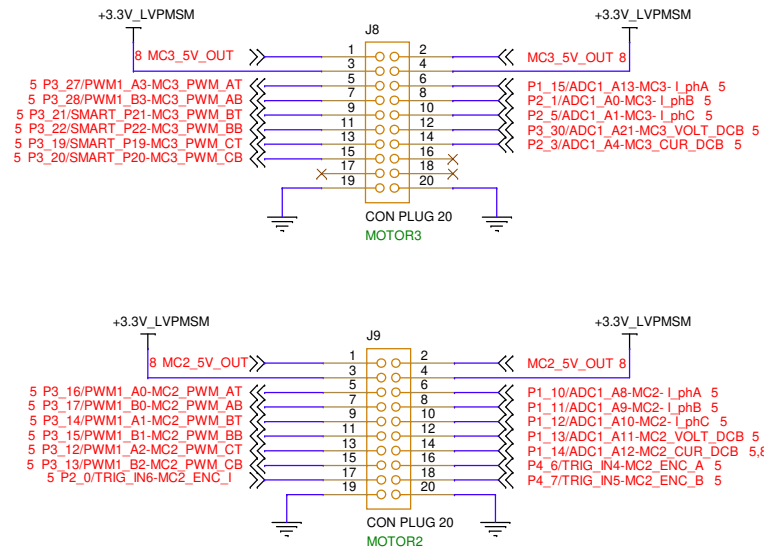


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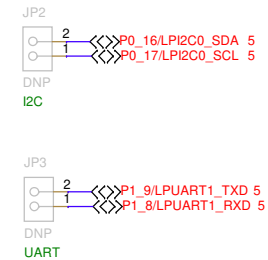
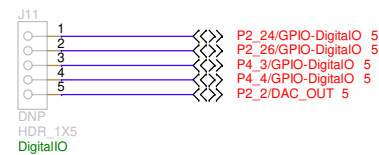
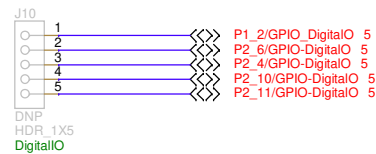


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Size C	Document Number SCH-95101 PDF: SPF-95101	Rev A2
Date: Friday, August 08, 2025	Sheet 7 of 8	

LV Motor Interface



DigitalIO



Classification: Public
Drawing Title:

X-MCXA34X-3MC

Page Title:
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