Mnemonic	Type	Perf ID	Description
BRANCHES_MISPREDICTED	Core	F	Counts branch instructions mispredicted for any reason, target (for example if the CTR contents change), or IAB prediction. Does not count instructions that the branch predictor incorrectly
BTB_HITS_AND_PSEUDO_HITS	Core	11	Branch instructions that hit in the BTB or miss in the
CACHE_INHIBITED_ACCESSES_TRA	Core	1F	Cache inhibited accesses translated
CACHEOPS_TRANSLATED	Core	1A	dcba, dcbf, dcbst, and dcbz instructions translated.
CRITICAL_INPUT_INTERRUPTS_TAK	Core	56	Critical input interrupts
CYCLES_DECODE_STALLED	Core	12	Cycles the IQ is not empty but 0 instructions decoded.
CYCLES_ISSUE_STALLED	Core	13	Cycles the issue buffer is not empty but 0 instructions
DATA_L1_CACHE_CASTOUTS	Core	2A	#N/A
DATA_L1_CACHE_RELOADS	Core	29	Counts cache reloads for any reason. Typically used to determine data cache miss rate (along with
DATA_LINE_FILL_BUFFER_LOAD_M	Core	4C	Instances when the number of cycles between a load
DATA_MMU_BUSY	Core	31	Counts number of stalls
DATA_MMU_BUSY_CYCLES	Core	39	Data MMU Busy stall cycles
DATA_MMU_MISS	Core	30	Counts number of stalls
DATA_MMU_MISS_CYCLES	Core	38	Data MMU miss stall cycles
DATA_MMU_TLB4K_RELOADS	Core	40	Counts reloads in the level 1 data MMU TLB4K. A reload in the level 2 MMU TLB4K is not counted.
DATA_MMU_VSP_RELOADS	Core	41	Counts reloads in the level 1 data MMU VSP
EXTERNAL_INPUT_INTERRUPTS_TAKEN	Core	57	External input interrupts taken
GUARDED_LOADS_TRANSLATED	Core	20	Guarded loads translated
IAC1S_DETECTED	Core	8C	Every valid IAC1 detection
IAC2S_DETECTED	Core	8D	Every valid IAC2 detection
INSTR_COMPLETED	Core	2	Completed instructions. 0, 1, or 2 per cycle
INSTR_L1_RELOADS	Core	3C	L1 Instruction cache reloads.
INSTRUCTION_FETCHED	Core	4	Fetched instructions. 0, 1, 2, 3, or 4 per cycle. (instructions written to the IQ.)

Mnemonic	Type	Perf ID	Description
INSTRUCTION_MMU_TLB4K_RELOADS	Core	3E	Counts reloads in the level 1 instruction MMU TLB4K. A reload in the level 2 MMU TLB4Kis not counted.
INSTRUCTION_MMU_VSP_RELOAD	Core	3F	Counts reloads in the level 1 instruction MMU VSP. A
L2_CACHE_ACCESSES	Core	6E	L2 cache Accesses Included: load/store/fetch/dcba/dcbz/dcblc CT=1/icblc
L2_DATA_ACC	Core	70	Data accesses to L2 Cache
L2_DATA_HITS	Core	71	Data hits to L2 Cache
L2_INSTR_ACC	Core	72	Instruction accesses to L2 Cache
L2_INSTR_HITS	Core	73	Instruction hits to L2 Cache
L2MMU_MISSES	Core	42	Counts instruction TLB/data TLB error interrupts BIU Interface Usage
LOAD_GUARDED_MISS_WHEN_THE_LOAD_IS_NOT_YET_AT_THE_BOTTOM_OF_THE_CQ	Core	35	Counts number of stalls. Load guarded miss stalls when the load is not yet at the bottom of the cq.
LOAD_GUARDED_MISS_WHEN_TH	Core	2D	Load guarded miss stall cycles when the load is not
LOAD_MISS_WITH_DLFB_FULL	Core	2B	Counts number of stalls
LOAD_MISS_WITH_DLFB_FULL_CYCLES	Core	33	Load miss with DLFB full stall cycles
LOAD_MISS_WITH_LOAD_QUEUE_	Core	34	Counts number of stalls
LOAD_MISS_WITH_LOAD_QUEUE_FULL_CYCLES	Core	2C	Load miss with load queue full stall cycles
LOADS_TRANSLATED	Core	1B	Cacheable l* or evl* micro-ops translated. (includes
LOADS_TRANSLATED_AND_ALLOC	Core	24	Applies to same class of instructions as loads
MISALIGNED_LOAD_OR_STORE_AC	Core	22	Misaligned load or store accesses translated.
NUM_FETCHES	Core	3D	Counts fetches that write at least one instruction to
PROC_CYCLES	Core	1	Every processor cycle
SECOND_PART_OF_MISALIGNED_ACCESSWHEN_FIRST_PART_MISSED	Core	32	Counts number of stalls
SECOND_PART_OF_MISALIGNED_A	Core	3A	Stall cycles for second part of misaligned access
SNOOP_HITS	Core	49	Snoop Hits on Data Cache
SNOOP_PUSHES	Core	4A	Snoop pushes from all data-side resources. (Counts snoop ARTRYs and WOPs.)

Mnemonic	Type	Perf ID	Description
SNOOP_REQ	Core	48	Snoop Requests to Data Cache
STASH_ACCESS_HIT	Core	66	Access Hits on Stash DLFB
STASH_HIT_L1	Core	61	Stash Hits in L1
STASH_REQ_L1	Core	6B	Stash Requests to DL1
STASH_REQUESTS	Core	6A	Stash Requests
SYSTEM_CALL_AND_TRAP_INTERRUPTS	Core	59	System call and trap interrupts
TOTAL_ALLOCATED_TO_DLFB	Core	23	Total allocated to DLFB
TOTAL_TRANSLATED	Core	1A	Total of load and store micro-ops that reach the
TOUCHES_TRANSLATED	Core	1D	Cacheable dcbt and dcbtst instructions translated (L1
TOUCHES_TRANSLATED_AND_ALLOCATED_TO_DLFB	Core	26	Applies to same class of instructions as touches translated.
TRANSLATE_A_STORE_WHEN_THE_STORE_QUEUE_IS_FULL	Core	2E	Counts number of stalls for translate a store when the store queue is full.
CYCLES_BRANCH_ISSUE_STALLED	Core	14	Cycles branch issue stalled.
CYCLES_BU_SCHEDULE_STALLED	Core	19	Cycles BU is not empty but 0 instructions scheduled.
CYCLES_LRU_SCHEDULE_STALLED	Core	18	Cycles LRU is not empty but 0 instructions scheduled.
CYCLES_MU_SCHEDULE_STALLED	Core	17	Cycles MU is not empty but 0 instructions scheduled.
TRANSLATE_A_STORE_WHEN_THE_STORE_QUEUE_IS_FULL_CYCLES	Core	36	Stall cycles for translate a store queue is full
SIMPLE_0_READ_CYCLES_DDR1	DDR	A0000000	Counting read access cycles that are returning data from DRAM (each data beat returned from the
SIMPLE_0_READ_CYCLES_DDR2	DDR	A0000100	Counting read access cycles that are returning data from DRAM (each data beat returned from the DRAM)
SIMPLE_1_WRITE_CYCLES_DDR1	DDR	A0000001	Counting write access cycles is sending data to DRAM (each data beat transmitted to the DRAM)
SIMPLE_1_WRITE_CYCLES_DDR2	DDR	A0000101	Counting write access cycles is sending data to DRAM (each data beat transmitted to the DRAM)
SIMPLE_2_FORCED_PAGE_CLOSINGS_NONREFRESH_DDR1	DDR	A0000002	Forced Page Closings not caused by a refresh
SIMPLE_2_FORCED_PAGE_CLOSIN	DDR	A0000102	Forced Page Closings not caused by a refresh
SIMPLE_3_FORCED_PAGE_CLOSIN	DDR	A0000003	Forced Page Closings
SIMPLE_3_FORCED_PAGE_CLOSIN	DDR	A0000103	Forced Page Closings
SIMPLE_4_FORCED_PAGE_CLOSIN	DDR	A0000004	Forced Page Closings due to collision in bank and
SIMPLE_4_FORCED_PAGE_CLOSIN	DDR	A0000104	Forced Page Closings due to collision in bank and

Mnemonic	Type	Perf ID	Description
DDR1_Page_Hit	DDR	C0000000	DDR1 Access with Page Hit (custom configuration by
DDR1_Page_Miss	DDR	C0000001	DDR1 Access with Page Miss (custom configuration by
DDR2_Page_Hit	DDR	C0000002	DDR2 Access with Page Hit (custom configuration by
DDR2_Page_Miss	DDR	C0000003	DDR2 Access with Page Miss (custom configuration by
DDR1_Page_Hit_CORE	DDR	C603E000	DDR1 Access with Page Hit (from Cores)
DDR1_Page_Miss_CORE	DDR	C603E001	DDR1 Access with Page Miss (from Cores)
DDR2_Page_Hit_CORE	DDR	C603E002	DDR2 Access with Page Hit (from Cores)
DDR2_Page_Miss_CORE	DDR	C603E003	DDR2 Access with Page Miss (from Cores)
DDR1_Page_Hit_SEC	DDR	C487FC00	DDR1 Access with Page Hit (from SEC)
DDR1_Page_Miss_SEC	DDR	C487FC01	DDR1 Access with Page Miss (from SEC)
DDR2_Page_Hit_SEC	DDR	C487FC02	DDR2 Access with Page Hit (from SEC)
DDR2_Page_Miss_SEC	DDR	C487FC03	DDR2 Access with Page Miss (from SEC)
DDR1_Page_Hit_DMA	DDR	C5C3F800	DDR1 Access with Page Hit (from DMA)
DDR1_Page_Miss_DMA	DDR	C5C3F801	DDR1 Access with Page Miss (from DMA)
DDR2_Page_Hit_DMA	DDR	C5C3F802	DDR2 Access with Page Hit (from DMA)
DDR2_Page_Miss_DMA	DDR	C5C3F803	DDR2 Access with Page Miss (from DMA)
DDR1_Page_Hit_FMAN	DDR	C703C000	DDR1 Access with Page Hit (from FMAN)
DDR1_Page_Miss_FMAN	DDR	C703C001	DDR1 Access with Page Miss (from FMAN)
DDR2_Page_Hit_FMAN	DDR	C703C002	DDR2 Access with Page Hit (from FMAN)
DDR2_Page_Miss_FMAN	DDR	C703C003	DDR2 Access with Page Miss (from FMAN)
DDR1_Page_Hit_QMAN	DDR	C4F3FC00	DDR1 Access with Page Hit (from QMAN)
DDR1_Page_Miss_QMAN	DDR	C4F3FC01	DDR1 Access with Page Miss (from QMAN)
DDR2_Page_Hit_QMAN	DDR	C4F3FC02	DDR2 Access with Page Hit (from QMAN)
DDR2_Page_Miss_QMAN	DDR	C4F3FC03	DDR2 Access with Page Miss (from QMAN)
QM_DEQUEUE_CMD_FIFO_DCP0_FULL	DPAA	30000054	Counts whenever the dequeue command FIFO in a DCP0 is full.
QM_DEQUEUE_CMD_FIFO_DCP1_FULL	DPAA	30000055	Counts whenever the dequeue command FIFO in a DCP1 is full.
QM_DEQUEUE_CMD_FIFO_DCP2_FULL	DPAA	30000056	Counts whenever the dequeue command FIFO in a DCP2 is full.

Mnemonic	Type	Perf ID	Description
QM_DEQUEUE_CMD_FIFO_DCP3_FULL	DPAA	30000057	Counts whenever the dequeue command FIFO in a DCP3 is full.
QM_DEQUEUE_RESPONSE_FIFO_DCP0_FULL	DPAA	30000058	Counts whenever the dequeue response FIFO in DPC0 is full.
QM_DEQUEUE_RESPONSE_FIFO_DCP1_FULL	DPAA	30000059	Counts whenever the dequeue response FIFO in DPC1 is full.
QM_DEQUEUE_SEQUENCE_DELIVERS_1_MORE_ANY_SP	DPAA	30000074	Counts for every dequeue sequence that completes and delivers 1 or more frames for any software
QM_DEQUEUE_SEQUENCE_DELIVERS_1_MORE_DCP0	DPAA	30000070	Counts for every dequeue sequence that completes and delivers 1 or more frames for DCP0.
QM_DEQUEUE_SEQUENCE_DELIVERS_1_MORE_DCP1	DPAA	30000071	Counts for every dequeue sequence that completes and delivers 1 or more frames for DCP1.
QM_DEQUEUE_SEQUENCE_DELIVERS_1_MORE_DCP2	DPAA	30000072	Counts for every dequeue sequence that completes and delivers 1 or more frames for DCP2.
QM_DEQUEUE_SEQUENCE_DELIVERS_2_MORE_ANY_SP	DPAA	30000079	Counts for every dequeue sequence that completes and delivers 2 or more frames for any software
QM_DEQUEUE_SEQUENCE_DELIVERS_2_MORE_DCP0	DPAA	30000075	Counts for every dequeue sequence that completes and delivers 2 or more frames for DCP0.
QM_DEQUEUE_SEQUENCE_DELIVERS_2_MORE_DCP1	DPAA	30000076	Counts for every dequeue sequence that completes and delivers 2 or more frames for DCP1.
QM_DEQUEUE_SEQUENCE_DELIVERS_2_MORE_DCP2	DPAA	30000077	Counts for every dequeue sequence that completes and delivers 2 or more frames for DCP2.
QM_DEQUEUE_SEQUENCE_DELIVERS_3_ANY_SP	DPAA	3000007E	Counts for every dequeue sequence that completes and delivers 3 frames for any software portal.
QM_DEQUEUE_SEQUENCE_DELIVERS_3_DCP0	DPAA	3000007A	Counts for every dequeue sequence that completes and delivers 3 frames for DCP0.
QM_DEQUEUE_SEQUENCE_DELIVERS_3_DCP1	DPAA	3000007B	Counts for every dequeue sequence that completes and delivers 3 frames for DCP1.
QM_DEQUEUE_SEQUENCE_DELIVERS_3_DCP2	DPAA	3000007C	Counts for every dequeue sequence that completes and delivers 3 frames for DCP2.
QM_ENQUEUE_CMD_DCP0	DPAA	30000037	Counts every enqueue command received in DCP0.
QM_ENQUEUE_CMD_DCP1	DPAA	30000038	Counts every enqueue command received in DCP1.
QM_ENQUEUE_CMD_DCP2_CUST	DPAA	30000039	Custom QMan Enqueue command on DCP2 by DataPath Reference event. Setup
QM_ENQUEUE_CMD_FIFO_DCP0_FULL	DPAA	3000004F	Counts whenever the enqueue command FIFO in a direct connect portal is full in DCP0.
QM_ENQUEUE_CMD_FIFO_DCP1_FULL	DPAA	30000050	Counts whenever the enqueue command FIFO in a direct connect portal is full in DCP1.
QM_ENQUEUE_CMD_FIFO_DCP2_FULL	DPAA	30000051	Counts whenever the enqueue command FIFO in a direct connect portal is full in DCP2.

Mnemonic	Type	Perf ID	Description
QM_ENQUEUE_CMD_FIFO_DCP3_FULL	DPAA	30000052	Counts whenever the enqueue command FIFO in a direct connect portal is full in DCP3.
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP0	DPAA	30000045	#N/A
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP1	DPAA	30000046	#N/A
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP2	DPAA	30000047	#N/A
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP3	DPAA	30000048	#N/A
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP4	DPAA	30000049	#N/A
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP5	DPAA	3000004A	#N/A
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP6	DPAA	3000004B	#N/A
QM_ENQUEUE_CMD_PULLED_FROM_EQCR_RING_IS_FULL_SP7	DPAA	3000004C	#N/A
QM_ENQUEUE_CMD_SP0_S23	DPAA	300002E0	Counts every enqueue command received in SP0 (Software Portal)
QM_ENQUEUE_CMD_SP1_S23	DPAA	300002E1	Counts every enqueue command received in SP 1.
QM_ENQUEUE_CMD_SP2_S23	DPAA	300002E2	Counts every enqueue command received in SP 2.
QM_ENQUEUE_CMD_SP3_S23	DPAA	300002E3	Counts every enqueue command received in SP 3.
QM_ENQUEUE_CMD_SP4_S23	DPAA	300002E4	Counts every enqueue command received in SP 4.
QM_ENQUEUE_CMD_SP5_REF	DPAA	300002E5	Counts every enqueue command received in SP5. Setup DPRESCR0[REFEV0_SEL] to 0x40.
QM_ENQUEUE_CMD_SP6_REF	DPAA	300002E6	Counts every enqueue command received in SP6.
QM_ENQUEUE_CMD_SP7_REF	DPAA	300002E7	Counts every enqueue command received in SP7.
QM_ENQUEUE_SEQUENCE_DISPAT	DPAA	30000066	Counts for every enqueue sequence that is
QM_ENQUEUE_SEQUENCE_DISPAT	DPAA	30000067	Counts for every enqueue sequence that is
SEC_CMD_IN_DECO0_ENCOUNTER	DPAA	3000012F	Counts when an actual operation command in DECO0
SEC_CMD_IN_DECO1_ENCOUNTERED_JOB_SHARED_TRASTED_DESCR	DPAA	30000133	Counts when an actual operation command in DECO1 is encountered in a job descriptor

Mnemonic	Type	Perf ID	Description
SEC_CMD_IN_DECO2_ENCOUNTERED_JOB_SHARED_TRASTED_DESCR	DPAA	30000137	Counts when an actual operation command in DECO2 is encountered in a job descriptor
SEC_CMD_IN_DECO3_ENCOUNTERED_JOB_SHARED_TRASTED_DESCR	DPAA	3000013B	Counts when an actual operation command in DECO3 is encountered in a job descriptor
SEC_CMD_IN_DECO4_ENCOUNTERED_JOB_SHARED_TRASTED_DESCR	DPAA	3000013F	Counts when an actual operation command in DECO4 is encountered in a job descriptor
SEC_DECO_0_IS_IDLE	DPAA	3000012D	[Grp9-Evt14]Counts whenever DECO 0 is idle.
SEC_DECO_1_IS_IDLE	DPAA	30000131	[Grp9-Evt18]Counts whenever DECO 1 is idle.
SEC_DECO_2_IS_IDLE	DPAA	30000135	Counts whenever DECO 2 is idle. 9-22
SEC_DECO_3_IS_IDLE	DPAA	30000139	Counts whenever DECO 3 is idle. 9-26
SEC_DECO_4_IS_IDLE	DPAA	3000013D	Counts whenever DECO 4 is idle. 9-30
SEC_INPUT_FIFO_EMPTY_DECO0_	DPAA	3000012E	(Custom) Counts whenever the input FIFO is empty
SEC_INPUT_FIFO_EMPTY_DECO1_AWAITS_DMA_DECO_1_AWAITS_DMA	DPAA	30000132	Counts whenever the input FIFO is empty and DECO1 is awaiting a response to a DMA read or output FIFO is full
SEC_INPUT_FIFO_EMPTY_DECO2_AWAITS_DMA_DECO_2_AWAITS_DMA	DPAA	30000136	Counts whenever the input FIFO is empty and DECO2 is awaiting a response to a DMA read or output FIFO is full
SEC_INPUT_FIFO_EMPTY_DECO3_AWAITS_DMA_DECO_3_AWAITS_DMA	DPAA	3000013A	Counts whenever the input FIFO is empty and DECO3 is awaiting a response to a DMA read or output FIFO is full
SEC_INPUT_FIFO_EMPTY_DECO4_AWAITS_DMA_DECO_4_AWAITS_D	DPAA	3000013E	Counts whenever the input FIFO is empty and DECO4 is awaiting a response to a DMA read or output FIFO