

*Real Time Operating Systems Design and Programming*

## **Homework**

### **CPU Caching Homework**

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# 1 Overview

You are expected to work out the following questions once you have gone through the lecture. Please go over the lecture slides and any relevant textbook so that you can grasp the basic ideas behind the CPU cache. The questions are set up and designed as examples to help you understand the concepts in more details.

Some extended concepts:

A Cache miss can be further defined into two categories:

- Compulsory Miss: An unavoidable miss – the first reference to a location that has never before been requested. The size of the cache and associativity have no effect.
- Conflict Miss: An avoidable miss – the replacement policy has replaced the requested block.

## 2 system setup for Questions

Consider the following system setup:

- Byte addressed
- 64KB Main Memory (16-bit address)
- 4KB Cache
- 4 Word Block size
- 4 Bytes per word (32-bit words)

Read operations:

- 0x0021
- 0xA030
- 0x5029
- 0x002D
- 0xA030

## 3 Questions

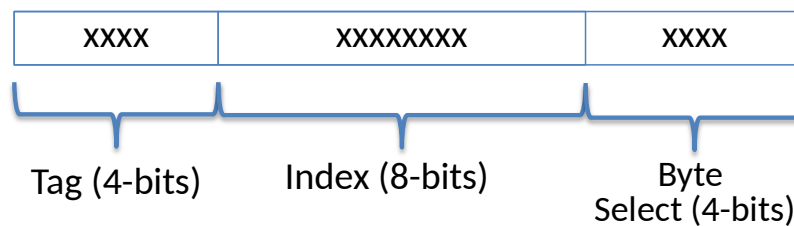
1. Assuming a Direct Mapped cache; for each of the read operations, determine whether they result in a cache hit, compulsory miss, capacity miss or conflict miss.

2. What is the hit rate for this Direct Mapped cache?
3. Now consider a 2-Way Set Associative cache that uses a Round Robin (first-in, first-out) replacement policy; for each of the read operations, determine whether they result in a cache hit, compulsory miss, capacity miss or conflict miss. Additionally determine the hit rate and compare it to the Direct Mapped Cache.
4. Perform these additional accesses to force a replacement:
  - 0x4026
  - 0x0021
5. What is the hit rate for this 2-Way Set Associative Cache?
6. Suggest a replacement policy that could increase the hit rate of this cache.

## 4 Answers

1. Assuming a Direct Mapped cache; for each of the read operations, determine whether they result in a cache hit, compulsory miss, capacity miss or conflict miss.

Each block contains  $2^4$  bytes. The cache has a  $2^{12}$  byte capacity. Therefore the cache consists of  $2^8$  blocks.



- 0x0021 – Compulsory Miss

Tag	Index	Byte Select
0x0	0x02	0x1

Index	V	Tag	Word 0	Word 1	Word 2	Word 3
0	0					
1	0					
2	1	0x0	A	B	C	D
3	0					
4	0					
5	0					
6	0					
7	0					
...						
255	0					

- 0xA060 – Compulsory Miss

Tag	Index	Byte Select
0xA	0x06	0x0

Index	V	Tag	Word 0	Word 1	Word 2	Word 3
0	0					
1	0					
2	1	0x0 (0000)	A	B	C	D
3	0	0xA (1010)	E	F	G	H
4	0					
5	0					
6	1					
7	0					
...						
255	0					

- 0x5029 – Compulsory Miss

Tag	Index	Byte Select
0x5	0x02	0x9

Index	V	Tag	Word 0	Word 1	Word 2	Word 3
0	0					
1	0					
2	1	0x5 (0101)	I	J	K	L
3	0	0xA (1010)	E	F	G	H
4	0					
5	0					
6	1					
7	0					
...						
255	0					

- 0x002D – Conflict Miss

Tag	Index	Byte Select
0x0	0x02	0xD

Index	V	Tag	Word 0	Word 1	Word 2	Word 3
0	0					
1	0					
2	1	0x0 (0000)	A	B	C	D
3	0	0xA (1010)	E	F	G	H
4	0					
5	0					
6	1					
7	0					
...						
255	0					

- 0xA030 – Hit

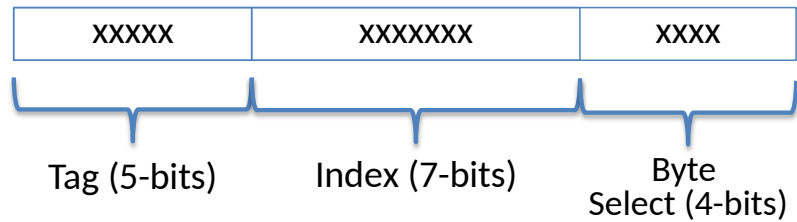
Tag	Index	Byte Select
0xA	0x03	0x0

Index	V	Tag	Word 0	Word 1	Word 2	Word 3
0	0					
1	0					
2	1	0x0 (0000)	A	B	C	D
3	0	0xA (1010)	E	F	G	H
4	0					
5	0					
6	1					
7	0					
...						
255	0					

2. What is the hit rate for this Direct Mapped cache?

0.2

3. Now consider a 2-Way Set Associative cache that uses a Round Robin (first-in, first-out) replacement policy; for each of the read operations, determine whether they result in a cache hit, compulsory miss, capacity miss or conflict miss. Additionally determine the hit rate and compare it to the Direct Mapped Cache.



- 0x0021 – Compulsory Miss

Tag	Index	Byte Select
0x00	0x02	0x1

Set	Index	V	Tag	Word 0	Word 1	Word 2	Word 3	Age
0	0	0						
	1	0						
1	2	0						
	3	0						
2	4	0	0x00 (00000)	A	B	C	D	1
	5	0						
3	6	0						
	7	0						
...								
127	255	0						

- 0xA030 – Compulsory Miss

Tag	Index	Byte Select
0x14	0x03	0x0

Set	Index	V	Tag	Word 0	Word 1	Word 2	Word 3	Age
0	0	0						
	1	0						
1	2	0						
	3	0						
2	4	1	0x00 (00000)	A	B	C	D	1
	5	0						
3	6	1	0x14 (10100)	E	F	G	H	1
	7	0						
...								
127	255	0						

- 0x5029 – Compulsory Miss

Tag	Index	Byte Select
0x0A (01010)	0x02	0x9





127	255	0						
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Hit rate: 0.4

4. Perform these additional accesses to force a replacement:

- 0x4026
- 0x0021
- 0x4026 – Compulsory Miss

Tag	Index	Byte Select
0x08 (01000)	0x02	0x6

Set	Index	V	Tag	Word 0	Word 1	Word 2	Word 3	Age
0	0	0						
	1	0						
1	2	0						
	3	0						
2	4	1	0x01 (01000)	M	N	O	P	3
	5	1	0x0A (01010)	I	J	K	L	2
3	6	1	0x14 (10100)	E	F	G	H	1
	7	0						
			...					
127	255	0						

- 0x0021 – Conflict Miss

Tag	Index	Byte Select
0x00 (00000)	0x02	0x1

Set	Index	V	Tag	Word 0	Word 1	Word 2	Word 3	Age
0	0	0						
	1	0						
1	2	0						
	3	0						
2	4	1	0x08 (01000)	M	N	O	P	3
	5	1	0x0A (01010)	A	B	C	D	4
3	6	1	0x14 (10100)	E	F	G	H	1
	7	0						
			...					
127	255	0						

5. What is the hit rate for this 2-Way Set Associative Cache?

$$2 / 7 = 0.28$$

6. Suggest a replacement policy that could increase the hit rate of this cache.

Least Recently Used. The process is identical to that in Q3 up until the first replacement. State of the cache prior to the 0x4026 access:

Set	Index	V	Tag	Word 0	Word 1	Word 2	Word 3	LRU
0	0	0						
	1	0						
1	2	0						
	3	0						
2	4	1	0x00 (00000)	A	B	C	D	
	5	1	0x0A (01010)	I	J	K	L	
3	6	1	0x14 (10100)	E	F	G	H	
	7	0						
...								
127	255	0						

- 0x4026 – Compulsory Miss

Tag	Index	Byte Select
0x08 (01000)	0x02	0x6

Set	Index	V	Tag	Word 0	Word 1	Word 2	Word 3	LRU
0	0	0						
	1	0						
1	2	0						
	3	0						
2	4	1	0x00 (00000)	A	B	C	D	
	5	1	0x0A (01000)	M	N	O	P	
3	6	1	0x14 (10100)	E	F	G	H	
	7	0						
...								
127	255	0						

- 0x0021 – Hit

Tag	Index	Byte Select
0x00 (00000)	0x02	0x1

Set	Index	V	Tag	Word 0	Word 1	Word 2	Word 3	LRU
0	0	0						
	1	0						
1	2	0						
	3	0						
2	4	1	0x00 (00000)	A	B	C	D	
	5	1	0x0A (01000)	M	N	O	P	
3	6	1	0x14 (10100)	E	F	G	H	
	7	0						
			...					
127	255	0						

Hit rate: 3 / 7 = 0.42