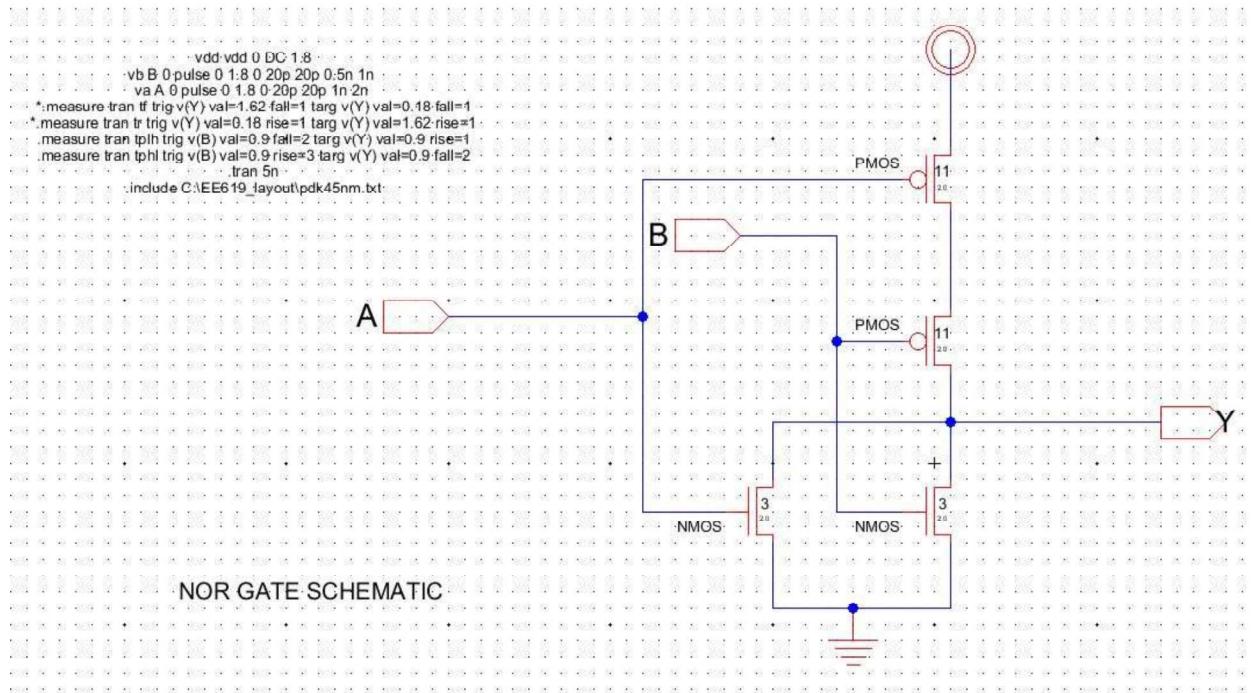


SCHEMATIC:



TRANSISTOR SIZE EXPLANATION:

For a reference inverter,

In order to equate the worst case t_{phh} and

t_{phe} , we need resistance in pMOS side and nMOS

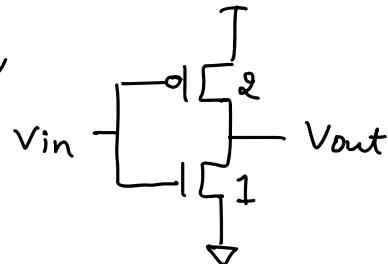
side for worst case input to be same.

For NOR Gate,

(i) worst case t_{phh} (i/p condition): $A=0, B=0$.

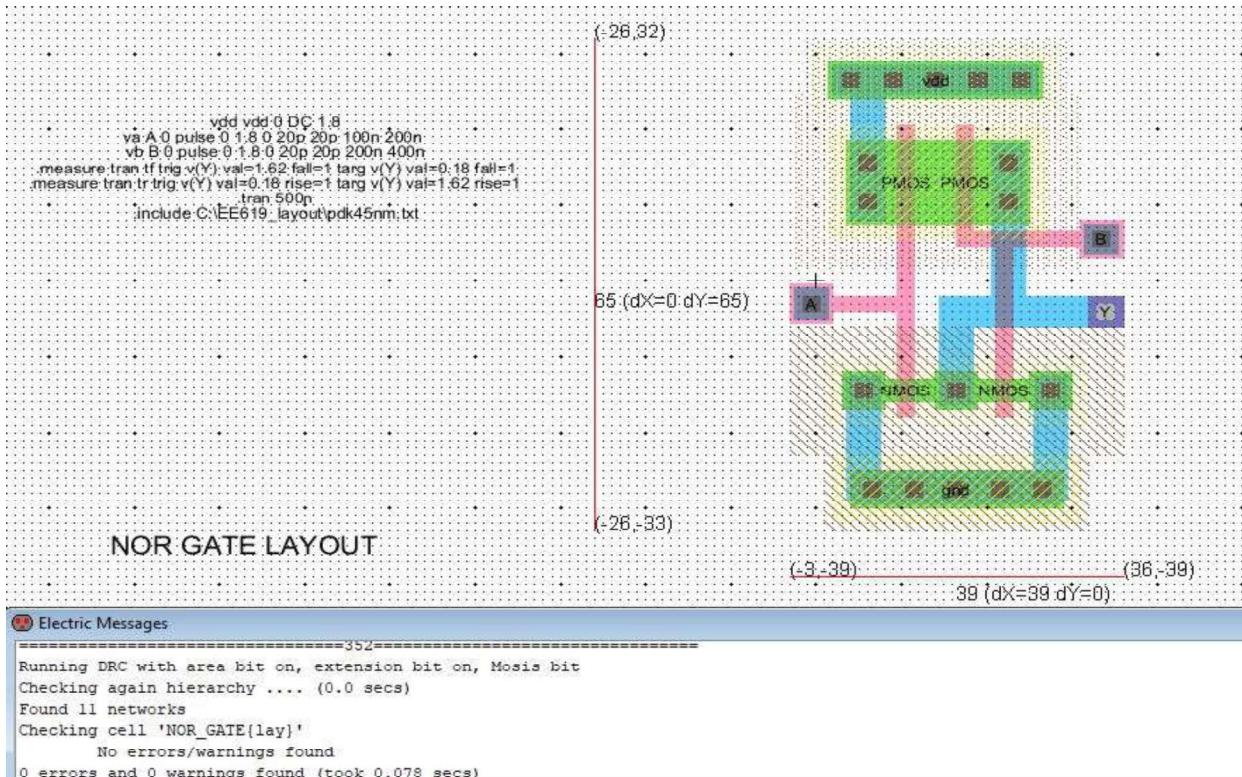
(ii) worst case t_{phe} (i/p condition): $A=1, B=0$ ($\text{or } A=0, B=1$)
We have manipulated gate sizes to match t_{phh} and

t_{phe} for given inputs. Thus, we have arrived at pMOS size 11 and nMOS size 3, which is in accordance with theoretical value of pMOS size 4 and nMOS size 1.

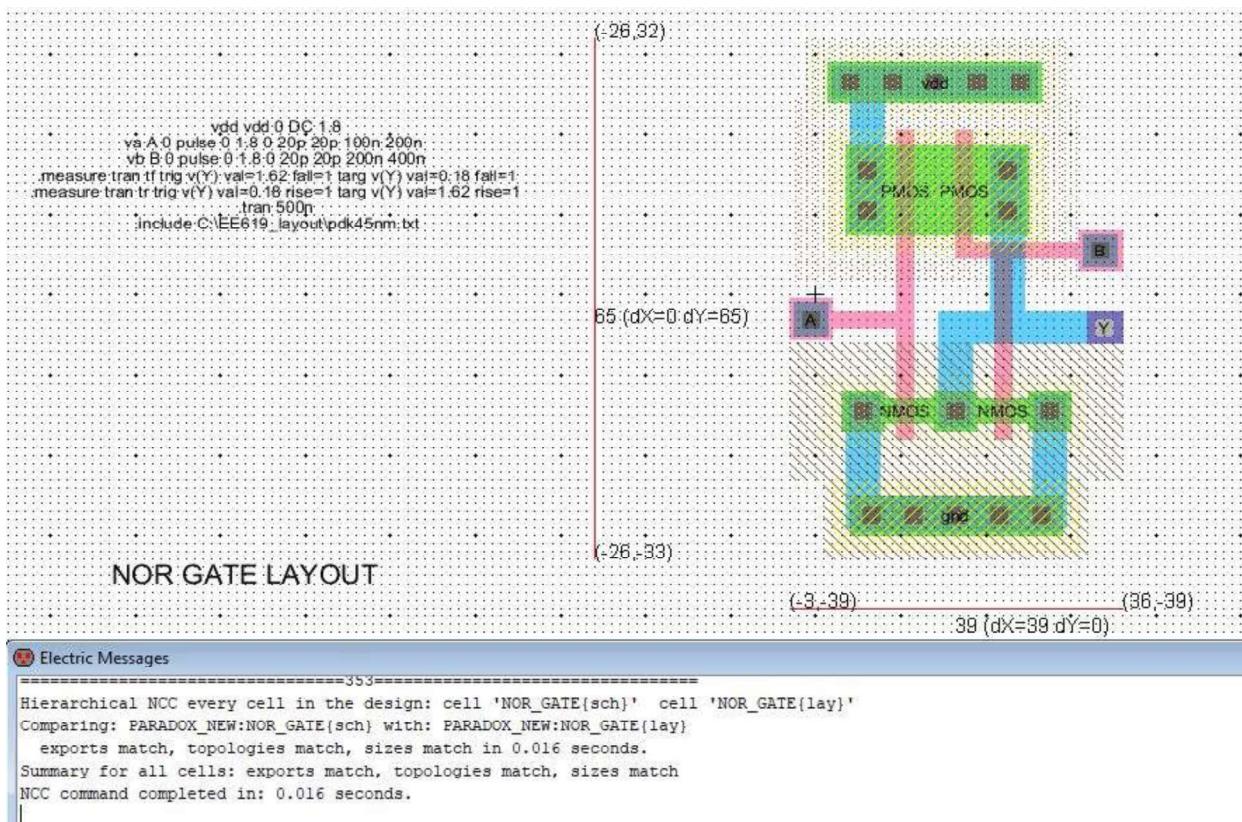


The input given to the circuit is of frequency 1GHz
as specified in project problem statement.

LAYOUT WITH DRC LOG:



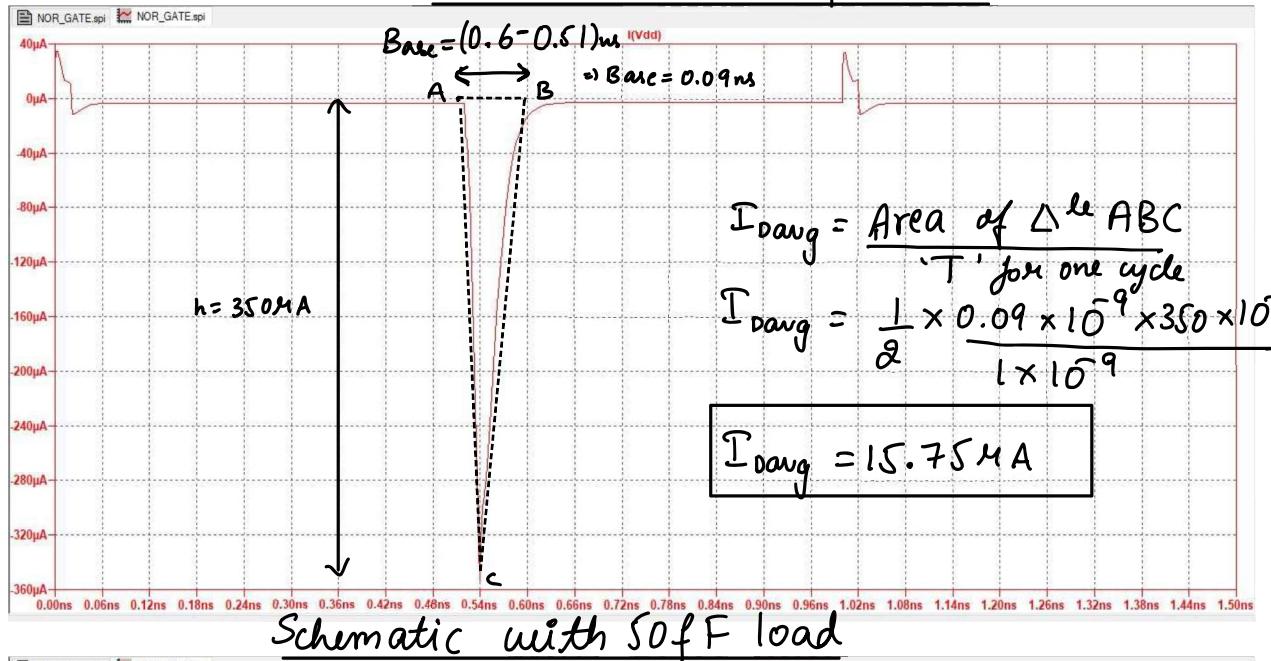
LAYOUT WITH LVS LOG:



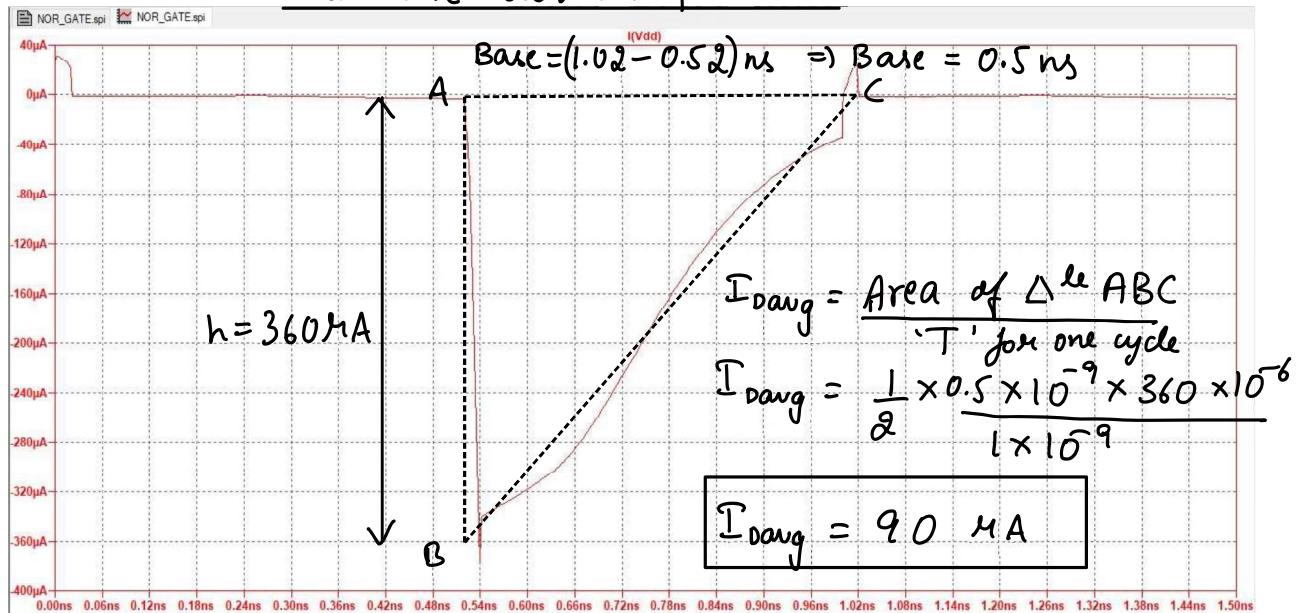
PROPAGATION DELAY:

NOR	Schematic			Layout		
Load capacitance	tplh	tphl	average	tplh	tphl	average
5fF	17.091ps	15.3343ps	16.21265ps	18.1325ps	16.0517ps	17.0921ps
50fF	143.706ps	111.859ps	127.7825ps	144.741ps	112.329ps	128.535ps

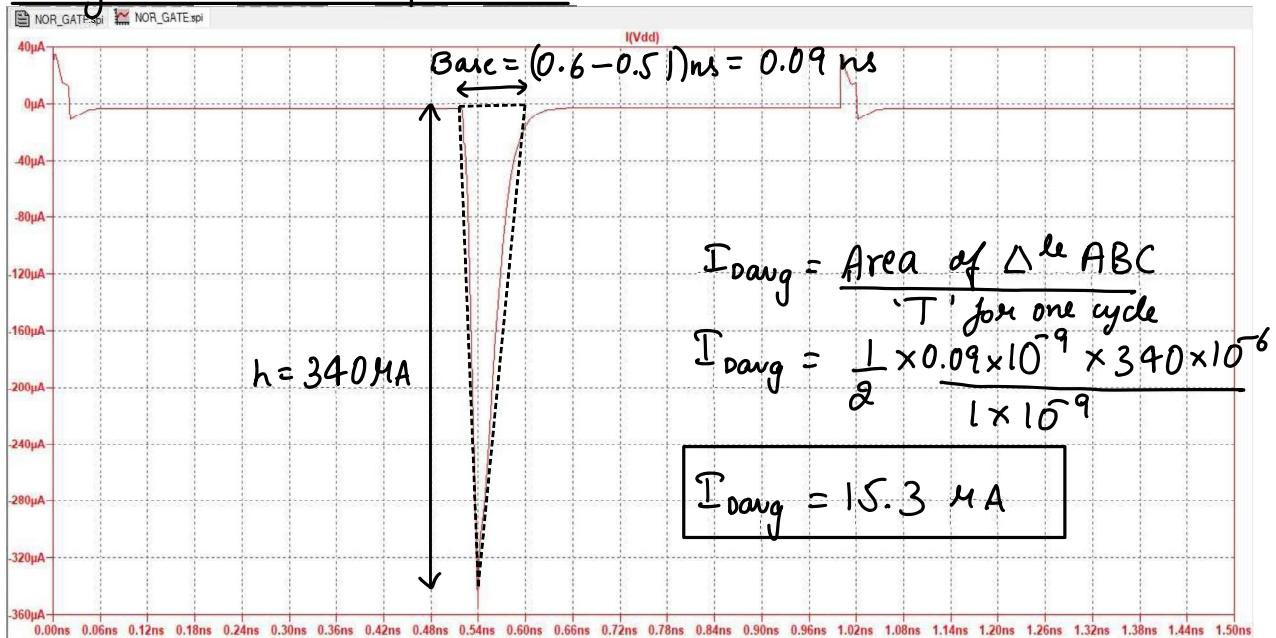
POWER CONSUMPTION: Schematic with 5fF load



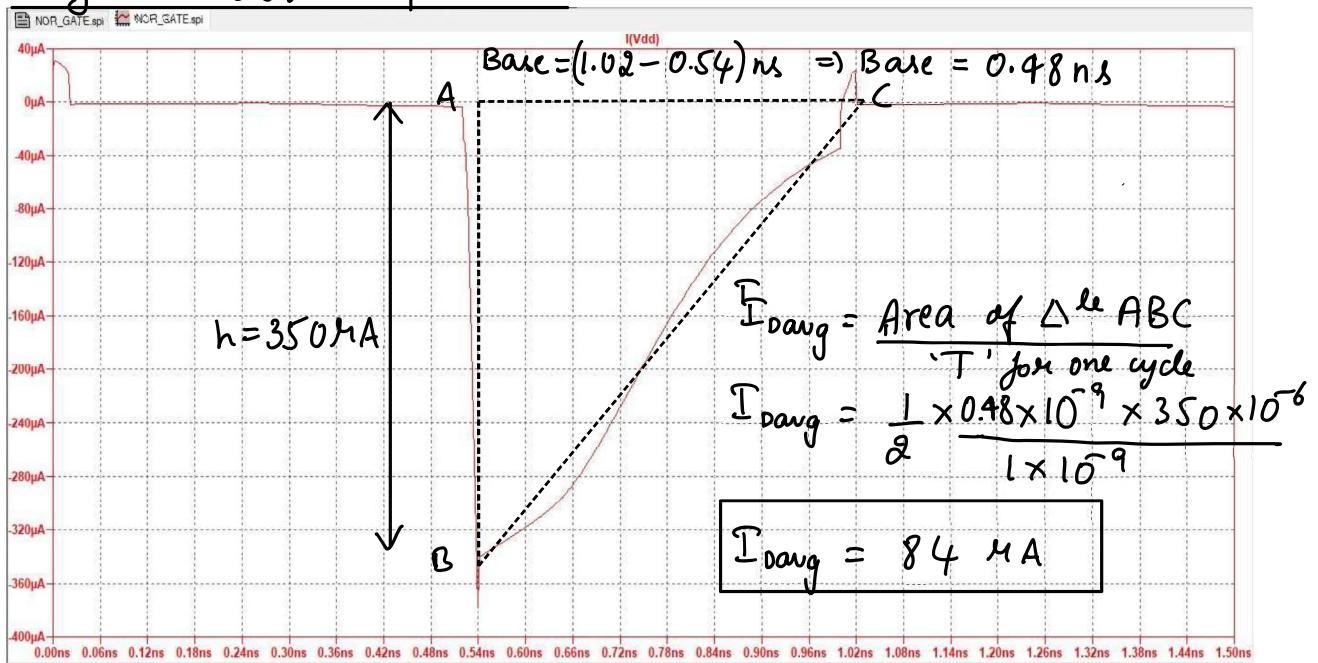
Schematic with 50fF load



Layout with 5fF load



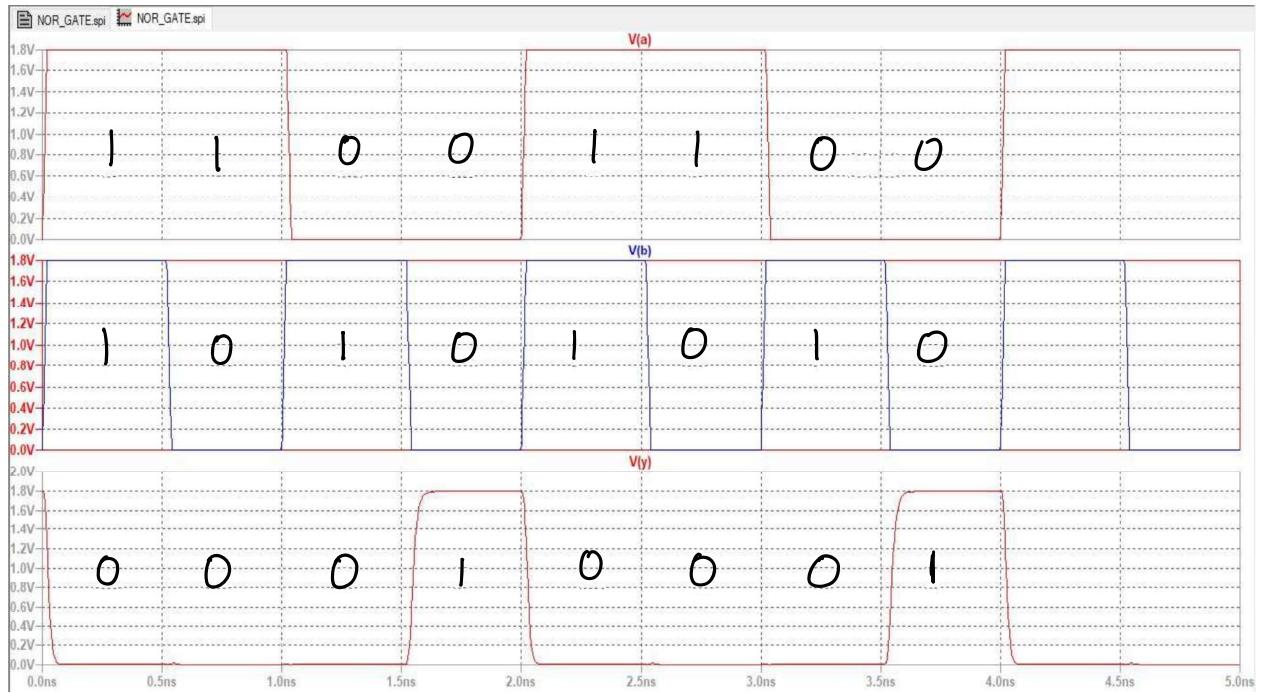
Layout with 50fF load



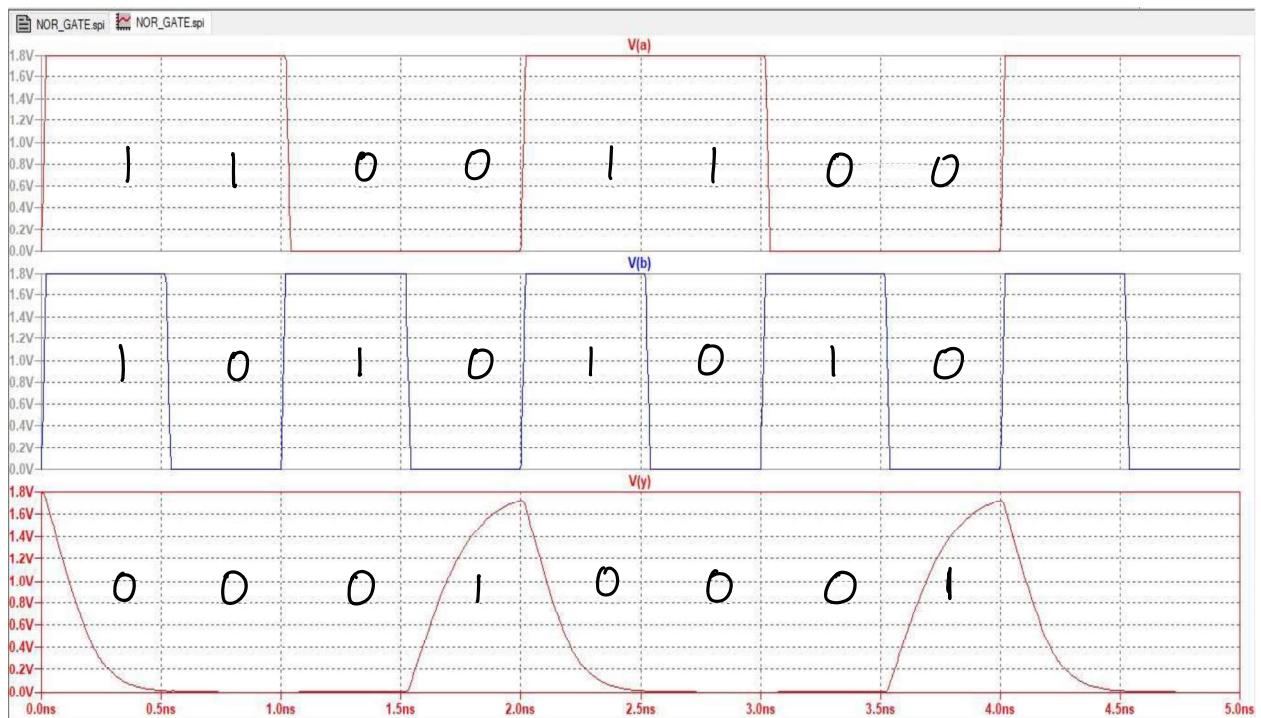
NOR	Schematic			Layout		
Load Capacitance	Average Id	Vdd	Power	Average Id	Vdd	Power
5fF	15.75 mA	1.8	28.35 mW	15.3 mA	1.8	27.54 mW
50fF	90 mA	1.8	162 mW	84 mA	1.8	151.2 mW

TRANSIENT I/O WAVEFORMS:

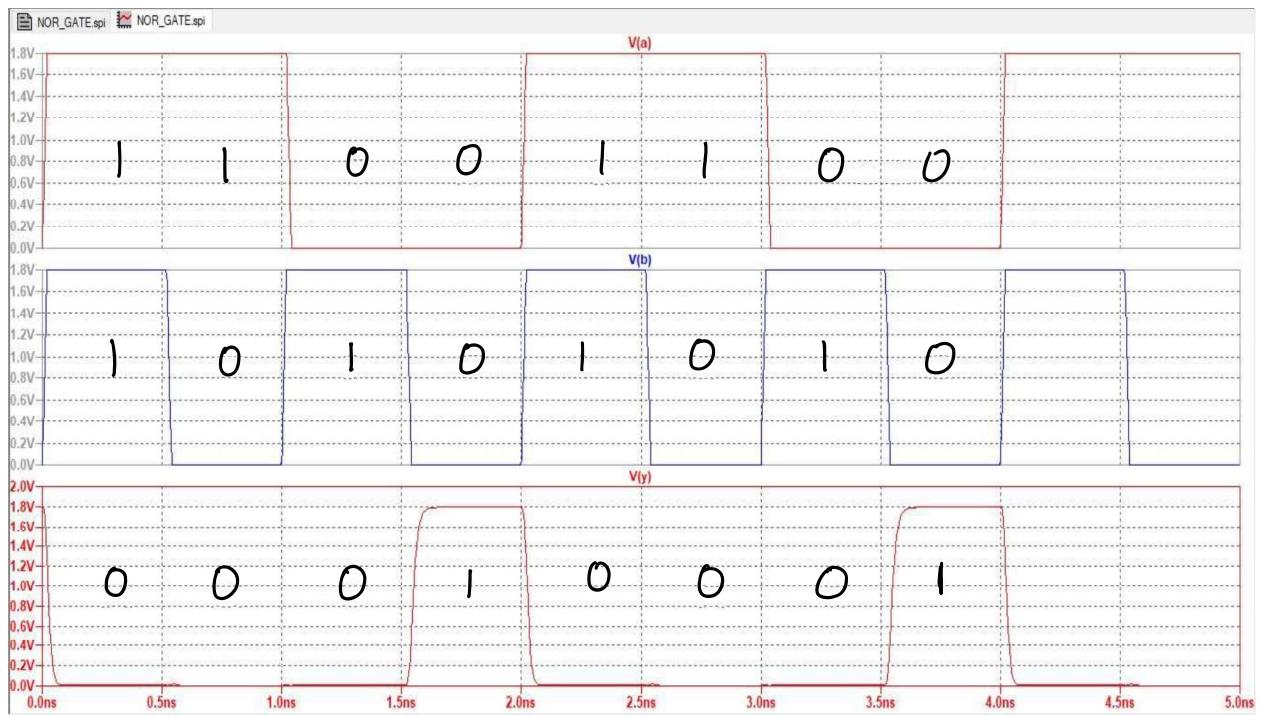
1) FOR SCHEMATIC WITH 5fF LOAD.



2) FOR SCHEMATIC WITH 50fF LOAD



3) FOR LAYOUT WITH 5fF LOAD



4) FOR LAYOUT WITH 50fF LOAD

