EXERCISES

1) [10] In a server farm such as that used by Amazon or Google, a single failure does not cause the entire system to crash. Instead, it will reduce the number of requests that can be satisfied at any one time. If a company has 7,500 computers, each with a MTTF of 30 days, and it experiences catastrophic failure only if 1/3 of the computers fail. If it costs an extra $1000, per computer, to double the MTTF of the system, would this be a good business decision? Show your work

   Solution:
   MTTF = 30/7500 * 7500/3 = 10 days
   Number of computer failing per hour = 7500/3/10/24 = 10.41
   Time required for a single computer to fail = 60/10.41 = 5.76

   Increasing time required to replace a failed computer every 11.52 minutes from 5.76, thus proving sufficient for computer replace.

2) [12] Assume that for a C program, compiler A results in a dynamic instruction count of 600 million and has an execution time of 2.1s, while compiler B results ion a dynamic instruction count of 900 million and an execution time of 3s?

a) Find the average CPI for each compiled program given that the processor has clock cycle time of 2ns.

   Solution:
   CPU Time = Instruction count * Clock Cycle per instruction * Clock Cycle time

   For A,
   CPU(Execution Time) = 2.1s
   Instruction count = 600 million
   Clock cycle time = 2 ns

   $2.1 = 600 * 10^6 * CPI * 2 * 10^{-9}$
   CPI(A) = 1.75

   For B,
   CPU(Execution Time) = 3
   Instruction count = 900 million
   Clock cycle time = 2 ns

   $3 = 900 * 10^6 * CPI * 2 * 10^{-9}$
   CPI(A) = 1.66

b) Assume the compiled programs run on two different processors, i.e. A program runs on processor I and B program on processor II. If the execution times on the two processors are the same, which processor is how much faster (i.e., performance ratio) running its code?

CPU Time (A) = CPU Time(B)
Instruction count(A) * Clock Cycle per instruction(A) / Clock Rate(I) = Instruction count(B) * Clock Cycle per instruction(B) / Clock Rate(II)

Clock Rate(I)/Clock Rate(II) = (Instruction count(B) * Clock Cycle per instruction(B))/ Instruction count(A) * Clock Cycle per instruction(A)

$$=(900 * 10^6 * 1.66)/ (600 * 10^6 * 1.75) = 1.42$$

3) [10] The following MIPS program is to be run on a MIPS pipeline processor of 5 stages (IF-ID-EX-MEM-WB). Work out and diagram the optimal pipeline schedule using full forwarding from EX or MEM stages to any other stage, Draw the pipeline execution diagram for this code and then compute the pipeline CPI:

```
addi $t6, $t6, 10
sub $t5, $t6, $t4
srl $t5, $t5, 2
sw $t5, 20($t5)
lw $t2, 0($t6)
add $t7, $t2, $t3
beq $t5, $t7, End
```

1la	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	F	D	E	M	W													
2		F	D	E	M	W												
3			F	D	E	M	W											
4				F	D	E	M	W										
5					F	D	E	M	W									
6						X	F	D	E	M	W							
7								F	D	E	M	W						

CPI = 12/7

4) 10] Assume a five-stage single-pipeline microarchitecture (fetch, decode, execute, memory, write-back) and the code given below. All ops are one cycle except LW and SW, which are 1+2 cycles, and branches, which are 1+1 cycles. There is no forwarding. Show the phases of each instruction per clock cycle for one iteration of the loop.

```
Loop: lw x1,0(x2)
      addi x1,x1, 1
      sw x1,0(x2)
      addi x2,x2,4
      sub x4,x3,x2
      bnz x4,Loop
```

a) How many clock cycles per loop iteration are lost to branch overhead? 4/5

b) Assume a static branch predictor, capable of recognizing a backward branch in the Decode stage. Now how many clock cycles are wasted on branch overhead? 2/3

c) Assume a dynamic branch predictor. How many cycles are lost on a correct prediction? 0

5) [15] The 5 stages of the processor have the followings:

S1	S2	S3	S4	S5
200 PS	100 PS	450 PS	300 PS	100 PS

A) Non-pipelined (single cycle) processor: What is cycle time? What is latency of instruction?

Cycle time = 200 + 100 + 450 + 300 + 100 = 1150 ps
Latency = 1150 ps

B) Pipelined processor: What is cycle time? What is latency of instruction?

Cycle time = 450 ps
Latency = 450 * 5 = 2250 ps

C) If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time? What is new latency?

pipeline stages to split into 2 equal halves = S3

S1	S2	S3	S4	S5	S6
200 PS	100 PS	225 PS	225 PS	300 PS	100 PS

Cycle time = 300 ps
Latency = 300 * 6 = 1800 ps

CASE STUDIES

A) [20] In this exercise, we assume that the following MIPS code is executed on a pipelined processor with a 5-stage pipeline(IF, ID, EX, MEM, WB), full forwarding, and a predict- taken branch predictor.

```
        LW R2, 0(R1)
LABEL1: BEQ R2, R0, LABEL2      #Not taken once, then always taken
        LW R3, 0(R2)
        BEQ R3, R0, LABEL1      #Always taken
        ADD R1, R3, R1
LABEL2: SW R1, 0(R2)
        ADD R4, R5, R6
```

Draw the pipeline execution diagram for this code, assuming that branches execute in the EX stage.

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14
LW R2, 0(R1)	IF	ID	EX	MEM	WB									
BEQ R2, R0, LABEL2		IF	*	ID	EX	MEM	WB							
LABEL2:SW R1,0(R2)				IF	ID	*	*	*						
ADD R4, R5, R6					IF	*	*	*	*					
LW R3, 0(R2)						IF	ID	EX	MEM	WB				
BEQ R3, R0, LABEL1							IF	*	ID	EX	MEM	WB		
LABEL1: BEQ R2, R0, LABEL2									IF	ID	EX	MEM	WB	
LABEL2: SW R1, 0(R2)										IF	ID	EX	MEM	WB