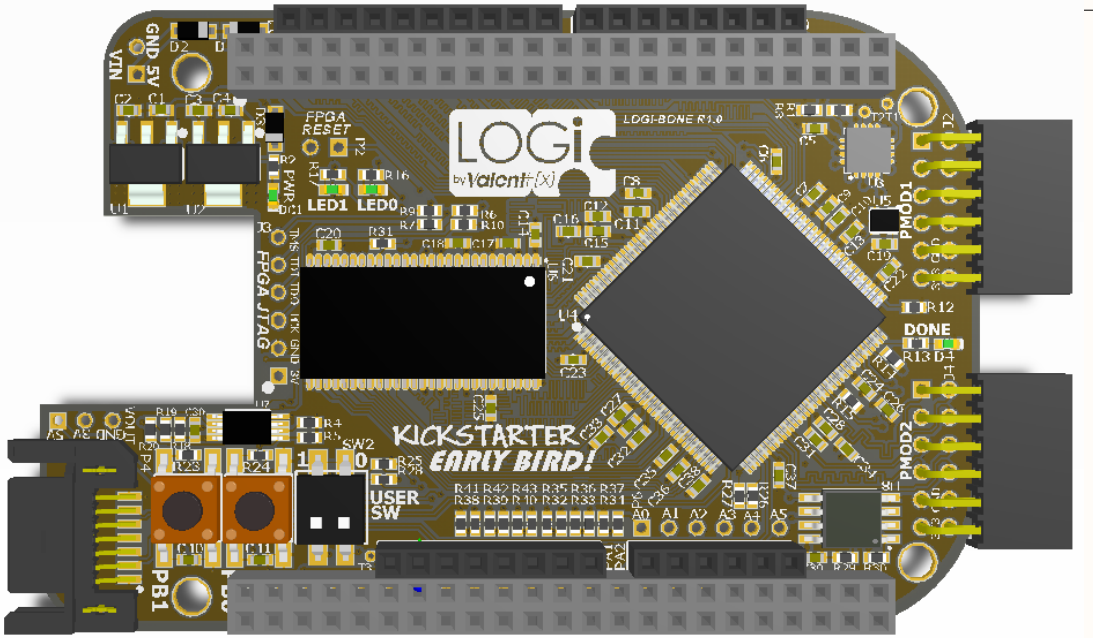

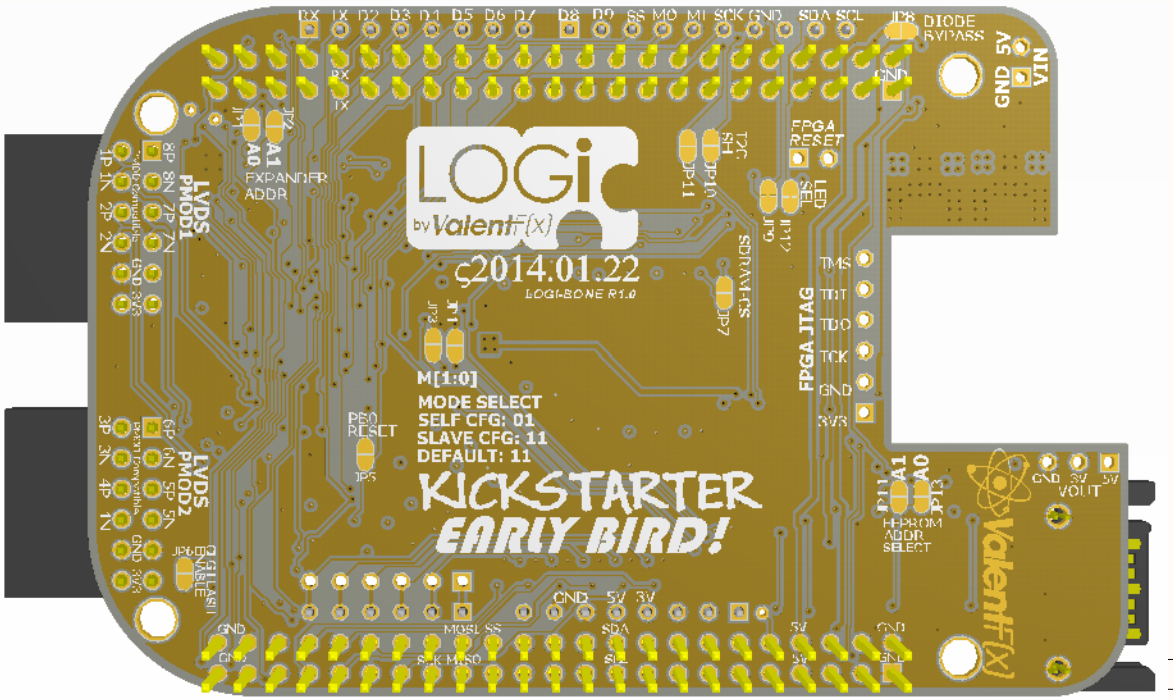

U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_RAM
RAM.SchDoc

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

LOGi-Bone Top Level			
Revision:	R1.0	Sheet	1 of 7
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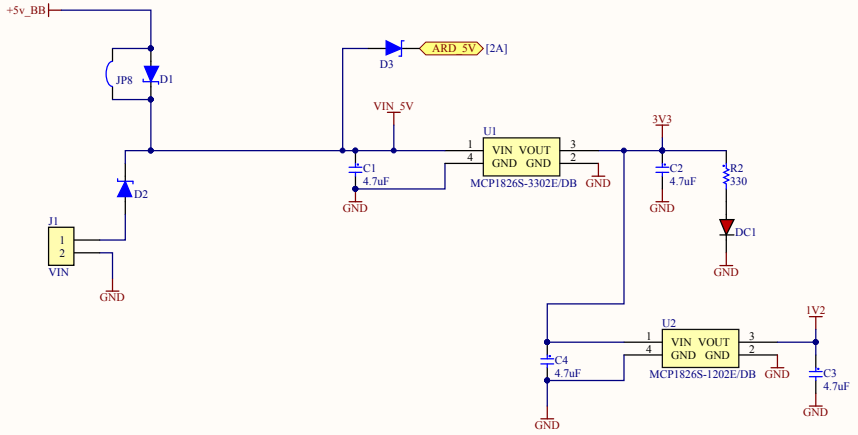
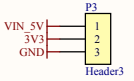
ValentF(x) ELECTRONICS INNOVATION

Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header J1.



1 x Auxillary Power output Headers



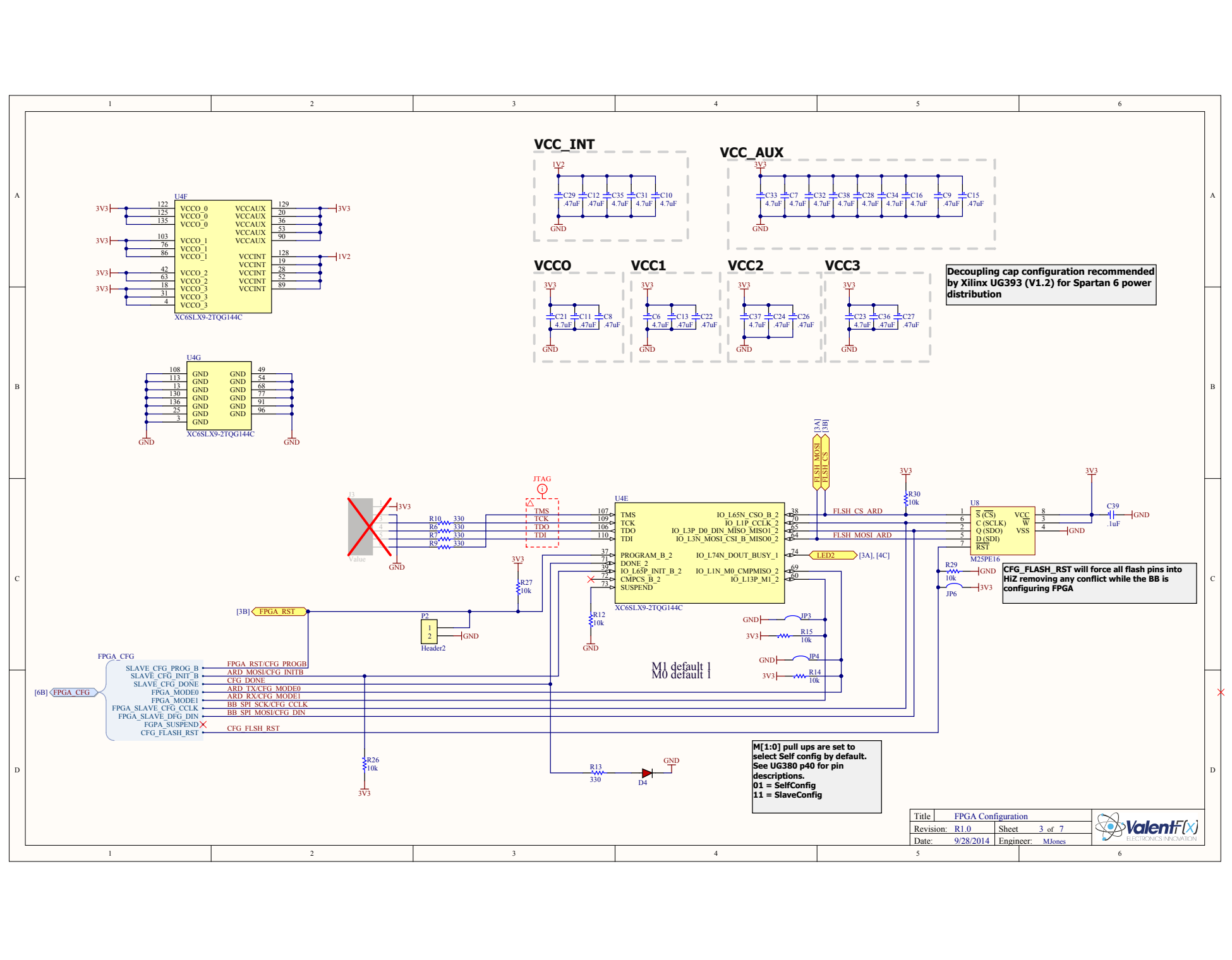
LOGI-LOGO-600
LOGO3

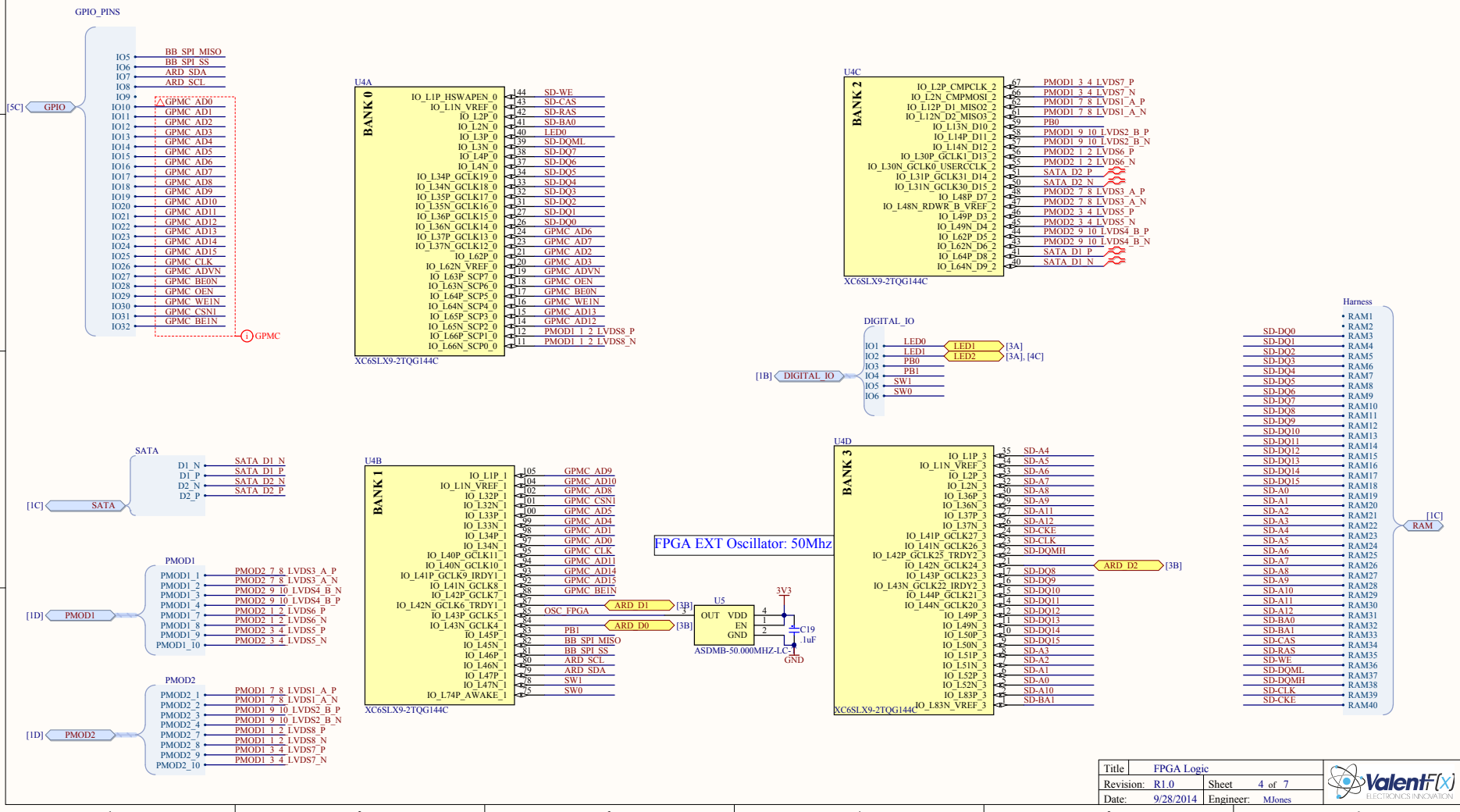
VALENTFX-LOGO-750
Logo5

LOGI-LOGO-750
LOGO4

Title	Power Supply		
Revision:	R1.0	Sheet	2 of 7
Date:	9/28/2014	Engineer:	MJones

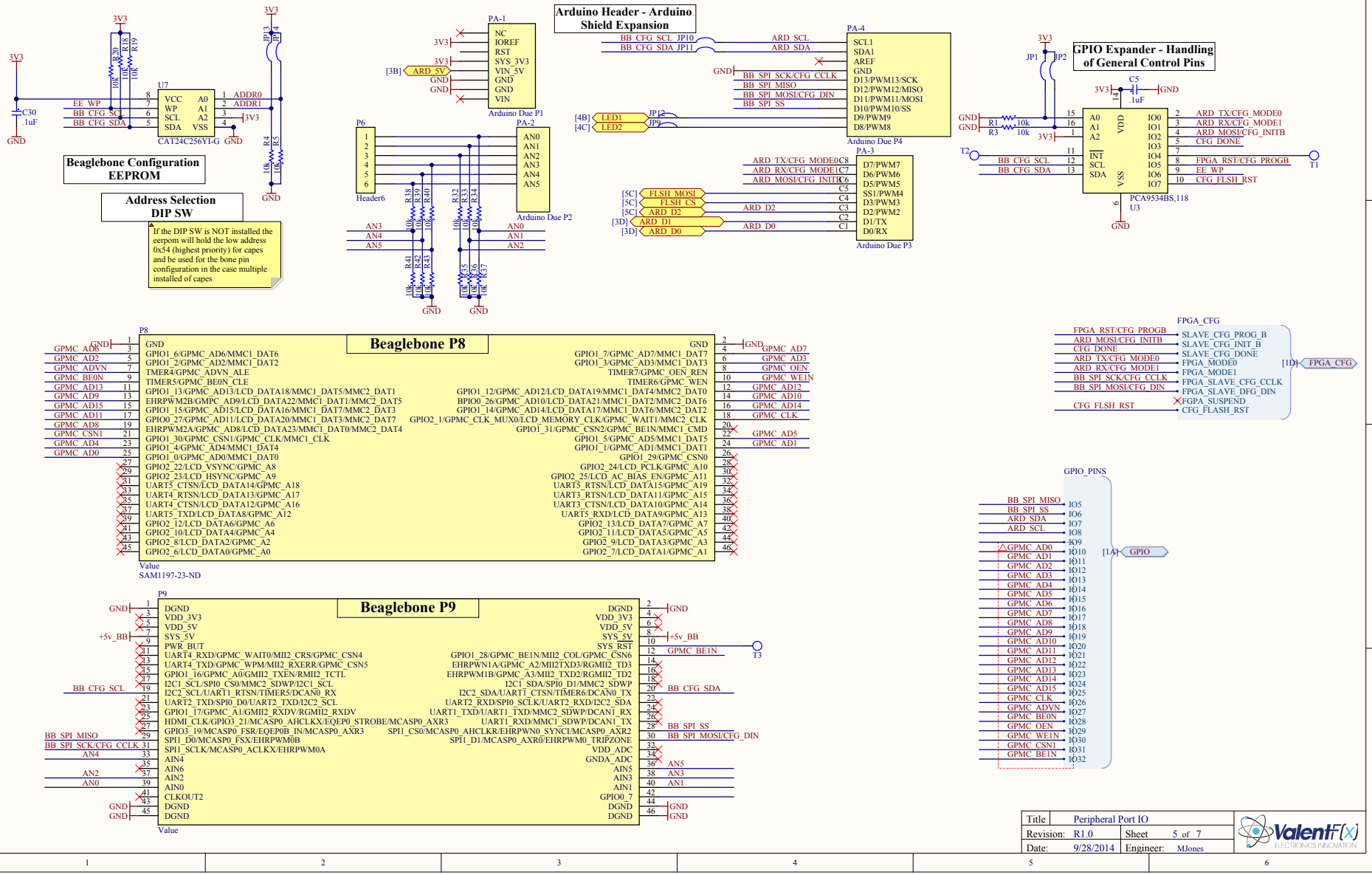
ValentFX ELECTRONICS INNOVATION

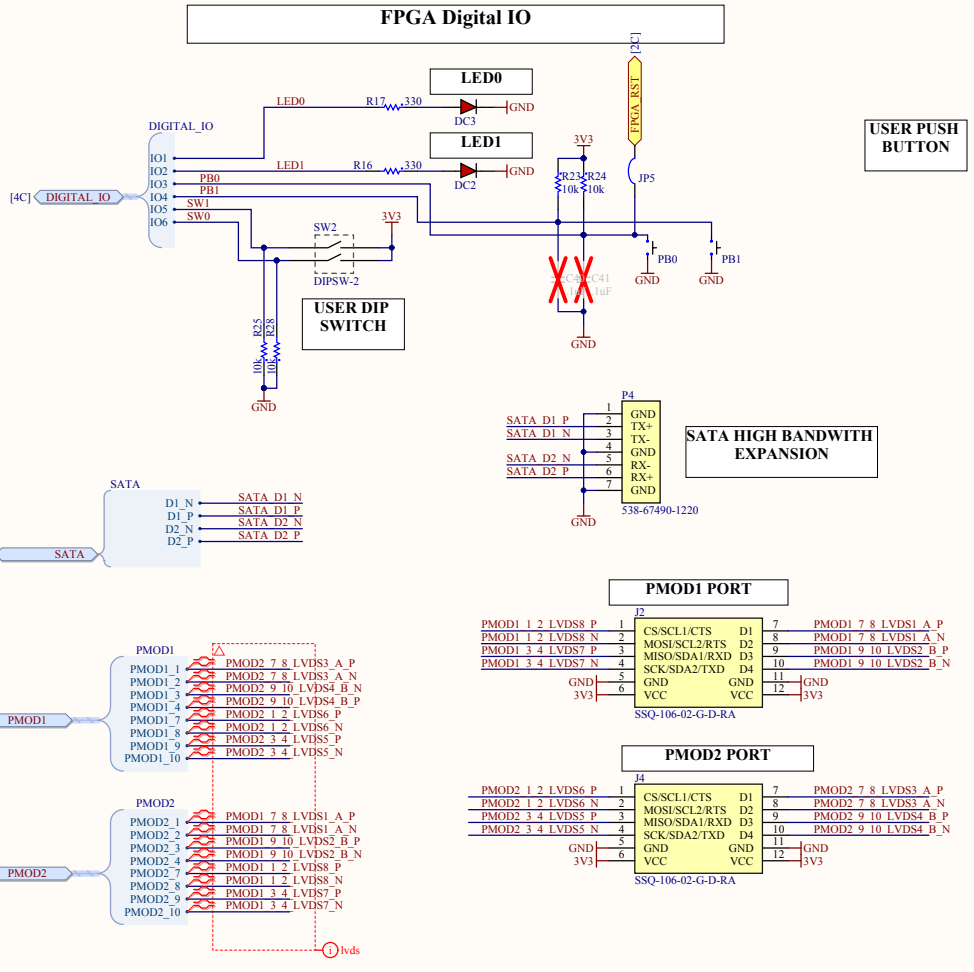

VCC_INT
VCC_AUX
VCCO
VCC1
VCC2
VCC3
Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution
U4F
XC6SLX9-2TQG144C
U4G
XC6SLX9-2TQG144C
U4E
XC6SLX9-2TQG144C
JTAG
U8
M25PE16
FLSH_MOSI
FLSH_CS
FLSH_CS_ARD
FLSH_MOSI_ARD
LED2
FPGA_RST
FPGA_CFG
SLAVE_CFG_PROG_B
SLAVE_CFG_INIT_B
SLAVE_CFG_DONE
FPGA_MODE0
FPGA_MODE1
FPGA_SLAVE_CFG_CCLK
FPGA_SLAVE_CFG_DIN
FGPA_SUSPEND
CFG_FLASH_RST
FPGA_RST/CFG_PROGB
ARD_MOSI/CFG_INITB
CFG_DONE
ARD_TX/CFG_MODE0
ARD_RX/CFG_MODE1
BB_SPI_SCK/CFG_CCLK
BB_SPI_MOSI/CFG_DIN
CFG_FLSH_RST
M1 default 1
M0 default 1
CFG_FLASH_RST will force all flash pins into HiZ removing any conflict while the BB is configuring FPGA
M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig
Title FPGA Configuration
Revision: R1.0
Sheet 3 of 7
Date: 9/28/2014
Engineer: MJones
ValentF(x)
ELECTRONICS INNOVATION

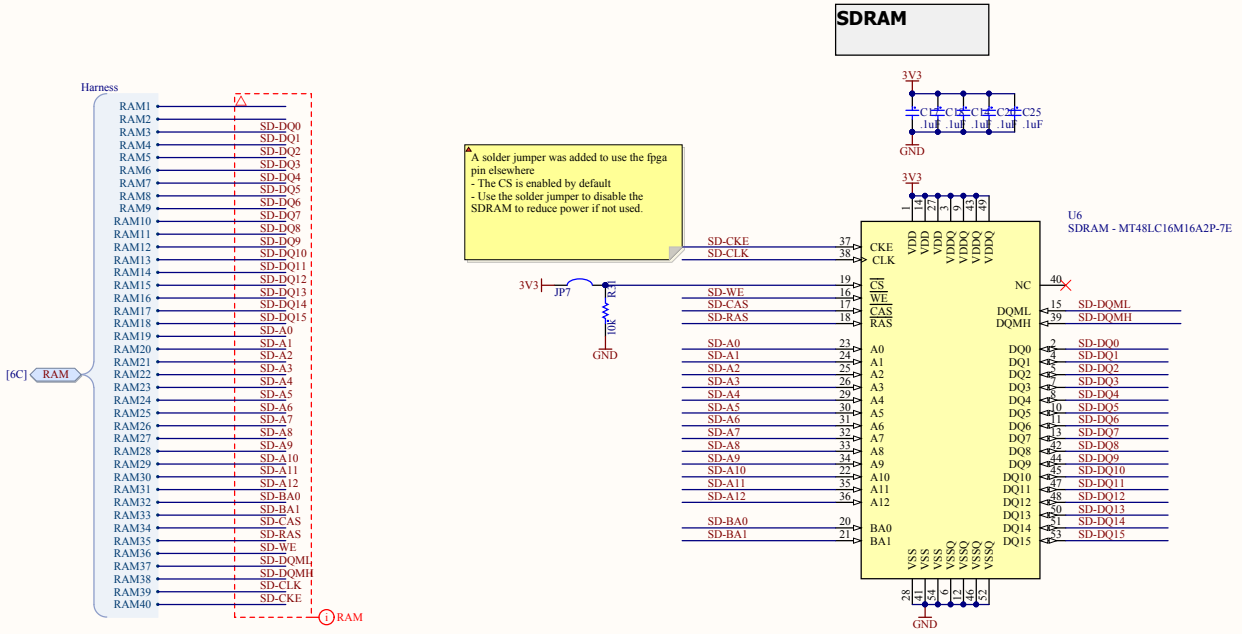


Title	FPGA Logic		
Revision:	R1.0	Sheet	4 of 7
Date:	9/28/2014	Engineer:	MJones

ValentF(x) ELECTRONICS INNOVATION


Beaglebone Configuration EEPROM
CAT24C256YI-G
Address Selection DIP SW
If the DIP SW is NOT installed the eerpom will hold the low address 0x54 (highest priority) for capes and be used for the bone pin configuration in the case multiple installed of capes
Arduino Header - Arduino Shield Expansion
Arduino Due P1
Arduino Due P2
Arduino Due P3
Arduino Due P4
GPIO Expander - Handling of General Control Pins
PCA9534BS,118
Beaglebone P8
Beaglebone P9
FPGA_CFG
GPIO_PINS
Title Peripheral Port IO
Revision: R1.0
Sheet 5 of 7
Date: 9/28/2014
Engineer: MJones
ValentF(x)
ELECTRONICS INNOVATION


FPGA Digital IO
LED0
LED1
USER PUSH BUTTON
USER DIP SWITCH
SATA HIGH BANDWITH EXPANSION
PMOD1 PORT
PMOD2 PORT
DIGITAL_IO
SATA
PMOD1
PMOD2
SSQ-106-02-G-D-RA
538-67490-1220
Title Digital IO
Revision: R1.0
Sheet 6 of 7
Date: 9/28/2014
Engineer: MJones
ValentF(x)
ELECTRONICS INNOVATION



Title	RAM		
Revision:	R1.0	Sheet	7 of 7
Date:	9/28/2014	Engineer:	MJones

ValentF(x) ELECTRONICS INNOVATION