Figure 2a: I/O interface of the DE10-Standard FPGA board

Figure 2b: I/O interface of the DE2-115 FPGA board

Figure 2 : I/O interface of the DE10-Standard and the DE2-115 FPGA boards

The digital system is composed of two concurrent parts, combinatorial and synchronous, as shown in Figures 3 and 4.

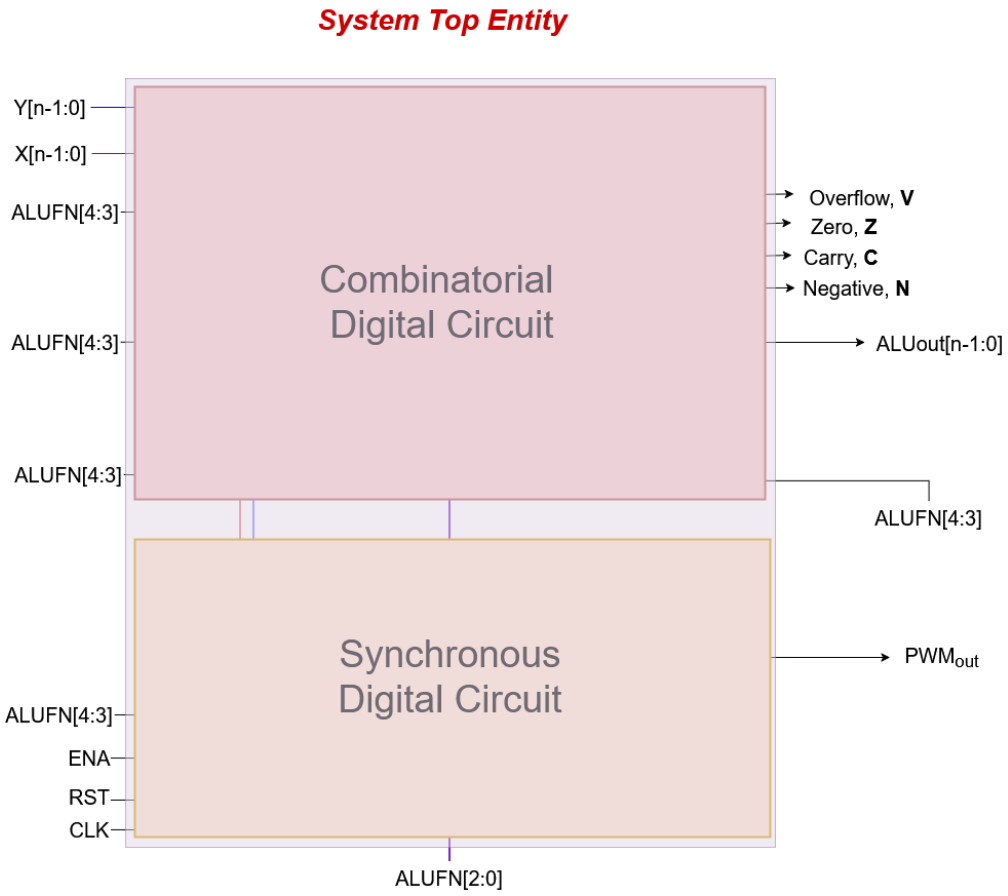


Figure 3: Digital System subparts

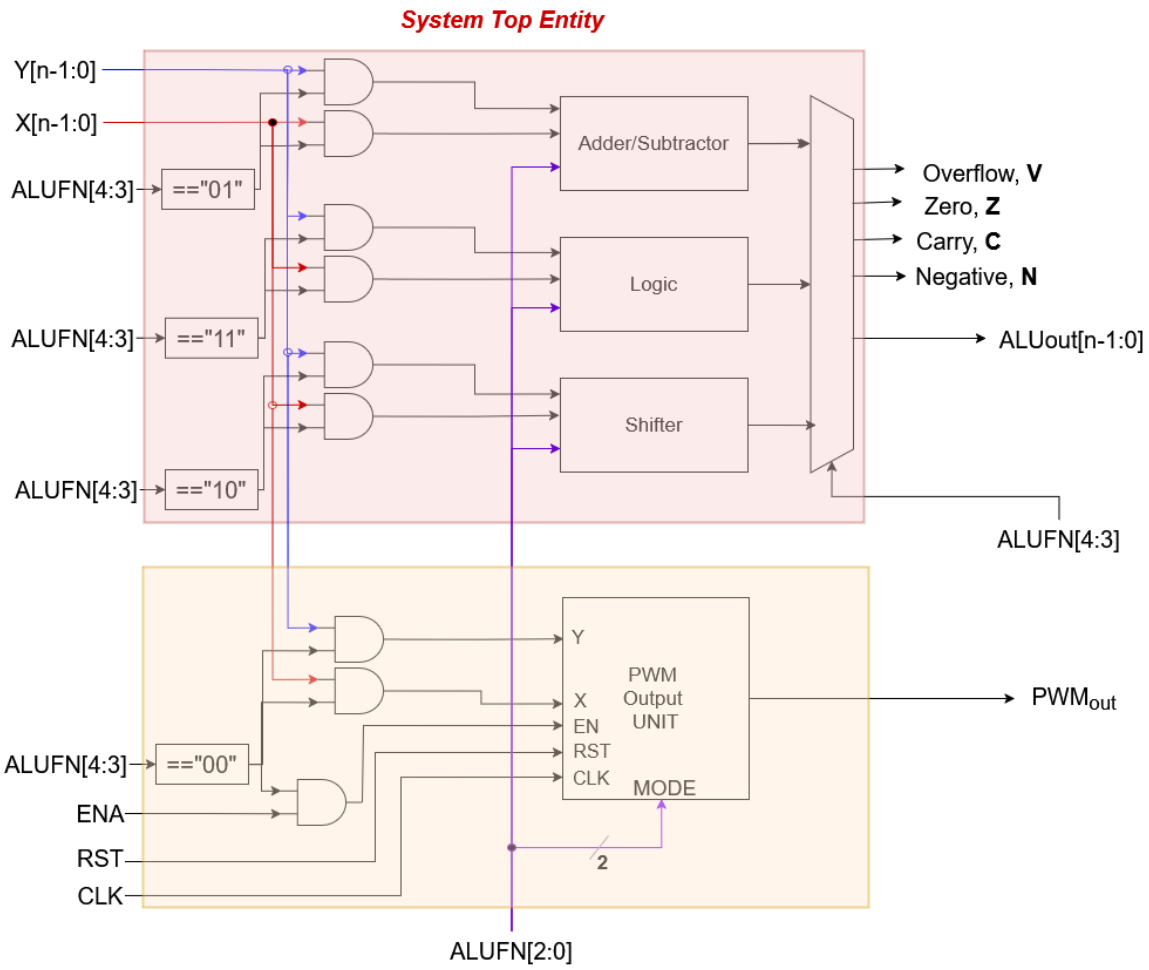


Figure 4: Digital System subparts architecture

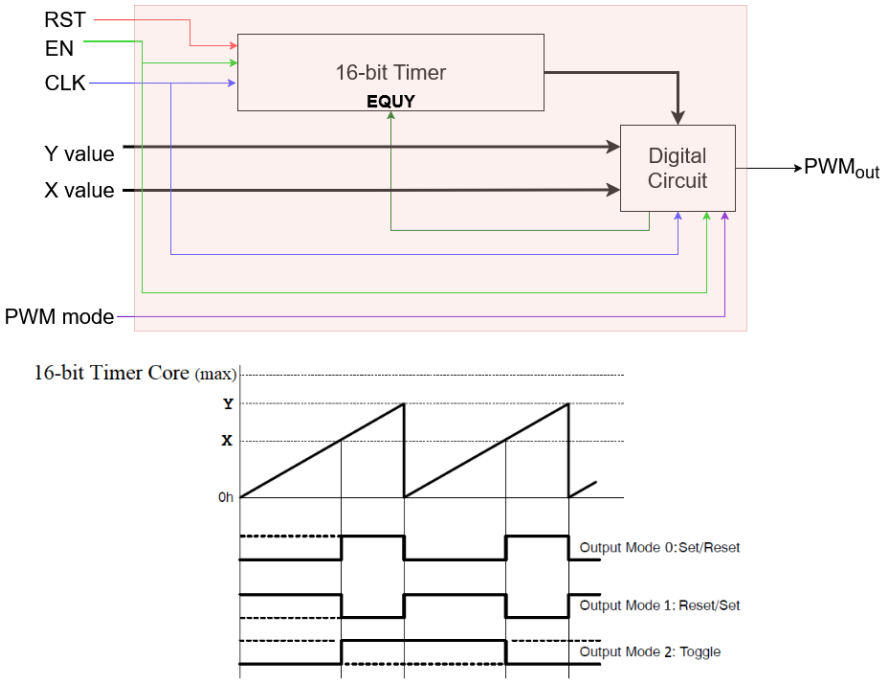
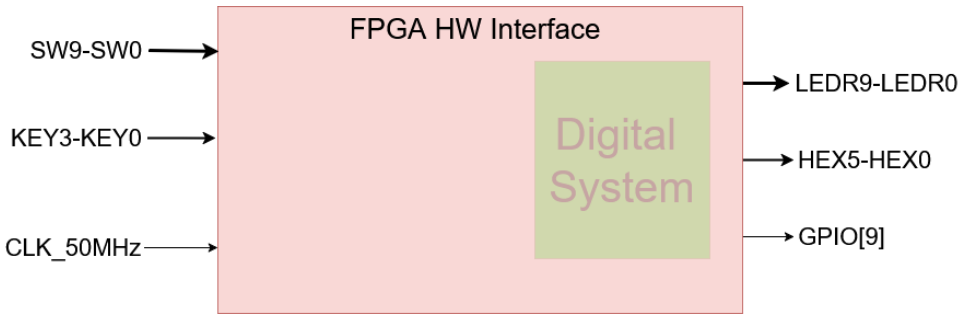


Figure 5: PWM output unit architecture

The whole system must be connected to the Altera board interfaces according to the following diagram:



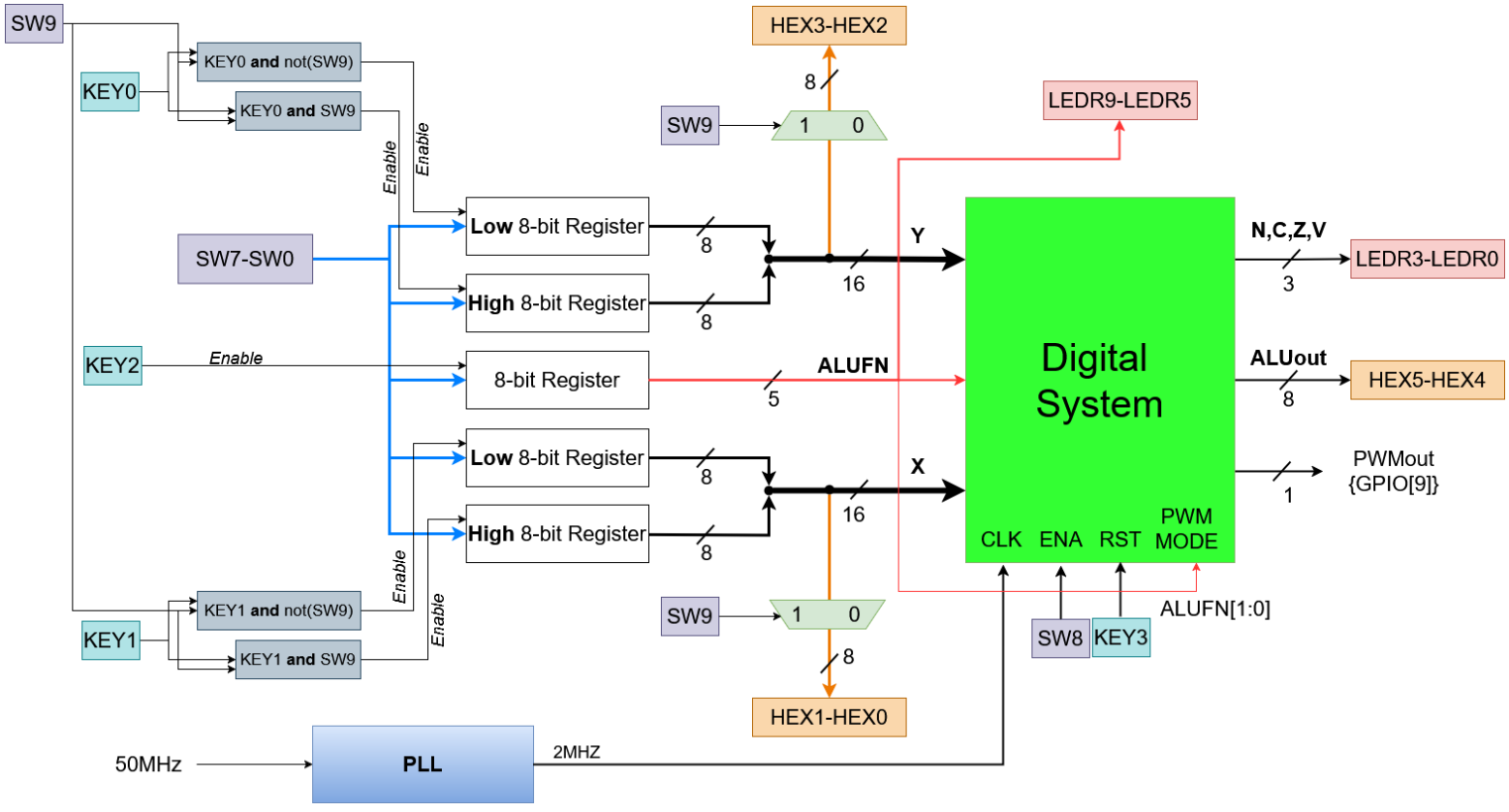


Figure 6: Digital system with I/O interface

The ISA of the combinatorial subpart is given in Figure 7, which is associated with the LAB1 task.

Function Type	Decimal value	ALUFN	Operation	Note
PWM Output (*Y and X are 16-bit width*)	0	**00**000	PWM MODE0	PWM Mode is Set/Reset
	1	**00**001	PWM MODE1	PWM Mode is Reset/Set
	2	**00**010	PWM MODE2	PWM Mode is Toggle
Arithmetic (*Y and X are 8-bit width*)	8	**01**000	Res=Y+X	
	9	**01**001	Res=Y-X	Used also for comparison operation
	10	**01**010	Res=neg(X)	
	11	**01**011	Res=Y+1	Increment of Y in one
	12	**01**100	Res=Y-1	Decrement of Y in one
	13	**01**101	Res=swap(Y)	Res=(Y_{LSHW}, Y_{MSHW})
Shift (*Y and X are 8-bit width*)	16	**10**000	Res=SHL Y,X(k-1 to 0)	Shift Left Y of q≙X(k-1 ..0) times Res=Y(n-1-q…0)#(q@0) ***When*** $k = log_2 n$
	17	**10**001	Res=SHR Y,X(k-1 to 0)	Shift Right Y of q≙X(k-1 ..0) times Res=(q@0)#Y(n-1...q) ***When*** $k = log_2 n$
Boolean (*Y and X are 8-bit width*)	24	**11**000	Res=not(Y)	
	25	**11**001	Res=Y or X	
	26	**11**010	Res=Y and X	
	27	**11**011	Res=Y xor X	
	28	**11**100	Res=Y nor X	
	29	**11**101	Res=Y nand X	
	30	**11**110	Res=Y xnor X	

Figure 7: ISA of the combinatorial subpart of digital design