

Lab 3

MPEG-2 SIP Design and Realization

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Outline

3.1 Design Environment of the PXA/255 FPGA Module

3.2 IP Design and Realization of IDCT

3.3 IP Functional Verification

3.1 Design Environment of the FPGA Module

3.1 Design Environment of the PXA/255 FPGA Module

3.2 IP Design and Realization of IDCT

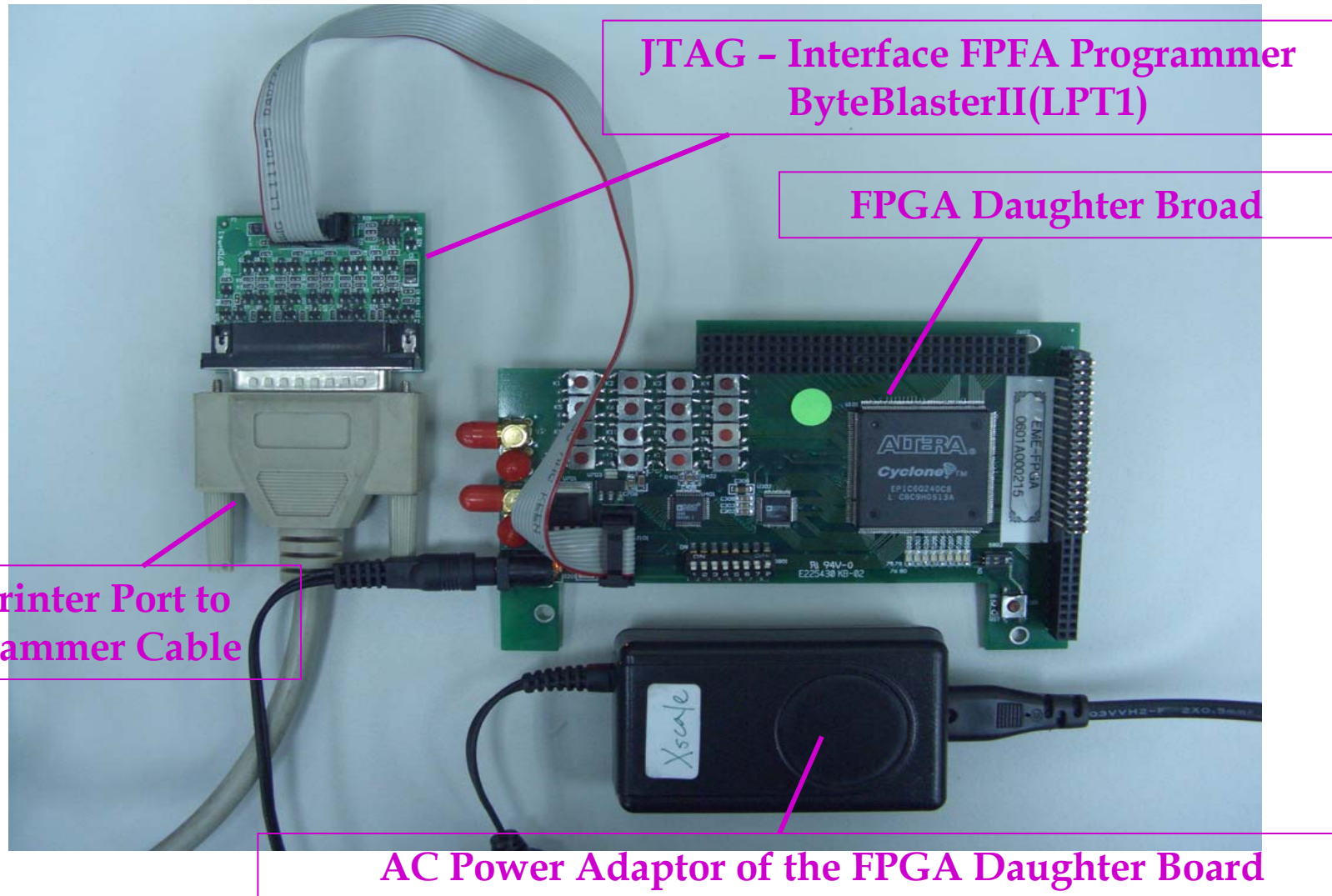
3.3 IP Functional Verification

3.1 Design Environment of the FPGA Module

- ◆ FPGA Design Environments
- ◆ FPGA Daughter Board & Hardware Debug Tools
- ◆ Procedures the FPGA Programming

3.1 Design Environment of the FPGA Module

■ FPGA Daughter Board & Hardware Debug Tools



3.1 Design Environment of the FPGA Module

■ FPGA Design Environments

◆ FPGA IDE Tool

- Quartus-II Version 5.1
- + Service Pack 2

◆ FPGA Daughter Board

- Altera EP1C6Q240C8 Specifications:

Feature	EP1C6
LEs	5,980
M4K RAM blocks (128 x 36 bits)	20
Total RAM bits	92,160
PLLs	2
Maximum USER I/O pins	185

3.1 Design Environment of the FPGA Module

■ FPGA Design Environments

◆ Hardware Debug Tool

- JTAG - Interface FPGA Programmer
- PC Printer Port to Programmer Cable
- AC Power Adaptor of the FPGA Daughter Board

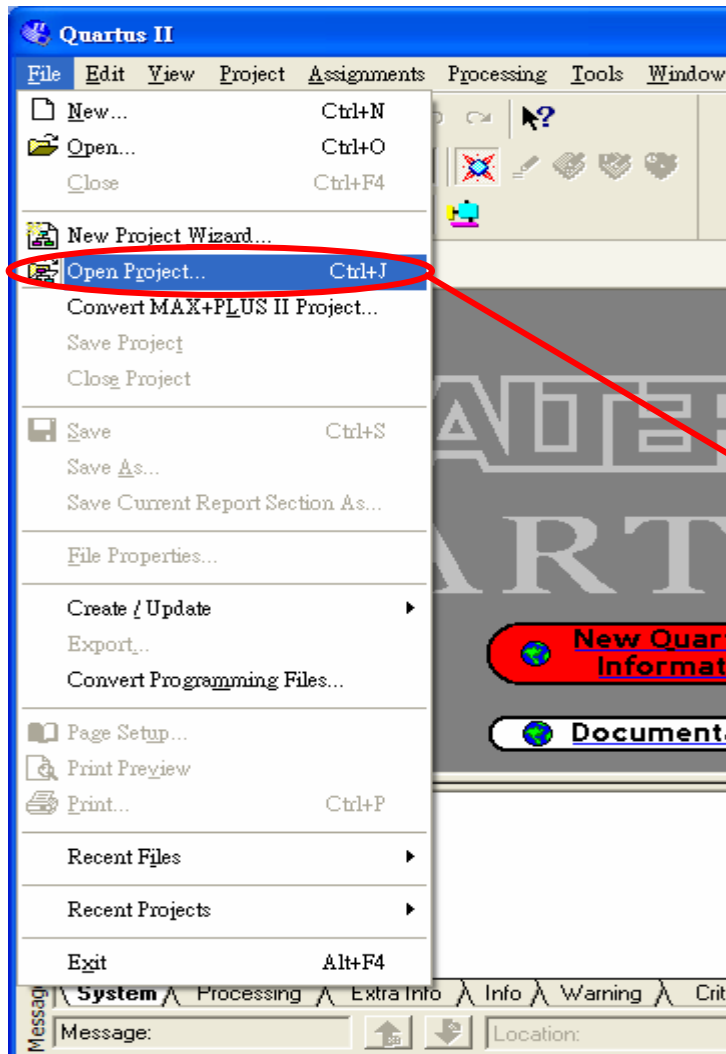
3.1 Design Environment of the FPGA Module

■ Procedures of the FPGA Module Programming

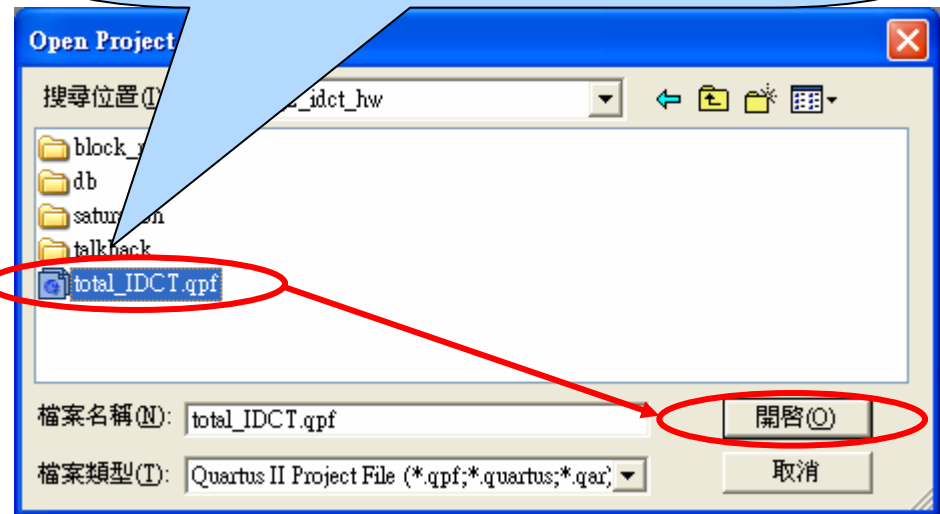
1. Open Project
2. FPGA Device Selection
3. Compilation
4. Programming
5. Programming Status Check

3.1 Design Environment of the FPGA Module

■ Procedure 1 - Open Project

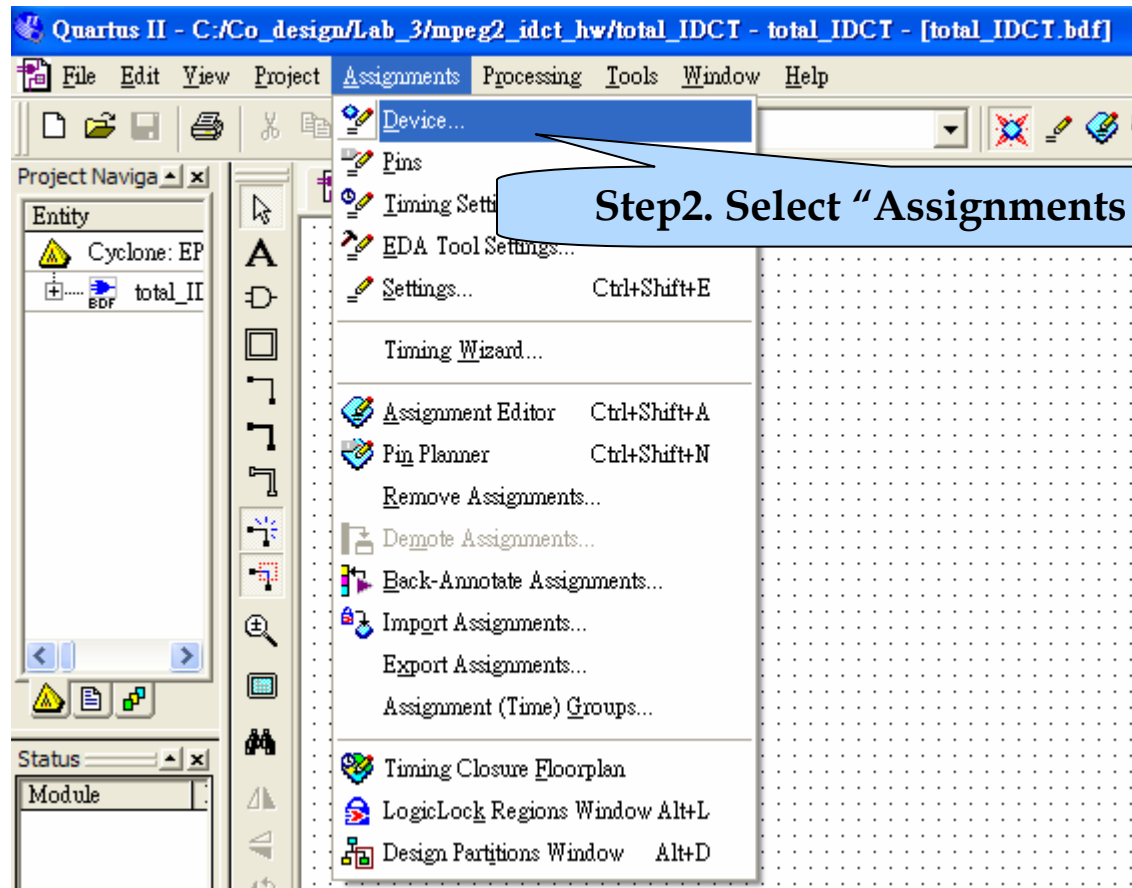


Step1. Select the Project :
C:/Co_design/Lab_3/mpeg2_idct_hw/
total_IDCT.qpf



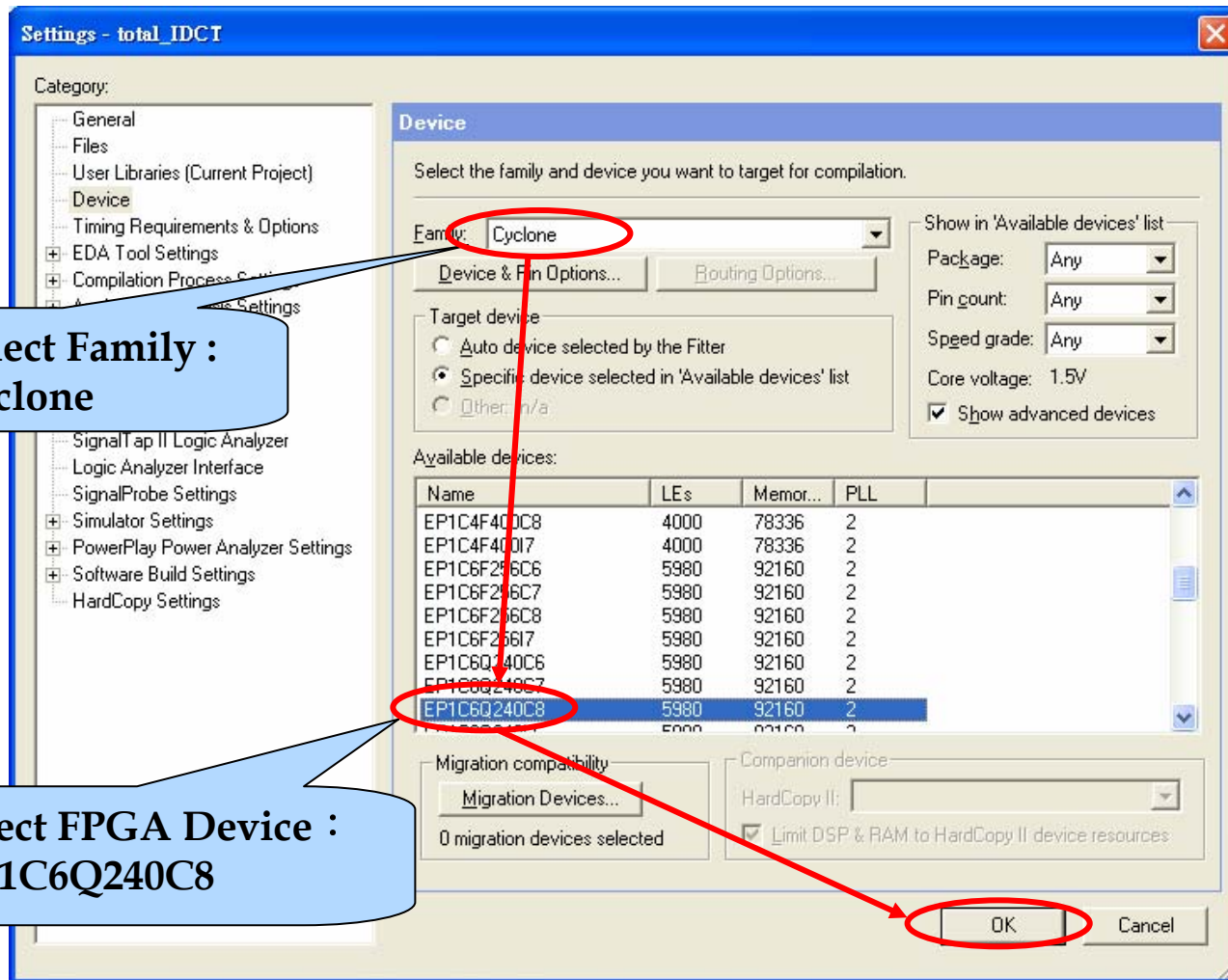
3.1 Design Environment of the FPGA Module

■ Procedure 2 - FPGA Device Selection



3.1 Design Environment of the FPGA Module

■ Procedure 2 - FPGA Device Selection



3.1 Design Environment of the FPGA Module

■ Procedure 2 - FPGA Device Selection

The screenshot shows the 'Device & Pin Options' dialog box in the FPGA Design Environment. The dialog has several tabs: 'General', 'Configuration', 'Pin Placement', 'Error Detection CRC', 'Programming Files', and 'Unused Pins'. The 'Configuration' tab is selected. The 'Configuration scheme' dropdown is set to 'Active Serial (can use Configuration Device)'. The 'Configuration mode' dropdown is set to 'Standard'. The 'Configuration device' dropdown is set to 'EPCS1'. The 'Description' text box contains the text: 'The method used to configure the device. Two configuration schemes are available: Passive Serial (PS) and Active Serial (AS)'. The 'Reset' button is at the bottom right. The '確定' (OK) button is at the bottom right, and the '取消' (Cancel) button is at the bottom right.

Step5. Click "Device & Pin Options.."

Step6. Click "Configuration"

Step7. Select Configuration Scheme : Active Serial

Step8. Select Configuration Device : EPCS1

確定

3.1 Design Environment of the FPGA Module

■ Procedure 3 - Compilation

Quartus II - C:\Co_design\Lab_3\mpeg2_idct_hw\total_IDCT - total_IDCT - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

total_IDCT

Project Navigator

Entity

Cyclone: EP

total_IDCT

total_IDCT.bdf

Compilation Report - Flow Summary

Flow Summary

Flow Elapsed Time

Flow Log

Analysis & Synthesis

Fitter

Assembler

Timing Analyzer

Flow Status

Successful - Thu Sep 13 16:28:47 2007

Quartus II Version

5.1 Build 216 03/06/2006 SP 2 SJ Full Version

Revision Name

total_IDCT

Top-level Entity Name

total_IDCT

Family

Cyclone

Device

Timing Models

Met timing requirements

Total logic elements

Total pins

Total virtual pins

Total memory bits

Total PLLs

Successful Message

Quartus II

Full Compilation was successful (298 warnings)

確定

Info: too from clock "CLKIN" to destination pin "SA_D[1]" through memory "RAM3:inst22\altsyncram:altsyncram_component\altsyncram_54e1:auto_generatedram_block1a8-

Info: Longest tpd from source pin "nSA-WE" to destination pin "SA_D[28]" is 15.891 ns

Info: th for memory "RAM1:inst13\altsyncram:altsyncram_component\altsyncram_pj1:auto_generatedram_block1a11~porta_datain_reg16" (data pin = "SA_D[19]", clock pin

Info: Quartus II Timing Analyzer was successful. 0 errors, 30 warnings

Info: Quartus II Full Compilation was successful. 0 errors, 298 warnings

Messages

System Processing Extra Info Info Warning Critical Warning Error Suppressed

Message: 0 of 909

Location:

Locate

For Help, press F1

Idle

NUM

3.1 Design Environment of the FPGA Module

■ Procedure 4 - Programming

The screenshot displays the Quartus II software interface. The title bar indicates the project path: "C:/Co_design/Lab_3/mpeg2_idct_hw/total_IDCT - total_IDCT - [total_IDCT.cdf]". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons, with the "Programming Setup" icon (a hand holding a chip) circled in red. A blue callout box with the text "Step10. Click 'Programming Setup' Icon" points to this icon. A red arrow points from the text "FPGA Programming" to the same icon. The Project Navigator on the left shows the project hierarchy: Entity, Cyclone: EP, and total_IDCT. The Status window on the left shows the compilation process: Full Compilation, Analysis & Syn, Fitter, Assembler, and Timing Analyzer. The Messages window at the bottom shows the compilation results, including information about the clock "CLKIN" and the longest tpd from source pin "nSA-WE" to destination pin "SA_D[28]" (15.891 ns). The Messages window also indicates that the Quartus II Timing Analyzer was successful with 0 errors and 30 warnings, and the Quartus II Full Compilation was successful with 0 errors and 298 warnings.

Step10. Click "Programming Setup" Icon

FPGA Programming

3.1 Design Environment of the FPGA Module

■ Procedure 4 - Programming

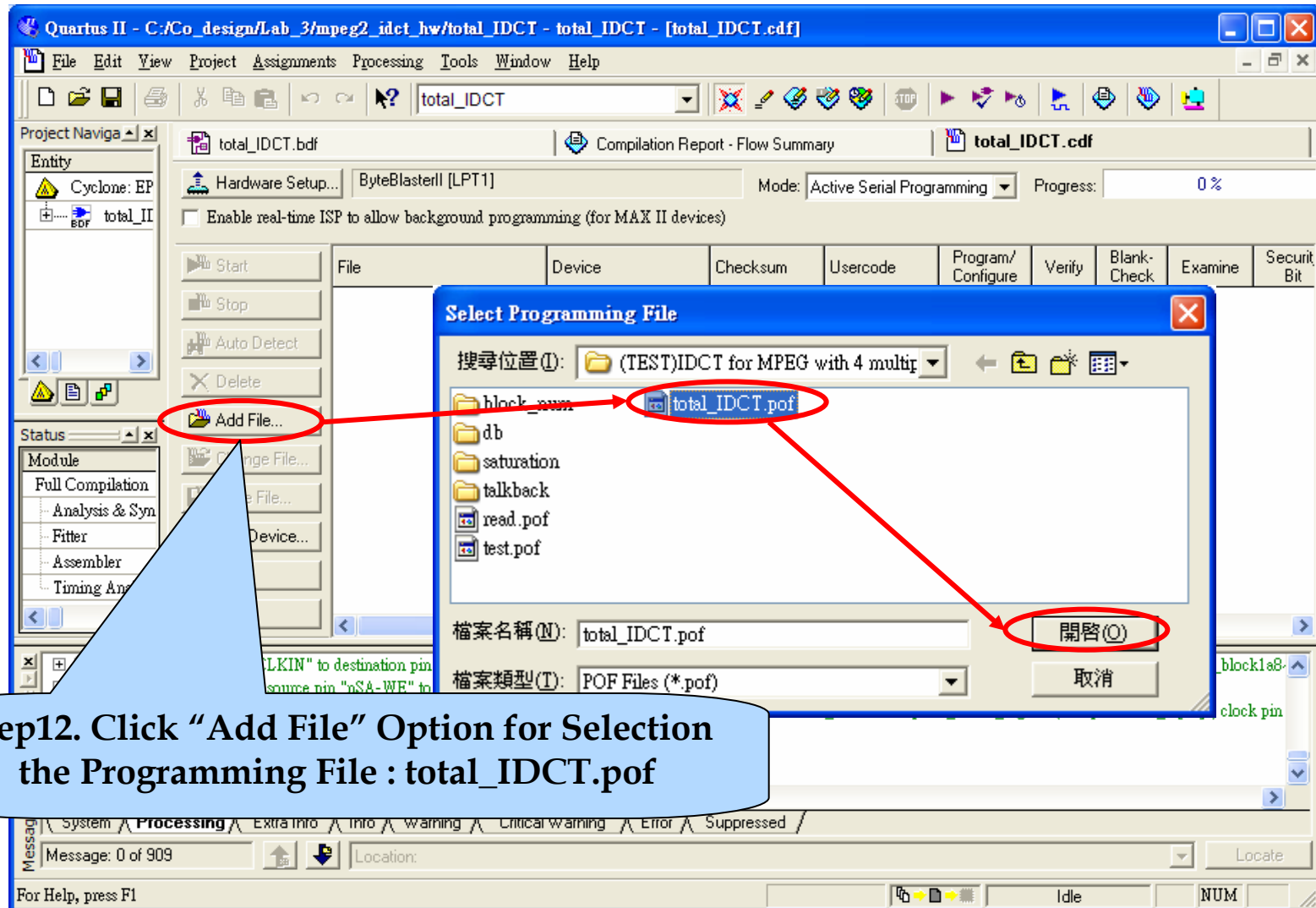
Step11. Click "Hardware Setup" Option for Selection the FPGA Programmer: ByteBlasterII(LPT1)

The screenshot shows the Quartus II software interface. The main window displays the 'Project Navigator' on the left, the 'Messages' pane at the bottom, and the 'Processing' tab. The 'Hardware Setup' dialog box is open, showing the 'Hardware Settings' tab. The 'Currently selected hardware' dropdown menu is set to 'ByteBlasterII [LPT1]'. The 'Available hardware items' table lists 'ByteBlasterII' with 'Local' as the server and 'LPT1' as the port. The 'Close' button is highlighted with a red circle. Red arrows point from the 'Hardware Setup' button in the main window to the dialog box, and from the 'ByteBlasterII [LPT1]' dropdown to the 'Close' button.

Hardware	Server	Port
ByteBlasterII	Local	LPT1

3.1 Design Environment of the FPGA Module

■ Procedure 4 - Programming



3.1 Design Environment of the FPGA Module

■ Procedure 4 - Programming

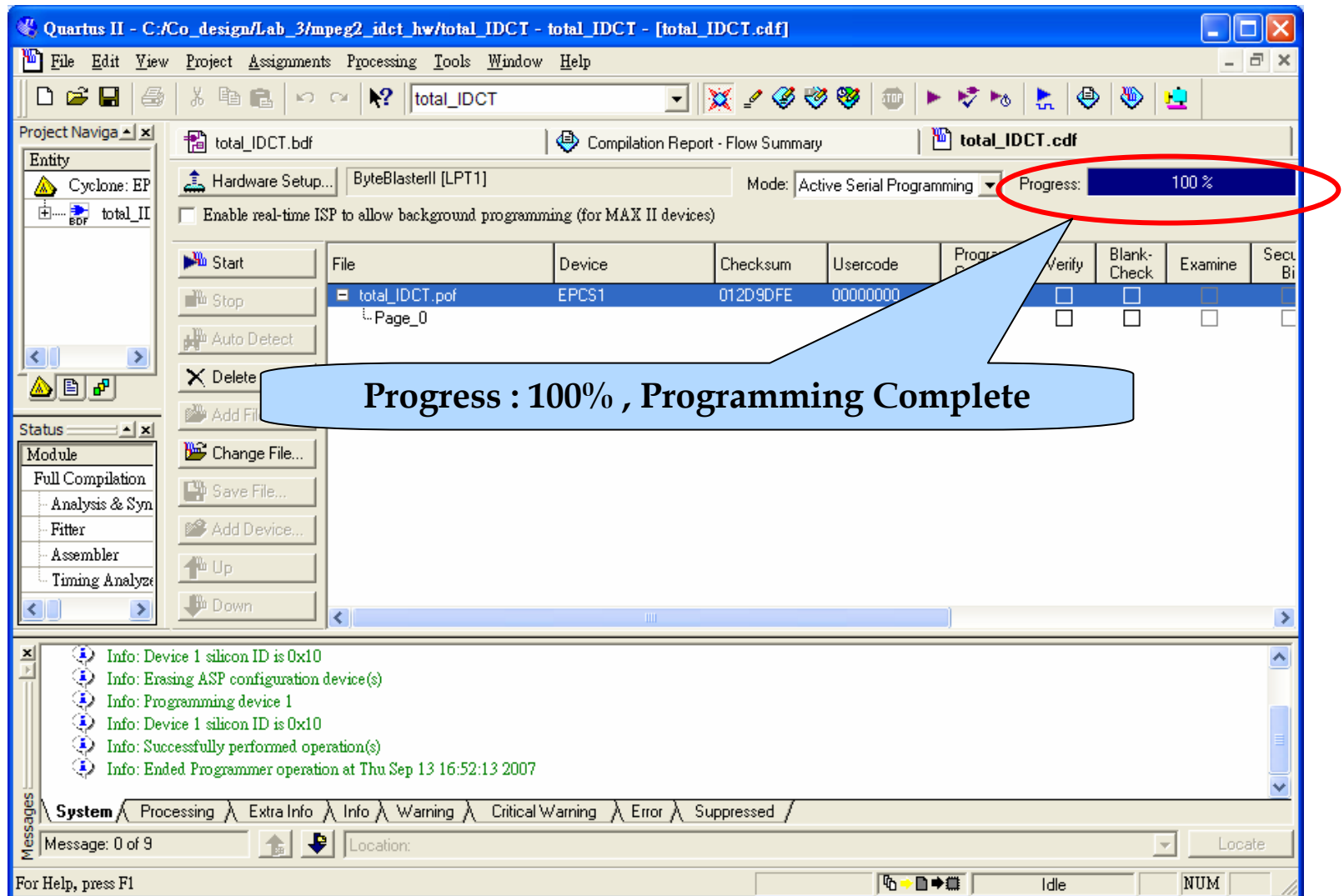
The screenshot shows the Quartus II software interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons for file operations and project management. The Project Navigator on the left shows the project structure. The main window displays the 'total_IDCT.cdf' file, which is selected in the 'File' list. The 'Device' column shows 'EPCS1'. The 'Checksum' column shows '013090FF'. The 'Usercode' column shows '00000000'. The 'Program/Configure' checkbox is checked. The 'Verify' checkbox is unchecked. The 'Blank-Check' checkbox is unchecked. The 'Examine' checkbox is unchecked. The 'Secu Bi' checkbox is unchecked. The 'Start' button is circled in red. A callout box points to the 'Start' button with the text: 'Step14. Click "Start" Option for Programming Design File to FPGA'. Another callout box points to the 'Program/Configure' checkbox with the text: 'Step13. Select the Programming Option'. The bottom of the window shows the 'Messages' pane with the following text: 'Info: too from clock "CLKIN" to destination pin "SA_D[1]" through memory "RAM3:inst22altsyncram:altsyncram_componentaltsyncram_54e1:auto_generatedram_block1a8-'. 'Info: Longest tpd from source pin "nSA-WE" to destination pin "SA_D[28]" is 15.891 ns'. 'Info: th for memory "RAM1:inst13altsyncram:altsyncram_componentaltsyncram_pj1:auto_generatedram_block1a11~porta_datain_reg16" (data pin = "SA_D[19]", clock pin'. 'Info: Quartus II Timing Analyzer was successful. 0 errors, 30 warnings'. 'Info: Quartus II Full Compilation was successful. 0 errors, 298 warnings'. The status bar at the bottom shows 'For Help, press F1' and 'Idle'.

Step14. Click "Start" Option for Programming Design File to FPGA

Step13. Select the Programming Option

3.1 Design Environment of the FPGA Module

■ Procedure 5 – Programming Status Check



3.2 IP Design and Realization of IDCT

3.1 Design Environment of the PXA/255 FPGA Module

3.2 IP Design and Realization of IDCT

3.3 IP Functional Verification

3.2 IP Design and Realization of IDCT

- ◆ Introduction to IDCT
- ◆ IDCT IP Design
- ◆ IDCT IP Realization

3.2 IP Design and Realization of IDCT

■ Introduction to IDCT

- ◆ 2D Inverse Discrete Cosine Transform (IDCT) of an $N \times N$ Sample Block

$$Y = A^T X A$$

Where X is a matrix of samples, Y is a matrix of coefficients and A is an $N \times N$ transform matrix.

$$A_{ij} = C_i \cos \frac{(2j+1)i\pi}{2N} \text{ where } C_i = \sqrt{\frac{1}{N}} (i=0), C_i = \sqrt{\frac{2}{N}} (i>0)$$

$$Y_{ij} = \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} C_x C_y X_{xy} \cos \frac{(2j+1)y\pi}{2N} \cos \frac{(2i+1)x\pi}{2N}$$

i, j, x, y : Matrix coordinate (range 0 ~ N-1)

3.2 IP Design and Realization of IDCT

■ Introduction to IDCT

- ◆ The operation complexity of 2D IDCT is very high, 2D IDCT of one $N \times N$, there is the operation amount of N^4 .

(Total operation : 64 multiplication and 64 addition)

- ◆ For the amount of operation decreased, so has proposed the fast algorithms of IDCT.

- IDCT is the orthogonal transform, we can dismantle **two-dimensional IDCT into 2 one-dimensional IDCTs**.

(Total operation : 32 multiplication and 32 addition)

- First time, do the every column
- Second time, do the every row

- The operation complexity is reduced from N^4 to $2N^3$

3.2 IP Design and Realization of IDCT

■ 2D IDCT Design

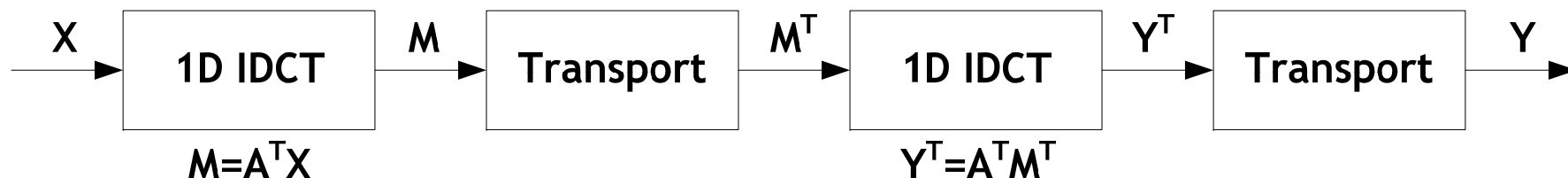
◆ 2D IDCT

$$Y = A^T X A$$

◆ Can be separated into two 1D-IDCT with Transpose Operations

$$\text{LET } A^T X = M$$

$$\text{Then } Y = MA, \quad Y^T = (MA)^T, \quad Y^T = A^T M^T$$



3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

◆ Block Size : 8x8, N=8

$$M = A^T X, \quad M(i, j) = c(j) \sum_{k=0}^7 x(i, k) \cos\left[\frac{(2k+1)j\pi}{16}\right]$$

$$Y = MA, \quad Y(i, j) = c(i) \sum_{k=0}^7 M(v, j) \cos\left[\frac{(2v+1)i\pi}{16}\right]$$

$$\begin{cases} C(k) = \sqrt{\frac{1}{8}} & (k = 0) \\ C(k) = \frac{1}{2} & (k > 0) \end{cases}$$

3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

◆ IDCT Coefficients

■ 7 values of the IDCT coefficients)

Coefficient	Real Value	×256 (Scale to 8-bits Int)	Variables
$\sqrt{1/4}\cos(1\pi/16)$	0.490393	125	a
$\sqrt{1/4}\cos(2\pi/16)$	0.461940	118	b
$\sqrt{1/4}\cos(3\pi/16)$	0.415735	106	c
$\sqrt{1/4}\cos(4\pi/16)$	0.353553	90	d
$\sqrt{1/4}\cos(5\pi/16)$	0.277785	71	e
$\sqrt{1/4}\cos(6\pi/16)$	0.191342	48	f
$\sqrt{1/4}\cos(7\pi/16)$	0.097545	24	g

3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

◆ Coefficients Matrix of 8x8 2D IDCT

$$A^T = \begin{bmatrix} d & a & b & c & d & e & f & g \\ d & c & f & -g & -d & -a & -b & -e \\ d & e & -f & -a & -d & g & b & c \\ d & g & -b & -e & d & c & -f & -a \\ d & -g & -b & e & d & -c & -f & a \\ d & -e & -f & a & -d & -g & b & -c \\ d & -c & f & g & -d & a & -b & e \\ d & -a & b & -c & d & -e & f & -g \end{bmatrix}$$

3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

◆ 2D 8x8 Coefficients Matrix

$$\begin{bmatrix} Y0 \\ Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \\ Y6 \\ Y7 \end{bmatrix} = \begin{bmatrix} d & a & b & c & d & e & f & g \\ d & c & f & -g & -d & -a & -b & -e \\ d & e & -f & -a & -d & g & b & c \\ d & g & -b & -e & d & c & -f & -a \\ d & -g & -b & e & d & -c & -f & a \\ d & -e & -f & a & -d & -g & b & -c \\ d & -c & f & g & -d & a & -b & e \\ d & -a & b & -c & d & -e & f & -g \end{bmatrix} \begin{bmatrix} X0 \\ X1 \\ X2 \\ X3 \\ X4 \\ X5 \\ X6 \\ X7 \end{bmatrix}$$

$Y = A^T X$

Total Operations : 64 multiplications + 64 additions

3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

◆ Outputs of 1D - IDCT :

$$Y0 = dX0 + aX1 + bX2 + cX3 + dX4 + eX5 + fX6 + gX7$$

$$Y1 = dX0 + cX1 + fX2 - gX3 - dX4 - aX5 - bX6 - eX7$$

$$Y2 = dX0 + eX1 - fX2 - aX3 - dX4 + gX5 + bX6 + cX7$$

$$Y3 = dX0 + gX1 - bX2 - eX3 + dX4 + cX5 - fX6 - aX7$$

$$Y4 = dX0 - gX1 - bX2 - eX3 + dX4 - cX5 - fX6 + aX7$$

$$Y5 = dX0 - eX1 - fX2 + aX3 - dX4 - gX5 + bX6 - cX7$$

$$Y6 = dX0 - cX1 + fX2 + gX3 - dX4 + aX5 - bX6 + eX7$$

$$Y7 = dX0 - aX1 + bX2 - cX3 + dX4 - eX5 + fX6 - gX7$$

3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

◆ Reorganization 1 :

$$Y0 + Y7 = (dX0 + bX2 + dX4 + fX6) \times 2$$

$$Y1 + Y6 = (dX0 + fX2 - dX4 - bX6) \times 2$$

$$Y2 + Y5 = (dX0 - fX2 - dX4 + bX6) \times 2$$

$$Y3 + Y4 = (dX0 - bX2 + dX4 - fX6) \times 2$$

$$\frac{1}{2} \begin{bmatrix} Y0 + Y7 \\ Y1 + Y6 \\ Y2 + Y5 \\ Y3 + Y4 \end{bmatrix} = \begin{bmatrix} d & b & d & f \\ d & f & -d & -b \\ d & -f & -d & b \\ d & -b & d & -f \end{bmatrix} \begin{bmatrix} X0 \\ X2 \\ X4 \\ X6 \end{bmatrix}$$

3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

◆ Reorganization 2 :

$$Y0 - Y7 = (aX1 + cX3 + eX5 + gX7) \times 2$$

$$Y1 - Y6 = (cX1 - gX3 - aX5 - eX7) \times 2$$

$$Y2 - Y5 = (eX1 - aX3 + gX5 + cX7) \times 2$$

$$Y3 - Y4 = (gX1 - eX3 + cX5 - aX7) \times 2$$

$$\frac{1}{2} \begin{bmatrix} Y0 - Y7 \\ Y1 - Y6 \\ Y2 - Y5 \\ Y3 - Y4 \end{bmatrix} = \begin{bmatrix} a & c & e & g \\ c & -g & -a & -e \\ e & -a & g & c \\ g & -e & c & -a \end{bmatrix} \begin{bmatrix} X1 \\ X3 \\ X5 \\ X7 \end{bmatrix}$$

3.2 IP Design and Realization of IDCT

■ 8x8 2D IDCT Design Example

- ◆ Fast Algorithm: Decomposed 2D 8x8 IDCT to two 1D 4x4 IDCTs

$$\begin{bmatrix} Y_0 \\ Y_1 \\ Y_2 \\ Y_3 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} Y_0 + Y_7 \\ Y_1 + Y_6 \\ Y_2 + Y_5 \\ Y_3 + Y_4 \end{bmatrix} + \frac{1}{2} \begin{bmatrix} Y_0 - Y_7 \\ Y_1 - Y_6 \\ Y_2 - Y_5 \\ Y_3 - Y_4 \end{bmatrix}$$
$$\begin{bmatrix} Y_7 \\ Y_6 \\ Y_5 \\ Y_4 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} Y_0 + Y_7 \\ Y_1 + Y_6 \\ Y_2 + Y_5 \\ Y_3 + Y_4 \end{bmatrix} - \frac{1}{2} \begin{bmatrix} Y_0 - Y_7 \\ Y_1 - Y_6 \\ Y_2 - Y_5 \\ Y_3 - Y_4 \end{bmatrix}$$

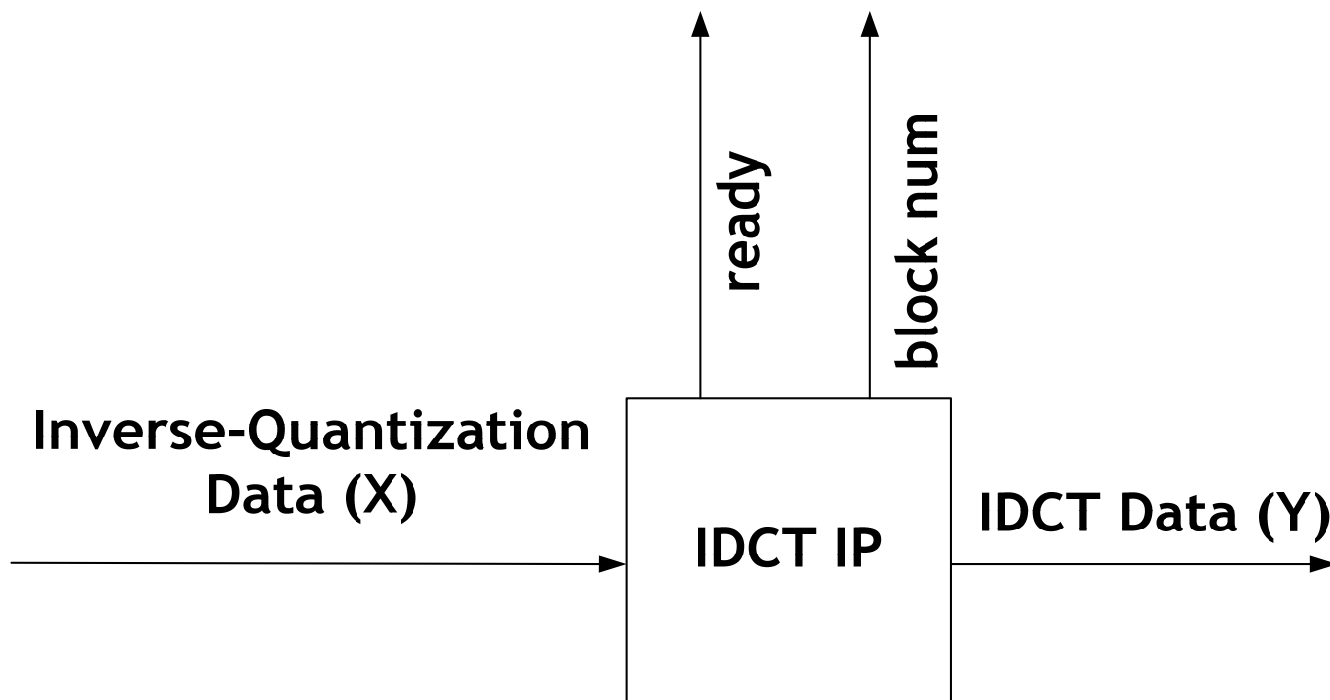
3.2 IP Design and Realization of IDCT

■ IDCT IP Realization

- ◆ IDCT IP Architecture
- ◆ IDCT IP Block Function
- ◆ IDCT IP Circuit Design

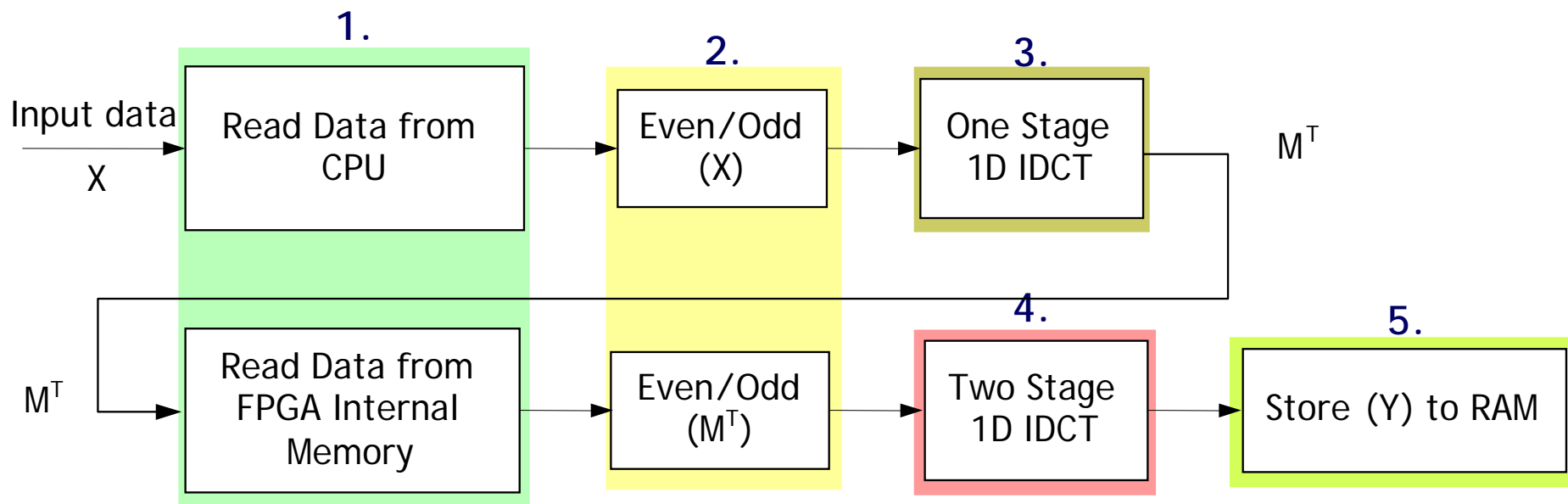
3.2 IP Design and Realization of IDCT

■ Input / Output of IDCT IP



3.2 IP Design and Realization of IDCT

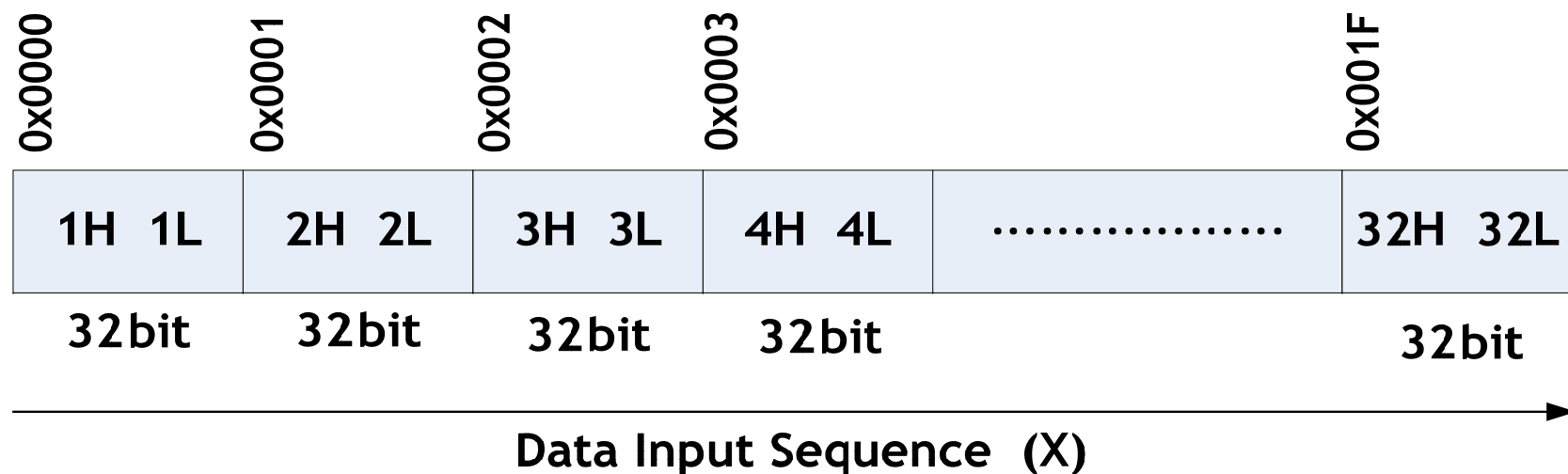
■ IDCT IP Architecture



3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

◆ Data Sequence of the IQ Coefficients from CPU to FPGA



L : [11:0] bit data

H : [27:16] bit data

3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

◆ Relations of the Input Sequence and 8x8 IDCT Coefficients

1 L	5 L	9 L	13 L	17 L	21 L	25 L	29 L
1 H	5 H	9 H	13 H	17 H	21 H	25 H	29 H
2 L	6 L	10 L	14 L	18 L	22 L	26 L	30 L
2 H	6 H	10 H	14 H	18 H	22 H	26 H	30 H
3 L	7 L	11 L	15 L	19 L	23 L	27 L	31 L
3 H	7 H	11 H	15 H	19 H	23 H	27 H	31 H
4 L	8 L	12 L	16 L	20 L	24 L	28 L	32 L
4 H	8 H	12 H	16 H	20 H	24 H	28 H	32 H

■ **L** : 16 LSB bits of a 32-bit data access

■ **H** : 16 MSB bits of a 32-bit data access

3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

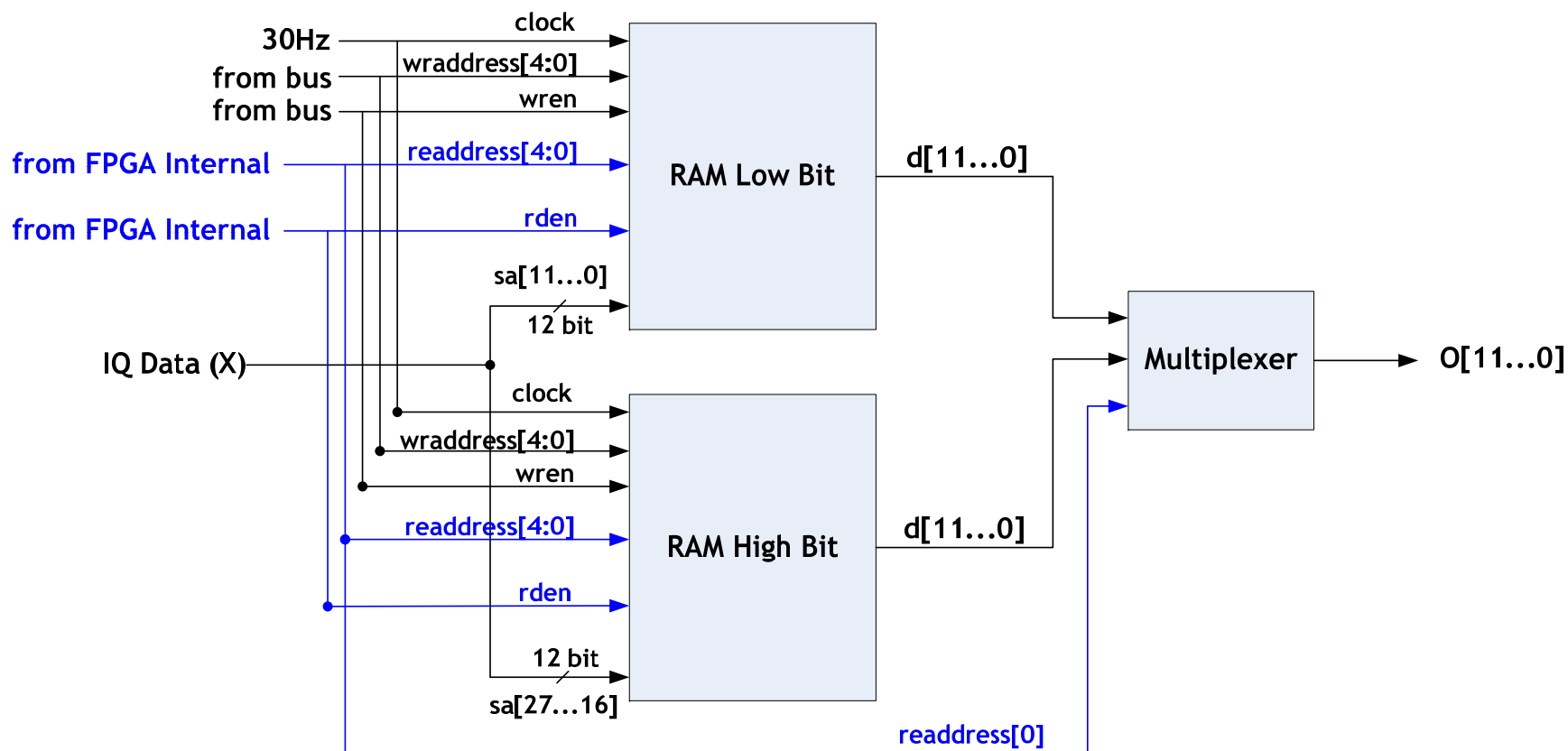
◆ IQ Data Location in the FPGA Internal Memory

RAM – High Bit			RAM – Low Bit		
0x0000	1 H	12bit	0x0000	1 L	12bit
0x0001	2 H	12bit	0x0001	2 L	12bit
0x0002	3 H	12bit	0x0002	3 L	12bit
0x0003	4 H	12bit	0x0003	4 L	12bit
⋮	⋮		⋮	⋮	
0x001F	32 H	12bit	0x001F	32 L	12bit

3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

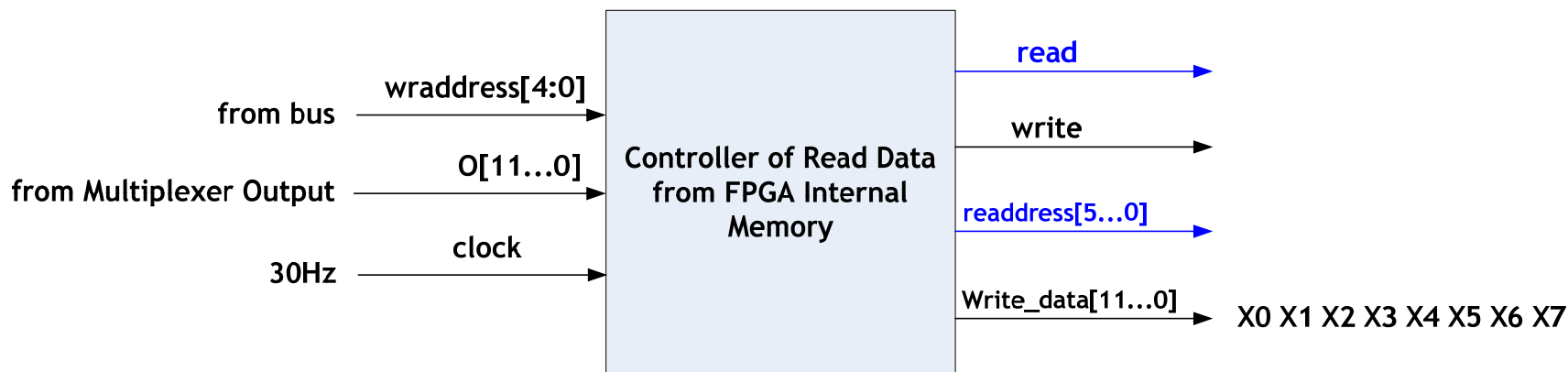
◆ Multiplexer to read and select the data



3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

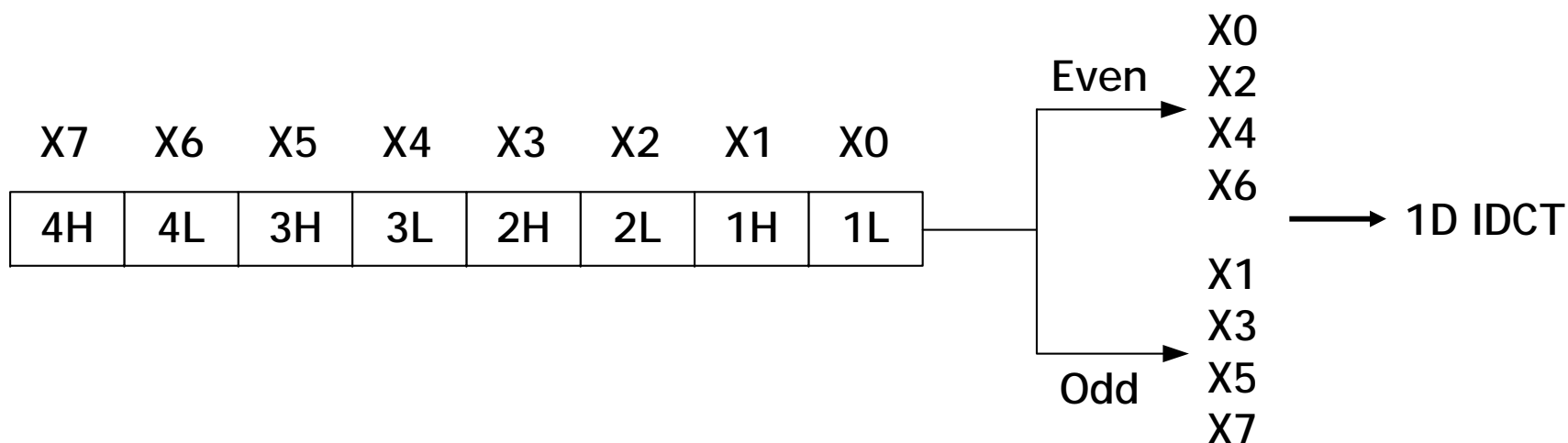
- ◆ Controller of the data read from the FPGA internal memory



3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

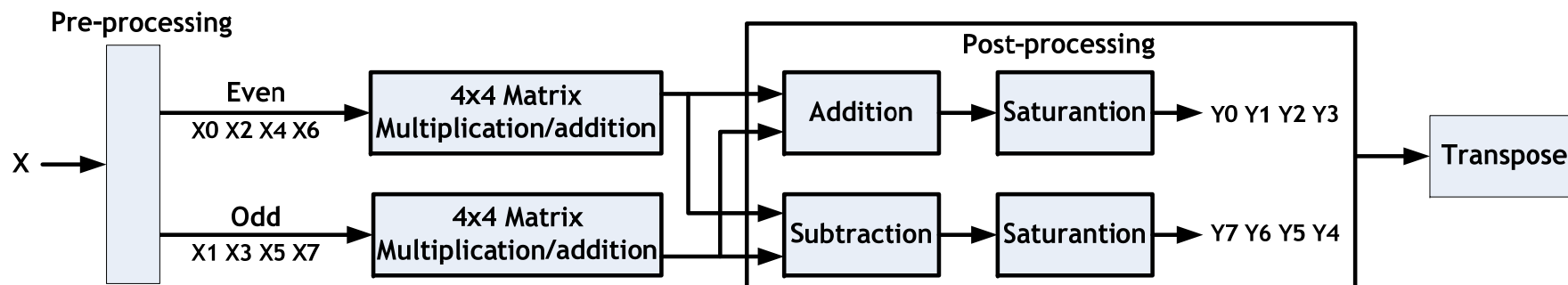
◆ Even/Odd IQ Coefficients of Decomposition



3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

◆ 4x4 1D IDCT

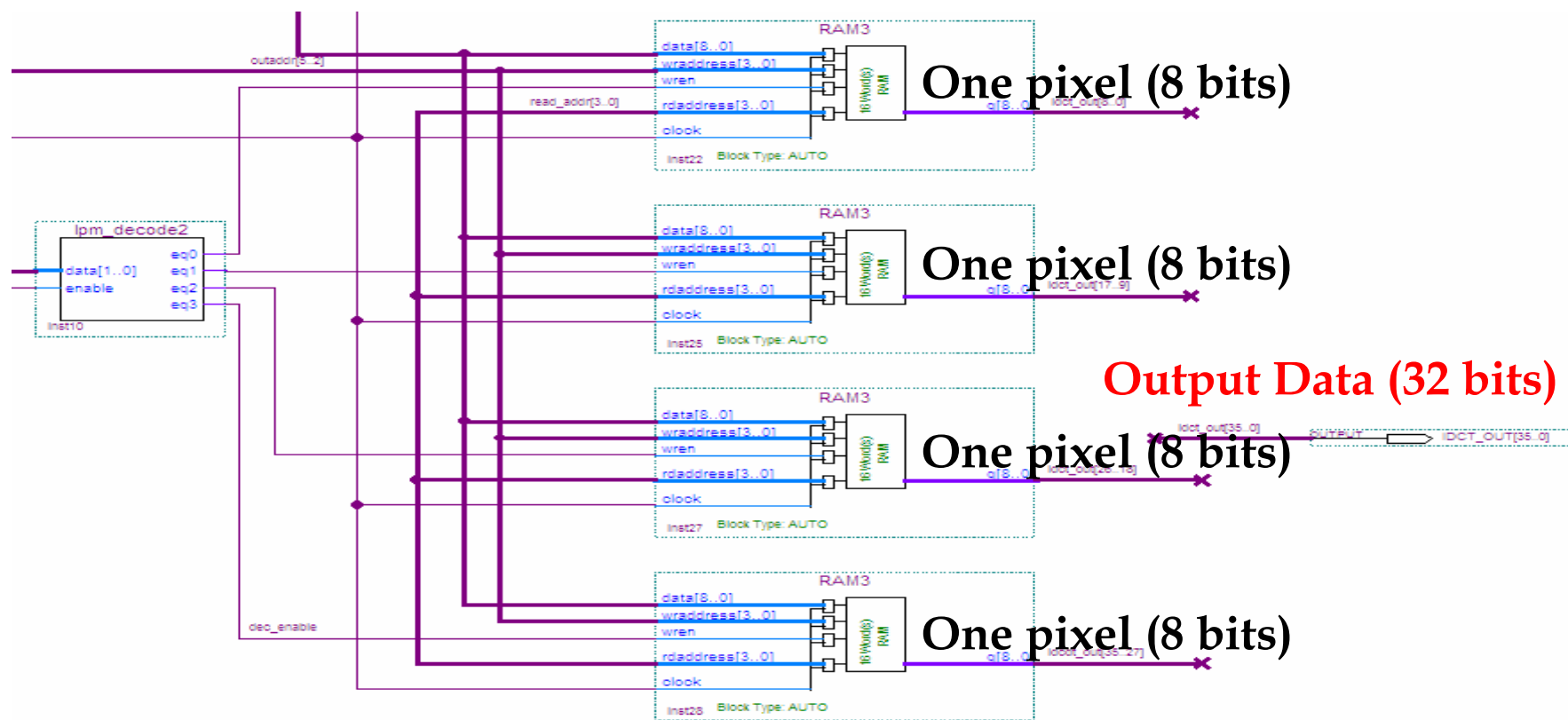


3.2 IP Design and Realization of IDCT

■ IDCT IP Block Function

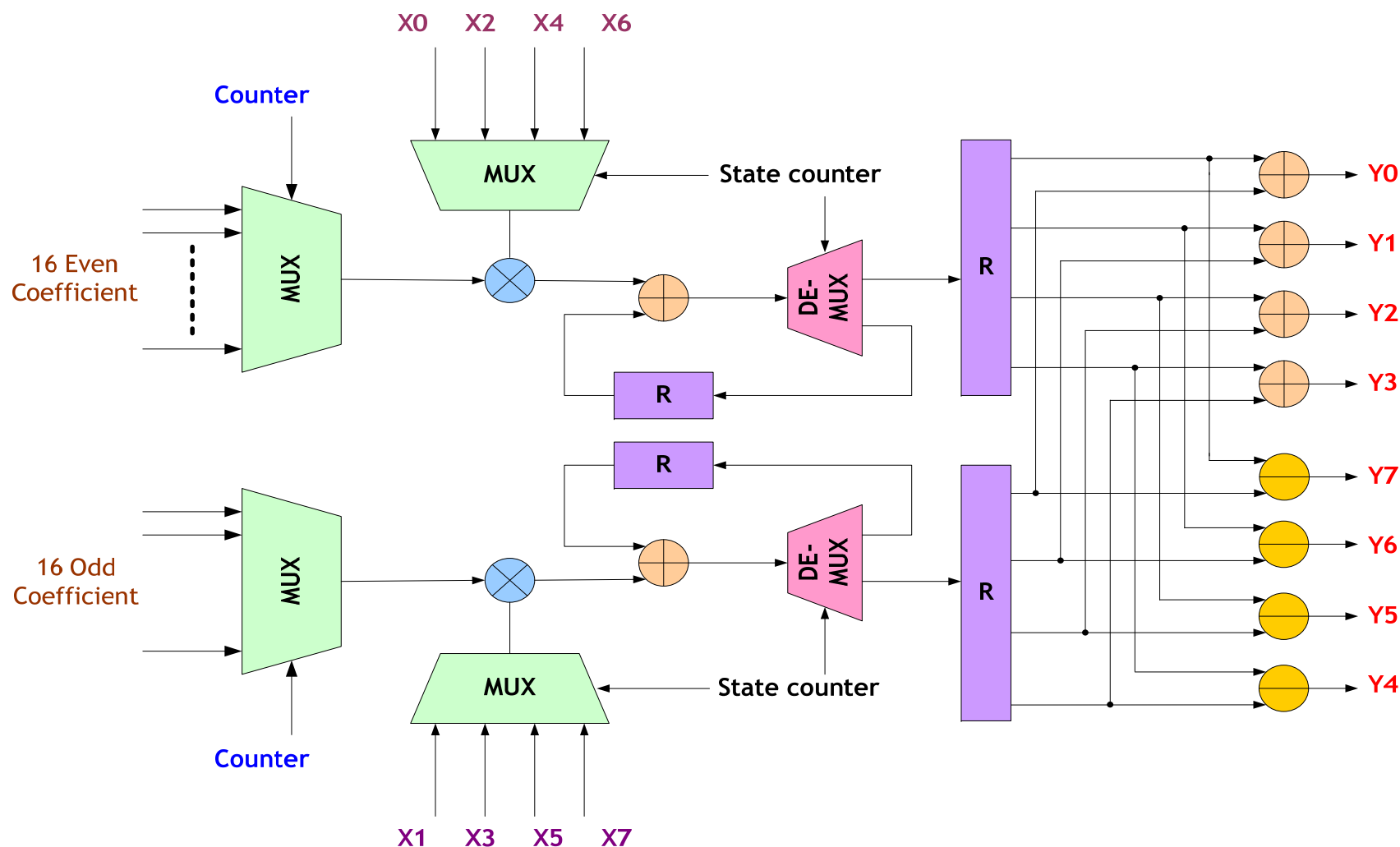
◆ Store Output Data to RAM

■ One pixel = 8 bits



3.2 IP Design and Realization of IDCT

■ IDCT IP Circuit Design



3.3 IP Functional Verification

3.1 Design Environment of the PXA/255 FPGA Module

3.2 IP Design and Realization of IDCT

3.3 IP Functional Verification

3.3 IP Functional Verification

■ 2D IDCT IP Verification

Step1: Dump the IDCT I/P and O/P Data from the MPEG-2 Reference Software

Step2: Create Input Waveform into Quartus-II

Step3: Check of the Quartus-II Output Waveform

3.3 IP Functional Verification

■ Dump IDCT I/P and O/P Data from Reference SW

◆ File Name : idct.c

```
-----  
static void idctcol(blk)  
short *blk;  
{  
FILE *IDCT_OUT;  
int x0,x1,x2,x3,x4,x5,x6,x7,x8;  
IDCT_OUT=fopen("c:\IDCT_OUT.txt","a");  
x0 = (blk[8*0]<<8) + 8192;  
/* first stage */  
x8 = W7*(x4+x5) + 4;  
x4 = (x8+(W1-W7)*x4)>>3;  
x5 = (x8-(W1+W7)*x5)>>3;  
x8 = W3*(x6+x7) + 4;  
x6 = (x8-(W3-W5)*x6)>>3;  
x7 = (x8-(W3+W5)*x7)>>3;  
/* second stage */  
x8 = x0 + x1;  
x0 -= x1;  
x1 = W6*(x3+x2) + 4;  
x2 = (x1-(W2+W6)*x2)>>3;  
x3 = (x1+(W2-W6)*x3)>>3;  
x1 = x4 + x6;  
x4 -= x6;  
-----
```

3.3 IP Functional Verification

■ Dump IDCT I/P and O/P Data from Reference SW

```
-----  
x6 = x5 + x7;  
x5 -= x7;  
/* third stage */  
x7 = x8 + x3;  
x8 -= x3;  
x3 = x0 + x2;  
x0 -= x2;  
x2 = (181*(x4+x5)+128)>>8;  
x4 = (181*(x4-x5)+128)>>8;  
/* fourth stage */  
blk[8*0] = iclp[(x7+x1)>>14];  
blk[8*1] = iclp[(x3+x2)>>14];  
blk[8*2] = iclp[(x0+x4)>>14];  
blk[8*3] = iclp[(x8+x6)>>14];  
blk[8*4] = iclp[(x8-x6)>>14];  
blk[8*5] = iclp[(x0-x4)>>14];  
blk[8*6] = iclp[(x3-x2)>>14];  
blk[8*7] = iclp[(x7-x1)>>14];  
-----
```

```
-----  
fprintf(IDCT_OUT,"idct_out1=%d\n",blk[8*0]);  
fprintf(IDCT_OUT,"idct_out2=%d\n",blk[8*1]);  
fprintf(IDCT_OUT,"idct_out3=%d\n",blk[8*2]);  
fprintf(IDCT_OUT,"idct_out4=%d\n",blk[8*3]);  
fprintf(IDCT_OUT,"idct_out5=%d\n",blk[8*4]);  
fprintf(IDCT_OUT,"idct_out6=%d\n",blk[8*5]);  
fprintf(IDCT_OUT,"idct_out7=%d\n",blk[8*6]);  
fprintf(IDCT_OUT,"idct_out8=%d\n",blk[8*7]);  
fclose(IDCT_OUT);  
}  
-----
```

3.3 IP Functional Verification

■ Dump IDCT I/P Data from Reference SW

◆ Simulation Result of the MPEG-2 Reference Software

■ IQ_data (X)

[0]	224
[1]	-380
[2]	-403
[3]	-220
[4]	0
[5]	135
[6]	72
[7]	0
[8]	100
[9]	-100
[10]	55
[11]	0
[12]	0
[13]	0
[14]	0
[15]	0
[16]	71
[17]	-55
[18]	-32
[19]	67
[20]	0
[21]	0
[22]	0
[23]	0
[24]	55
[25]	-27
[26]	-32
[27]	33
[28]	0
[29]	-42
[30]	0
[31]	0
[32]	-27
[33]	0
[34]	101

3.3 IP Functional Verification

■ Dump IDCT I/P Data from Reference SW

◆ Simulation Result of the MPEG-2 Reference Software

■ IDCT_out (Y)

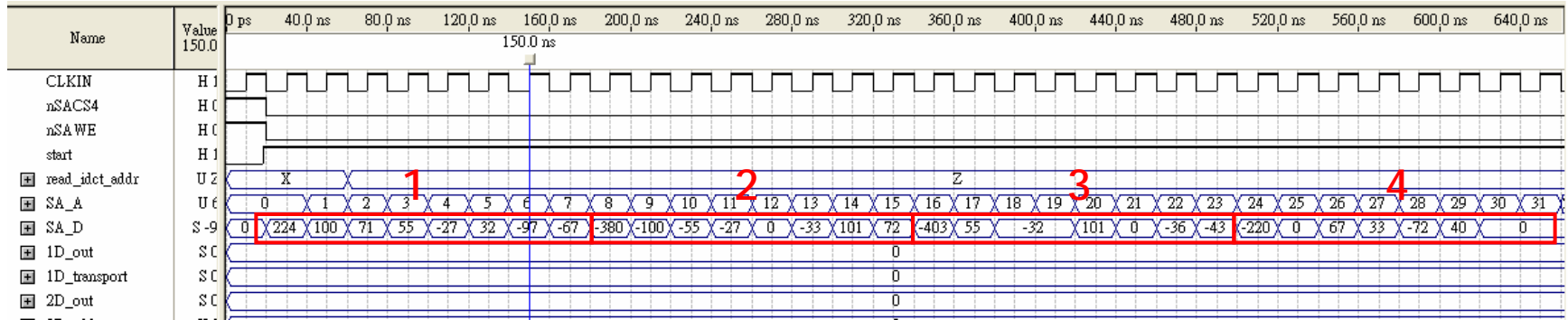
```
idct_out1=-98
idct_out2=-128
idct_out3=-116
idct_out4=-107
idct_out5=-131
idct_out6=-124
idct_out7=-132
idct_out8=-109
idct_out1=-84
idct_out2=-72
idct_out3=-96
idct_out4=-83
idct_out5=-70
idct_out6=-77
idct_out7=-79
idct_out8=-100
idct_out1=59
idct_out2=79
idct_out3=65
idct_out4=78
idct_out5=96
idct_out6=64
idct_out7=67
idct_out8=72
idct_out1=121
```

3.3 IP Functional Verification

■ Create the Quartus-II Input Waveform

◆ Created Input Waveform (1)

■ IQ_data (X)



● 8x8 IQ_data (X)

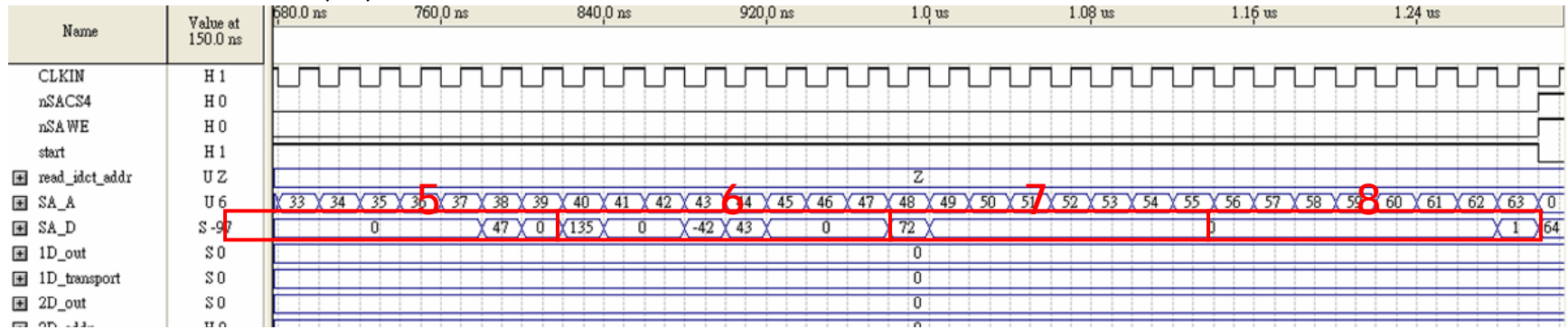
	1	2	3	4				
	224	-380	-403	-220	0	135	72	0
	100	-100	55	0	0	0	0	0
	71	-55	-32	67	0	0	0	0
	55	-27	-32	33	0	-42	0	0
	-27	0	101	-72	0	43	0	0
	32	-33	0	40	0	0	0	0
	-97	101	-36	0	47	0	0	0
	-67	72	-43	0	0	0	0	1

3.3 IP Functional Verification

■ Create the Quartus-II Input Waveform

◆ Created Input Waveform (2)

■ IQ_data (X)



- 8x8 IQ_data (X)

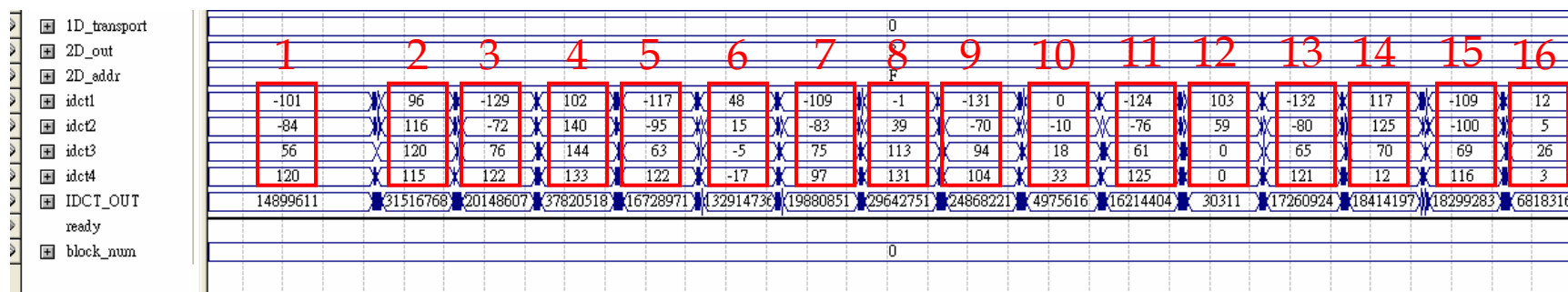
				5	6	7	8
224	-380	-403	-220	0	135	72	0
100	-100	55	0	0	0	0	0
71	-55	-32	67	0	0	0	0
55	-27	-32	33	0	-42	0	0
-27	0	101	-72	0	43	0	0
32	-33	0	40	0	0	0	0
-97	101	-36	0	47	0	0	0
-67	72	-43	0	0	0	0	1

3.3 IP Functional Verification

■ Create the Quartus-II Input Waveform

◆ Simulation Output of 2D IDCT

■ IDCT_out (Y)



3.3 IP Functional Verification

■ Check of the Quartus-II Output Waveform

◆ Comparisons

224	-380	-403	-220	0	135	72	0
100	-100	55	0	0	0	0	0
71	-55	-32	67	0	0	0	0
55	-27	-32	33	0	-42	0	0
-27	0	101	-72	0	43	0	0
32	-33	0	40	0	0	0	0
-97	101	-36	0	47	0	0	0
-67	72	-43	0	0	0	0	1

IDCT
Transform



1	3	5	7	9	11	13	15
-98	-128	-116	-107	-131	-124	-132	-109
-84	-72	-96	-83	-70	-77	-79	-100
59	79	65	78	96	64	67	72
121	123	123	98	106	126	122	118
97	103	49	0	0	104	119	13
116	141	15	39	-10	60	127	5
120	146	-5	115	17	-1	69	24
116	134	-17	133	34	1	12	4
2	4	6	8	10	12	14	16

Check OK !