PROJECT UAS ELEKTRONIKA DAYA

Buck Converter and Three Phase Grid-Tie Inverter

Nama : Farel Sijabat

NIM : 22/493206/TK/54018

DEPARTEMEN TEKNIK ELEKTRO DAN TEKNOLOGI INFORMASI

FAKULTAS TEKNIK UNIVERSITAS GADJAH MADA YOGYAKARTA

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Task 1

Strategy: To choose our specifications of the buck converter, it is essential to first determine the desired use of our buck converter, along with giving it physical meaning. Due to the increasing need of DC-DC conversion to 5V or 3.3V from 4 cell or 6 cell battery in Capstone Project, an efficient and controllable buck converter poses as one feasible solution. Each cell of common battery (Li-Po or Li-Ion) consists of 4.2-4.3V full charged voltage. To power some devices and sensors, we also get a gist of the required power, and in turn, current.

1. **The key specifications**

   - Input Voltage : With input from 4 or 6 cell DC battery, we determine the input current as $6\ x\ 4.2V = \mathbf{25.2}\boldsymbol{V}$. Accounting for some safety margin, a semiconductor rated above 35V would be preferrable, we'll get to choosing it later.
   - Output voltage : **3.3V or 5V**. STM32 requires 3.3V as its source, while most sensors use 5V as their input voltage. Considering the task 1 number 8 requires us to change voltage, we will design this buck converter so that it is hopefully able to change its voltage references, making it more flexible in its application as the user would be able to use it for powering up sensors or STM32.
   - Switching frequency: A high switching frequency benefits from smaller inductor and capacitor sizes, while it has more switching losses and higher EMI. We do not need to create an exceptionally small sized PSU, so fsw of **25kHz** is chosen for its moderate balance in efficiency and passive component sizes.
   - Output power : One device that would use most of the power is a UV lamp (8 or 16 Watt) While STM32 uses low power when active (70-100mW), along with up to 3 sensors (490mW total), the power specification plus safety margin is $(16 + 0.1 + 0.49) * 1.5 = \boldsymbol{25W}$, giving us a rated **7.54A** max current specification.
   - Permissible inductor current ripple: According to Texas Instruments Design Guideline, the acceptable current ripple is 20-40% of the output current, however 10% ripple is often more preferred. Therefore, the ripple current is $0.1 * \left(\frac{25W}{5V}\right) = \mathbf{0.5}\boldsymbol{A}$, note that we used the higher voltage for calculating less ripple (stricter, as in design we always tend to follow the worst operating case)
   - Permissible output voltage ripple : analog filter introduces noises from the power line ripples to the measurement data pin, and it is crucial as analog IC uses voltage measurement as its data. A low PSSR IC would bring the noise to the data line, as such, a low ripple is needed to limit the noise magnitude. But how low? The most ideal number is the voltage to make the measurements still remains in the same digital data when converted using ADC (for example in a sensor of a data reading from 0 up to 1000, using 5V power supply would

make each data shifts worth 5/1000V = 0.005V, which is often too low, or would result in a very high C value, but we will see later in no 2, how much would the resulting C be), as for now, we determine that the permissible output voltage ripple is **0.1-1%**.

Bonus: Semiconductor device used: One of the widely used MOSFET for converter design, the IRLZ44N is very suitable for above specs, we take a look at the snippets from the IRLZ44N datasheet below:

- The continuous drain current is 33A for the hotter temp and a gate opened with $V_{GS} = 10V$, giving us a huge margin for the current rating. The power rating is very sufficient at 110W.

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	47	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	33	
I_{DM}	Pulsed Drain Current ①	160	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C

- The MOSFET is capable of holding up to 55V between its drain and source, a very safe from our 25V input. Its R_{DS} is relatively low, ensuring manageable conductive loss.

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.070	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.022	Ω	V_{GS} = 10V, I_D = 25A ④
		—	—	0.025		V_{GS} = 5.0V, I_D = 25A ④
		—	—	0.035		V_{GS} = 4.0V, I_D = 21A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250μA

- With the gate voltage opened at a safe logic level 2V and fully operational at around 5V from the characteristic curve below, the comparator gating output in PSIM can reach 5V safely. The IRLZ44N is also fully avalanche rated, adding more to its value.

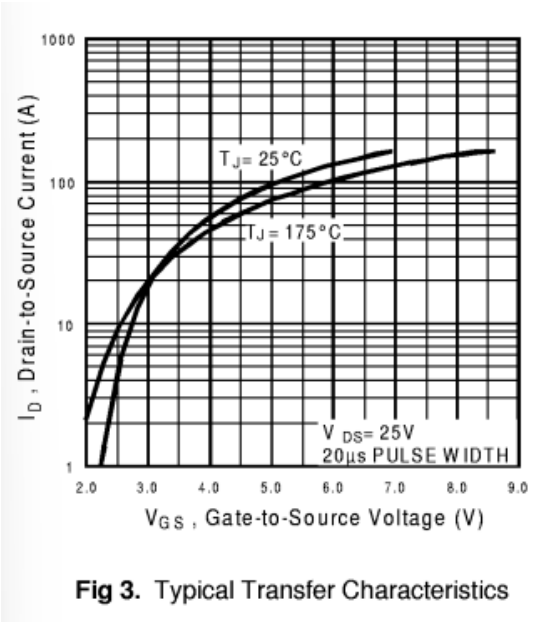


Fig 3. Typical Transfer Characteristics

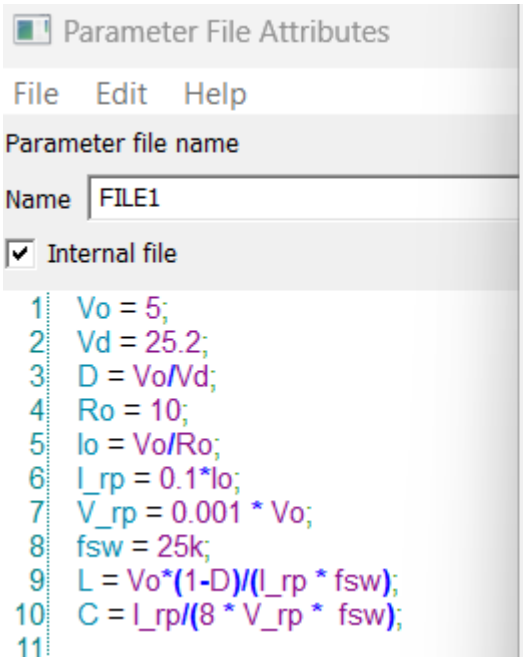
2. **Calculate and determine suitable values for the inductor (L) and capacitor (C) to meet your design specifications**

According to the material from before midterm on converter passive component design, the value of L and C can be determined as follows:

$C = \frac{I_{ripple}}{8\ x\ f_{sw}\ x\ V_{ripple}} = \frac{0.05}{8\ x\ 25k\ x\ 0.005} =$ $\mathbf{50\mu C}$ (still small and acceptable)

$L = \frac{(V_{in}-V_{out}).D}{f_{sw}\ x\ I_{ripple}} = \frac{(25.2-5)\ x\frac{V_o}{V_D}}{25k\ x\ 0.5} =$ $\mathbf{3.2mH}$ (Also, still acceptable)

The implementation of L and C values can be designed with the parameter script below in PSIM, so that it can automatically calculate new L and C values when there is changes in Vo or other parameters. The values also match with below:



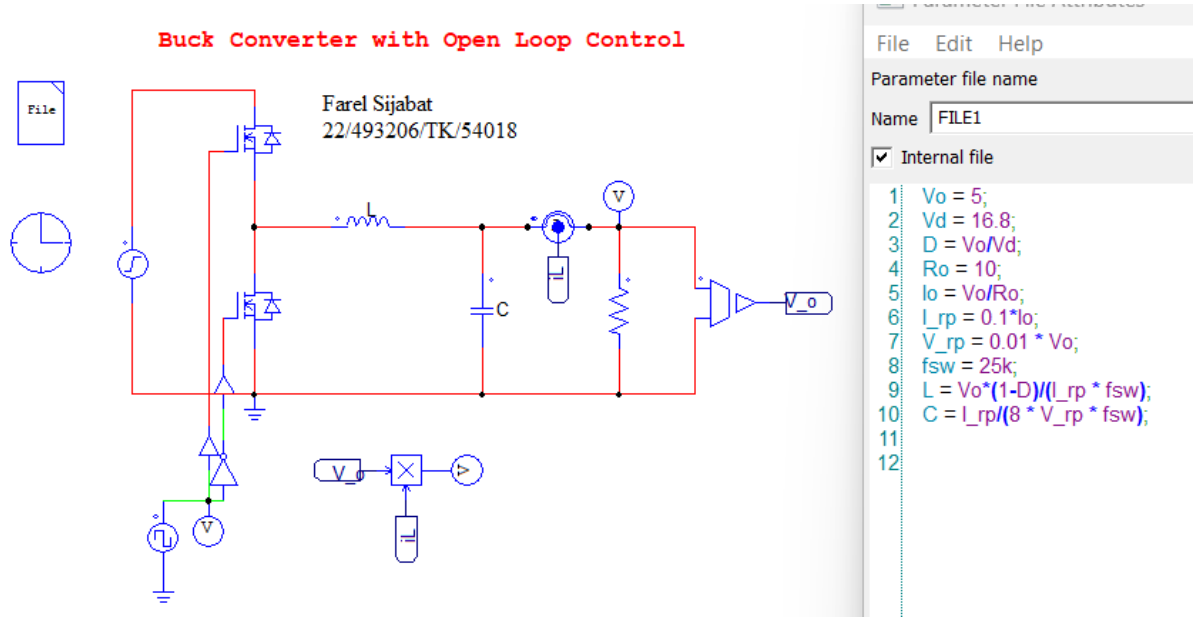
Property	Value
Vo	5
Vd	25.2
D	0.1984127
Ro	10
Io	0.5
I_rp	0.05
V_rp	0.005
fsw	25000
L	0.0032063492
C	5E-05
Kp_i	20.7389
Ki_i	257040
Ti_i	8.0683551E-05
Kp_v	0
Ti_v	1E-06

3. **Develop and simulate the open-loop operation of the buck converter without feedback control**

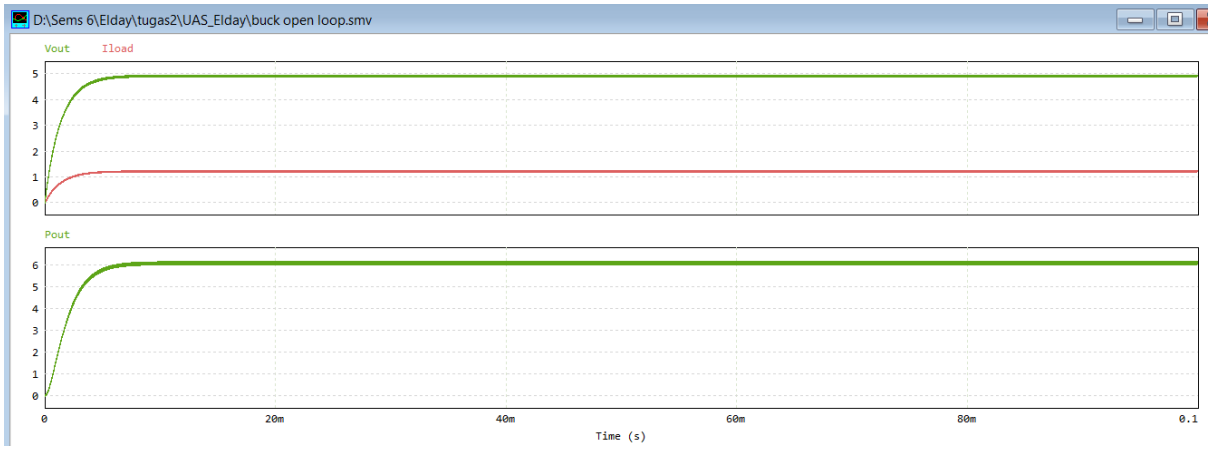
The open loop buck converter control consists of the components with the objective of:

- Voltage regulation from the input to our desired voltage level
- Acceptable voltage and current ripples, confirming our L and C choices
- Unable to "know" the real output, therefore it doesn't have any corrective measure if it doesn't reach its reference, we'll test this hopefully in this project
- Is able to change voltage if we directly change its reference in the parameter (forward or open loop control) manually

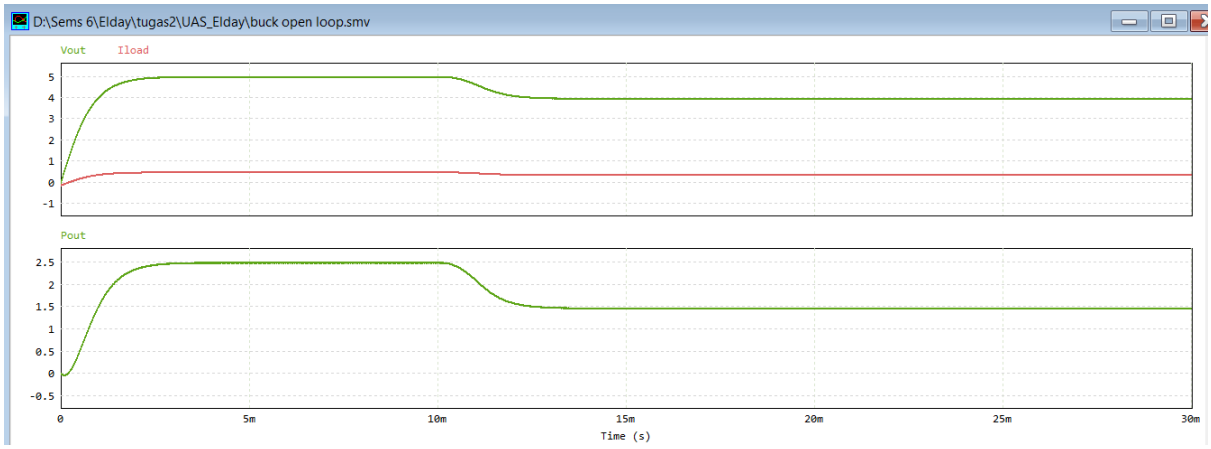
First draft implementation:



Result: As we can see in the picture below, with the desired Vout set at 5V, the open loop is able to calculate the required duty cycle from the formula of $\frac{V_o}{V_{in}}$ manually, the duty cycle determines how long does the MOSFET open during one period of switching.



However, now we see the weakness of open loop control, we now change the input voltage suddenly, as in physical representation, this can occur as the battery cells are starting to discharge most of its charge. We observe below that open loop control is unable to correct the voltage back to its reference 5V.



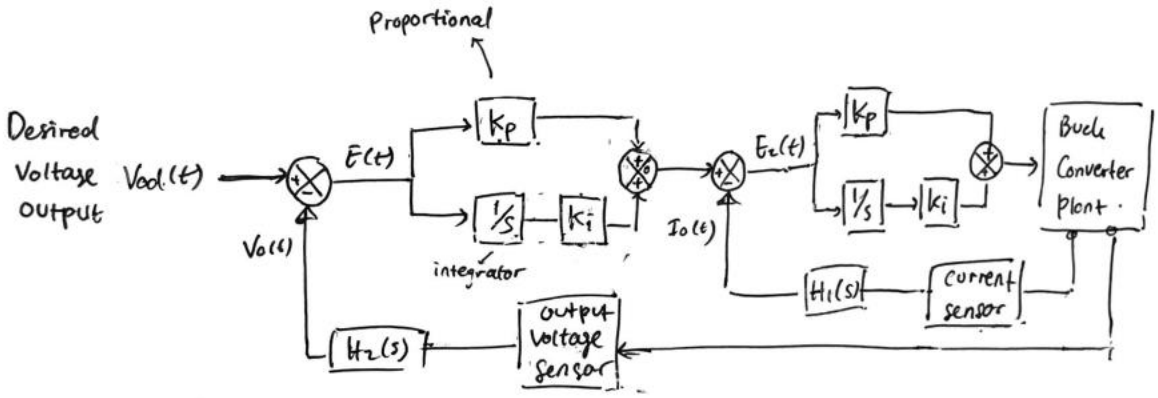
This is where closed loop comes in handy, as we know, the duty cycle governs the output voltage, and a controller is able to change the modulating voltage that is compared to the triangle carrier signal, thereby modifying the duty cycle of the resulting PWM signal.

4. Design a cascaded control system for voltage regulation of the buck converter

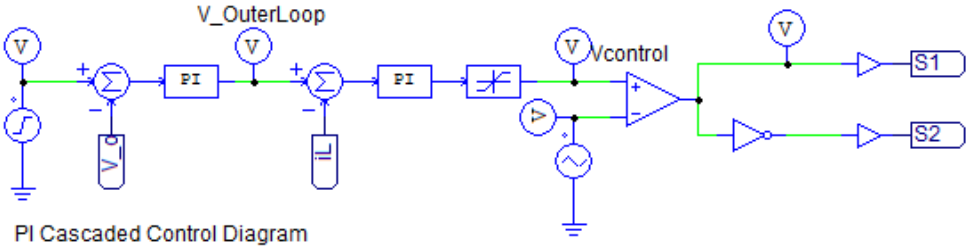
a. Block diagram and control architecture

Analyze: To design the control architecture for a cascaded control system, we first need to understand the essence of cascaded control of closed loop. The outer loop is designed as the controller of our desired variable, for example we want to control the voltage, or the active power, etc. Then, the inner loop consisted of current control is built as the current loop is faster to control (the dynamic changes of current is faster than the outer loop).

Strategy: A common control strategy for this case consisted of cascaded PI controller, as derivative is often not needed for rushing the change, as the cascade loop design itself could help fasten the response while smoothly adjusting to the changes using Proportional and Integral only. The reference of voltage are set, and compared with the current value of voltage, resulting in the first error term, before going to the outer control block. The output from the outer control block is compared with the output current resulting in the second error term, controlled with the second PI block, and the output goes into the plant (although physically in between there is modulation step)



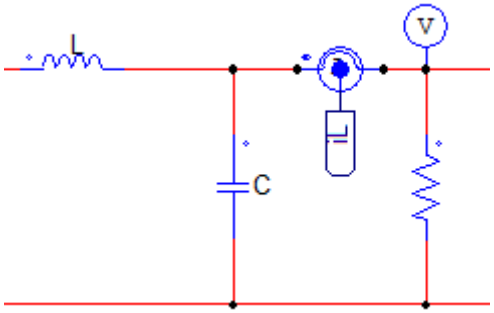
With references from PSIM libraries, the control architecture is given below:



PI Cascaded Control Diagram

b. The calculation or tuning procedures for the control gain

The control gain however, is a bit complicated, as we can see that the output from voltage loop can even be the input into the current loop, so there must be a math equation guiding them. With the research and findings from PSIM forums, we need to model the plant (preferably using transfer function and then tune the model afterwards). We start by modelling the plant as an LC-R circuit and use KVL and KCL to derive the transfer function



As we can see above, we first have to get the input and output correctly to get the transfer function, we start with the voltage across the inductor is $V_L = V_{buck} - V_{out}$, V_{buck} is the input in the circuit above (it is the output of the buck converter, although for the transfer function, the input is not V_{buck}, but I_L, as the transfer function uses current as the input and outputting V_{buck} as the inner loop output, through modulation of course), and V_{out} is the output (the voltage in the resistor load). But the V_L needs to be further bisected, as we know, it is comprised of $X_L . I_L = s.L.I_L$, we need to model I_L in terms of the input or the output. We used current divider from the I_L to get the current in the load I_{load}, that is $\frac{\frac{1}{sC}}{R+\frac{1}{sC}} . I_L = \frac{1}{1+RCs} . I_L$, now we can get the

$$V_{out} = R.I_{load} = \frac{R}{1+RCs} . I_L,$$

We then get back to the $s.L.I_L = V_{buck} - V_{out}$, we substitute for V_{out} and we got

$I_L = \frac{1}{s.L+\frac{R}{1+RCs}} . V_{buck}$,

As mentioned previously, $plant\ P(s) = \frac{I_L}{V_{buck}} = \frac{1}{s.L+\frac{R}{1+RCs}}$

After that, we model the PI controller logic using the basic configuration of PI transfer function:

$$G_{PI}(s) = \frac{K_p.(1+s.T_i)}{s.T_i}$$

then multiply it with the P(s), we then account for the feedback sensor gain by multiplying the resulting transfer function by the sensor multiplier constant, the whole ordeal was done in matlab as seen below, do note that in the constant defining, the sensor gains are calculated in the biggest possible gain to scale max current and voltage to 3.3V reading ADC sensor. Then we define s as laplace and the magic happens next after defining the final transfer function by combining plant (denoted as Hi), times the sensor and PWM modulation gain (as the bridge between the PI controller output to the V_{buck}).

The tuning magic happens with pidtune, an automatic tuner that could help us find the required gains according to our controller type. The result, denoted as C_i is then put into PI transfer function G_i, then a full closed loop transfer function is formed within the controller.

```
% Define constants (same as current loop)
Vin = 25.2;
L = 0.0029166667;
C = 3.125e-06;
R = 10;
Ksen_i = 3.3/47;
Ksen_v = 3.3/50;
Kpwm = Vin;
fx_i = 2e3;
fx_v = 500; % Voltage loop crossover freq (Hz)

% Define s
s = tf('s');

% Inner loop design
Hi = 1 / (L*s + R / (1 + R*C*s));
Ti_target_i = 2*pi*fx_i;
[C_pi, info_i] = pidtune(Hi * Ksen_i * Kpwm, 'PI', Ti_target_i);
Gi = C_pi;
Ti_loop = Hi * Gi * Ksen_i * Kpwm;
Tic_loop = feedback(Ti_loop, 1) / Ksen_i;
```

Figure 1 Matlab System Modelling in Transfer Function

But remember, that is only the inner loop controller, for the outer loop, we design the controller base as the regular PI controller, then tune it with pidtune, the difference is, now we requested a phase margin, that is a certain margin of stability in respect to the phase degree, how much could the system tolerate any phase delay before instability, which also determine response speed, (larger phase margin is safer but are slower).

The next step is verification using time domain (unit step response) and frequency domain response (bode plot) to see if our system and controller configuration is tuned to our desired design.

```
% Voltage plant: Hv(s) = Vo / iL = R / (RCs + 1)
Hv = R / (R*C*s + 1);

% Outer loop tuning
Ti_target_v = 2*pi*fx_v;
opts = pidtuneOptions(PhaseMargin=60);  % Desired PM
[C_pv, info_v] = pidtune(Hv * Tic_loop * Ksen_v, 'PI', Ti_target_v, opts);
Gv = C_pv;

% Voltage loop open-loop and closed-loop TFs
Tv_loop = Hv * Gv * Ksen_v * Tic_loop;
Tvo_cl = feedback(Tv_loop, 1);

% Display tuned gains
Kpv = C_pv.Kp;
Kiv = C_pv.Ki;
disp("Outer Loop PI Gains:");
fprintf("Kp_v = %.5f, Ki_v = %.5f\n", Kpv, Kiv);

% Bode and Step plots
figure;
margin(Tv_loop);
title('Voltage Loop Open-Loop Bode Plot');
```

Figure 2 Matlab Tuning Process using PIDtune

We can observe below that the bode plot, the representatives of frequency domain is stable with phase margin of 60° as our tuning process design. The gain crossover frequency is in $1.26\ x\ 10^4$, which means that in the event of no gain (gain = 1 or 0 dB), the response is fast, and that would hopefully align with the time domain response that we're going to simulate. Matlab also determines that the closed loop system is stable, hence the design in frequency domain is successfully checked and approved.

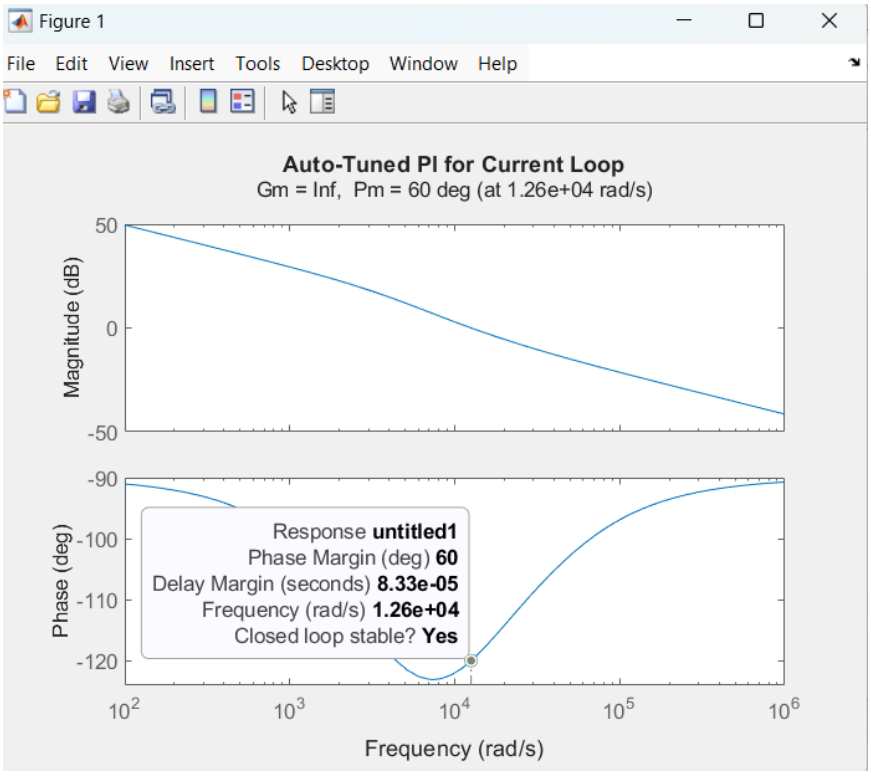


Figure 3 Bode Plot Analysis in Frequency Domain

As for the step response, we observe that the overshoot is less than 20% with a settling time of 0.005s, which indicates a good time domain response with a relative short time of transient that aligns with the phase margin estimation, low overshoot, and for voltage regulations, the duration of 0.005 second of transient is still very fast even for the standard of safety and obey the allowable transient duration time according to the grid code of 2020 of Ministry of ESDM Indonesia.

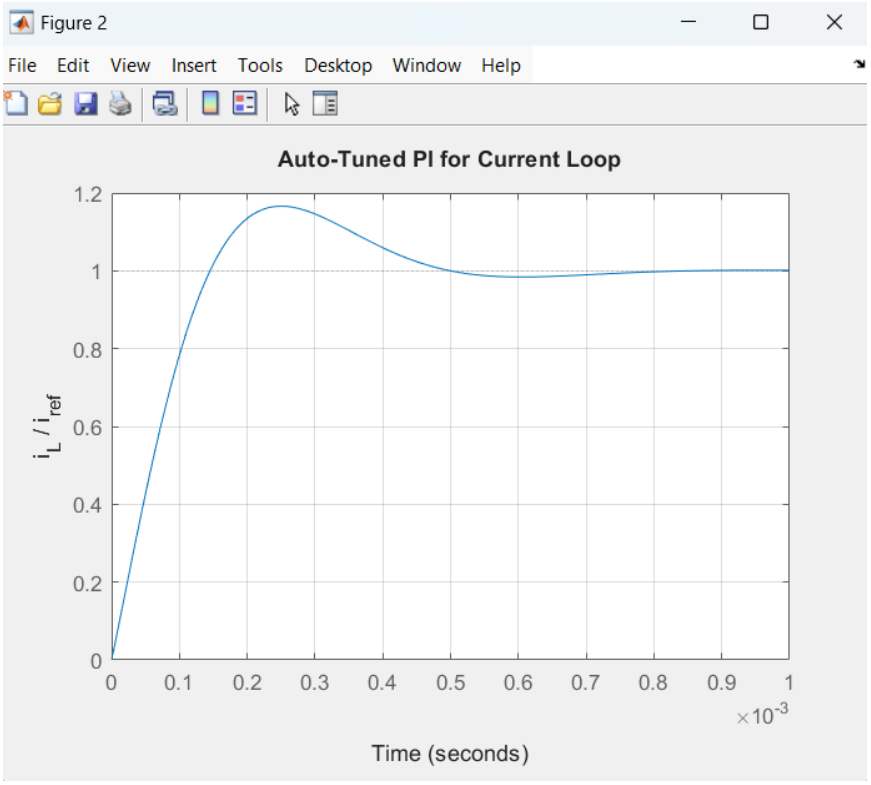


Figure 4 Time Domain Analysis using Step Response

5. Plot the inductor current waveform and verify that the ripple meets your design criteria

We will now plot the inductor current and voltage waveform to confirm our passive component design selection accuracy, as the inductor and capacitor is the one responsible for managing the ripple, and we've chose the inductor and capacitor to meet the balance between physical constraint of sizes and ripple.

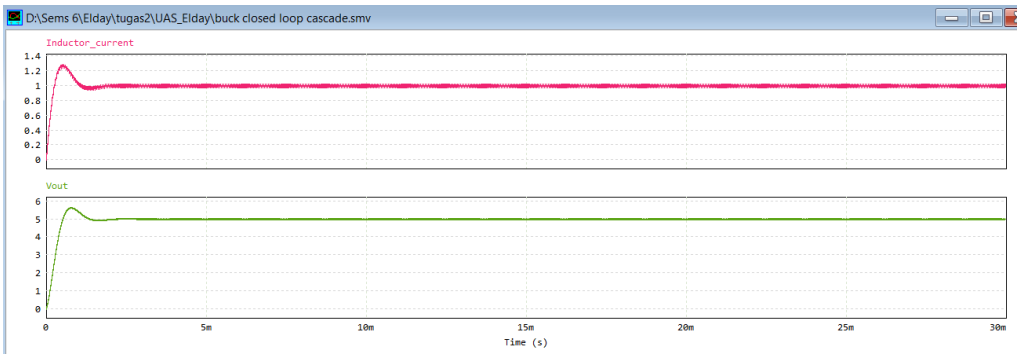


Figure 5 Inductor current and Output Voltage Waveform

Before diving into each plot separately, note that the waveforms resemble that of step response, as we know that the initial conditions of the simulations start with zero voltage at exactly t = 0s with also zero charges inside the capacitor and no magnetic flux at the inductor, hence when at

t = 0+ the DC source is on, it resembles a step response. We can confirm that the current and voltage step response perfectly matches the time domain step simulation in the previous number, as we did model the system plant transfer function using the topology and circuit laws of the buck converter. Do note that there is a slight imperfection in the overshoot as it reached 20% in the current and voltage simulation, unlike 18% in the time domain model simulation. This is caused by the non-linearities of the components model, such as $R_{ds(ON)}$ of the semiconductor devices.

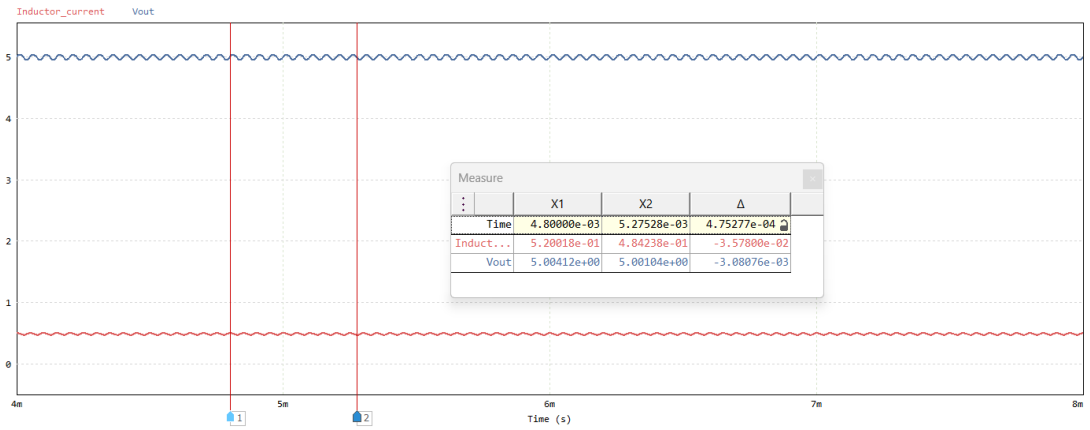


Figure 6 Inductor Current Waveform Ripple Observation

Observe that the **inductor current waveform** when observed in its highest and lowest point of the oscillation is spaced at **0.4A**, a slight difference but manageable from **0.5A** ripple from our design.

6. **Plot the output voltage waveform and verify that the ripple is within the allowable range**

The **output voltage waveform** is seen within the allowable range, as we observe in the simulation below that the distance between the highest point and the low crevices is ≈**0.005V**, which is the number that confirms our design

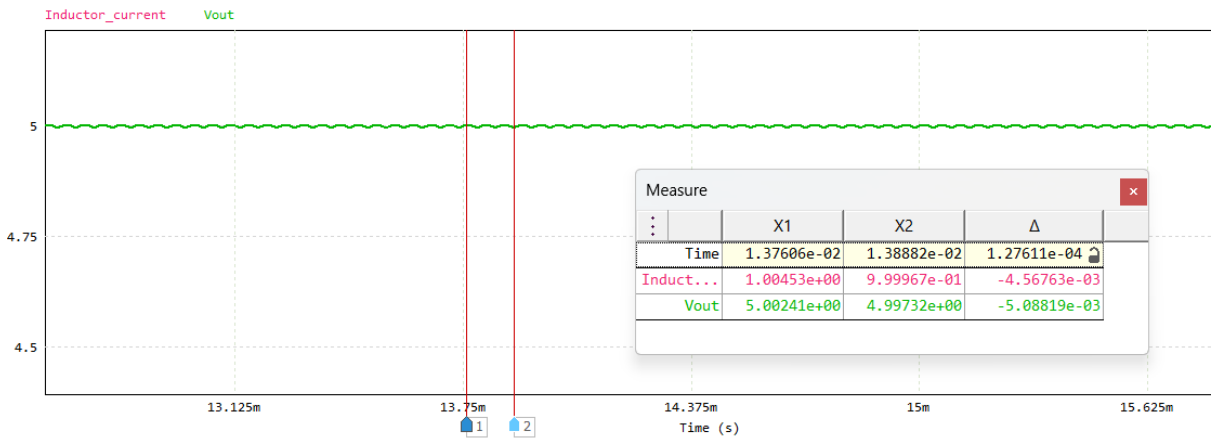


Figure 7 Voltage Waveform Ripple Observation

7. **Simulate a sudden load change and analyze the converter's dynamic response. Demonstrate how the controller maintains stability and restores regulation**

To simulate a sudden load change, we used a Rheostat component in PSIM, and at t = 20ms we apply a step change to reduce the load directly to its half, we observe the system variables in the plot below

Figure 8 Current, Voltage, and Power During Sudden Load Change

We observe 3 important things:

- When the load drops to its half of its value, the voltage waveform experiences a slight dip, caused by the ohm's law of $V = I.R$ and a sudden change in R results in sudden change in V also. But it quickly adjusts to its reference value at 5V, that's right, while the system obviously couldn't change the load, it can change the current I
- The inductor current experience a slight increase, not just for a moment, but it keeps its new higher value after the load change event, this is to keep the voltage back in its reference V with the new lower R, such that $V = I_{new}\ x\ R_{new}$
- The power also increases as we know that $P = V.I$, and as the buck converter keeps the voltage the same with higher I value, consequently, the P increases.

Figure 9 Observation of Voltage Dip and Current Increase

As we see above, the voltage experiences a drop for **0.15V,** a 3% drop before the controller regulates the current to set the voltage back to its reference in less than 5ms, as per our time domain simulation. The current increases **0.1A,** a 10% increase from the original value. Hence, we can conclude that the voltage regulation is a success

8. **Simulate the system response to a step change in the voltage reference. Show how effectively the controller tracks the new reference value**

Onto the next part, we simulate a step change in the voltage reference. We used a step DC voltage as the buck reference voltage so that we may change the reference, modeled in the voltage outer loop control input. As our design and specifications of the closed loop cascade buck, the converter should be able to follow its reference voltage value

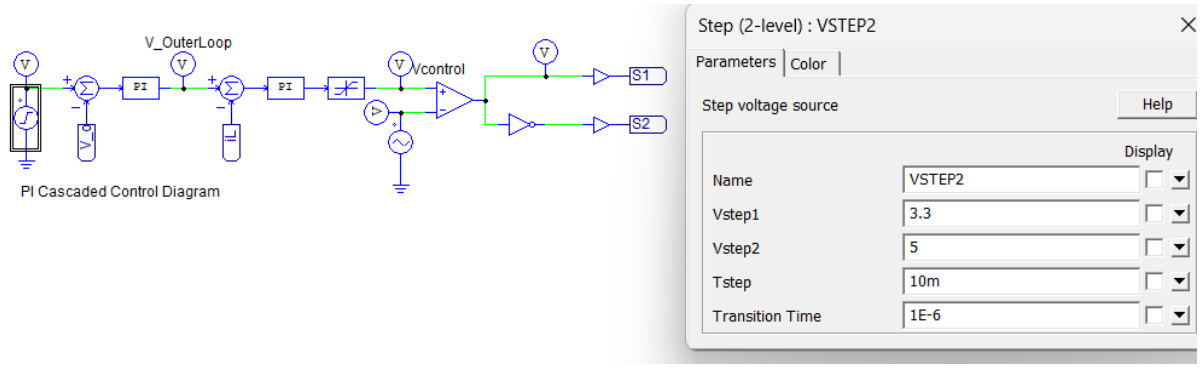


Figure 10 Step Voltage Reference in the Outer Loop Input

The result in the output voltage when compared to the reference voltage is as follows

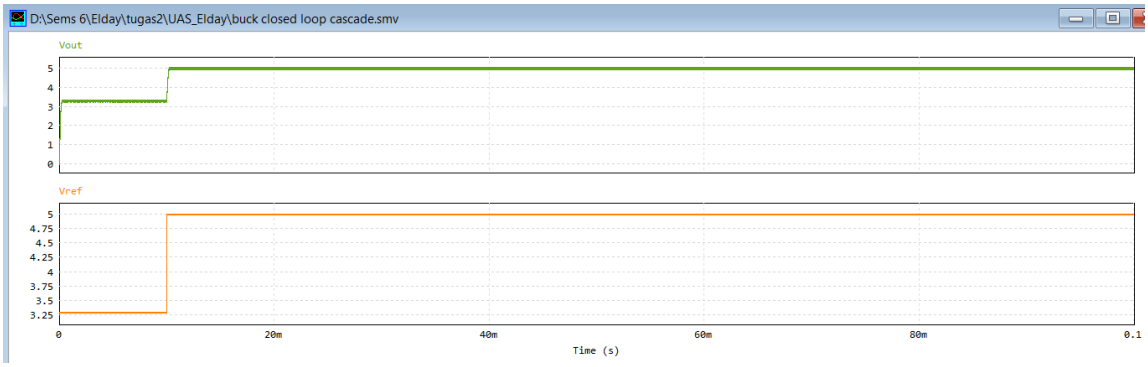


Figure 11 Step Change in Reference Voltage

In this step change, we change the reference voltage from 3.3V to 5V, and we observe that the controller effectively tracks the new value as seen in the Vout adjusting right after the step change of Vref happens.

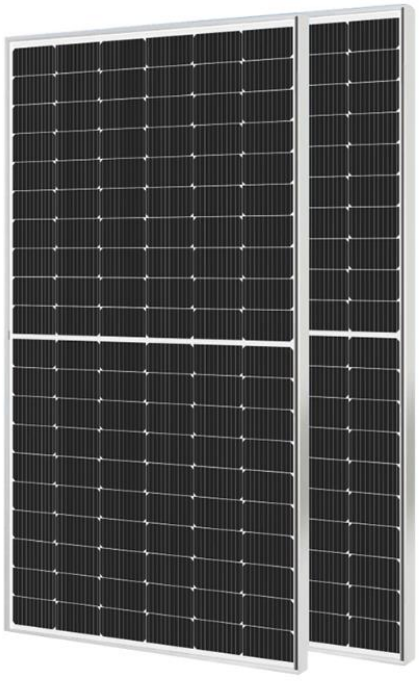
Physically, the controller would regulate and manage this change in input value by adjusting its duty cycle, as we can analyze that the increase in reference voltage would increase the output from the outer loop, then the inner loop which increase the modulating waveform, thereby increasing the duty cycle

Task 2

Objective: to make the design more applicable, we're assuming a household of medium power rating from PLN of 2200VA wants our PV-Inverter module, there are three houses that want the module, so we had to provide at least 6600VA for the bare minimum, although how long the PV configuration could provide power during the night were determined by the BESS, and it is not on our scope.

1. **Define the configuration of the photovoltaic (PV) array. Specify key parameters such as module voltage, current, and how modules are arranged (series/parallel)**

   The PV array is connected in series to stack up voltage (using KVL) as each panel have 41.25V and peak power of 450Wp, then we connect 13 panels in series to reach a voltage of 536.25V, as with Indonesian Standard of Solar Panel Installation (details in the appendix) the safety recommended limits of rooftop PV panels lies within 400V, 600V and 1000V for large household. We aimed for around 600V in the middle ground with stacking **13 panels in series** resulting in total of **536.25V**



Spesifikasi Elektrikal Panel Surya TKDN Monocrystalline 450W	
Rate Maximum Power (Pmax/W)	450W
Module Efficiency (%)	20.80%
Open Circuit Voltage (Voc/V)	41.25V
Short Circuit Current (Isc/A)	13.89A
Voltage at Pmax (Vmp/V)	34.67V
Current at Pmax (Imp/A)	12.98A
Power Tolerance	±5w
STC: Irradiance l000W/m² Cell Temperature 25°C AMl.5	

Spesifikasi Mekanikal Panel Surya TKDN Monocrystalline 450W	
Solar Cell (Type/Size)	Mono (182mm)
Solar Cells Number	120 pcs (6*10)
Dimension	1909*1134*35mm

Figure 12 Commercial Specification of Solar Panel

2. **Determine the PV module configuration and its rating such as voltage and current**

In PSIM, we can model the solar module using the commercial specs given, as we can see, the voltage in maximum power is given at **34.67V,** with the open circuit voltage $\boldsymbol{V_{OC} = 41.25V}$, the rated current is rated at **13.89A** short circuit current, while at maximum power, it is given at **12.98A**. We can note that the open circuit voltage and short circuit current is given as the optimal rating on no load condition and maximum possible current at short circuit event, whereas at maximum power (loaded), the voltage drops slightly and the current of course would not reach the short circuit current. The V_{OC} *and* I_{SC} is meant for the maximum or absolute rating for component sizing, while the Pmax is meant for operational limits. We can also see the power voltage and current voltage curves. However, using physical models in PSIM introduces nonlinearities and non-ideal conditions, such when we adopted the PSIM project that is related to solar panels, the use of physical models requires a convergence capacitor, something out of our scope.

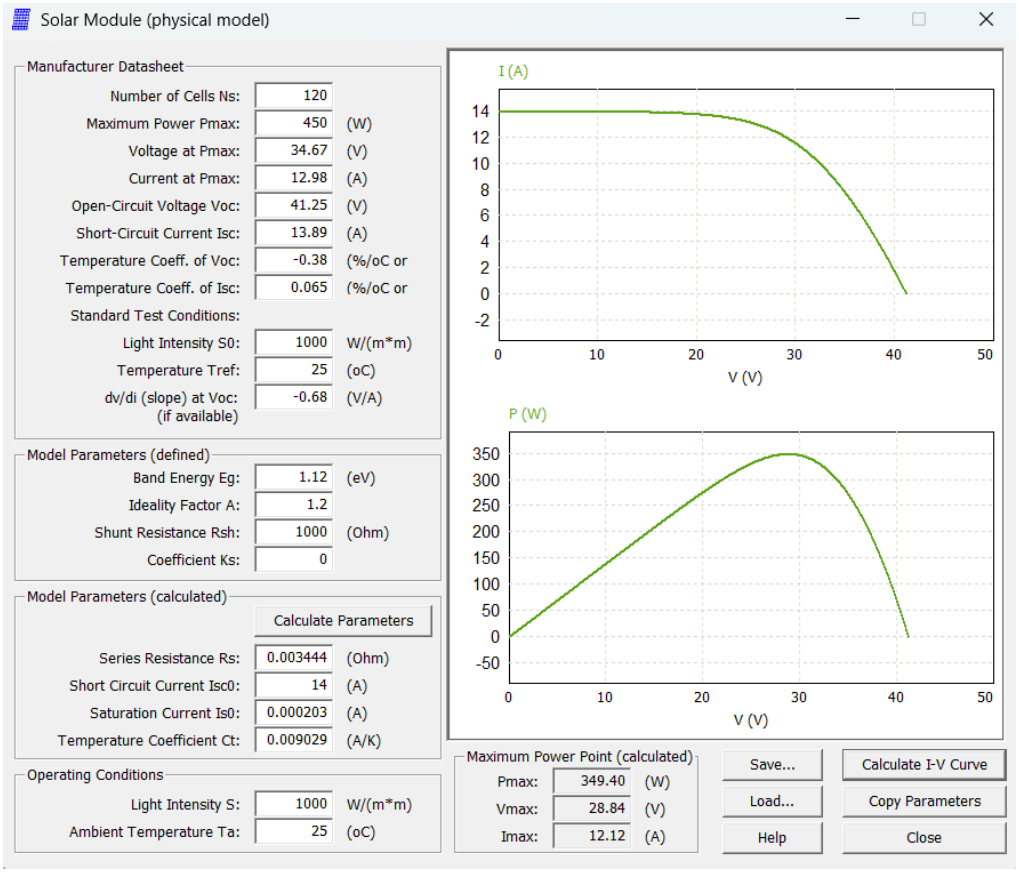
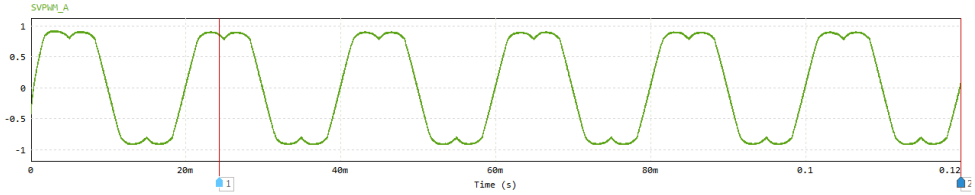


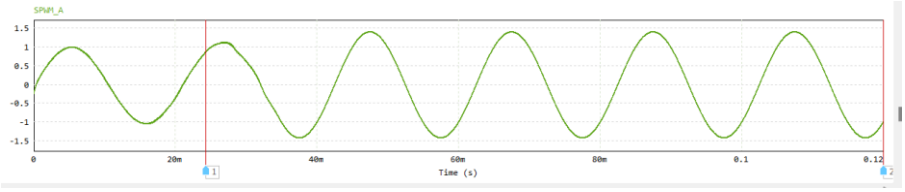
Figure 13 Physical Solar Panel Module Modelling

As such, we will use a DC power source instead of physical solar devices.

3. **The inverter is rated as the researched commercial options such follows:**

- Rated DC-link voltage :**700V**, giving headroom for our rated PV configurations
- AC output voltage :**380V**, as per the grid output voltage
- Power rating =input voltage * rated input current = 536.25 * 13 = **6.9kW**
- Semiconductor device used is Infineon IMDQ75R025M2H **SiC MOSFET** due to its fit in the ratings, having 750V V_{DSS}, with rated drain current at 49A and high efficiency as it has low $R_{DS(ON)}$, ensuring low conductive losses at around 6W. This SiC MOSFET is one of Infineon flagship in its second generation SiC, with high switching frequency and best performance in its class.
- Our Modulation strategy is SVPWM, as it bested SPWM in its DC input voltage utilization, meaning it gave headroom before reaching *overmodulation.* This is proven useful as on our latter experiments, we found out that the v_{gate} is actually nearing its overmodulation limit, and SVPWM also have similar physical effect on the waveform as 3rd harmonic addition to the signal, giving 15% more headroom of the voltage before modulation compared to regular SPWM, as seen below:





4. **Calculate the value of the inductor (L) connecting the inverter to the grid (three-phase voltage of 380 V**

To calculate the value of inductor, we used the formula in the research paper of "Design and Control of an LCL-Filter-Based Three-Phase Active Rectifier", the value of inductor determines the current ripple, a crucial parameter in the grid with the following formula:

$$L_{ind} = \frac{V_{dc}}{6\ x\ f_{SW}\ x\ I_{ripple}}$$

As there is no definite standard of Indonesian current ripple, we would assume a 2 times tighter standard from the converter current ripple rule, that is quantized as 5% ripple.

$$L_{ind} = \frac{550}{6\ x\ 35k\ x\ 0.05\ x\ 14} \approx 4\ mH$$

Designing a larger inductance in the grid output helps reduce current ripple as it works just like a low pass filter for the current, although it has a constraint given by the fact that inductance introduces a phase lag in the current, and the more inductance the line has, the more lag it will introduce, and that isn't good as when we want in phase current, the current will lag behind the voltage. The example below is drawn to show a leading voltage, for it will occur as the $j\omega L\ times\ I$ would stretch a vertical line at the imaginary axis, then the voltage would lead the current, which is lagging by 90° behind, as seen below:

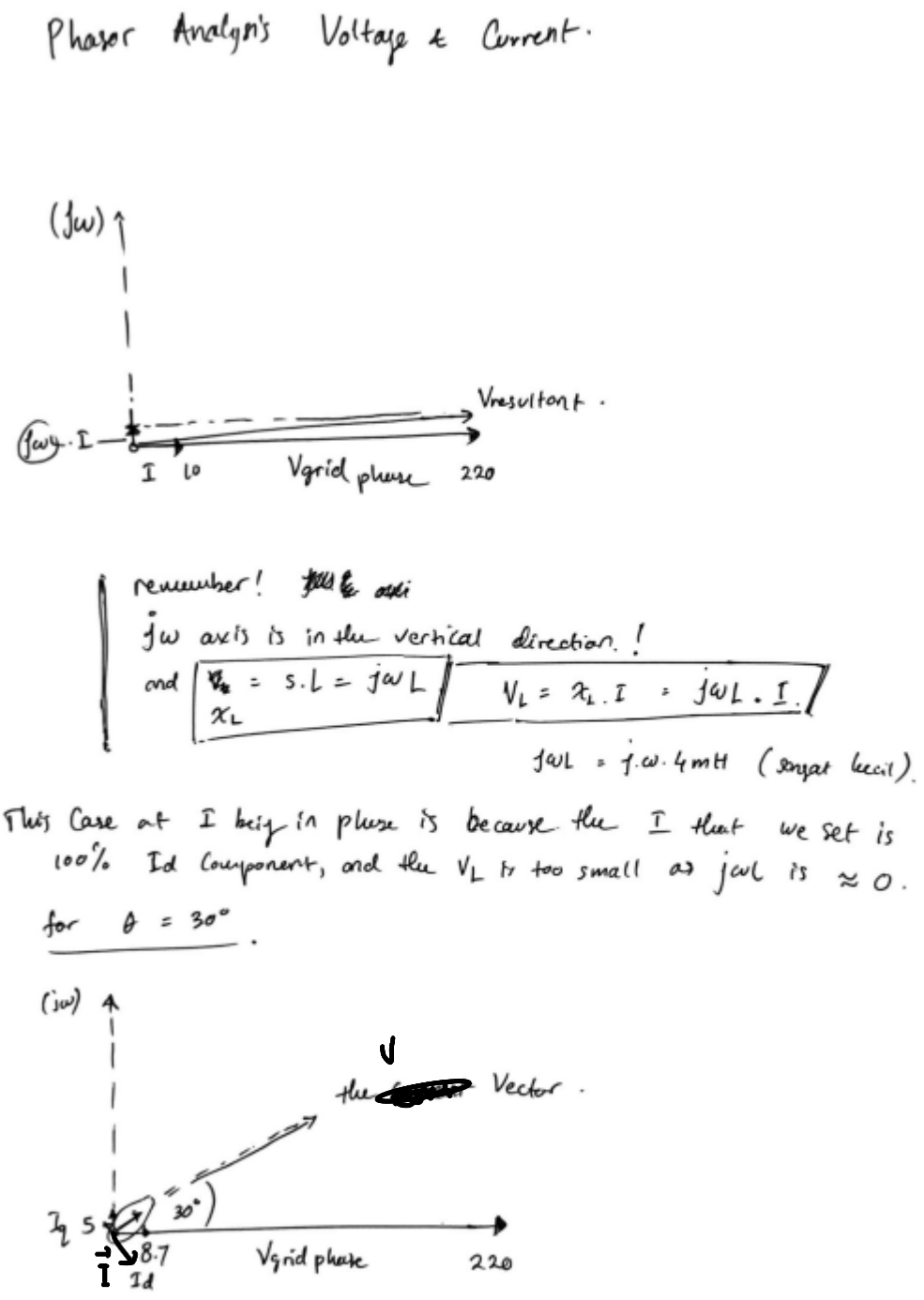


Figure 14 Voltage and Current Phasor

5. **Now we will design a controller capable of regulating active and reactive power, to begin, we will start with these steps:**

- Construct the relationship of active and reactive power as the outer loop to the inner loop variable, that is current in dq axis.
- Build a block diagram based on the current and power relationship
- Add a controller to the block diagram, the simplest is PI controller, this will complete the closed loop diagram of the whole system
- Tune the Kp and Ki gains, although this is harder than the previous model as unlike a RLC components in the buck converter before, this consist of a grid connection. With the models unknown, we could use the Zieger Nichols method.

Power Equation For Control:

$$P = \frac{3}{2}(V_d I_d + V_q I_q)$$

$$Q = \frac{3}{2}(V_q I_d - V_d I_q)$$

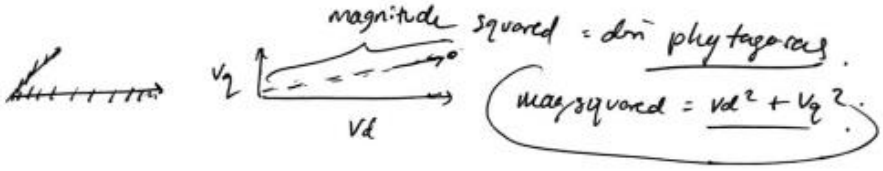
$\xrightarrow{\text{current decoupling}}$

$$I_d = \frac{2}{3}\left(\frac{P V_d + Q V_q}{V_d^2 + V_q^2}\right)$$

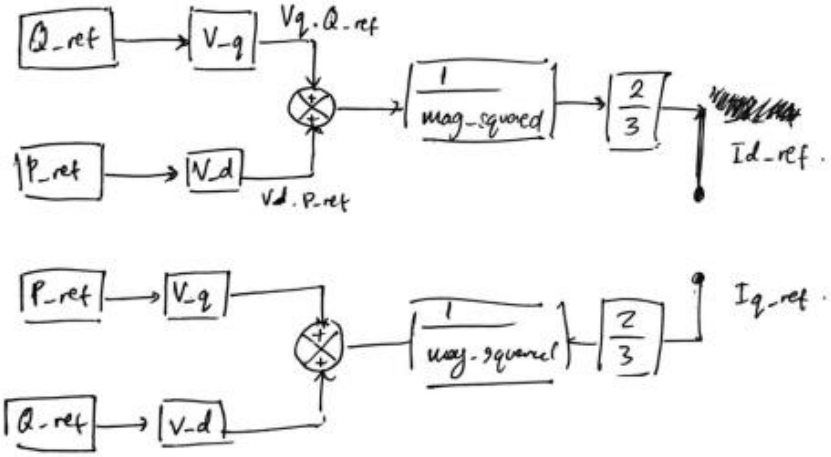
$$I_q = \frac{2}{3}\left(\frac{P \cdot V_q - Q V_d}{V_d^2 + V_q^2}\right)$$

in d-q frame

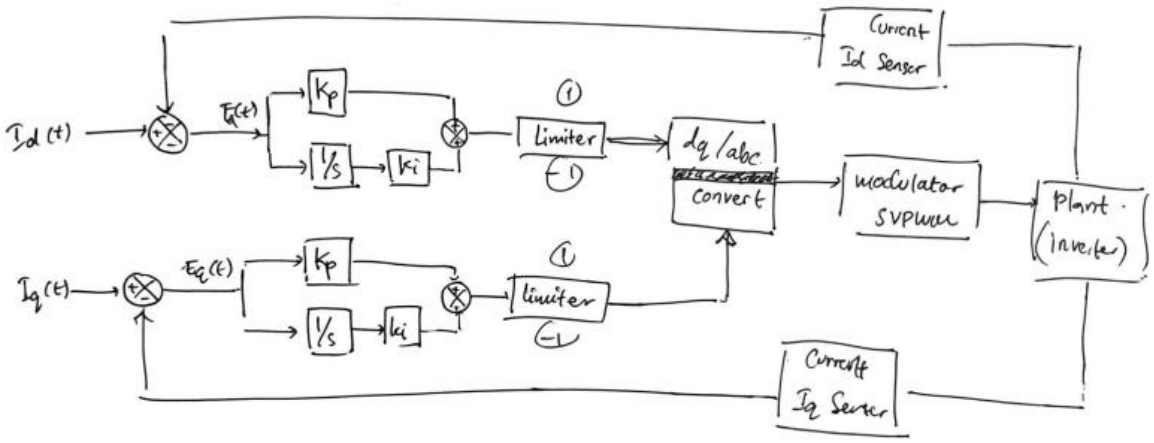
Untuk mempermudah diagram, $V_d^2 + V_q^2$ dibuat jadi' salah satu variabel lain.



referencing:

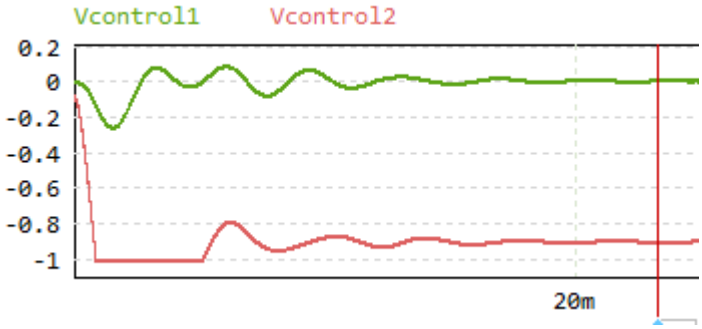


Control blocks diagram using PI Controller.



The Zieger Nichols tuning method that we are going to use is the ZN2, that is the closed loop gain method, it is done by doing the following steps:

- We set the controller as just proportional only, removing the Integral
- We increase the proportional Kp until the system output oscillates with constant amplitude (to first estimate the gain Kp without guessing it out of the blue, we have a simple logic by determining the input and output maximum mapping, as we know, the input is the current error in dq axis, while the output is the control modulating voltage, given below:



The control modulating voltage is limited from -1 to 1, as a prevention of overmodulation, we can see that the cropped output in the Vcontrol2 (red) is caused by high Kp guess, and we can reduce or mitigate it by choosing a lower Kp by the rule of thumb of → $K_{p(est)} = \frac{V_{limit}}{I_{\max(in)}} = \frac{1}{10} = \mathbf{100}\boldsymbol{m}$

File Edit Help

Parameter file name

Name FILE1

Internal file

```
1  pi = 22/7;
2  alpha = 0;
3
4  I_mag = 10;
5  Iq = I_mag * (-1)*cos(alpha);
6  Id = I_mag * (-1)*sin(alpha);
7
8  Kp = 100m;
9  Ki = 0.00001;
10 Ti = Kp/Ki;
11
```

Note that we don't set the Ki as 0 directly as it is the divider for finding Ti, as it is the input for the PI control block.

- Now we use the 2nd zieger Nichols tuning table as follows

Controller	K_p	T_i	T_d
P	$0.5\ K_{pa}$	-	–
PI	$0.45K_{pa}$	$\frac{P_a}{1.2}$	–
PID	$0.6K_{pa}$	$\frac{P_a}{2}$	$\frac{P_a}{8}$

- Therefore, we set the Kp at 50m, although through further fine tuning, we set the Kp at **47m** as follows

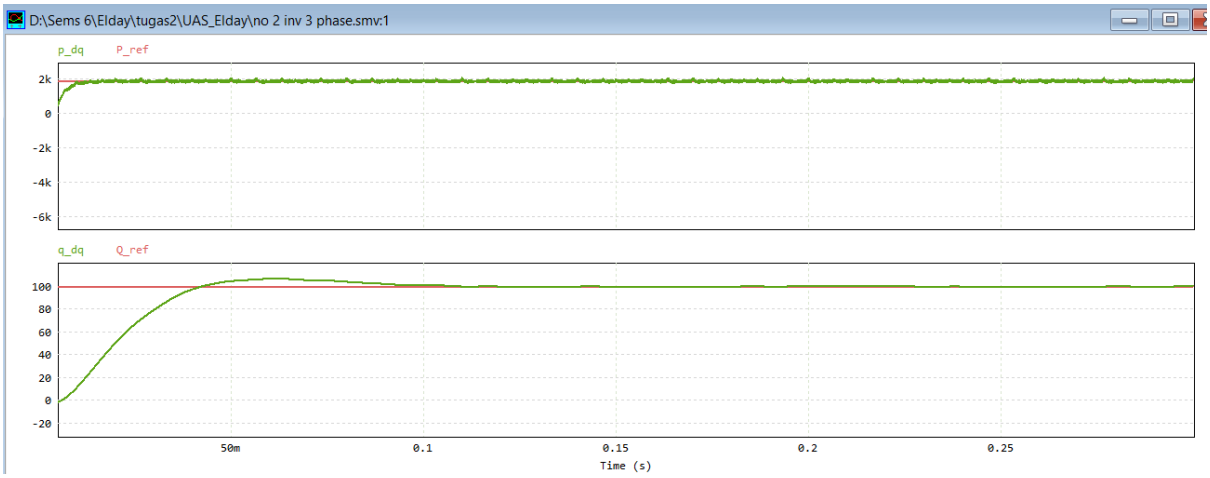
Parameter file name

Name FILE1

Internal file

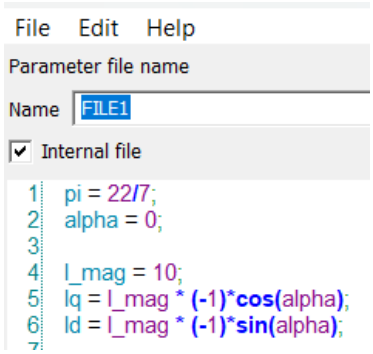
```
1  pi = 22/7;
2  alpha = 0;
3
4  I_mag = 10;
5  Iq = I_mag * (-1)*cos(alpha);
6  Id = I_mag * (-1)*sin(alpha);
7
8  Kp = 47m;
9  Ki = 18;
10 Ti = Kp/Ki;
11
```

- We now see the resulting output by plotting the reference (input) and output power, and see if the output reaches the references successfully, both active and reactive power.



6. Simulate and plot inverter currents in the dq-reference frame

We will now simulate the inverter capabilities to exert leading or lagging current in the grid. It is the representation of controlling the current in d and q axis, as it would introduces lag and lead in the phase, according to the composition of the d and q component. For the reference, we set the values using constant block, while the script automatically calculate the d and q value based on the input of our delta angle, that is the leading or lagging angle, as it is drawn in the dq plane as the angle that can decompose the current vector into d and q component



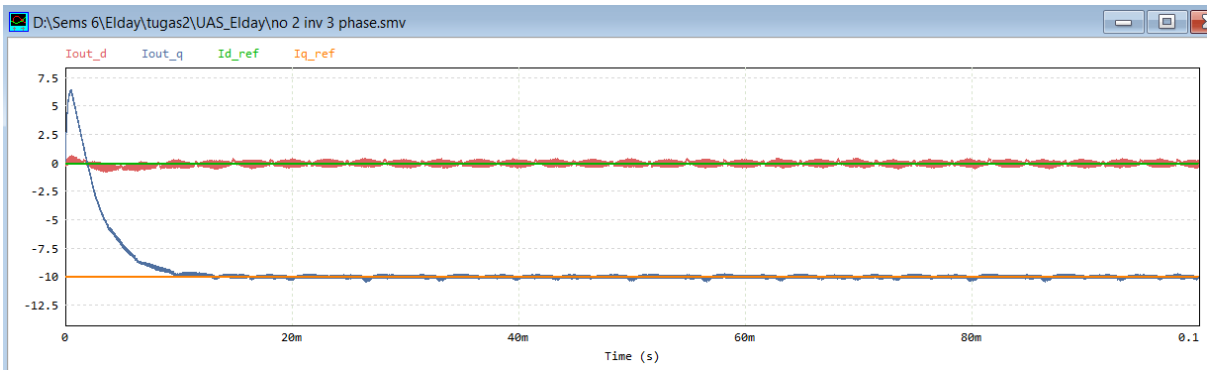
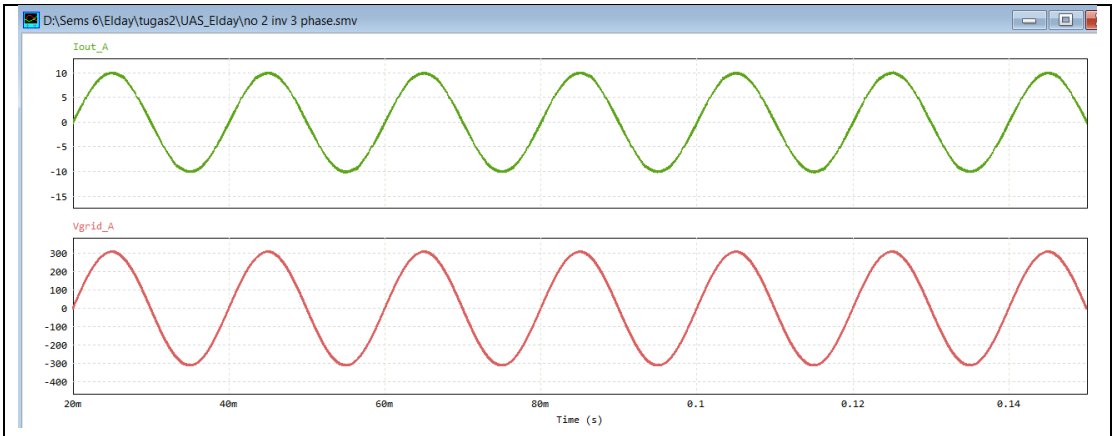
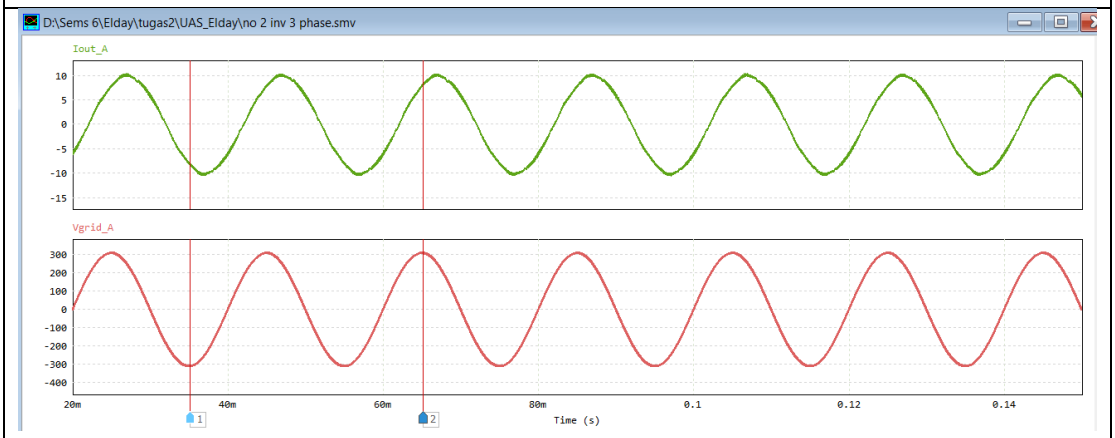


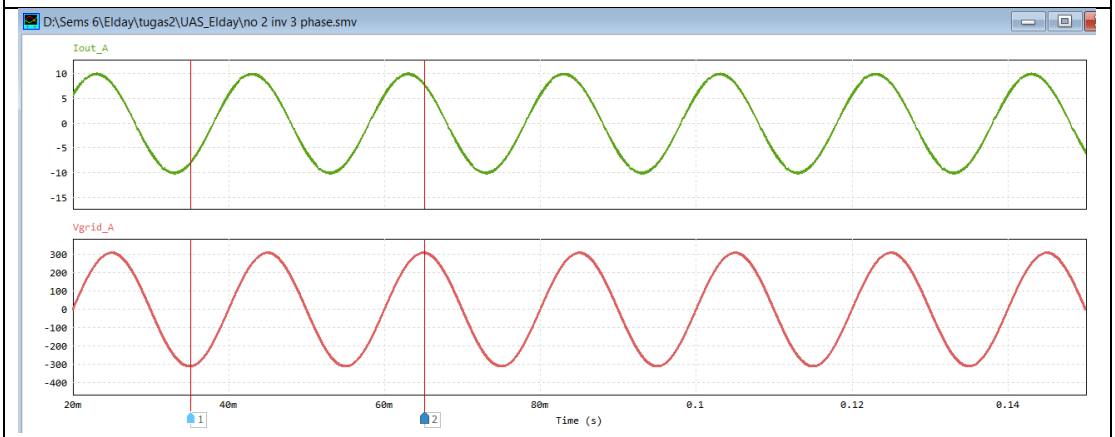
Figure 15 Comparing Reference and Measured Currents



Unity Power Factor



Leading Power Factor



Lagging Power Factor

7. **Plot the inverter output voltage (phase and line) in both time domain and frequency domain. Perform FFT analysis on the time-domain waveform to evaluate harmonic content**

To evaluate the performance of the output voltage, the parameter that were related to the power quality, we can plot the output waveform in the time domain to see if it matches with the grid voltage and plot it in frequency domain using FFT to evaluate its harmonic content.

A. Time Domain Performance

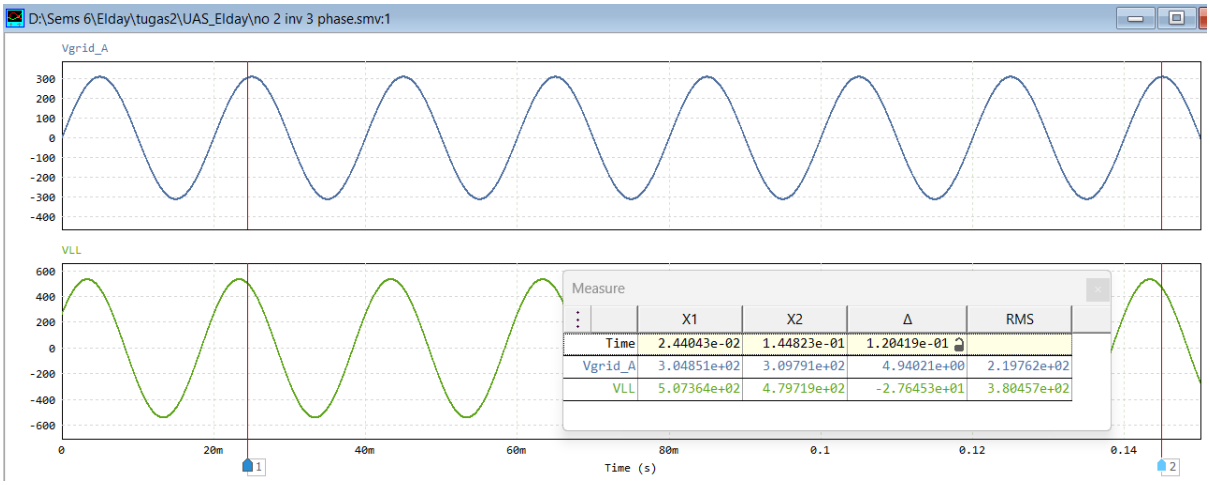


Figure 16 Time domain waveform of phase and line to line voltage

We may observe that the Vgrid_A voltage (phase voltage) is a good sinusoidal waveform with the peak reaching up to almost 311V, which is the number of $V_{peak(phase)} = \frac{V_{LL(rms)}}{\sqrt{3}} x \sqrt{2}$, and as we know the $\frac{V_{LL(rms)}}{\sqrt{3}}$ part changes the rms voltage of line to line to phase, which is **220V** as denoted in the rms value of Vgrid_A, whereas the $\sqrt{2}$ part changes from rms to peak-peak, hence **311V** peak is the result. The line to line rms value (VLL) is seen at 380V, the nominal specified grid voltage.

B. Frequency domain performance

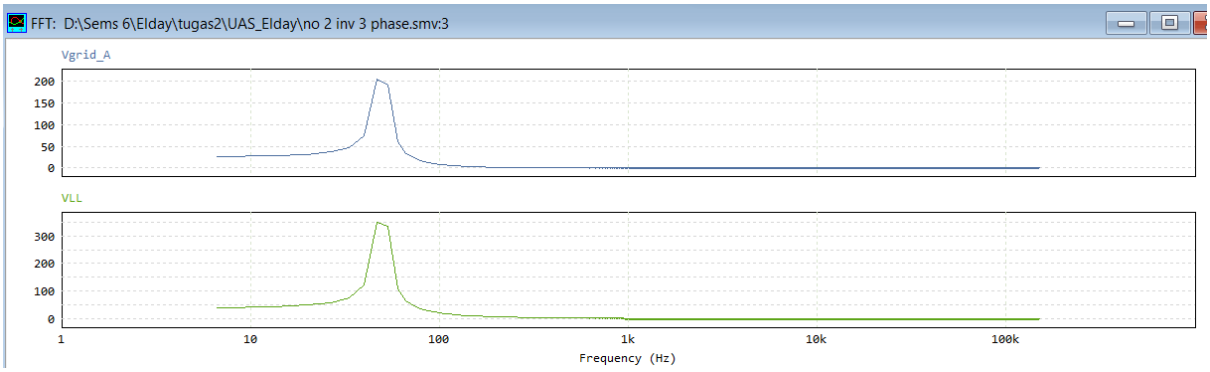


Figure 17 Frequency Domain Plot of phase and line to line voltage

From the frequency domain plot above, we can observe that the harmonic content is very low, as given in the following concept, the total harmonic distortion is given as the square root magnitude squared of the harmonic voltage component other than the fundamental frequency, or as follows:

$$THD = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}}{V1} = \frac{\sqrt{19^2 + 5^2 + 3^2}}{400} = \frac{19{,}8746}{400} = 0.0497 = \mathbf{4.97}\%$$

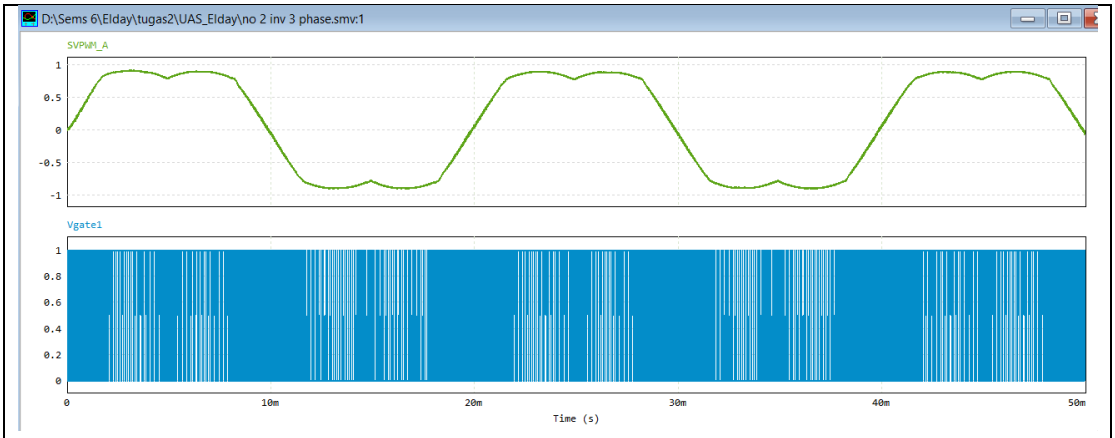
The resulting THD component still adheres to the ESDM Grid Code 2020 of the THDv (Total Harmonic Distortion of Voltage) that regulates the 5% THD limit.

8. **Analyze the system behavior under overmodulation conditions**

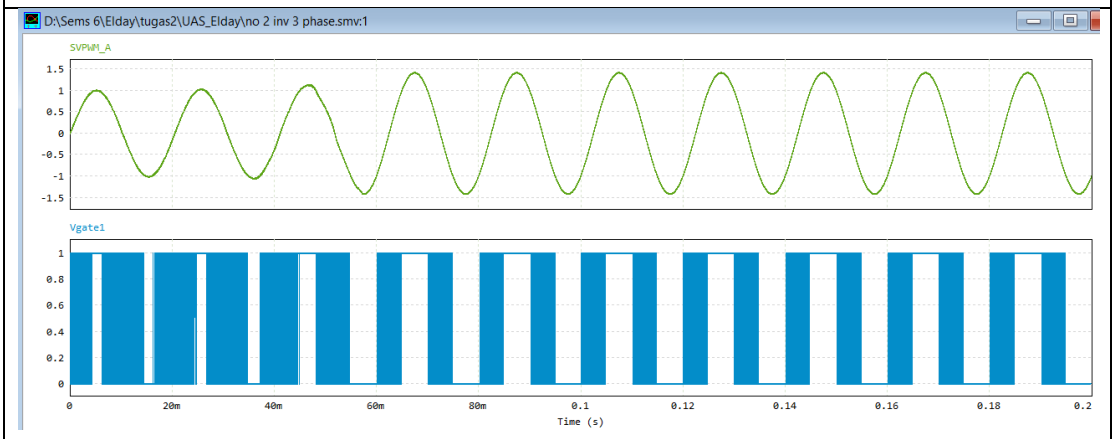
The system behavior under overmodulation is unpredictable, to sum the concepts, here is a recap on overmodulation effects

Analyze: Overmodulation may occur if for a set input voltage, the output is set for too high, and the control demand is high enough so that the modulating control signal is higher than 1, then it sometimes (at the peak) reaches higher or lower value than the entirety of the carrier signal, in that time, non-linearity occurs, as the resulting gate PWM voltage would result in a complete flat 1 or flat 0. The non linearity is caused by the fact that the control signal reaches voltage higher or lower than the carrier signal, the output will be flat regardless of the control signal value with respect to the carrier signal value, whereas on ideal condition, the relation between them is essentially linear and given as modulation index $m = \frac{V_{control}}{V_{carrier}}$, and the m essentially determines the duty cycle in the semiconductor gating. If overmodulation occurs, we lost the linearity of the modulation index.

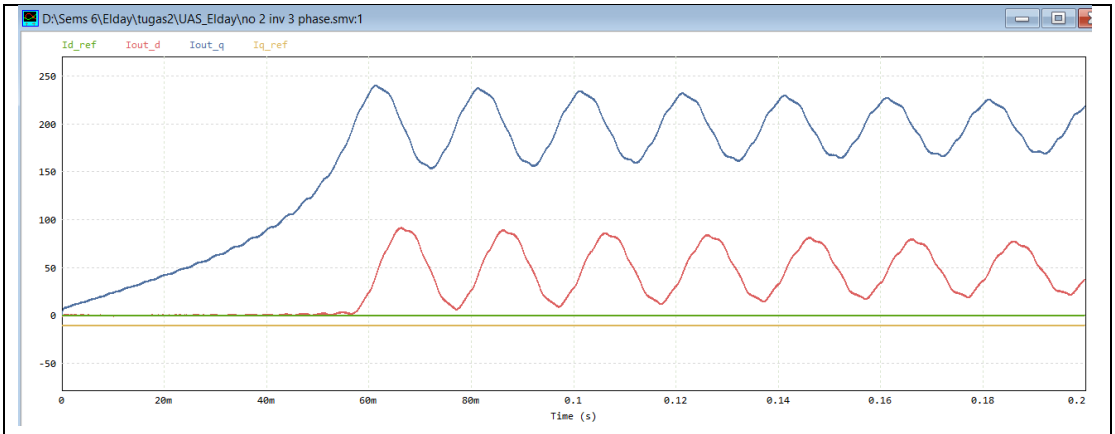
Strategy: to evaluate the effects overmodulation had on the waveform and control performance, below we will compare 3 things, the normal condition, overmodulated waveform, and overmodulation control performance degradation.



Analysis: The normal operation of the modulation occurs when the control signal magnitude is ≤ 1, in normal operation, the PWM value would result in 1 when the control signal is more than carrier signal (not plotted as it is too fast) and 0 when the control signal is less than the carrier signal. The carrier switches 35000 times per second, and we can observe than during the time when the control signal reaches its peak, the PWM is more "spaced out" as the 0s and 1s is uneven, caused by majority of the carrier is less than the control signal, only the tip of the carrier (the tip of each triangle) could get more than the control signal and produce the zeroes, this periodic spacing out and tightening is normal as it would make the output produce sine wave after the high freq carrier component is filtered out using inductor as the LPF



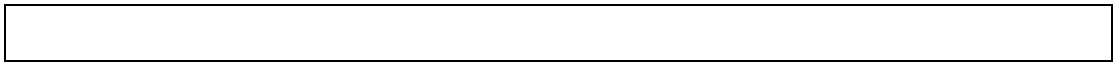
This second simulation is for overmodulation condition, we can see that the SVPWM control signal is distorted and even reaches 1.5, resulting in the switching gate output voltage getting flat values on 1 and 0



Although at first glance the voltage seems normal, we can see that the overmodulation messes the control performance as we seen in above. The Iout_d and q that should follow the Id_ref and Iq_ref slips from the stability boundaries and oscillate in an unstable value, up to hundreds of errors. This is caused by the period of flats ones and zeroes by the PWM gating signal, which is explain by the concept and relation of voltage and current in and inductor circuit as follows:

$$V_L = L.\frac{dI}{dt}$$

Analyze: When the PWM voltage is flat ones or zeroes like in the second simulation, it makes the output voltage also holds in the values of $V_{dc(in)}$ for a sufficiently long period of time, and as the output voltage is the V_L, this increases the current as during that time $\frac{dI}{dt}$ is non zero. Although at ideal condition (not overmodulated) the same event of increasing current occurs as there are times when the output voltage is $V_{dc(in)}$ when the PWM value is 1, the **key differences** lie in the duration of the ones and zeroes, as in ideal condition the average PWM frequency is the carrier frequency, this makes the period of ones and zeroes **very quick** so even with the same $\frac{dI}{dt}$ the change of current is only for a very short period of time, that is the duration of the switching period. This is why we always will have current ripple, as it is caused by the nature of the inductor reacting to sudden changes in voltage, but do note that through this logic also we can derive the current ripple specs, as we can analyze that from $V_L = L.\frac{dI}{dt}$, with the same V_L, higher inductance L results in lower values of ripple caused by $\frac{dI}{dt}$, and that the ripple was actually $\frac{dI}{dt}\ times\ t$, we can see that faster switching results in lower period t, this is why switching frequency and inductance value is the denominator in the ripple current formula, as an increase in lowers the ripple.



Appendix

https://www.ti.com/lit/an/slva477b/slva477b.pdf

- instalasi Pembangkit Listrik Tenaga Surya: Dos & Don’ts, GIZ dan Ditjen EBTKE Kementerian ESDM, 2018.
- PERATURAN MENTERI ENERGI DAN SUMBER DAYA MINERAL REPUBLIK INDONESIA NOMOR 2 TAHUN 2024
- • Panduan Perencanaan dan Pemanfaatan PLTS Atap di Indonesia, ICED II, 2020.
- • Buku Panduan Pengoperasian dan Pemeliharaan PLTS OffGrid, Ditjen EBTKE Kementerian ESDM, 2017.
- PLN Grid Code (SPLN D5.004-1:2012) and Ministerial Regulation (ESDM No. 20/2020)