R61581B0

262,144–Color, 320x480-Dot Graphics LCD Controller Driver for a-Si TFT Panel

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Description

The R61581B0 is liquid crystal controller driver LSI with internal frame memory for a-Si TFT panel sized 320RGB x 480-dot at the maximum. The driver supports MIPI DBI Type B （18/16/9/8 bits） and Type C (Options 1 and 3) as system interface to microcomputer as well as high-speed frame memory write function, enabling efficient data transfer.

The R61581B0 is also compliant with MIPI DPI (VSYNC, HSYNC, PCLK, DE, and DB[17:0]) for video image display.

The R61581B0 incorporates step-up and voltage follower circuits to generate drive voltage required for a-Si TFT panel and dynamic backlight control function to control backlight brightness depending on image data reducing power consumption at the backlight with slightest influence on the display quality.

Other features include 8-color display and power management functions, making the driver best suitable for small or mid sized portable devices such as digital mobile phones, small Pads and mobile TV devices.

*MIPI: Mobile Industrial Processor Interface, DBI: Display Bus Interface, DPI: Display Pixel Interface

Features

- Single chip driver for 262,144-color TFT 320RGB x 480-dot graphics (with internal gate and power supply circuits)
- Command set (Compliant with MIPI DCS Version 1.01.00) *DCS: Display Command Set
- System interface
  - MIPI-DBI (Compliant with MIPI DBI Version 2.00)
    - Type B 18/16/9/8 bits, 24 bits (dither)
    - Type C 4-line 9-bit (Option 1), 8-bit (Option 3)
- Video image display interface (see Note 1)
  - TE-I/F (MIPI DBI + TE synchronization signal output)
  - VSYNC I/F (MIPI DBI + VSYNC)
  - MIPI DPI (Compliant with MIPI DPI-2 Version 2.00)
- Abundant color display and drawing functions
  - 262,144-color display
  - Partial display function
- Low-power consumption architecture (allowing direct input of interface I/O power supply)
  - Deep standby mode
  - 8-color mode (Idle Mode)
  - Input power supply voltage:
    - Interface I/O and logic power supply: IOVCC1
    - Liquid crystal analog circuit power supply: VCI
- Dynamic backlight control function
- Internal liquid crystal drive power supply circuit
  - Liquid crystal drive (source driver/VCOM): DDVDH, VREG, VCL
  - Gate drive: VGH, VGL
  - VCOM drive (common VCOM method): VCOMH, VCOML

- TFT display storage capacitance: Cst (common VCOM method)
- Internal frame memory: 345,600 bytes
- Liquid crystal display drive circuits: 960 source signal lines and 480 gate signal lines
- One-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- RGB common gamma correction function
- Internal NVM (32 bits for user identification code, 7 bits for VCOM adjustment, and 5 bits for VDV): Rewriting data is guaranteed up to 5 times.
- Dummy pins used to fix pin to VCC or GND (see Note 2)

Notes: 1. Japanese Patent No.3,826,159
Korean Patent No.747, 636
United States Patent No. 7,176,870

2. Japanese Patent No. 3,980,066
Korean Patent No. 401,270
Taiwan Patent No. 175,413
United States Patent No. 6,323,930
Japanese Patent No. 4,226,627
United States Patent No. 6,924,868

Power Supply Specification

Table 1 R61581B0 Power Supply Specification

No.	Item		R61581B0
1	TFT data line drive circuit		960 outputs
2	TFT gate line drive circuit		480 outputs
3	TFT display storage capacitance		Cst (common VCOM method)
4	Liquid crystal drive output	S[960:1]	V0 ~ V63 grayscales
		G[480:1]	VGH-VGL
		VCOM	Change amplitude between VCOMH and VCOML using electronic volume
5	Input voltages	IOVCC1 (interface voltage)	1.65V ~ 3.3V Power supply to CSX, DCX, WRX/SCL, RDX, DB[17:0], DIN, DOUT, VSYNC, HSYNC, PCLK, DE, TE, IM[2:0], RESX, LEDPWM, and LEDON (when MIPI DBI Type B, MIPI Type C, or DPI is selected) Connect it to VCI on the FPC when it is set at the same electrical potential as VCI.
		IOVCC2	Unused power supply. Leave it open.
		VCI (LCD drive power supply)	2.5V ~ 3.3V
6	LCD drive supply voltages	DDVDH	4.5V ~ 6.0V
		VGH	10 ~ 18.0V
		VGL	-4.5V ~ -13.0V
		VGH-VGL	Max. 28V
		VCL	-1.9V ~ -3.0V
		VCI-VCL	Max. 6V
7	Internal step-up circuit	DDVDH	VCI1 x 2
		VGH	VCI1 x 5, x 6
		VGL	VCI1 x -3, x -4, x -5
		VCL	VCI1 x –1

Note: For voltage, see DC Characteristics in Electrical Characteristics. Set registers so that the voltage is satisfied.

Block Diagram

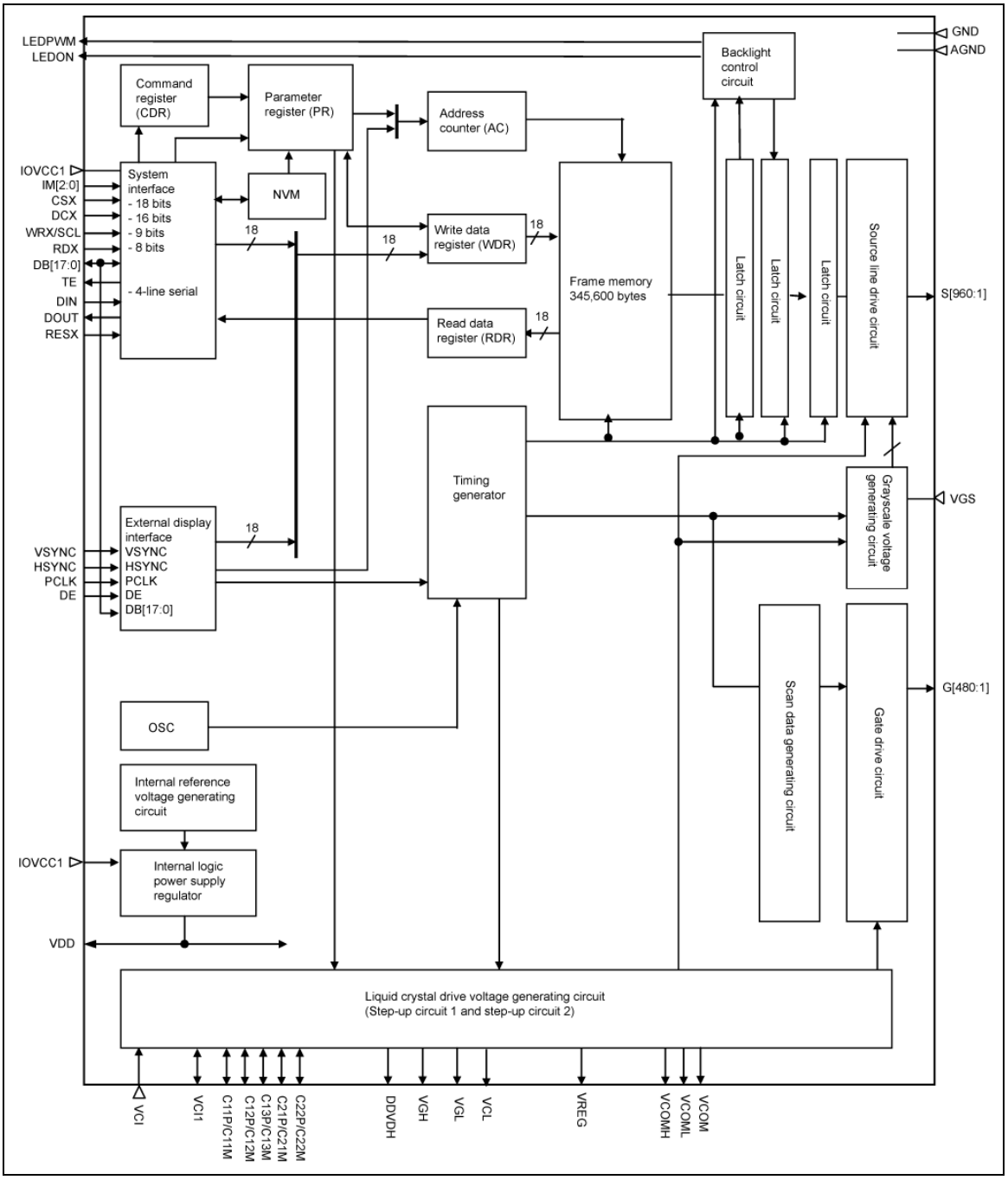


Figure 1

Block Function

1. System Interface

The R61581B0 supports MIPI DBI Type B (18/16/9/8 bits) and MIPI DBI Type C (Options 1 and 3). The interface is selected by setting IM[2:0] pin.

Table 2

IM2	IM1	IM0	Interface	Used pin	Available color number
0	0	0	DBI Type B 18 bits	DB[17:0]	262,144
0	0	1	DBI Type B 9 bits	DB[8:0]	262,144
0	1	0	DBI Type B 16 bits	DB[15:0]	65,536 / 262,144
0	1	1	DBI Type B 8 bits	DB[7:0]	65,536 / 262,144
1	0	0	Setting inhibited	—	—
1	0	1	DBI Type C 9 bits (Option 1)	DIN, DOUT	8 / 262,144
1	1	0	Setting inhibited		
1	1	1	DBI Type C 8 bits (Option 3)	DIN, DOUT	8 / 262,144

Set number of colors using set_pixel_format (3Ah).

(a) MIPI DBI Type B (18/16/9/8 Bits)

The R61581B0 supports MIPI DBI Type B (18/16/9/8 bits) that uses command method which has 8-bit command registers and 8-bit parameter registers. Also, the R61581B0 has an 18-bit write register (WDR) and read register (RDR). The WDR is used to store data temporarily that is automatically written to the internal frame memory through internal operation of the chip. The RDR is used to temporarily store the data read out from the frame memory.

The WDR is used to temporarily store the data read out from the host processor to the frame memory. For this reason, invalid data is sent to the data bus at first and valid data is sent as the R61581B0 reads second and subsequent data from the frame memory via RDR.

Table 3 Register Selection

DCX	RDX	WRX	Function
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(b) MIPI DBI Type C (Options 1 and 3)

The R61581B0 supports 9-bit (Option 1) and 8-bit (Option 3) serial interface that uses signals CSX, DCX, SCL, DIN, and DOUT.

2. Video Image Interface (TE-Signal, DPI, and VSYNC-I/F)

The R61581B0 supports TE, DPI, and VSYNC I/F as external display interface for video image.

When DBI is selected, display data is written in synchronization with TE signal which is generated from internal clock to prevent flicker on the panel.

When DPI is selected, externally supplied VSYNC, HSYNC, and PCLK signals drive the chip. Display data (DB[17:0]) is written in synchronization with those synchronous signals following data enable signal (DE). This enables updating image data without flicker on the panel.

When VSYNC-I/F is selected, the entire operation, except for synchronization with synchronous signal VSYNC, is in synchronization with internal clock. System interface (DBI) is used when display data is written to the frame memory.

3. Address Counter (AC)

The address counter (AC) gives an address to the frame memory. Address information defined by CDR and PR is transferred to the AC. The AC is automatically updated plus or minus 1 as the R61581B0 writes/reads data to/from the frame memory. Display data is may be written only to the rectangular area defined in the frame memory.

4. Frame Memory

The R61581B0 incorporates the frame memory that has a capacity of 345,600 bytes, which can store bit-pattern data of 320RGB x 480 graphics display at the maximum using 18 bits to represent one pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale setting value in the γ-correction register. RGB separate gamma correction setting enables the maximum of 262,144-color display.

6. LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates VREG, VGH, VGL, and VCOM levels to drive the liquid crystal panel.

7. Timing Generator

The timing generator is used to generate timing signals for the operation of internal circuits such as frame memory. The timing signals for display operation such as frame memory read and frame memory access by host processor are generated separately so that the two do not interfere with each other.

8. Oscillator (OSC)

The R61581B0 incorporates an oscillator. The frame frequency can be adjusted by commands.

9. LCD Driver Circuit

The LCD driver circuit consists of a 960-channel source driver (S[1:960]). The display pattern data is latched when 320RGB pixels of data are input. The voltage is output from the source driver according to the latched data. The shift direction of source output can be changed by setting SS bit (C0h). The gate driver circuit consists of a 480-channel gate driver (G[1:480]). The voltage at VGH level or VGL level is output from the gate driver. The shift direction of gate output can be changed by GS bit (C0h). The scan mode of the gate driver can be changed by SM bit (C0h) according to the mounting condition.

10. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates power supply for internal logic circuit.

11. Backlight Control Circuit

Backlight control circuit adjusts backlight brightness according to histogram of the image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

Pin Function

Table 4 System Interface Pins (Amplitude: IOVCC1 - GND)

Signal	I/O	Connect to	Function	Not in use
CSX	I	Host Processor	Chip select signal. Low: Select (Accessible) High: Not select (Inaccessible) Make sure to connect to host processor. Follow AC timing to control the signal.	-
DCX	I	Host Processor	Command/data select signal Low: Select command High: Select data	IOVCC1
WRX/SCL	I	Host Processor	Write strobe signal in DBI Type B operation. Write data when WRX is Low. Synchronous clock signal in DBI Type C operation.	-
RDX	I	Host Processor	Read strobe signal. Read out data when RDX is Low.	IOVCC1
DIN	I	Host Processor	Serial data input pin in DBI Type C operation to input data on the rising edge of SCL signal.	GND/IOVCC1
DOUT	O	Host Processor	Serial data output pin in DBI Type C operation to input data on the falling edge of SCL signal.	Open
DB[17:0]	I/O	Host Processor	18-bit bi-directional data bus in DBI Type B operation. 8-bit interface: Use DB [7:0] 9-bit interface: Use DB[8:0] 16-bit interface: Use DB [15:0] 18-bit interface: Use DB[17:0] Abnormal current (through current) does not occur when CSX is High and the data bus is Hi-z. 18-bit input data bus in DPI operation. 16-bit interface: Use DB[15:0] 18-bit interface: Use DB[17:0]	GND/IOVCC1
DE	I	Host Processor	Data enable signal in DPI operation. Low: Select (Accessible) High: Not select (inaccessible)	GND/IOVCC1
VSYNC	I	Host Processor	Frame synchronous signal. Low active.	GND/IOVCC1
HSYNC	I	Host Processor	Line synchronous signal. Low active.	GND/IOVCC1
PCLK	I	Host Processor	Pixel clock signal. The data input timing is set on the rising edge.	GND/IOVCC1
TE	O	Host Processor	Tearing Effect output signal	Open
IM[2:0]	I	Host Processor	Interface select signal. Select from DBI Type B (18/16/9/8 bits) and Type C (Option 1 / Option 3).	-
RESX	I	Host Processor or external RC oscillator	Reset pin. The R61581B0 is initialized when RESX is Low. Make sure to execute power-on reset when turning the power supply on.	-

Table 5 LED Driver Control Pins (Amplitude: IOVCC1-GND)

Signal	I/O	Connect to	Function	Not in use
LEDPWM	O	LED driver	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High).	Open
LEDON	O	LED driver	The value written in the LEDON register becomes LEDON signal and it is output. When LED is controlled by this product, it is useful.	Open

Table 6 External Power Supply Pins

Signal	I/O	Connect to	Function	Not in use
IOVCC1	I	Power supply	Power supply to interface pins and internal VDD regulator.	-
IOVCC2	I	Power supply	Unused power supply. Leave it open.	-
VCI	I	Power supply	Power supply to liquid crystal power supply analog circuit.	-
GND	I	Power supply	GND for Internal logic and interface pins.	-
AGND	I	Power supply	Analog GND (logic regulator and liquid crystal power supply circuit). Connect to GND on the FPC to prevent noise in case of COG.	

Note: GND and AGND pins are located on several places on the chip. Make sure to connect electrical potential to all of them as "R61581B0 Wiring Example and Recommended Wiring Resistance" instructs.

Table 7 Power Supply Circuit Pins

Signal	I/O	Connect to	Function	Not in use
VDD	O	Stabilizing capacitor	Output from internal logic regulator. Connect to stabilizing capacitor.	-
VCI1	I/O	Stabilizing capacitor	Reference voltage for a step-up circuit 1. Set the VCI1 level so that DDVDH, VGH, and VGL do not exceed the respective voltage setting ranges.	-
DDVDH	O	Stabilizing capacitor	Source driver liquid crystal and VCOM drive power supply. The output level from the step-up circuit 1, generated from VCI1. The step-up factor is 2. Connect to stabilizing capacitor.	-
VGH	O	Stabilizing capacitor, liquid crystal panel	Liquid crystal drives power supply. The output level form a step-up circuit 2, generated from VCI1 and DDVDH. The output level is determined by the step-up factor, which is set by instruction (BT[2:0]). Connect to stabilizing capacitor.	-
VGL	O	Stabilizing capacitor, liquid crystal panel	Liquid crystal drives power supply. The output level form the step-up circuit 2, generated from VCI1 and DDVDH. The output level is determined by the step-up factor, which is set by instruction (BT[2:0]). Connect to stabilizing capacitor.	-
VCL	O	Stabilizing capacitor	VCOML drive power supply. Connect to stabilizing capacitor.	-
C11P, C11M, C12P, C12M,	I/O	Step-up capacitor	Capacitor connection pins for step-up circuit 1.	-
C13P, C13M, C21P, C21M, C22P, C22M	I/O	Step-up capacitor	Capacitor connection pins for step-up circuit 2.	-

Table 8 LCD Drive Power Supply Pins

Signal	I/O	Connect to	Function	Not in use
VREG	O	Stabilizing capacitor	The output level generated from VCIR. The output level from the internal reference power supply is determined by the factor, which is set by instruction (VRH*). VREG serves as reference of (1) source driver grayscale, (2) VCOMH level, and (3) VCOM width. Connect a stabilizing capacitor to use this pin.	-
VCOM	O	TFT common electrode	Power supply to TFT panel's common electrode. VCOM output level alternates between VCOMH and VCOML. The alternating cycle is set by a register. Also, the VCOM output can be started and halted by register setting.	-
VCOMH	O	Stabilizing capacitor	VCOM High level.	-
VCOML	O	Stabilizing capacitor	VCOM Low level, which is set by instruction (VDV).	-
VGS	I	GND	Reference level of the grayscale voltage generating circuit.	-
S[1:960]	O	Liquid crystal panel	Liquid crystal application voltages.	Open
G[1:480]	O	Liquid crystal panel	Gate line output signals. VGH: Gate line is selected. VGL: Gate line is not selected.	Open

Table 9 Other Pins (Test and Dummy)

Signal	I/O	Connect to	Function	Not in use
VREFC	I	Open	Test pin. Leave it open (connected to a pull-down resistor).	Open
VREFD	O	Open	Test pin. Leave it open.	Open
VREF	O	Open	Test pin. Leave it open.	Open
VDDTEST	I	Open	Test pin. Leave it open (connected to a pull-down resistor).	Open
GNDDUM[16:1] AGNDDUM[3:1]	O	-	Pins to fix electrical potential. The electrical potential can be fixed by connecting unused interface pins and test pins to these dummy pins on the glass. Leave them open when they are not used.	Open
DUMMY[2:1]	O	-	Dummy pins. Leave them open.	Open
TESTO[16:1]	I	Open	Test pin. Leave it open.	Open
TEST[2:1]	I	Open	Test pin. Leave it open (connected to a pull-down resistor).	Open
TSC	I	Open	Test pin. Leave it open (connected to a pull-down resistor).	Open
VPP1	I	GND	Test pin. Connect to GND or leave it open.	Open

PATENT ISSUED: Japanese Patent No. 3,980,066
Korean Patent No. 401,270
Taiwan Patent No. 175,413
United States Patent No. 6,323,930
Japanese Patent No. 4,226,627
United States Patent No. 6,924,868

Alignment Mark

- Chip size: 22.77mm x 0.77mm
- Chip thickness: 280um (typ.)
- Pad coordinate: Pad center
- Pad origin: Chip center

- Au bump size:
(1) 50um x 102um (I/O side No.1-320)
(2) 15um x 100um (liquid crystal output side No.321-1776)

- Au bump pitch: See "Bump Arrangement."
- Au bump heightness: 12um

- Alignment mark

Alignment mark	X	Y
(1-a)	-11300.0	-268.0
(1-b)	11300.0	-268.0

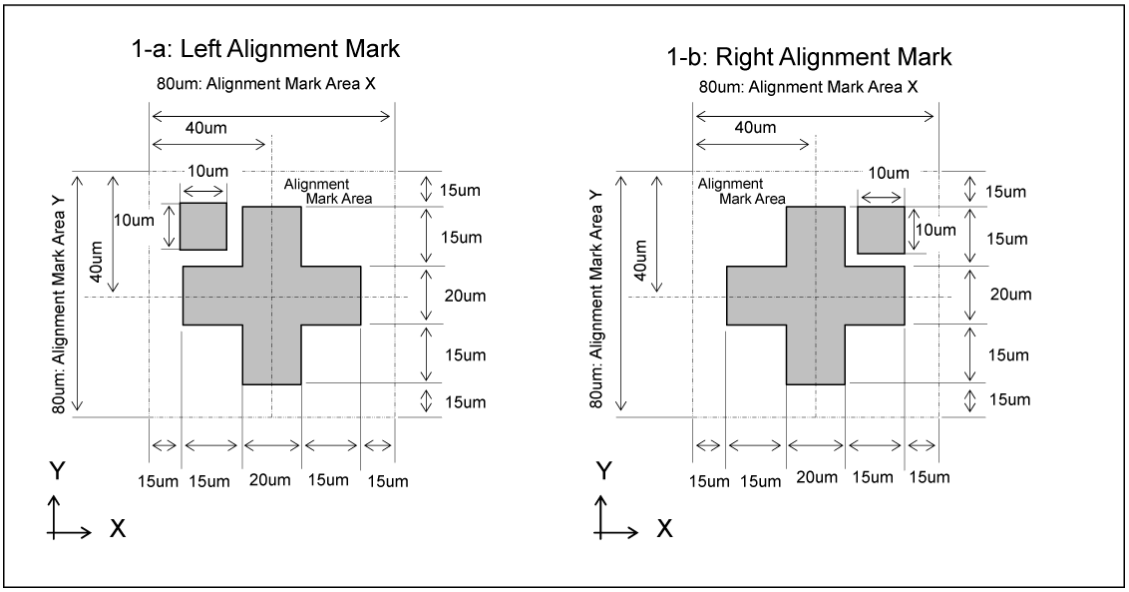


Figure 2

R61581B0 Pad Coordinates (No.1)

(unit: um)

Pad No.	Pad Name	X	Y
1	VPP1	-11165.0	-288.0
2	VPP1	-11095.0	-288.0
3	GND	-11025.0	-288.0
4	GND	-10955.0	-288.0
5	GNDDUM1	-10885.0	-288.0
6	GNDDUM2	-10815.0	-288.0
7	GNDDUM3	-10745.0	-288.0
8	LEDON	-10675.0	-288.0
9	LEDPWM	-10605.0	-288.0
10	GNDDUM4	-10535.0	-288.0
11	GNDDUM5	-10465.0	-288.0
12	GNDDUM6	-10395.0	-288.0
13	IOVCC2	-10325.0	-288.0
14	IOVCC2	-10255.0	-288.0
15	IOVCC2	-10185.0	-288.0
16	GNDDUM[9]	-10115.0	-288.0
17	GNDDUM[10]	-10045.0	-288.0
18	GNDDUM[11]	-9975.0	-288.0
19	GNDDUM[12]	-9905.0	-288.0
20	GNDDUM[13]	-9835.0	-288.0
21	GNDDUM[14]	-9765.0	-288.0
22	GNDDUM[15]	-9695.0	-288.0
23	GNDDUM[16]	-9625.0	-288.0
24	GNDDUM7	-9555.0	-288.0
25	VREF	-9485.0	-288.0
26	VREFD	-9415.0	-288.0
27	VREFC	-9345.0	-288.0
28	VDDTEST	-9275.0	-288.0
29	GNDDUM8	-9205.0	-288.0
30	TSC	-9135.0	-288.0
31	TEST1	-9065.0	-288.0
32	TEST2	-8995.0	-288.0
33	DUMMY1	-8925.0	-288.0
34	DUMMY2	-8855.0	-288.0
35	IM0	-8785.0	-288.0
36	IM1	-8715.0	-288.0
37	IM2	-8645.0	-288.0
38	RESX	-8575.0	-288.0
39	VSYNC	-8505.0	-288.0
40	HSYNC	-8435.0	-288.0
41	PCLK	-8365.0	-288.0
42	DE	-8295.0	-288.0
43	DB17	-8225.0	-288.0
44	DB16	-8155.0	-288.0
45	DB15	-8085.0	-288.0
46	DB14	-8015.0	-288.0
47	DB13	-7945.0	-288.0
48	DB12	-7875.0	-288.0
49	DB11	-7805.0	-288.0
50	DB10	-7735.0	-288.0

(unit: um)

Pad No.	Pad Name	X	Y
51	DB9	-7665.0	-288.0
52	DB8	-7595.0	-288.0
53	DB7	-7525.0	-288.0
54	DB6	-7455.0	-288.0
55	DB5	-7385.0	-288.0
56	DB4	-7315.0	-288.0
57	DB3	-7245.0	-288.0
58	DB2	-7175.0	-288.0
59	DB1	-7105.0	-288.0
60	DB0	-7035.0	-288.0
61	DOUT	-6965.0	-288.0
62	DIN	-6895.0	-288.0
63	RDX	-6825.0	-288.0
64	WRX	-6755.0	-288.0
65	DCX	-6685.0	-288.0
66	CSX	-6615.0	-288.0
67	TE	-6545.0	-288.0
68	IOVCC1	-6475.0	-288.0
69	IOVCC1	-6405.0	-288.0
70	IOVCC1	-6335.0	-288.0
71	IOVCC1	-6265.0	-288.0
72	IOVCC1	-6195.0	-288.0
73	IOVCC1	-6125.0	-288.0
74	IOVCC1	-6055.0	-288.0
75	VDD	-5985.0	-288.0
76	VDD	-5915.0	-288.0
77	VDD	-5845.0	-288.0
78	VDD	-5775.0	-288.0
79	VDD	-5705.0	-288.0
80	VDD	-5635.0	-288.0
81	VDD	-5565.0	-288.0
82	VDD	-5495.0	-288.0
83	VDD	-5425.0	-288.0
84	VDD	-5355.0	-288.0
85	VDD	-5285.0	-288.0
86	GND	-5215.0	-288.0
87	GND	-5145.0	-288.0
88	GND	-5075.0	-288.0
89	GND	-5005.0	-288.0
90	GND	-4935.0	-288.0
91	GND	-4865.0	-288.0
92	GND	-4795.0	-288.0
93	GND	-4725.0	-288.0
94	VGS	-4655.0	-288.0
95	VGS	-4585.0	-288.0
96	AGNDDUM1	-4515.0	-288.0
97	AGND	-4445.0	-288.0
98	AGND	-4375.0	-288.0
99	AGND	-4305.0	-288.0
100	AGND	-4235.0	-288.0

R61581B0 Pad Coordinates (No.2)

(unit: um)

Pad No.	Pad Name	X	Y
101	AGND	-4165.0	-288.0
102	AGND	-4095.0	-288.0
103	AGND	-4025.0	-288.0
104	AGND	-3955.0	-288.0
105	AGND	-3885.0	-288.0
106	AGND	-3815.0	-288.0
107	VCOM	-3745.0	-288.0
108	VCOM	-3675.0	-288.0
109	VCOM	-3605.0	-288.0
110	VCOM	-3535.0	-288.0
111	VCOM	-3465.0	-288.0
112	VCOM	-3395.0	-288.0
113	VCOM	-3325.0	-288.0
114	VCOM	-3255.0	-288.0
115	VCOM	-3185.0	-288.0
116	VCOM	-3115.0	-288.0
117	VCOM	-3045.0	-288.0
118	VCOM	-2975.0	-288.0
119	VCOM	-2905.0	-288.0
120	VCOM	-2835.0	-288.0
121	VCOM	-2765.0	-288.0
122	VCOM	-2695.0	-288.0
123	VCOMH	-2625.0	-288.0
124	VCOMH	-2555.0	-288.0
125	VCOMH	-2485.0	-288.0
126	VCOMH	-2415.0	-288.0
127	VCOMH	-2345.0	-288.0
128	VCOMH	-2275.0	-288.0
129	VCOMH	-2205.0	-288.0
130	VCOMH	-2135.0	-288.0
131	VCOMH	-2065.0	-288.0
132	VCOMH	-1995.0	-288.0
133	VCOML	-1925.0	-288.0
134	VCOML	-1855.0	-288.0
135	VCOML	-1785.0	-288.0
136	VCOML	-1715.0	-288.0
137	VCOML	-1645.0	-288.0
138	VCOML	-1575.0	-288.0
139	VCOML	-1505.0	-288.0
140	VREG1OUT	-1435.0	-288.0
141	VREG1OUT	-1365.0	-288.0
142	VREG1OUT	-1295.0	-288.0
143	VREG1OUT	-1225.0	-288.0
144	AGNDDUM2	-1155.0	-288.0
145	VCL	-1085.0	-288.0
146	VCL	-1015.0	-288.0
147	VCL	-945.0	-288.0
148	VCL	-875.0	-288.0
149	VCL	-805.0	-288.0
150	VCL	-735.0	-288.0

(unit: um)

Pad No.	Pad Name	X	Y
151	VCL	-665.0	-288.0
152	VCL	-595.0	-288.0
153	VCL	-525.0	-288.0
154	DDVDH	-455.0	-288.0
155	DDVDH	-385.0	-288.0
156	DDVDH	-315.0	-288.0
157	DDVDH	-245.0	-288.0
158	DDVDH	-175.0	-288.0
159	DDVDH	-105.0	-288.0
160	DDVDH	-35.0	-288.0
161	DDVDH	35.0	-288.0
162	DDVDH	105.0	-288.0
163	VCI1	175.0	-288.0
164	VCI1	245.0	-288.0
165	VCI1	315.0	-288.0
166	VCI1	385.0	-288.0
167	VCI1	455.0	-288.0
168	VCI1	525.0	-288.0
169	VCI1	595.0	-288.0
170	VCI1	665.0	-288.0
171	VCI1	735.0	-288.0
172	VCI1	805.0	-288.0
173	VCI1	875.0	-288.0
174	VCI	945.0	-288.0
175	VCI	1015.0	-288.0
176	VCI	1085.0	-288.0
177	VCI	1155.0	-288.0
178	VCI	1225.0	-288.0
179	VCI	1295.0	-288.0
180	VCI	1365.0	-288.0
181	VCI	1435.0	-288.0
182	VCI	1505.0	-288.0
183	VCI	1575.0	-288.0
184	VCI	1645.0	-288.0
185	VCI	1715.0	-288.0
186	VCI	1785.0	-288.0
187	VCI	1855.0	-288.0
188	VCI	1925.0	-288.0
189	VCI	1995.0	-288.0
190	VCI	2065.0	-288.0
191	VCI	2135.0	-288.0
192	VCI	2205.0	-288.0
193	AGNDDUM3	2275.0	-288.0
194	C11M	2345.0	-288.0
195	C11M	2415.0	-288.0
196	C11M	2485.0	-288.0
197	C11M	2555.0	-288.0
198	C11M	2625.0	-288.0
199	C11M	2695.0	-288.0
200	C11M	2765.0	-288.0

R61581B0 Pad Coordinates (No.3)

(unit: um)

Pad No.	Pad Name	X	Y
201	C11M	2835.0	-288.0
202	C11M	2905.0	-288.0
203	C11M	2975.0	-288.0
204	C11M	3045.0	-288.0
205	C11P	3115.0	-288.0
206	C11P	3185.0	-288.0
207	C11P	3255.0	-288.0
208	C11P	3325.0	-288.0
209	C11P	3395.0	-288.0
210	C11P	3465.0	-288.0
211	C11P	3535.0	-288.0
212	C11P	3605.0	-288.0
213	C11P	3675.0	-288.0
214	C11P	3745.0	-288.0
215	C11P	3815.0	-288.0
216	C12M	3885.0	-288.0
217	C12M	3955.0	-288.0
218	C12M	4025.0	-288.0
219	C12M	4095.0	-288.0
220	C12M	4165.0	-288.0
221	C12M	4235.0	-288.0
222	C12M	4305.0	-288.0
223	C12M	4375.0	-288.0
224	C12M	4445.0	-288.0
225	C12M	4515.0	-288.0
226	C12P	4585.0	-288.0
227	C12P	4655.0	-288.0
228	C12P	4725.0	-288.0
229	C12P	4795.0	-288.0
230	C12P	4865.0	-288.0
231	C12P	4935.0	-288.0
232	C12P	5005.0	-288.0
233	C12P	5075.0	-288.0
234	C12P	5145.0	-288.0
235	C12P	5215.0	-288.0
236	VGL	5285.0	-288.0
237	VGL	5355.0	-288.0
238	VGL	5425.0	-288.0
239	VGL	5495.0	-288.0
240	VGL	5565.0	-288.0
241	VGL	5635.0	-288.0
242	VGL	5705.0	-288.0
243	VGL	5775.0	-288.0
244	VGL	5845.0	-288.0
245	VGL	5915.0	-288.0
246	AGND	5985.0	-288.0
247	AGND	6055.0	-288.0
248	AGND	6125.0	-288.0
249	VGH	6195.0	-288.0
250	VGH	6265.0	-288.0

(unit: um)

Pad No.	Pad Name	X	Y
251	VGH	6335.0	-288.0
252	VGH	6405.0	-288.0
253	VGH	6475.0	-288.0
254	VGH	6545.0	-288.0
255	VGH	6615.0	-288.0
256	VGH	6685.0	-288.0
257	C13M	6755.0	-288.0
258	C13M	6825.0	-288.0
259	C13M	6895.0	-288.0
260	C13M	6965.0	-288.0
261	C13M	7035.0	-288.0
262	C13M	7105.0	-288.0
263	C13P	7175.0	-288.0
264	C13P	7245.0	-288.0
265	C13P	7315.0	-288.0
266	C13P	7385.0	-288.0
267	C13P	7455.0	-288.0
268	C13P	7525.0	-288.0
269	C21M	7595.0	-288.0
270	C21M	7665.0	-288.0
271	C21M	7735.0	-288.0
272	C21M	7805.0	-288.0
273	C21M	7875.0	-288.0
274	C21M	7945.0	-288.0
275	C21M	8015.0	-288.0
276	C21M	8085.0	-288.0
277	C21M	8155.0	-288.0
278	C21M	8225.0	-288.0
279	C21M	8295.0	-288.0
280	C21M	8365.0	-288.0
281	C21M	8435.0	-288.0
282	C21M	8505.0	-288.0
283	C21P	8575.0	-288.0
284	C21P	8645.0	-288.0
285	C21P	8715.0	-288.0
286	C21P	8785.0	-288.0
287	C21P	8855.0	-288.0
288	C21P	8925.0	-288.0
289	C21P	8995.0	-288.0
290	C21P	9065.0	-288.0
291	C21P	9135.0	-288.0
292	C21P	9205.0	-288.0
293	C21P	9275.0	-288.0
294	C21P	9345.0	-288.0
295	C21P	9415.0	-288.0
296	C22M	9485.0	-288.0
297	C22M	9555.0	-288.0
298	C22M	9625.0	-288.0
299	C22M	9695.0	-288.0
300	C22M	9765.0	-288.0

R61581B0 Pad Coordinates (No.4)

(unit: um)

Pad No.	Pad Name	X	Y
301	C22M	9835.0	-288.0
302	C22M	9905.0	-288.0
303	C22M	9975.0	-288.0
304	C22M	10045.0	-288.0
305	C22M	10115.0	-288.0
306	C22M	10185.0	-288.0
307	C22M	10255.0	-288.0
308	C22P	10325.0	-288.0
309	C22P	10395.0	-288.0
310	C22P	10465.0	-288.0
311	C22P	10535.0	-288.0
312	C22P	10605.0	-288.0
313	C22P	10675.0	-288.0
314	C22P	10745.0	-288.0
315	C22P	10815.0	-288.0
316	C22P	10885.0	-288.0
317	C22P	10955.0	-288.0
318	C22P	11025.0	-288.0
319	C22P	11095.0	-288.0
320	C22P	11165.0	-288.0
321	TESTO1	11205.0	166.0
322	TESTO2	11190.0	291.0
323	G1	11175.0	166.0
324	G3	11160.0	291.0
325	G5	11145.0	166.0
326	G7	11130.0	291.0
327	G9	11115.0	166.0
328	G11	11100.0	291.0
329	G13	11085.0	166.0
330	G15	11070.0	291.0
331	G17	11055.0	166.0
332	G19	11040.0	291.0
333	G21	11025.0	166.0
334	G23	11010.0	291.0
335	G25	10995.0	166.0
336	G27	10980.0	291.0
337	G29	10965.0	166.0
338	G31	10950.0	291.0
339	G33	10935.0	166.0
340	G35	10920.0	291.0
341	G37	10905.0	166.0
342	G39	10890.0	291.0
343	G41	10875.0	166.0
344	G43	10860.0	291.0
345	G45	10845.0	166.0
346	G47	10830.0	291.0
347	G49	10815.0	166.0
348	G51	10800.0	291.0
349	G53	10785.0	166.0
350	G55	10770.0	291.0

(unit: um)

Pad No.	Pad Name	X	Y
351	G57	10755.0	166.0
352	G59	10740.0	291.0
353	G61	10725.0	166.0
354	G63	10710.0	291.0
355	G65	10695.0	166.0
356	G67	10680.0	291.0
357	G69	10665.0	166.0
358	G71	10650.0	291.0
359	G73	10635.0	166.0
360	G75	10620.0	291.0
361	G77	10605.0	166.0
362	G79	10590.0	291.0
363	G81	10575.0	166.0
364	G83	10560.0	291.0
365	G85	10545.0	166.0
366	G87	10530.0	291.0
367	G89	10515.0	166.0
368	G91	10500.0	291.0
369	G93	10485.0	166.0
370	G95	10470.0	291.0
371	G97	10455.0	166.0
372	G99	10440.0	291.0
373	G101	10425.0	166.0
374	G103	10410.0	291.0
375	G105	10395.0	166.0
376	G107	10380.0	291.0
377	G109	10365.0	166.0
378	G111	10350.0	291.0
379	G113	10335.0	166.0
380	G115	10320.0	291.0
381	G117	10305.0	166.0
382	G119	10290.0	291.0
383	G121	10275.0	166.0
384	G123	10260.0	291.0
385	G125	10245.0	166.0
386	G127	10230.0	291.0
387	G129	10215.0	166.0
388	G131	10200.0	291.0
389	G133	10185.0	166.0
390	G135	10170.0	291.0
391	G137	10155.0	166.0
392	G139	10140.0	291.0
393	G141	10125.0	166.0
394	G143	10110.0	291.0
395	G145	10095.0	166.0
396	G147	10080.0	291.0
397	G149	10065.0	166.0
398	G151	10050.0	291.0
399	G153	10035.0	166.0
400	G155	10020.0	291.0

R61581B0 Pad Coordinates (No.5)

(unit: um)

Pad No.	Pad Name	X	Y
401	G157	10005.0	166.0
402	G159	9990.0	291.0
403	G161	9975.0	166.0
404	G163	9960.0	291.0
405	G165	9945.0	166.0
406	G167	9930.0	291.0
407	G169	9915.0	166.0
408	G171	9900.0	291.0
409	G173	9885.0	166.0
410	G175	9870.0	291.0
411	G177	9855.0	166.0
412	G179	9840.0	291.0
413	G181	9825.0	166.0
414	G183	9810.0	291.0
415	G185	9795.0	166.0
416	G187	9780.0	291.0
417	G189	9765.0	166.0
418	G191	9750.0	291.0
419	G193	9735.0	166.0
420	G195	9720.0	291.0
421	G197	9705.0	166.0
422	G199	9690.0	291.0
423	G201	9675.0	166.0
424	G203	9660.0	291.0
425	G205	9645.0	166.0
426	G207	9630.0	291.0
427	G209	9615.0	166.0
428	G211	9600.0	291.0
429	G213	9585.0	166.0
430	G215	9570.0	291.0
431	G217	9555.0	166.0
432	G219	9540.0	291.0
433	G221	9525.0	166.0
434	G223	9510.0	291.0
435	G225	9495.0	166.0
436	G227	9480.0	291.0
437	G229	9465.0	166.0
438	G231	9450.0	291.0
439	G233	9435.0	166.0
440	G235	9420.0	291.0
441	G237	9405.0	166.0
442	G239	9390.0	291.0
443	G241	9375.0	166.0
444	G243	9360.0	291.0
445	G245	9345.0	166.0
446	G247	9330.0	291.0
447	G249	9315.0	166.0
448	G251	9300.0	291.0
449	G253	9285.0	166.0
450	G255	9270.0	291.0

(unit: um)

Pad No.	Pad Name	X	Y
451	G257	9255.0	166.0
452	G259	9240.0	291.0
453	G261	9225.0	166.0
454	G263	9210.0	291.0
455	G265	9195.0	166.0
456	G267	9180.0	291.0
457	G269	9165.0	166.0
458	G271	9150.0	291.0
459	G273	9135.0	166.0
460	G275	9120.0	291.0
461	G277	9105.0	166.0
462	G279	9090.0	291.0
463	G281	9075.0	166.0
464	G283	9060.0	291.0
465	G285	9045.0	166.0
466	G287	9030.0	291.0
467	G289	9015.0	166.0
468	G291	9000.0	291.0
469	G293	8985.0	166.0
470	G295	8970.0	291.0
471	G297	8955.0	166.0
472	G299	8940.0	291.0
473	G301	8925.0	166.0
474	G303	8910.0	291.0
475	G305	8895.0	166.0
476	G307	8880.0	291.0
477	G309	8865.0	166.0
478	G311	8850.0	291.0
479	G313	8835.0	166.0
480	G315	8820.0	291.0
481	G317	8805.0	166.0
482	G319	8790.0	291.0
483	G321	8775.0	166.0
484	G323	8760.0	291.0
485	G325	8745.0	166.0
486	G327	8730.0	291.0
487	G329	8715.0	166.0
488	G331	8700.0	291.0
489	G333	8685.0	166.0
490	G335	8670.0	291.0
491	G337	8655.0	166.0
492	G339	8640.0	291.0
493	G341	8625.0	166.0
494	G343	8610.0	291.0
495	G345	8595.0	166.0
496	G347	8580.0	291.0
497	G349	8565.0	166.0
498	G351	8550.0	291.0
499	G353	8535.0	166.0
500	G355	8520.0	291.0

R61581B0 Pad Coordinates (No.6)

(unit: um)

Pad No.	Pad Name	X	Y
501	G357	8505.0	166.0
502	G359	8490.0	291.0
503	G361	8475.0	166.0
504	G363	8460.0	291.0
505	G365	8445.0	166.0
506	G367	8430.0	291.0
507	G369	8415.0	166.0
508	G371	8400.0	291.0
509	G373	8385.0	166.0
510	G375	8370.0	291.0
511	G377	8355.0	166.0
512	G379	8340.0	291.0
513	G381	8325.0	166.0
514	G383	8310.0	291.0
515	G385	8295.0	166.0
516	G387	8280.0	291.0
517	G389	8265.0	166.0
518	G391	8250.0	291.0
519	G393	8235.0	166.0
520	G395	8220.0	291.0
521	G397	8205.0	166.0
522	G399	8190.0	291.0
523	G401	8175.0	166.0
524	G403	8160.0	291.0
525	G405	8145.0	166.0
526	G407	8130.0	291.0
527	G409	8115.0	166.0
528	G411	8100.0	291.0
529	G413	8085.0	166.0
530	G415	8070.0	291.0
531	G417	8055.0	166.0
532	G419	8040.0	291.0
533	G421	8025.0	166.0
534	G423	8010.0	291.0
535	G425	7995.0	166.0
536	G427	7980.0	291.0
537	G429	7965.0	166.0
538	G431	7950.0	291.0
539	G433	7935.0	166.0
540	G435	7920.0	291.0
541	G437	7905.0	166.0
542	G439	7890.0	291.0
543	G441	7875.0	166.0
544	G443	7860.0	291.0
545	G445	7845.0	166.0
546	G447	7830.0	291.0
547	G449	7815.0	166.0
548	G451	7800.0	291.0
549	G453	7785.0	166.0
550	G455	7770.0	291.0

(unit: um)

Pad No.	Pad Name	X	Y
551	G457	7755.0	166.0
552	G459	7740.0	291.0
553	G461	7725.0	166.0
554	G463	7710.0	291.0
555	G465	7695.0	166.0
556	G467	7680.0	291.0
557	G469	7665.0	166.0
558	G471	7650.0	291.0
559	G473	7635.0	166.0
560	G475	7620.0	291.0
561	G477	7605.0	166.0
562	G479	7590.0	291.0
563	TESTO3	7575.0	166.0
564	TESTO4	7560.0	291.0
565	TESTO5	7395.0	166.0
566	TESTO6	7380.0	291.0
567	S960	7365.0	166.0
568	S959	7350.0	291.0
569	S958	7335.0	166.0
570	S957	7320.0	291.0
571	S956	7305.0	166.0
572	S955	7290.0	291.0
573	S954	7275.0	166.0
574	S953	7260.0	291.0
575	S952	7245.0	166.0
576	S951	7230.0	291.0
577	S950	7215.0	166.0
578	S949	7200.0	291.0
579	S948	7185.0	166.0
580	S947	7170.0	291.0
581	S946	7155.0	166.0
582	S945	7140.0	291.0
583	S944	7125.0	166.0
584	S943	7110.0	291.0
585	S942	7095.0	166.0
586	S941	7080.0	291.0
587	S940	7065.0	166.0
588	S939	7050.0	291.0
589	S938	7035.0	166.0
590	S937	7020.0	291.0
591	S936	7005.0	166.0
592	S935	6990.0	291.0
593	S934	6975.0	166.0
594	S933	6960.0	291.0
595	S932	6945.0	166.0
596	S931	6930.0	291.0
597	S930	6915.0	166.0
598	S929	6900.0	291.0
599	S928	6885.0	166.0
600	S927	6870.0	291.0

R61581B0 Pad Coordinates (No.7)

(unit: um)

Pad No.	Pad Name	X	Y
601	S926	6855.0	166.0
602	S925	6840.0	291.0
603	S924	6825.0	166.0
604	S923	6810.0	291.0
605	S922	6795.0	166.0
606	S921	6780.0	291.0
607	S920	6765.0	166.0
608	S919	6750.0	291.0
609	S918	6735.0	166.0
610	S917	6720.0	291.0
611	S916	6705.0	166.0
612	S915	6690.0	291.0
613	S914	6675.0	166.0
614	S913	6660.0	291.0
615	S912	6645.0	166.0
616	S911	6630.0	291.0
617	S910	6615.0	166.0
618	S909	6600.0	291.0
619	S908	6585.0	166.0
620	S907	6570.0	291.0
621	S906	6555.0	166.0
622	S905	6540.0	291.0
623	S904	6525.0	166.0
624	S903	6510.0	291.0
625	S902	6495.0	166.0
626	S901	6480.0	291.0
627	S900	6465.0	166.0
628	S899	6450.0	291.0
629	S898	6435.0	166.0
630	S897	6420.0	291.0
631	S896	6405.0	166.0
632	S895	6390.0	291.0
633	S894	6375.0	166.0
634	S893	6360.0	291.0
635	S892	6345.0	166.0
636	S891	6330.0	291.0
637	S890	6315.0	166.0
638	S889	6300.0	291.0
639	S888	6285.0	166.0
640	S887	6270.0	291.0
641	S886	6255.0	166.0
642	S885	6240.0	291.0
643	S884	6225.0	166.0
644	S883	6210.0	291.0
645	S882	6195.0	166.0
646	S881	6180.0	291.0
647	S880	6165.0	166.0
648	S879	6150.0	291.0
649	S878	6135.0	166.0
650	S877	6120.0	291.0

(unit: um)

Pad No.	Pad Name	X	Y
651	S876	6105.0	166.0
652	S875	6090.0	291.0
653	S874	6075.0	166.0
654	S873	6060.0	291.0
655	S872	6045.0	166.0
656	S871	6030.0	291.0
657	S870	6015.0	166.0
658	S869	6000.0	291.0
659	S868	5985.0	166.0
660	S867	5970.0	291.0
661	S866	5955.0	166.0
662	S865	5940.0	291.0
663	S864	5925.0	166.0
664	S863	5910.0	291.0
665	S862	5895.0	166.0
666	S861	5880.0	291.0
667	S860	5865.0	166.0
668	S859	5850.0	291.0
669	S858	5835.0	166.0
670	S857	5820.0	291.0
671	S856	5805.0	166.0
672	S855	5790.0	291.0
673	S854	5775.0	166.0
674	S853	5760.0	291.0
675	S852	5745.0	166.0
676	S851	5730.0	291.0
677	S850	5715.0	166.0
678	S849	5700.0	291.0
679	S848	5685.0	166.0
680	S847	5670.0	291.0
681	S846	5655.0	166.0
682	S845	5640.0	291.0
683	S844	5625.0	166.0
684	S843	5610.0	291.0
685	S842	5595.0	166.0
686	S841	5580.0	291.0
687	S840	5565.0	166.0
688	S839	5550.0	291.0
689	S838	5535.0	166.0
690	S837	5520.0	291.0
691	S836	5505.0	166.0
692	S835	5490.0	291.0
693	S834	5475.0	166.0
694	S833	5460.0	291.0
695	S832	5445.0	166.0
696	S831	5430.0	291.0
697	S830	5415.0	166.0
698	S829	5400.0	291.0
699	S828	5385.0	166.0
700	S827	5370.0	291.0

R61581B0 Pad Coordinates (No.8)

(unit: um)

Pad No.	Pad Name	X	Y
701	S826	5355.0	166.0
702	S825	5340.0	291.0
703	S824	5325.0	166.0
704	S823	5310.0	291.0
705	S822	5295.0	166.0
706	S821	5280.0	291.0
707	S820	5265.0	166.0
708	S819	5250.0	291.0
709	S818	5235.0	166.0
710	S817	5220.0	291.0
711	S816	5205.0	166.0
712	S815	5190.0	291.0
713	S814	5175.0	166.0
714	S813	5160.0	291.0
715	S812	5145.0	166.0
716	S811	5130.0	291.0
717	S810	5115.0	166.0
718	S809	5100.0	291.0
719	S808	5085.0	166.0
720	S807	5070.0	291.0
721	S806	5055.0	166.0
722	S805	5040.0	291.0
723	S804	5025.0	166.0
724	S803	5010.0	291.0
725	S802	4995.0	166.0
726	S801	4980.0	291.0
727	S800	4965.0	166.0
728	S799	4950.0	291.0
729	S798	4935.0	166.0
730	S797	4920.0	291.0
731	S796	4905.0	166.0
732	S795	4890.0	291.0
733	S794	4875.0	166.0
734	S793	4860.0	291.0
735	S792	4845.0	166.0
736	S791	4830.0	291.0
737	S790	4815.0	166.0
738	S789	4800.0	291.0
739	S788	4785.0	166.0
740	S787	4770.0	291.0
741	S786	4755.0	166.0
742	S785	4740.0	291.0
743	S784	4725.0	166.0
744	S783	4710.0	291.0
745	S782	4695.0	166.0
746	S781	4680.0	291.0
747	S780	4665.0	166.0
748	S779	4650.0	291.0
749	S778	4635.0	166.0
750	S777	4620.0	291.0

(unit: um)

Pad No.	Pad Name	X	Y
751	S776	4605.0	166.0
752	S775	4590.0	291.0
753	S774	4575.0	166.0
754	S773	4560.0	291.0
755	S772	4545.0	166.0
756	S771	4530.0	291.0
757	S770	4515.0	166.0
758	S769	4500.0	291.0
759	S768	4485.0	166.0
760	S767	4470.0	291.0
761	S766	4455.0	166.0
762	S765	4440.0	291.0
763	S764	4425.0	166.0
764	S763	4410.0	291.0
765	S762	4395.0	166.0
766	S761	4380.0	291.0
767	S760	4365.0	166.0
768	S759	4350.0	291.0
769	S758	4335.0	166.0
770	S757	4320.0	291.0
771	S756	4305.0	166.0
772	S755	4290.0	291.0
773	S754	4275.0	166.0
774	S753	4260.0	291.0
775	S752	4245.0	166.0
776	S751	4230.0	291.0
777	S750	4215.0	166.0
778	S749	4200.0	291.0
779	S748	4185.0	166.0
780	S747	4170.0	291.0
781	S746	4155.0	166.0
782	S745	4140.0	291.0
783	S744	4125.0	166.0
784	S743	4110.0	291.0
785	S742	4095.0	166.0
786	S741	4080.0	291.0
787	S740	4065.0	166.0
788	S739	4050.0	291.0
789	S738	4035.0	166.0
790	S737	4020.0	291.0
791	S736	4005.0	166.0
792	S735	3990.0	291.0
793	S734	3975.0	166.0
794	S733	3960.0	291.0
795	S732	3945.0	166.0
796	S731	3930.0	291.0
797	S730	3915.0	166.0
798	S729	3900.0	291.0
799	S728	3885.0	166.0
800	S727	3870.0	291.0

R61581B0 Pad Coordinates (No.9)

(unit: um)

Pad No.	Pad Name	X	Y
801	S726	3855.0	166.0
802	S725	3840.0	291.0
803	S724	3825.0	166.0
804	S723	3810.0	291.0
805	S722	3795.0	166.0
806	S721	3780.0	291.0
807	S720	3765.0	166.0
808	S719	3750.0	291.0
809	S718	3735.0	166.0
810	S717	3720.0	291.0
811	S716	3705.0	166.0
812	S715	3690.0	291.0
813	S714	3675.0	166.0
814	S713	3660.0	291.0
815	S712	3645.0	166.0
816	S711	3630.0	291.0
817	S710	3615.0	166.0
818	S709	3600.0	291.0
819	S708	3585.0	166.0
820	S707	3570.0	291.0
821	S706	3555.0	166.0
822	S705	3540.0	291.0
823	S704	3525.0	166.0
824	S703	3510.0	291.0
825	S702	3495.0	166.0
826	S701	3480.0	291.0
827	S700	3465.0	166.0
828	S699	3450.0	291.0
829	S698	3435.0	166.0
830	S697	3420.0	291.0
831	S696	3405.0	166.0
832	S695	3390.0	291.0
833	S694	3375.0	166.0
834	S693	3360.0	291.0
835	S692	3345.0	166.0
836	S691	3330.0	291.0
837	S690	3315.0	166.0
838	S689	3300.0	291.0
839	S688	3285.0	166.0
840	S687	3270.0	291.0
841	S686	3255.0	166.0
842	S685	3240.0	291.0
843	S684	3225.0	166.0
844	S683	3210.0	291.0
845	S682	3195.0	166.0
846	S681	3180.0	291.0
847	S680	3165.0	166.0
848	S679	3150.0	291.0
849	S678	3135.0	166.0
850	S677	3120.0	291.0

(unit: um)

Pad No.	Pad Name	X	Y
851	S676	3105.0	166.0
852	S675	3090.0	291.0
853	S674	3075.0	166.0
854	S673	3060.0	291.0
855	S672	3045.0	166.0
856	S671	3030.0	291.0
857	S670	3015.0	166.0
858	S669	3000.0	291.0
859	S668	2985.0	166.0
860	S667	2970.0	291.0
861	S666	2955.0	166.0
862	S665	2940.0	291.0
863	S664	2925.0	166.0
864	S663	2910.0	291.0
865	S662	2895.0	166.0
866	S661	2880.0	291.0
867	S660	2865.0	166.0
868	S659	2850.0	291.0
869	S658	2835.0	166.0
870	S657	2820.0	291.0
871	S656	2805.0	166.0
872	S655	2790.0	291.0
873	S654	2775.0	166.0
874	S653	2760.0	291.0
875	S652	2745.0	166.0
876	S651	2730.0	291.0
877	S650	2715.0	166.0
878	S649	2700.0	291.0
879	S648	2685.0	166.0
880	S647	2670.0	291.0
881	S646	2655.0	166.0
882	S645	2640.0	291.0
883	S644	2625.0	166.0
884	S643	2610.0	291.0
885	S642	2595.0	166.0
886	S641	2580.0	291.0
887	S640	2565.0	166.0
888	S639	2550.0	291.0
889	S638	2535.0	166.0
890	S637	2520.0	291.0
891	S636	2505.0	166.0
892	S635	2490.0	291.0
893	S634	2475.0	166.0
894	S633	2460.0	291.0
895	S632	2445.0	166.0
896	S631	2430.0	291.0
897	S630	2415.0	166.0
898	S629	2400.0	291.0
899	S628	2385.0	166.0
900	S627	2370.0	291.0

R61581B0 Pad Coordinates (No.10)

(unit: um)

Pad No.	Pad Name	X	Y
901	S626	2355.0	166.0
902	S625	2340.0	291.0
903	S624	2325.0	166.0
904	S623	2310.0	291.0
905	S622	2295.0	166.0
906	S621	2280.0	291.0
907	S620	2265.0	166.0
908	S619	2250.0	291.0
909	S618	2235.0	166.0
910	S617	2220.0	291.0
911	S616	2205.0	166.0
912	S615	2190.0	291.0
913	S614	2175.0	166.0
914	S613	2160.0	291.0
915	S612	2145.0	166.0
916	S611	2130.0	291.0
917	S610	2115.0	166.0
918	S609	2100.0	291.0
919	S608	2085.0	166.0
920	S607	2070.0	291.0
921	S606	2055.0	166.0
922	S605	2040.0	291.0
923	S604	2025.0	166.0
924	S603	2010.0	291.0
925	S602	1995.0	166.0
926	S601	1980.0	291.0
927	S600	1965.0	166.0
928	S599	1950.0	291.0
929	S598	1935.0	166.0
930	S597	1920.0	291.0
931	S596	1905.0	166.0
932	S595	1890.0	291.0
933	S594	1875.0	166.0
934	S593	1860.0	291.0
935	S592	1845.0	166.0
936	S591	1830.0	291.0
937	S590	1815.0	166.0
938	S589	1800.0	291.0
939	S588	1785.0	166.0
940	S587	1770.0	291.0
941	S586	1755.0	166.0
942	S585	1740.0	291.0
943	S584	1725.0	166.0
944	S583	1710.0	291.0
945	S582	1695.0	166.0
946	S581	1680.0	291.0
947	S580	1665.0	166.0
948	S579	1650.0	291.0
949	S578	1635.0	166.0
950	S577	1620.0	291.0

(unit: um)

Pad No.	Pad Name	X	Y
951	S576	1605.0	166.0
952	S575	1590.0	291.0
953	S574	1575.0	166.0
954	S573	1560.0	291.0
955	S572	1545.0	166.0
956	S571	1530.0	291.0
957	S570	1515.0	166.0
958	S569	1500.0	291.0
959	S568	1485.0	166.0
960	S567	1470.0	291.0
961	S566	1455.0	166.0
962	S565	1440.0	291.0
963	S564	1425.0	166.0
964	S563	1410.0	291.0
965	S562	1395.0	166.0
966	S561	1380.0	291.0
967	S560	1365.0	166.0
968	S559	1350.0	291.0
969	S558	1335.0	166.0
970	S557	1320.0	291.0
971	S556	1305.0	166.0
972	S555	1290.0	291.0
973	S554	1275.0	166.0
974	S553	1260.0	291.0
975	S552	1245.0	166.0
976	S551	1230.0	291.0
977	S550	1215.0	166.0
978	S549	1200.0	291.0
979	S548	1185.0	166.0
980	S547	1170.0	291.0
981	S546	1155.0	166.0
982	S545	1140.0	291.0
983	S544	1125.0	166.0
984	S543	1110.0	291.0
985	S542	1095.0	166.0
986	S541	1080.0	291.0
987	S540	1065.0	166.0
988	S539	1050.0	291.0
989	S538	1035.0	166.0
990	S537	1020.0	291.0
991	S536	1005.0	166.0
992	S535	990.0	291.0
993	S534	975.0	166.0
994	S533	960.0	291.0
995	S532	945.0	166.0
996	S531	930.0	291.0
997	S530	915.0	166.0
998	S529	900.0	291.0
999	S528	885.0	166.0
1000	S527	870.0	291.0

R61581B0 Pad Coordinates (No.11)

(unit: um)

Pad No.	Pad Name	X	Y
1001	S526	855.0	166.0
1002	S525	840.0	291.0
1003	S524	825.0	166.0
1004	S523	810.0	291.0
1005	S522	795.0	166.0
1006	S521	780.0	291.0
1007	S520	765.0	166.0
1008	S519	750.0	291.0
1009	S518	735.0	166.0
1010	S517	720.0	291.0
1011	S516	705.0	166.0
1012	S515	690.0	291.0
1013	S514	675.0	166.0
1014	S513	660.0	291.0
1015	S512	645.0	166.0
1016	S511	630.0	291.0
1017	S510	615.0	166.0
1018	S509	600.0	291.0
1019	S508	585.0	166.0
1020	S507	570.0	291.0
1021	S506	555.0	166.0
1022	S505	540.0	291.0
1023	S504	525.0	166.0
1024	S503	510.0	291.0
1025	S502	495.0	166.0
1026	S501	480.0	291.0
1027	S500	465.0	166.0
1028	S499	450.0	291.0
1029	S498	435.0	166.0
1030	S497	420.0	291.0
1031	S496	405.0	166.0
1032	S495	390.0	291.0
1033	S494	375.0	166.0
1034	S493	360.0	291.0
1035	S492	345.0	166.0
1036	S491	330.0	291.0
1037	S490	315.0	166.0
1038	S489	300.0	291.0
1039	S488	285.0	166.0
1040	S487	270.0	291.0
1041	S486	255.0	166.0
1042	S485	240.0	291.0
1043	S484	225.0	166.0
1044	S483	210.0	291.0
1045	S482	195.0	166.0
1046	S481	180.0	291.0
1047	TESTO7	165.0	166.0
1048	TESTO8	150.0	291.0
1049	TESTO9	-150.0	291.0
1050	TESTO10	-165.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1051	S480	-180.0	291.0
1052	S479	-195.0	166.0
1053	S478	-210.0	291.0
1054	S477	-225.0	166.0
1055	S476	-240.0	291.0
1056	S475	-255.0	166.0
1057	S474	-270.0	291.0
1058	S473	-285.0	166.0
1059	S472	-300.0	291.0
1060	S471	-315.0	166.0
1061	S470	-330.0	291.0
1062	S469	-345.0	166.0
1063	S468	-360.0	291.0
1064	S467	-375.0	166.0
1065	S466	-390.0	291.0
1066	S465	-405.0	166.0
1067	S464	-420.0	291.0
1068	S463	-435.0	166.0
1069	S462	-450.0	291.0
1070	S461	-465.0	166.0
1071	S460	-480.0	291.0
1072	S459	-495.0	166.0
1073	S458	-510.0	291.0
1074	S457	-525.0	166.0
1075	S456	-540.0	291.0
1076	S455	-555.0	166.0
1077	S454	-570.0	291.0
1078	S453	-585.0	166.0
1079	S452	-600.0	291.0
1080	S451	-615.0	166.0
1081	S450	-630.0	291.0
1082	S449	-645.0	166.0
1083	S448	-660.0	291.0
1084	S447	-675.0	166.0
1085	S446	-690.0	291.0
1086	S445	-705.0	166.0
1087	S444	-720.0	291.0
1088	S443	-735.0	166.0
1089	S442	-750.0	291.0
1090	S441	-765.0	166.0
1091	S440	-780.0	291.0
1092	S439	-795.0	166.0
1093	S438	-810.0	291.0
1094	S437	-825.0	166.0
1095	S436	-840.0	291.0
1096	S435	-855.0	166.0
1097	S434	-870.0	291.0
1098	S433	-885.0	166.0
1099	S432	-900.0	291.0
1100	S431	-915.0	166.0

R61581B0 Pad Coordinates (No.12)

(unit: um)

Pad No.	Pad Name	X	Y
1101	S430	-930.0	291.0
1102	S429	-945.0	166.0
1103	S428	-960.0	291.0
1104	S427	-975.0	166.0
1105	S426	-990.0	291.0
1106	S425	-1005.0	166.0
1107	S424	-1020.0	291.0
1108	S423	-1035.0	166.0
1109	S422	-1050.0	291.0
1110	S421	-1065.0	166.0
1111	S420	-1080.0	291.0
1112	S419	-1095.0	166.0
1113	S418	-1110.0	291.0
1114	S417	-1125.0	166.0
1115	S416	-1140.0	291.0
1116	S415	-1155.0	166.0
1117	S414	-1170.0	291.0
1118	S413	-1185.0	166.0
1119	S412	-1200.0	291.0
1120	S411	-1215.0	166.0
1121	S410	-1230.0	291.0
1122	S409	-1245.0	166.0
1123	S408	-1260.0	291.0
1124	S407	-1275.0	166.0
1125	S406	-1290.0	291.0
1126	S405	-1305.0	166.0
1127	S404	-1320.0	291.0
1128	S403	-1335.0	166.0
1129	S402	-1350.0	291.0
1130	S401	-1365.0	166.0
1131	S400	-1380.0	291.0
1132	S399	-1395.0	166.0
1133	S398	-1410.0	291.0
1134	S397	-1425.0	166.0
1135	S396	-1440.0	291.0
1136	S395	-1455.0	166.0
1137	S394	-1470.0	291.0
1138	S393	-1485.0	166.0
1139	S392	-1500.0	291.0
1140	S391	-1515.0	166.0
1141	S390	-1530.0	291.0
1142	S389	-1545.0	166.0
1143	S388	-1560.0	291.0
1144	S387	-1575.0	166.0
1145	S386	-1590.0	291.0
1146	S385	-1605.0	166.0
1147	S384	-1620.0	291.0
1148	S383	-1635.0	166.0
1149	S382	-1650.0	291.0
1150	S381	-1665.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1151	S380	-1680.0	291.0
1152	S379	-1695.0	166.0
1153	S378	-1710.0	291.0
1154	S377	-1725.0	166.0
1155	S376	-1740.0	291.0
1156	S375	-1755.0	166.0
1157	S374	-1770.0	291.0
1158	S373	-1785.0	166.0
1159	S372	-1800.0	291.0
1160	S371	-1815.0	166.0
1161	S370	-1830.0	291.0
1162	S369	-1845.0	166.0
1163	S368	-1860.0	291.0
1164	S367	-1875.0	166.0
1165	S366	-1890.0	291.0
1166	S365	-1905.0	166.0
1167	S364	-1920.0	291.0
1168	S363	-1935.0	166.0
1169	S362	-1950.0	291.0
1170	S361	-1965.0	166.0
1171	S360	-1980.0	291.0
1172	S359	-1995.0	166.0
1173	S358	-2010.0	291.0
1174	S357	-2025.0	166.0
1175	S356	-2040.0	291.0
1176	S355	-2055.0	166.0
1177	S354	-2070.0	291.0
1178	S353	-2085.0	166.0
1179	S352	-2100.0	291.0
1180	S351	-2115.0	166.0
1181	S350	-2130.0	291.0
1182	S349	-2145.0	166.0
1183	S348	-2160.0	291.0
1184	S347	-2175.0	166.0
1185	S346	-2190.0	291.0
1186	S345	-2205.0	166.0
1187	S344	-2220.0	291.0
1188	S343	-2235.0	166.0
1189	S342	-2250.0	291.0
1190	S341	-2265.0	166.0
1191	S340	-2280.0	291.0
1192	S339	-2295.0	166.0
1193	S338	-2310.0	291.0
1194	S337	-2325.0	166.0
1195	S336	-2340.0	291.0
1196	S335	-2355.0	166.0
1197	S334	-2370.0	291.0
1198	S333	-2385.0	166.0
1199	S332	-2400.0	291.0
1200	S331	-2415.0	166.0

R61581B0 Pad Coordinates (No.13)

(unit: um)

Pad No.	Pad Name	X	Y
1201	S330	-2430.0	291.0
1202	S329	-2445.0	166.0
1203	S328	-2460.0	291.0
1204	S327	-2475.0	166.0
1205	S326	-2490.0	291.0
1206	S325	-2505.0	166.0
1207	S324	-2520.0	291.0
1208	S323	-2535.0	166.0
1209	S322	-2550.0	291.0
1210	S321	-2565.0	166.0
1211	S320	-2580.0	291.0
1212	S319	-2595.0	166.0
1213	S318	-2610.0	291.0
1214	S317	-2625.0	166.0
1215	S316	-2640.0	291.0
1216	S315	-2655.0	166.0
1217	S314	-2670.0	291.0
1218	S313	-2685.0	166.0
1219	S312	-2700.0	291.0
1220	S311	-2715.0	166.0
1221	S310	-2730.0	291.0
1222	S309	-2745.0	166.0
1223	S308	-2760.0	291.0
1224	S307	-2775.0	166.0
1225	S306	-2790.0	291.0
1226	S305	-2805.0	166.0
1227	S304	-2820.0	291.0
1228	S303	-2835.0	166.0
1229	S302	-2850.0	291.0
1230	S301	-2865.0	166.0
1231	S300	-2880.0	291.0
1232	S299	-2895.0	166.0
1233	S298	-2910.0	291.0
1234	S297	-2925.0	166.0
1235	S296	-2940.0	291.0
1236	S295	-2955.0	166.0
1237	S294	-2970.0	291.0
1238	S293	-2985.0	166.0
1239	S292	-3000.0	291.0
1240	S291	-3015.0	166.0
1241	S290	-3030.0	291.0
1242	S289	-3045.0	166.0
1243	S288	-3060.0	291.0
1244	S287	-3075.0	166.0
1245	S286	-3090.0	291.0
1246	S285	-3105.0	166.0
1247	S284	-3120.0	291.0
1248	S283	-3135.0	166.0
1249	S282	-3150.0	291.0
1250	S281	-3165.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1251	S280	-3180.0	291.0
1252	S279	-3195.0	166.0
1253	S278	-3210.0	291.0
1254	S277	-3225.0	166.0
1255	S276	-3240.0	291.0
1256	S275	-3255.0	166.0
1257	S274	-3270.0	291.0
1258	S273	-3285.0	166.0
1259	S272	-3300.0	291.0
1260	S271	-3315.0	166.0
1261	S270	-3330.0	291.0
1262	S269	-3345.0	166.0
1263	S268	-3360.0	291.0
1264	S267	-3375.0	166.0
1265	S266	-3390.0	291.0
1266	S265	-3405.0	166.0
1267	S264	-3420.0	291.0
1268	S263	-3435.0	166.0
1269	S262	-3450.0	291.0
1270	S261	-3465.0	166.0
1271	S260	-3480.0	291.0
1272	S259	-3495.0	166.0
1273	S258	-3510.0	291.0
1274	S257	-3525.0	166.0
1275	S256	-3540.0	291.0
1276	S255	-3555.0	166.0
1277	S254	-3570.0	291.0
1278	S253	-3585.0	166.0
1279	S252	-3600.0	291.0
1280	S251	-3615.0	166.0
1281	S250	-3630.0	291.0
1282	S249	-3645.0	166.0
1283	S248	-3660.0	291.0
1284	S247	-3675.0	166.0
1285	S246	-3690.0	291.0
1286	S245	-3705.0	166.0
1287	S244	-3720.0	291.0
1288	S243	-3735.0	166.0
1289	S242	-3750.0	291.0
1290	S241	-3765.0	166.0
1291	S240	-3780.0	291.0
1292	S239	-3795.0	166.0
1293	S238	-3810.0	291.0
1294	S237	-3825.0	166.0
1295	S236	-3840.0	291.0
1296	S235	-3855.0	166.0
1297	S234	-3870.0	291.0
1298	S233	-3885.0	166.0
1299	S232	-3900.0	291.0
1300	S231	-3915.0	166.0

R61581B0 Pad Coordinates (No.14)

(unit: um)

Pad No.	Pad Name	X	Y
1301	S230	-3930.0	291.0
1302	S229	-3945.0	166.0
1303	S228	-3960.0	291.0
1304	S227	-3975.0	166.0
1305	S226	-3990.0	291.0
1306	S225	-4005.0	166.0
1307	S224	-4020.0	291.0
1308	S223	-4035.0	166.0
1309	S222	-4050.0	291.0
1310	S221	-4065.0	166.0
1311	S220	-4080.0	291.0
1312	S219	-4095.0	166.0
1313	S218	-4110.0	291.0
1314	S217	-4125.0	166.0
1315	S216	-4140.0	291.0
1316	S215	-4155.0	166.0
1317	S214	-4170.0	291.0
1318	S213	-4185.0	166.0
1319	S212	-4200.0	291.0
1320	S211	-4215.0	166.0
1321	S210	-4230.0	291.0
1322	S209	-4245.0	166.0
1323	S208	-4260.0	291.0
1324	S207	-4275.0	166.0
1325	S206	-4290.0	291.0
1326	S205	-4305.0	166.0
1327	S204	-4320.0	291.0
1328	S203	-4335.0	166.0
1329	S202	-4350.0	291.0
1330	S201	-4365.0	166.0
1331	S200	-4380.0	291.0
1332	S199	-4395.0	166.0
1333	S198	-4410.0	291.0
1334	S197	-4425.0	166.0
1335	S196	-4440.0	291.0
1336	S195	-4455.0	166.0
1337	S194	-4470.0	291.0
1338	S193	-4485.0	166.0
1339	S192	-4500.0	291.0
1340	S191	-4515.0	166.0
1341	S190	-4530.0	291.0
1342	S189	-4545.0	166.0
1343	S188	-4560.0	291.0
1344	S187	-4575.0	166.0
1345	S186	-4590.0	291.0
1346	S185	-4605.0	166.0
1347	S184	-4620.0	291.0
1348	S183	-4635.0	166.0
1349	S182	-4650.0	291.0
1350	S181	-4665.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1351	S180	-4680.0	291.0
1352	S179	-4695.0	166.0
1353	S178	-4710.0	291.0
1354	S177	-4725.0	166.0
1355	S176	-4740.0	291.0
1356	S175	-4755.0	166.0
1357	S174	-4770.0	291.0
1358	S173	-4785.0	166.0
1359	S172	-4800.0	291.0
1360	S171	-4815.0	166.0
1361	S170	-4830.0	291.0
1362	S169	-4845.0	166.0
1363	S168	-4860.0	291.0
1364	S167	-4875.0	166.0
1365	S166	-4890.0	291.0
1366	S165	-4905.0	166.0
1367	S164	-4920.0	291.0
1368	S163	-4935.0	166.0
1369	S162	-4950.0	291.0
1370	S161	-4965.0	166.0
1371	S160	-4980.0	291.0
1372	S159	-4995.0	166.0
1373	S158	-5010.0	291.0
1374	S157	-5025.0	166.0
1375	S156	-5040.0	291.0
1376	S155	-5055.0	166.0
1377	S154	-5070.0	291.0
1378	S153	-5085.0	166.0
1379	S152	-5100.0	291.0
1380	S151	-5115.0	166.0
1381	S150	-5130.0	291.0
1382	S149	-5145.0	166.0
1383	S148	-5160.0	291.0
1384	S147	-5175.0	166.0
1385	S146	-5190.0	291.0
1386	S145	-5205.0	166.0
1387	S144	-5220.0	291.0
1388	S143	-5235.0	166.0
1389	S142	-5250.0	291.0
1390	S141	-5265.0	166.0
1391	S140	-5280.0	291.0
1392	S139	-5295.0	166.0
1393	S138	-5310.0	291.0
1394	S137	-5325.0	166.0
1395	S136	-5340.0	291.0
1396	S135	-5355.0	166.0
1397	S134	-5370.0	291.0
1398	S133	-5385.0	166.0
1399	S132	-5400.0	291.0
1400	S131	-5415.0	166.0

R61581B0 Pad Coordinates (No.15)

(unit: um)

Pad No.	Pad Name	X	Y
1401	S130	-5430.0	291.0
1402	S129	-5445.0	166.0
1403	S128	-5460.0	291.0
1404	S127	-5475.0	166.0
1405	S126	-5490.0	291.0
1406	S125	-5505.0	166.0
1407	S124	-5520.0	291.0
1408	S123	-5535.0	166.0
1409	S122	-5550.0	291.0
1410	S121	-5565.0	166.0
1411	S120	-5580.0	291.0
1412	S119	-5595.0	166.0
1413	S118	-5610.0	291.0
1414	S117	-5625.0	166.0
1415	S116	-5640.0	291.0
1416	S115	-5655.0	166.0
1417	S114	-5670.0	291.0
1418	S113	-5685.0	166.0
1419	S112	-5700.0	291.0
1420	S111	-5715.0	166.0
1421	S110	-5730.0	291.0
1422	S109	-5745.0	166.0
1423	S108	-5760.0	291.0
1424	S107	-5775.0	166.0
1425	S106	-5790.0	291.0
1426	S105	-5805.0	166.0
1427	S104	-5820.0	291.0
1428	S103	-5835.0	166.0
1429	S102	-5850.0	291.0
1430	S101	-5865.0	166.0
1431	S100	-5880.0	291.0
1432	S99	-5895.0	166.0
1433	S98	-5910.0	291.0
1434	S97	-5925.0	166.0
1435	S96	-5940.0	291.0
1436	S95	-5955.0	166.0
1437	S94	-5970.0	291.0
1438	S93	-5985.0	166.0
1439	S92	-6000.0	291.0
1440	S91	-6015.0	166.0
1441	S90	-6030.0	291.0
1442	S89	-6045.0	166.0
1443	S88	-6060.0	291.0
1444	S87	-6075.0	166.0
1445	S86	-6090.0	291.0
1446	S85	-6105.0	166.0
1447	S84	-6120.0	291.0
1448	S83	-6135.0	166.0
1449	S82	-6150.0	291.0
1450	S81	-6165.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1451	S80	-6180.0	291.0
1452	S79	-6195.0	166.0
1453	S78	-6210.0	291.0
1454	S77	-6225.0	166.0
1455	S76	-6240.0	291.0
1456	S75	-6255.0	166.0
1457	S74	-6270.0	291.0
1458	S73	-6285.0	166.0
1459	S72	-6300.0	291.0
1460	S71	-6315.0	166.0
1461	S70	-6330.0	291.0
1462	S69	-6345.0	166.0
1463	S68	-6360.0	291.0
1464	S67	-6375.0	166.0
1465	S66	-6390.0	291.0
1466	S65	-6405.0	166.0
1467	S64	-6420.0	291.0
1468	S63	-6435.0	166.0
1469	S62	-6450.0	291.0
1470	S61	-6465.0	166.0
1471	S60	-6480.0	291.0
1472	S59	-6495.0	166.0
1473	S58	-6510.0	291.0
1474	S57	-6525.0	166.0
1475	S56	-6540.0	291.0
1476	S55	-6555.0	166.0
1477	S54	-6570.0	291.0
1478	S53	-6585.0	166.0
1479	S52	-6600.0	291.0
1480	S51	-6615.0	166.0
1481	S50	-6630.0	291.0
1482	S49	-6645.0	166.0
1483	S48	-6660.0	291.0
1484	S47	-6675.0	166.0
1485	S46	-6690.0	291.0
1486	S45	-6705.0	166.0
1487	S44	-6720.0	291.0
1488	S43	-6735.0	166.0
1489	S42	-6750.0	291.0
1490	S41	-6765.0	166.0
1491	S40	-6780.0	291.0
1492	S39	-6795.0	166.0
1493	S38	-6810.0	291.0
1494	S37	-6825.0	166.0
1495	S36	-6840.0	291.0
1496	S35	-6855.0	166.0
1497	S34	-6870.0	291.0
1498	S33	-6885.0	166.0
1499	S32	-6900.0	291.0
1500	S31	-6915.0	166.0

R61581B0 Pad Coordinates (No.16)

(unit: um)

Pad No.	Pad Name	X	Y
1501	S30	-6930.0	291.0
1502	S29	-6945.0	166.0
1503	S28	-6960.0	291.0
1504	S27	-6975.0	166.0
1505	S26	-6990.0	291.0
1506	S25	-7005.0	166.0
1507	S24	-7020.0	291.0
1508	S23	-7035.0	166.0
1509	S22	-7050.0	291.0
1510	S21	-7065.0	166.0
1511	S20	-7080.0	291.0
1512	S19	-7095.0	166.0
1513	S18	-7110.0	291.0
1514	S17	-7125.0	166.0
1515	S16	-7140.0	291.0
1516	S15	-7155.0	166.0
1517	S14	-7170.0	291.0
1518	S13	-7185.0	166.0
1519	S12	-7200.0	291.0
1520	S11	-7215.0	166.0
1521	S10	-7230.0	291.0
1522	S9	-7245.0	166.0
1523	S8	-7260.0	291.0
1524	S7	-7275.0	166.0
1525	S6	-7290.0	291.0
1526	S5	-7305.0	166.0
1527	S4	-7320.0	291.0
1528	S3	-7335.0	166.0
1529	S2	-7350.0	291.0
1530	S1	-7365.0	166.0
1531	TESTO11	-7380.0	291.0
1532	TESTO12	-7395.0	166.0
1533	TESTO13	-7560.0	291.0
1534	TESTO14	-7575.0	166.0
1535	G480	-7590.0	291.0
1536	G478	-7605.0	166.0
1537	G476	-7620.0	291.0
1538	G474	-7635.0	166.0
1539	G472	-7650.0	291.0
1540	G470	-7665.0	166.0
1541	G468	-7680.0	291.0
1542	G466	-7695.0	166.0
1543	G464	-7710.0	291.0
1544	G462	-7725.0	166.0
1545	G460	-7740.0	291.0
1546	G458	-7755.0	166.0
1547	G456	-7770.0	291.0
1548	G454	-7785.0	166.0
1549	G452	-7800.0	291.0
1550	G450	-7815.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1551	G448	-7830.0	291.0
1552	G446	-7845.0	166.0
1553	G444	-7860.0	291.0
1554	G442	-7875.0	166.0
1555	G440	-7890.0	291.0
1556	G438	-7905.0	166.0
1557	G436	-7920.0	291.0
1558	G434	-7935.0	166.0
1559	G432	-7950.0	291.0
1560	G430	-7965.0	166.0
1561	G428	-7980.0	291.0
1562	G426	-7995.0	166.0
1563	G424	-8010.0	291.0
1564	G422	-8025.0	166.0
1565	G420	-8040.0	291.0
1566	G418	-8055.0	166.0
1567	G416	-8070.0	291.0
1568	G414	-8085.0	166.0
1569	G412	-8100.0	291.0
1570	G410	-8115.0	166.0
1571	G408	-8130.0	291.0
1572	G406	-8145.0	166.0
1573	G404	-8160.0	291.0
1574	G402	-8175.0	166.0
1575	G400	-8190.0	291.0
1576	G398	-8205.0	166.0
1577	G396	-8220.0	291.0
1578	G394	-8235.0	166.0
1579	G392	-8250.0	291.0
1580	G390	-8265.0	166.0
1581	G388	-8280.0	291.0
1582	G386	-8295.0	166.0
1583	G384	-8310.0	291.0
1584	G382	-8325.0	166.0
1585	G380	-8340.0	291.0
1586	G378	-8355.0	166.0
1587	G376	-8370.0	291.0
1588	G374	-8385.0	166.0
1589	G372	-8400.0	291.0
1590	G370	-8415.0	166.0
1591	G368	-8430.0	291.0
1592	G366	-8445.0	166.0
1593	G364	-8460.0	291.0
1594	G362	-8475.0	166.0
1595	G360	-8490.0	291.0
1596	G358	-8505.0	166.0
1597	G356	-8520.0	291.0
1598	G354	-8535.0	166.0
1599	G352	-8550.0	291.0
1600	G350	-8565.0	166.0

R61581B0 Pad Coordinates (No.17)

(unit: um)

Pad No.	Pad Name	X	Y
1601	G348	-8580.0	291.0
1602	G346	-8595.0	166.0
1603	G344	-8610.0	291.0
1604	G342	-8625.0	166.0
1605	G340	-8640.0	291.0
1606	G338	-8655.0	166.0
1607	G336	-8670.0	291.0
1608	G334	-8685.0	166.0
1609	G332	-8700.0	291.0
1610	G330	-8715.0	166.0
1611	G328	-8730.0	291.0
1612	G326	-8745.0	166.0
1613	G324	-8760.0	291.0
1614	G322	-8775.0	166.0
1615	G320	-8790.0	291.0
1616	G318	-8805.0	166.0
1617	G316	-8820.0	291.0
1618	G314	-8835.0	166.0
1619	G312	-8850.0	291.0
1620	G310	-8865.0	166.0
1621	G308	-8880.0	291.0
1622	G306	-8895.0	166.0
1623	G304	-8910.0	291.0
1624	G302	-8925.0	166.0
1625	G300	-8940.0	291.0
1626	G298	-8955.0	166.0
1627	G296	-8970.0	291.0
1628	G294	-8985.0	166.0
1629	G292	-9000.0	291.0
1630	G290	-9015.0	166.0
1631	G288	-9030.0	291.0
1632	G286	-9045.0	166.0
1633	G284	-9060.0	291.0
1634	G282	-9075.0	166.0
1635	G280	-9090.0	291.0
1636	G278	-9105.0	166.0
1637	G276	-9120.0	291.0
1638	G274	-9135.0	166.0
1639	G272	-9150.0	291.0
1640	G270	-9165.0	166.0
1641	G268	-9180.0	291.0
1642	G266	-9195.0	166.0
1643	G264	-9210.0	291.0
1644	G262	-9225.0	166.0
1645	G260	-9240.0	291.0
1646	G258	-9255.0	166.0
1647	G256	-9270.0	291.0
1648	G254	-9285.0	166.0
1649	G252	-9300.0	291.0
1650	G250	-9315.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1651	G248	-9330.0	291.0
1652	G246	-9345.0	166.0
1653	G244	-9360.0	291.0
1654	G242	-9375.0	166.0
1655	G240	-9390.0	291.0
1656	G238	-9405.0	166.0
1657	G236	-9420.0	291.0
1658	G234	-9435.0	166.0
1659	G232	-9450.0	291.0
1660	G230	-9465.0	166.0
1661	G228	-9480.0	291.0
1662	G226	-9495.0	166.0
1663	G224	-9510.0	291.0
1664	G222	-9525.0	166.0
1665	G220	-9540.0	291.0
1666	G218	-9555.0	166.0
1667	G216	-9570.0	291.0
1668	G214	-9585.0	166.0
1669	G212	-9600.0	291.0
1670	G210	-9615.0	166.0
1671	G208	-9630.0	291.0
1672	G206	-9645.0	166.0
1673	G204	-9660.0	291.0
1674	G202	-9675.0	166.0
1675	G200	-9690.0	291.0
1676	G198	-9705.0	166.0
1677	G196	-9720.0	291.0
1678	G194	-9735.0	166.0
1679	G192	-9750.0	291.0
1680	G190	-9765.0	166.0
1681	G188	-9780.0	291.0
1682	G186	-9795.0	166.0
1683	G184	-9810.0	291.0
1684	G182	-9825.0	166.0
1685	G180	-9840.0	291.0
1686	G178	-9855.0	166.0
1687	G176	-9870.0	291.0
1688	G174	-9885.0	166.0
1689	G172	-9900.0	291.0
1690	G170	-9915.0	166.0
1691	G168	-9930.0	291.0
1692	G166	-9945.0	166.0
1693	G164	-9960.0	291.0
1694	G162	-9975.0	166.0
1695	G160	-9990.0	291.0
1696	G158	-10005.0	166.0
1697	G156	-10020.0	291.0
1698	G154	-10035.0	166.0
1699	G152	-10050.0	291.0
1700	G150	-10065.0	166.0

R61581B0 Pad Coordinates (No.18)

(unit: um)

Pad No.	Pad Name	X	Y
1701	G148	-10080.0	291.0
1702	G146	-10095.0	166.0
1703	G144	-10110.0	291.0
1704	G142	-10125.0	166.0
1705	G140	-10140.0	291.0
1706	G138	-10155.0	166.0
1707	G136	-10170.0	291.0
1708	G134	-10185.0	166.0
1709	G132	-10200.0	291.0
1710	G130	-10215.0	166.0
1711	G128	-10230.0	291.0
1712	G126	-10245.0	166.0
1713	G124	-10260.0	291.0
1714	G122	-10275.0	166.0
1715	G120	-10290.0	291.0
1716	G118	-10305.0	166.0
1717	G116	-10320.0	291.0
1718	G114	-10335.0	166.0
1719	G112	-10350.0	291.0
1720	G110	-10365.0	166.0
1721	G108	-10380.0	291.0
1722	G106	-10395.0	166.0
1723	G104	-10410.0	291.0
1724	G102	-10425.0	166.0
1725	G100	-10440.0	291.0
1726	G98	-10455.0	166.0
1727	G96	-10470.0	291.0
1728	G94	-10485.0	166.0
1729	G92	-10500.0	291.0
1730	G90	-10515.0	166.0
1731	G88	-10530.0	291.0
1732	G86	-10545.0	166.0
1733	G84	-10560.0	291.0
1734	G82	-10575.0	166.0
1735	G80	-10590.0	291.0
1736	G78	-10605.0	166.0
1737	G76	-10620.0	291.0
1738	G74	-10635.0	166.0
1739	G72	-10650.0	291.0
1740	G70	-10665.0	166.0
1741	G68	-10680.0	291.0
1742	G66	-10695.0	166.0
1743	G64	-10710.0	291.0
1744	G62	-10725.0	166.0
1745	G60	-10740.0	291.0
1746	G58	-10755.0	166.0
1747	G56	-10770.0	291.0
1748	G54	-10785.0	166.0
1749	G52	-10800.0	291.0
1750	G50	-10815.0	166.0

(unit: um)

Pad No.	Pad Name	X	Y
1751	G48	-10830.0	291.0
1752	G46	-10845.0	166.0
1753	G44	-10860.0	291.0
1754	G42	-10875.0	166.0
1755	G40	-10890.0	291.0
1756	G38	-10905.0	166.0
1757	G36	-10920.0	291.0
1758	G34	-10935.0	166.0
1759	G32	-10950.0	291.0
1760	G30	-10965.0	166.0
1761	G28	-10980.0	291.0
1762	G26	-10995.0	166.0
1763	G24	-11010.0	291.0
1764	G22	-11025.0	166.0
1765	G20	-11040.0	291.0
1766	G18	-11055.0	166.0
1767	G16	-11070.0	291.0
1768	G14	-11085.0	166.0
1769	G12	-11100.0	291.0
1770	G10	-11115.0	166.0
1771	G8	-11130.0	291.0
1772	G6	-11145.0	166.0
1773	G4	-11160.0	291.0
1774	G2	-11175.0	166.0
1775	TESTO15	-11190.0	291.0
1776	TESTO16	-11205.0	166.0

BUMP Arrangement

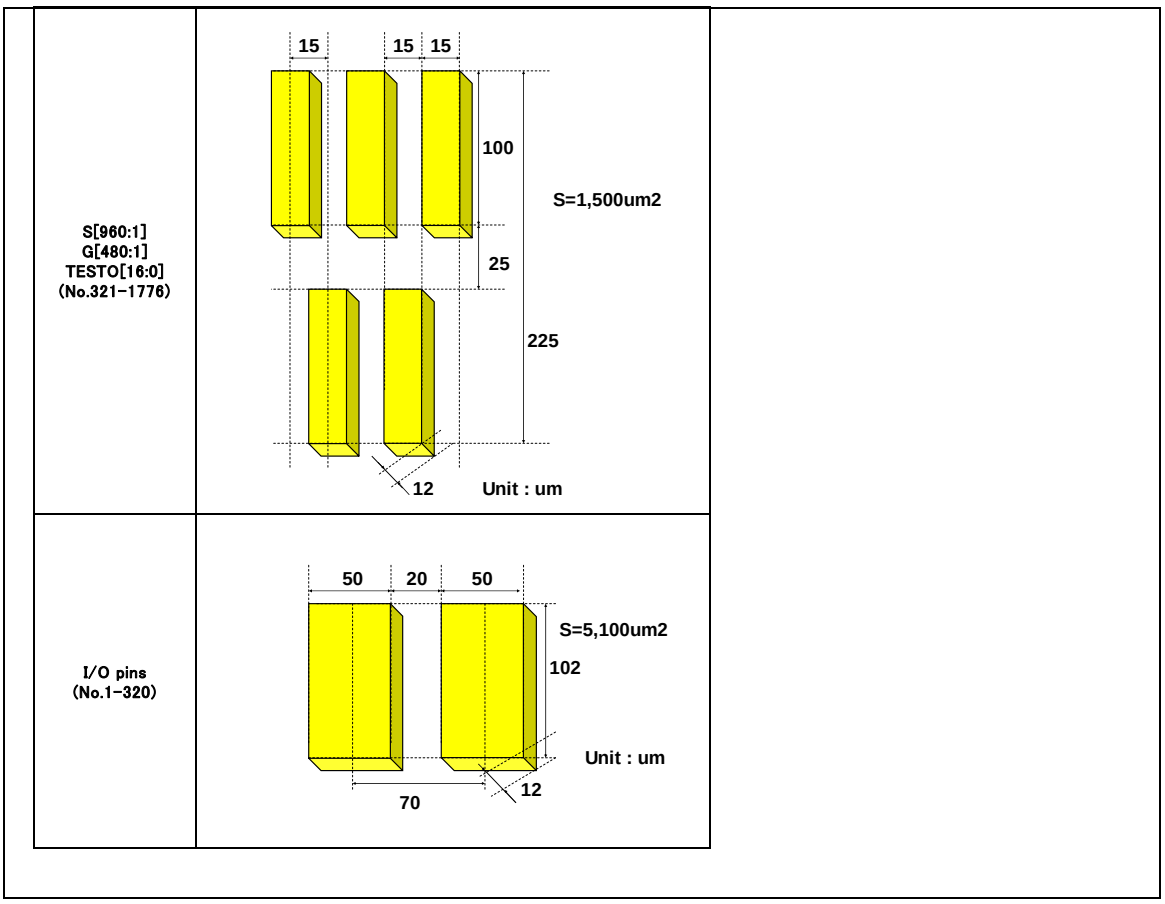


Figure 3

R61581 Recommended Resistance and Wiring Example Rev1.1

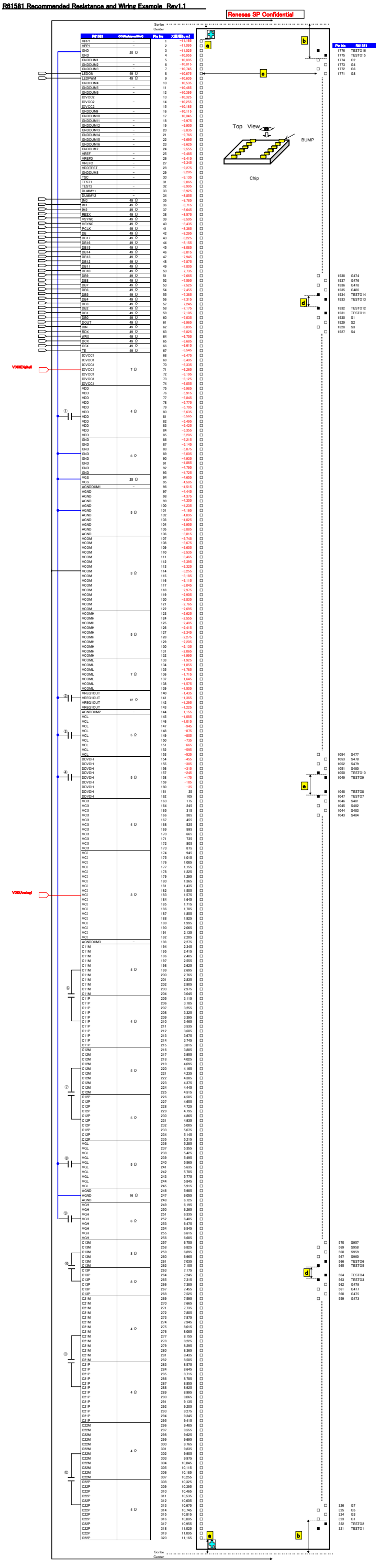
Renesas SP Confidential

RENESAS SP

R61581	COM/Pulldown(MΩ)	Pin No	X座標(um)
VPP1	-	1	-11,165
VPP1	-	2	-11,095
GND	25 Ω	3	-11,025
GND		4	-10,955
GNDDUM1	-	5	-10,885
GNDDUM2	-	6	-10,815
GNDDUM3	-	7	-10,745
LEDON	49 Ω	8	-10,675
LEDPWM	49 Ω	9	-10,605
GNDDUM4	-	10	-10,535
GNDDUM5	-	11	-10,465
GNDDUM6	-	12	-10,395
IOVCC2	-	13	-10,325
IOVCC2		14	-10,255
IOVCC2		15	-10,185
GNDDUM8	-	16	-10,115
GNDDUM10	-	17	-10,045
GNDDUM11	-	18	-9,975
GNDDUM12	-	19	-9,905
GNDDUM13	-	20	-9,835
GNDDUM14	-	21	-9,765
GNDDUM15	-	22	-9,695
GNDDUM16	-	23	-9,625
GNDDUM7	-	24	-9,555
VREF	-	25	-9,485
VREFD	-	26	-9,415
VREFC	-	27	-9,345
VDDTEST	-	28	-9,275
GNDDUM9	-	29	-9,205
TSC	-	30	-9,135
TEST1	-	31	-9,065
TEST2	-	32	-8,995
DUMMY1	-	33	-8,925
DUMMY2	-	34	-8,855
IM0	49 Ω	35	-8,785
IM1	49 Ω	36	-8,715
IM2	49 Ω	37	-8,645
RESX	49 Ω	38	-8,575
VSYNC	49 Ω	39	-8,505
HSYNC	49 Ω	40	-8,435
PCLK	49 Ω	41	-8,365
DE	49 Ω	42	-8,295
DB17	49 Ω	43	-8,225
DB16	49 Ω	44	-8,155
DB15	49 Ω	45	-8,085
DB14	49 Ω	46	-8,015
DB13	49 Ω	47	-7,945
DB12	49 Ω	48	-7,875
DB11	49 Ω	49	-7,805
DB10	49 Ω	50	-7,735
DB9	49 Ω	51	-7,665
DB8	49 Ω	52	-7,595
DB7	49 Ω	53	-7,525
DB6	49 Ω	54	-7,455
DB5	49 Ω	55	-7,385
DB4	49 Ω	56	-7,315
DB3	49 Ω	57	-7,245
DB2	49 Ω	58	-7,175
DB1	49 Ω	59	-7,105
DB0	49 Ω	60	-7,035
DOUT	49 Ω	61	-6,965
DIN	49 Ω	62	-6,895
RDX	49 Ω	63	-6,825
WRX	49 Ω	64	-6,755
DCX	49 Ω	65	-6,685
CSX	49 Ω	66	-6,615
TE	49 Ω	67	-6,545
IOVCC1	7 Ω	68	-6,475
IOVCC1		69	-6,405
IOVCC1		70	-6,335
IOVCC1		71	-6,265
IOVCC1		72	-6,195
IOVCC1		73	-6,125
IOVCC1		74	-6,055
VDD	4 Ω	75	-5,985
VDD		76	-5,915
VDD		77	-5,845
VDD		78	-5,775
VDD		79	-5,705
VDD		80	-5,635
VDD		81	-5,565
VDD		82	-5,495
VDD		83	-5,425
VDD		84	-5,355
VDD		85	-5,285
GND	6 Ω	86	-5,215
GND		87	-5,145
GND		88	-5,075
GND		89	-5,005
GND		90	-4,935
GND		91	-4,865
GND		92	-4,795
GND		93	-4,725
VGS	25 Ω	94	-4,655
VGS		95	-4,585
AGNDDUM1	-	96	-4,515
AGND	5 Ω	97	-4,445
AGND		98	-4,375
AGND		99	-4,305
AGND		100	-4,235
AGND		101	-4,165
AGND		102	-4,095
AGND		103	-4,025
AGND		104	-3,955
AGND		105	-3,885
AGND		106	-3,815
VCOM	3 Ω	107	-3,745
VCOM		108	-3,675
VCOM		109	-3,605
VCOM		110	-3,535
VCOM		111	-3,465
VCOM		112	-3,395
VCOM		113	-3,325
VCOM		114	-3,255
VCOM		115	-3,185
VCOM		116	-3,115
VCOM		117	-3,045
VCOM		118	-2,975
VCOM		119	-2,905
VCOM		120	-2,835
VCOM		121	-2,765
VCOM		122	-2,695
VCOMH	5 Ω	123	-2,625
VCOMH		124	-2,555
VCOMH		125	-2,485
VCOMH		126	-2,415
VCOMH		127	-2,345
VCOMH		128	-2,275
VCOMH		129	-2,205
VCOMH		130	-2,135
VCOMH		131	-2,065
VCOMH		132	-1,995
VCOML	7 Ω	133	-1,925
VCOML		134	-1,855
VCOML		135	-1,785
VCOML		136	-1,715
VCOML		137	-1,645
VCOML		138	-1,575
VCOML		139	-1,505
VREG1OUT	12 Ω	140	-1,435
VREG1OUT		141	-1,365
VREG1OUT		142	-1,295
VREG1OUT		143	-1,225
AGNDDUM2	-	144	-1,155
VCL	5 Ω	145	-1,085
VCL		146	-1,015
VCL		147	-945
VCL		148	-875
VCL		149	-805
VCL		150	-735
VCL		151	-665
VCL		152	-595
VCL		153	-525
DDVDH	5 Ω	154	-455
DDVDH		155	-385
DDVDH		156	-315
DDVDH		157	-245
DDVDH		158	-175
DDVDH		159	-105
DDVDH		160	-35
DDVDH		161	35
DDVDH		162	105
VCI1	4 Ω	163	175
VCI1		164	245
VCI1		165	315
VCI1		166	385
VCI1		167	455
VCI1		168	525
VCI1		169	595
VCI1		170	665
VCI1		171	735
VCI1		172	805
VCI1		173	875
VCI	3 Ω	174	945
VCI		175	1,015
VCI		176	1,085
VCI		177	1,155
VCI		178	1,225
VCI		179	1,295
VCI		180	1,365
VCI		181	1,435
VCI		182	1,505
VCI		183	1,575
VCI		184	1,645
VCI		185	1,715
VCI		186	1,785
VCI		187	1,855
VCI		188	1,925
VCI		189	1,995
VCI		190	2,065
VCI		191	2,135
VCI		192	2,205
AGNDDUM3	-	193	2,275
C11M	4 Ω	194	2,345
C11M		195	2,415
C11M		196	2,485
C11M		197	2,555
C11M		198	2,625
C11M		199	2,695
C11M		200	2,765
C11M		201	2,835
C11M		202	2,905
C11M		203	2,975
C11M		204	3,045
C11P	4 Ω	205	3,115
C11P		206	3,185
C11P		207	3,255
C11P		208	3,325
C11P		209	3,395
C11P		210	3,465
C11P		211	3,535
C11P		212	3,605
C11P		213	3,675
C11P		214	3,745
C11P		215	3,815
C12M	5 Ω	216	3,885
C12M		217	3,955
C12M		218	4,025
C12M		219	4,095
C12M		220	4,165
C12M		221	4,235
C12M		222	4,305
C12M		223	4,375
C12M		224	4,445
C12M		225	4,515
C12P	5 Ω	226	4,585
C12P		227	4,655
C12P		228	4,725
C12P		229	4,795
C12P		230	4,865
C12P		231	4,935
C12P		232	5,005
C12P		233	5,075
C12P		234	5,145
C12P		235	5,215
VGL	5 Ω	236	5,285
VGL		237	5,355
VGL		238	5,425
VGL		239	5,495
VGL		240	5,565
VGL		241	5,635
VGL		242	5,705
VGL		243	5,775
VGL		244	5,845
VGL		245	5,915
AGND	16 Ω	246	5,985
AGND		247	6,055
AGND		248	6,125
VGH	6 Ω	249	6,195
VGH		250	6,265
VGH		251	6,335
VGH		252	6,405
VGH		253	6,475
VGH		254	6,545
VGH		255	6,615
VGH		256	6,685
C13M	8 Ω	257	6,755
C13M		258	6,825
C13M		259	6,895
C13M		260	6,965
C13M		261	7,035
C13M		262	7,105
C13P	8 Ω	263	7,175
C13P		264	7,245
C13P		265	7,315
C13P		266	7,385
C13P		267	7,455
C13P		268	7,525
C21M	4 Ω	269	7,595
C21M		270	7,665
C21M		271	7,735
C21M		272	7,805
C21M		273	7,875
C21M		274	7,945
C21M		275	8,015
C21M		276	8,085
C21M		277	8,155
C21M		278	8,225
C21M		279	8,295
C21M		280	8,365
C21M		281	8,435
C21M		282	8,505
C21P	4 Ω	283	8,575
C21P		284	8,645
C21P		285	8,715
C21P		286	8,785
C21P		287	8,855
C21P		288	8,925
C21P		289	8,995
C21P		290	9,065
C21P		291	9,135
C21P		292	9,205
C21P		293	9,275
C21P		294	9,345
C21P		295	9,415
C22M	4 Ω	296	9,485
C22M		297	9,555
C22M		298	9,625
C22M		299	9,695
C22M		300	9,765
C22M		301	9,835
C22M		302	9,905
C22M		303	9,975
C22M		304	10,045
C22M		305	10,115
C22M		306	10,185
C22M		307	10,255
C22P	4 Ω	308	10,325
C22P		309	10,395
C22P		310	10,465
C22P		311	10,535
C22P		312	10,605
C22P		313	10,675
C22P		314	10,745
C22P		315	10,815
C22P		316	10,885
C22P		317	10,955
C22P		318	11,025
C22P		319	11,095
C22P		320	11,165

VDDIO(Digital)

VDD(Analog)



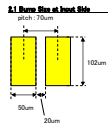
Pin No	R61581
1776	TESTO18
1775	TESTO15
1774	G2
1773	G4
1772	G6
1771	G8
1538	G474
1537	G476
1536	G478
1535	G480
1534	TESTO14
1533	TESTO13
1532	TESTO12
1531	TESTO11
1530	S1
1529	S2
1528	S3
1527	S4
1054	S477
1053	S478
1052	S479
1051	S480
1050	TESTO10
1049	TESTO9
1048	TESTO8
1047	TESTO7
1046	S481
1045	S482
1044	S483
1043	S484
570	S957
569	S958
568	S959
567	S960
566	TESTO6
565	TESTO5
564	TESTO4
563	TESTO3
562	G479
561	G477
560	G475
559	G473
326	G7
325	G5
324	G3
323	G1
322	TESTO2
321	TESTO1

1. Dis Size

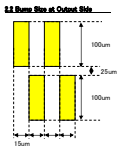
Item	Size(T.B.D.)
Short side(mm)	0.77
Long side(mm)	22.77
Area(mm2)	17.5329
Aspect(long/short side)	29.57

2.1 Bump Size at Input Side

pitch : 70um



2.2 Bump Size at Output Side



2.3 Number of Bump and Bump Area at Input/Output Side

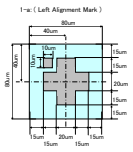
Item	Width(um)	Height(um)	Unit area (μm^2)	n	Sub Total(mm^2)
Input side	50	102	5,100	320	1.63
Output side	15	100	1,500	1,456	2.18
Ratio	-	-	-	-	0.75

2.4 Restriction in Bump Arrangement

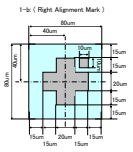
Item	Size(T.B.D.)
a: Chip edge - Active Bump(Input)	195 um
b: Chip edge - Active Bump(output)	202.5 um
c: Input Bump - Output Bump	353 um
d: Gate Bump- Source Bump	165 um
e: Source Bump- Source Bump	315 um

3. Alignment Mark Size

1-a: (Left Alignment Mark)



1-b: (Right Alignment Mark)



4. Number of External Elements

1.) External schottky barrier diode: 0

2.) External capacitor: See below

#	Connection(1 μ F)	Remark
①	VDD - GND	Power supply to logic and RAM
②	VREG1 - GND	
③	VCL - GND	VCL
④	DDVDH - GND	DDVDH
⑤	C11P - C11M	DDVDH step-up
⑦	C12P - C12M	
⑧	VGL - GND	
⑨	VGH - GND	
⑩	C13P - C13M	VGH/VGL step-up
⑪	C21P - C21M	
⑫	C22P - C22M	

Revision Record

Rev.	日付	内容
0.0	09.04.13	First issue
0.1	09.05.14	Error correction
1	09.11.20	
1.1	10.01.15	VCI1,VCOMH,VCOML Capacitor deletion

System Interface Configuration (MIPI DBI)

DBI Type B

Outline

The R61581B0 adopts 18-/16-/9-/8-bit bus display command interface to interface to high-performance host processor. The R61581B0 starts internal processing after storing control information of externally sent 18-/16-/9-/8-bit data in the command register (CDR) and the parameter register (PR). Since the internal operation of the R61581B0 is determined by signals sent from the host processor, command/parameter signal, read/write status signal (RDX/WRX), and internal 18-bit data bus signals (DB[17:0]) are called command.

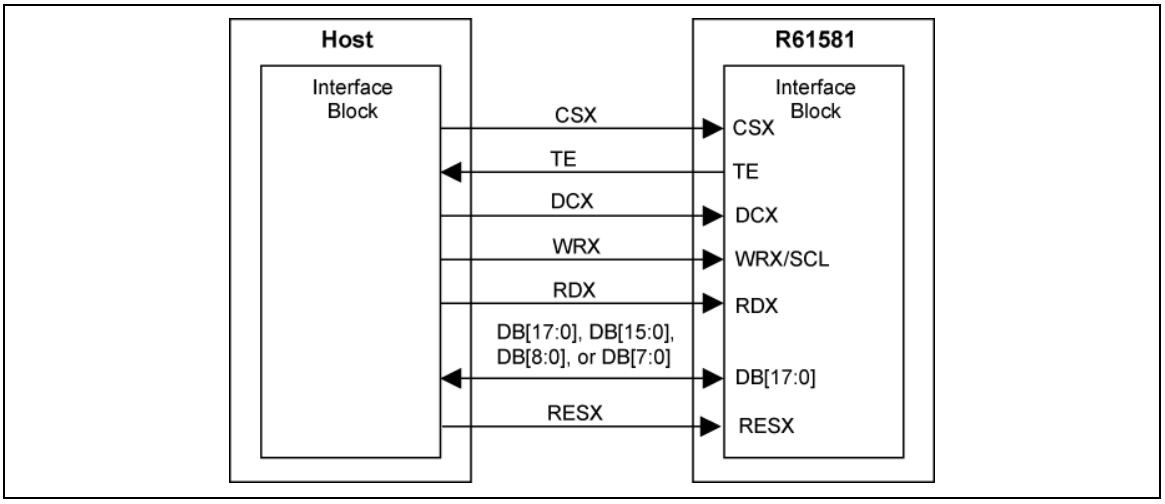


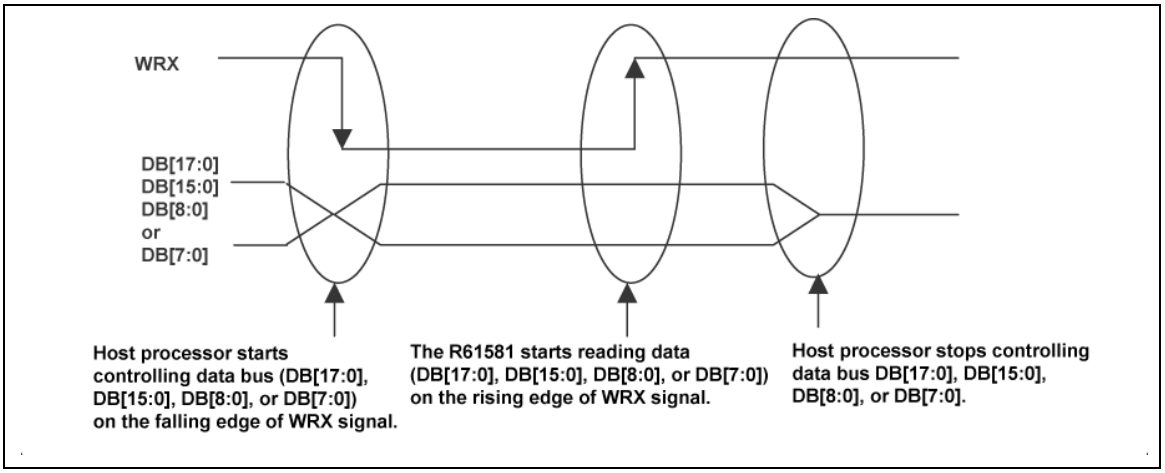
Figure 4 Example: DBI Type B

Write Cycle Sequence

In write cycle, data and/or command are written to the R61581B0 via the interface between the R61581B0 and the host processor. Each step of write cycle sequence (WRX high, WRX low, WRX high) comprises three control signals (DCX, RDX, WRX) and 8(DB[7:0]), 9(DB[8:0]), 16(DB[15:0]), or 18(DB[17:0]) bit data. The DCX bit indicates signal that is used to select command or data sent on the data bus.

When DCX = 1, data on DB[17:0], DB[15:0], DB[8:0] or DB[7:0] is image data or command parameter. When DCX = 0, data on DB[7:0] are command.

Setting RDX and WRX to “Low” simultaneously is prohibited. See the figure below for the write cycle sequence.



Note: WRX is not a synchronous signal (can be halted).

Figure 5 Write Cycle Sequence

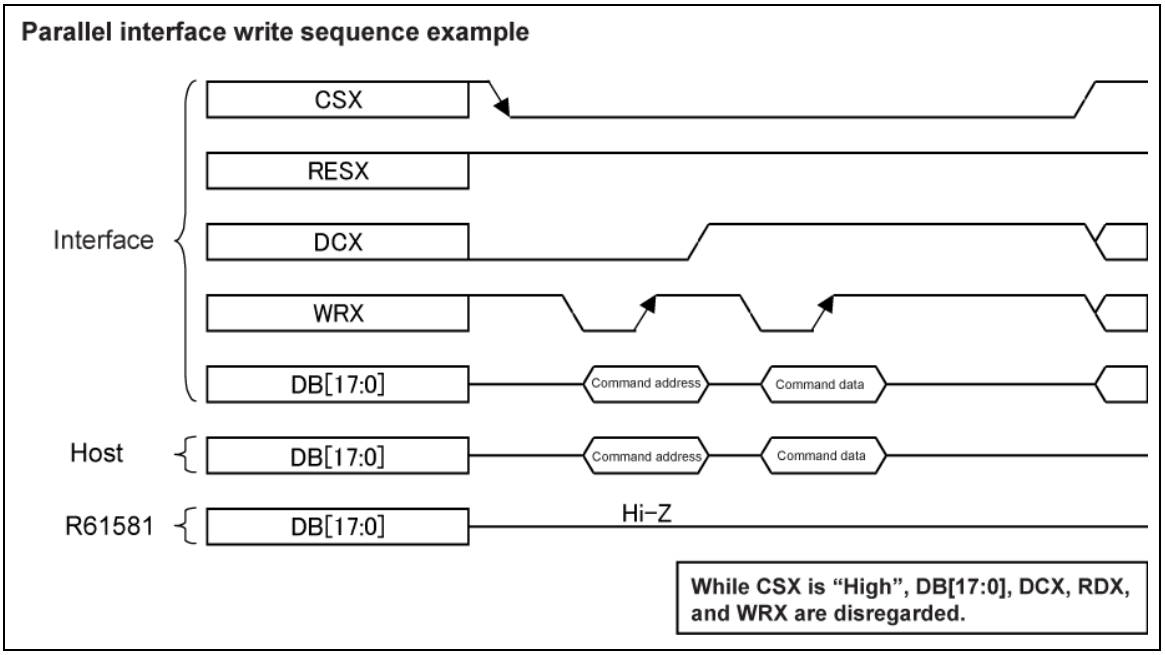
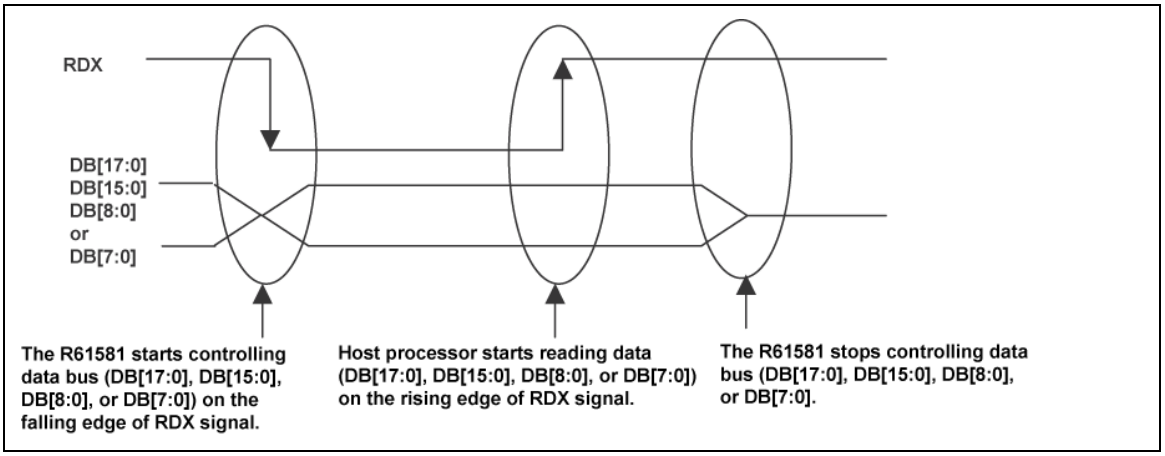


Figure 6

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61581B0 via the interface between the R61581B0 and the host processor. The data (DB[17:0], [15:0], [8:0] or [7:0]) are transmitted from the R61581B0 to the host processor on the falling edge of RDX. The host processor reads the data on the rising edge of RDX. Setting RDX and WRX to "Low" simultaneously is prohibited. See below for the write cycle sequence.



Note: RDX is not a synchronous signal (can be halted).

Figure 7

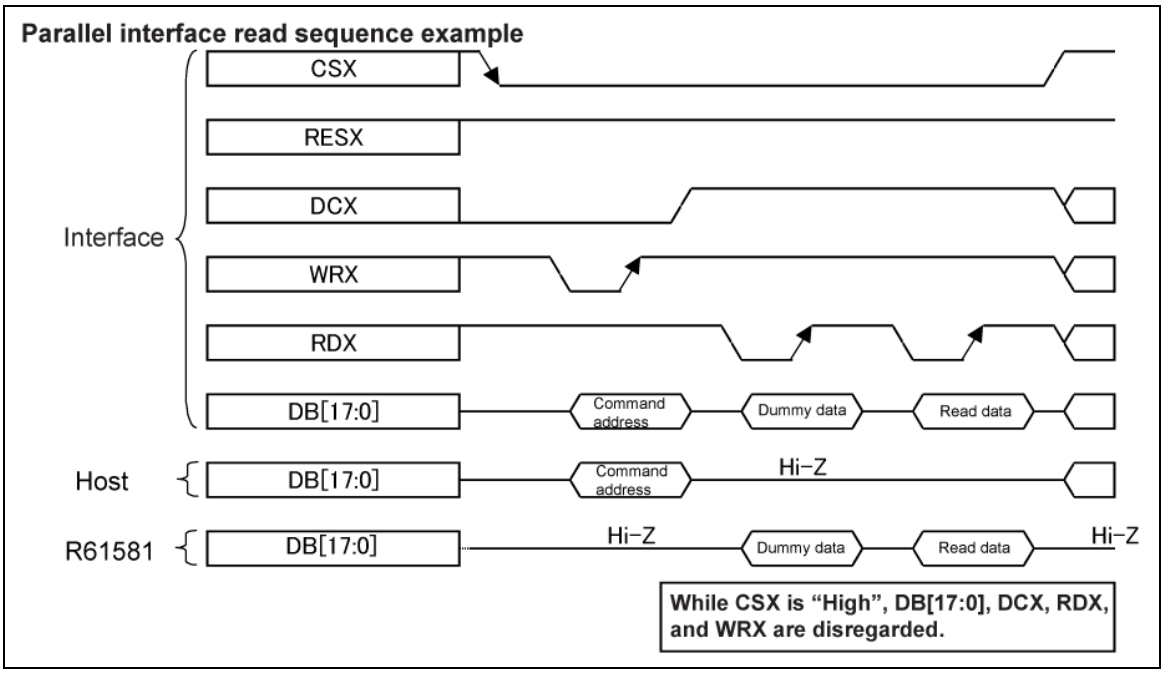


Figure 8

Data Transfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the R61581B0, the command parameters sent to the R61581B0 before the break occurs are stored in the register of the R61581B0 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the R61581B0. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

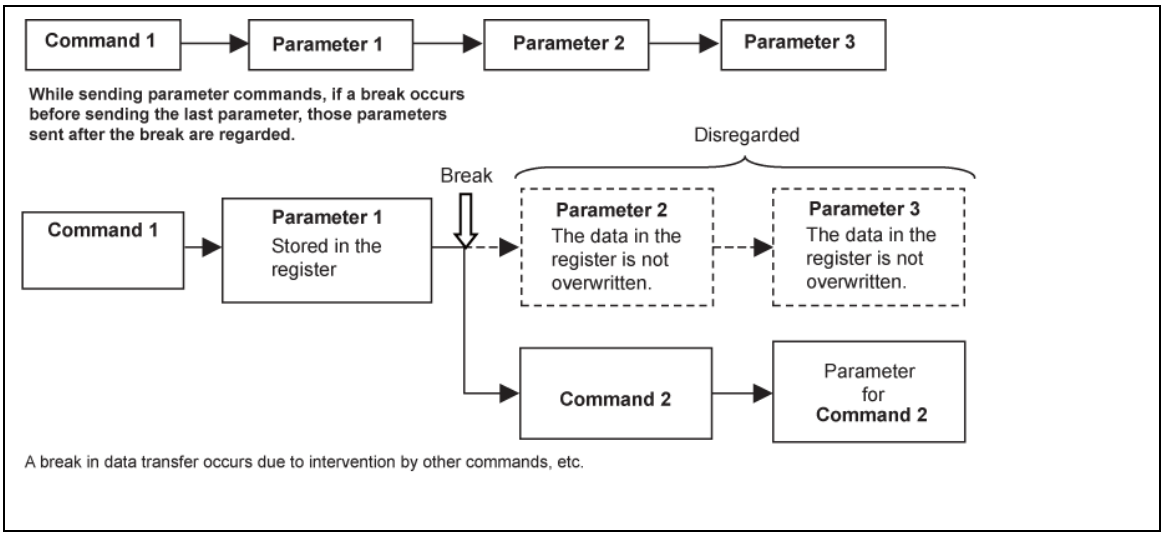


Figure 9

Note: A break is occurred, for example, by other command input.

Data Transfer Pause

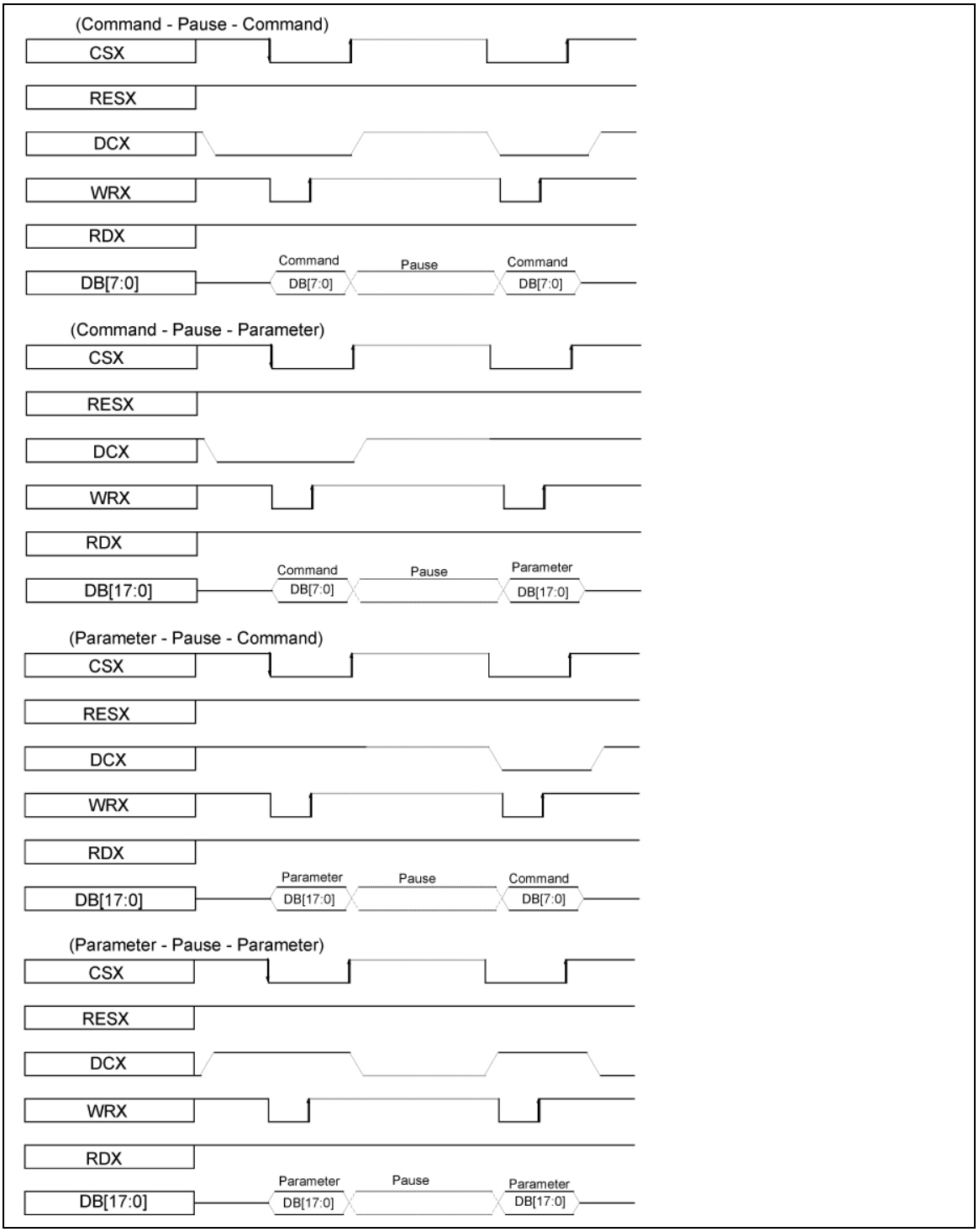


Figure 10

Data Transfer Mode

Two methods are available for writing data to the frame memory in the R61581B0.

(1) Write Method 1 (Default)

One frame of image data is written to the frame memory. The amount of the transmitted data is over 1 frame, the data are disregarded. The write operation of the data to the frame memory is terminated when a command intervenes in the middle of the course. The R61581B0 writes the image data to the next frame when write_memory_start command (2Ch) is written. Set WEMODE =0 (Frame Memory Access and Interface Setting (B3h)).

Start writing data to the frame memory (2Ch)	Image data for Frame 1	Any command	Start writing data to the frame memory (2Ch)	Image data for Frame 2	Any command

……	Any command

Figure 11

(2) Write Method 2

The image data are written consecutively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE =1 (Frame Memory Access and Interface setting (B3h)).

Start			Stop		
Start writing data to the frame memory (2Ch)	Image data for Frame 1	Image data for Frame 2	Image data for Frame 3	……	Any command

Figure 12

Notes: 1. Two write methods are available for all data transfer color modes in 18-/16-/9-/8-bit bus display command interface.

2. The number of pixel in one frame can be odd or even in both download methods. Only complete data sets are retained in the frame memory.

3. The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue (3Ch) is executed, the write operation can be started again from the address where the write operation is halted.

DBI Type C

The R61581B0 supports serial interface DBI Type C (Option 1 and Option 3).

Nine / Eight bit data, transmitted from the R61581B0 to the host processor, is stored in command register (CDR) or parameter register (PR) to start internal operation which is determined by signals from the host processor.

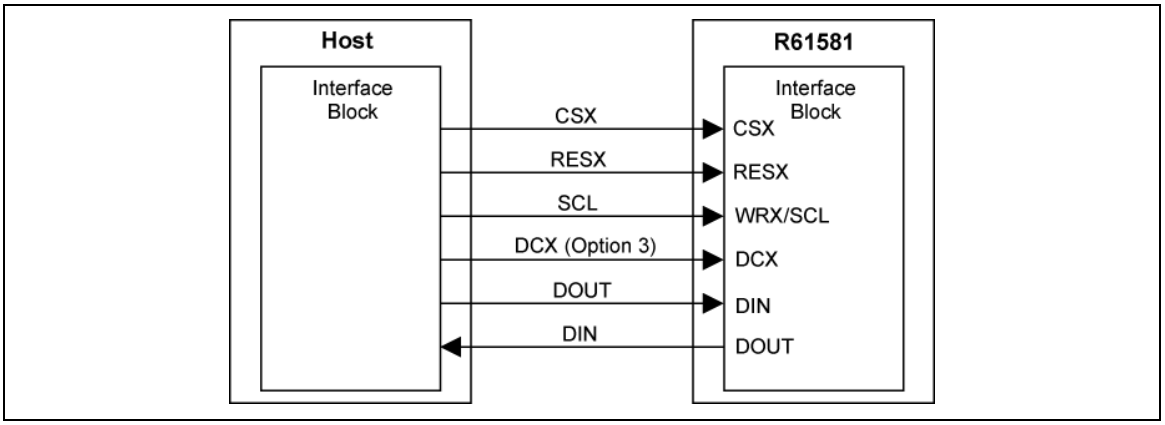
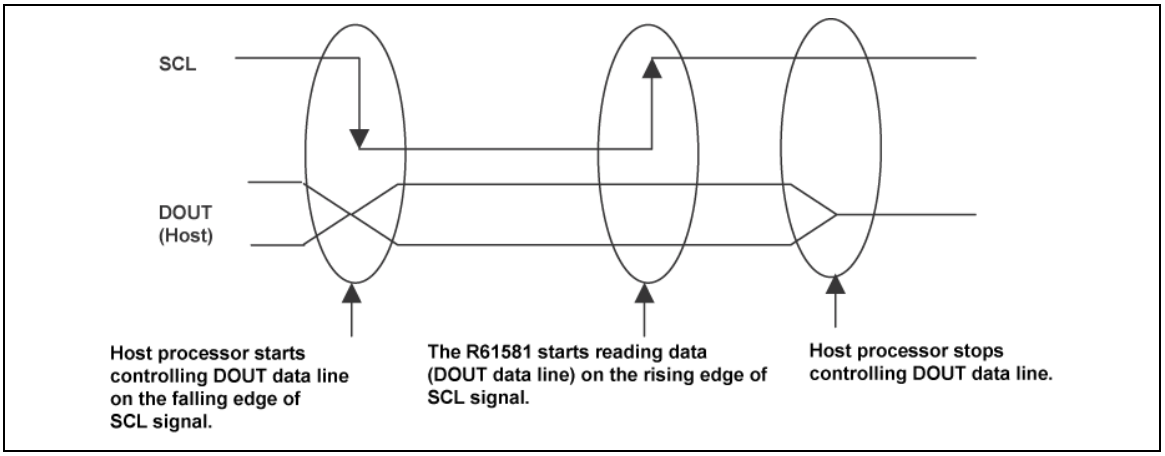


Figure 13 Example: DBI Type C

Write Cycle Sequence

In write cycle, data and/or command are written to the R61581B0 via the interface between the R61581B0 and the host processor. Each step of write cycle sequence (SCL: High, Low, High) has two or three control signals (CSX, SCL, DCX) and data output from DOUT. During Write Cycle Sequence, the host processor outputs data while the R61581B0 accepts data at the rising edge of SCL. If DCX is used in DBI Type C Option 3 operation, data on DOUT are command when DCX = 0. When DCX = 1, data on DOUT are image data or command parameter. See next figure for Write Cycle Sequence.



Note: SCL is not synchronous signal (can be halted).

Figure 14 Type C Write Cycle Sequence

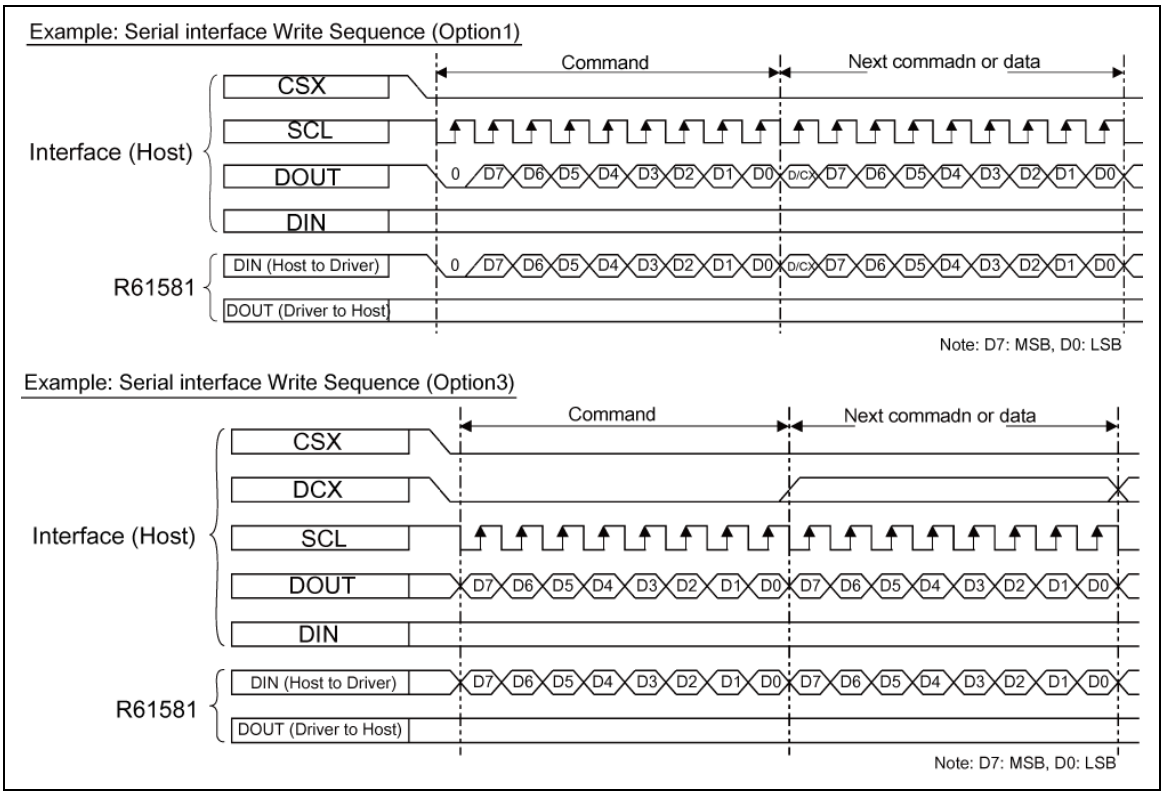
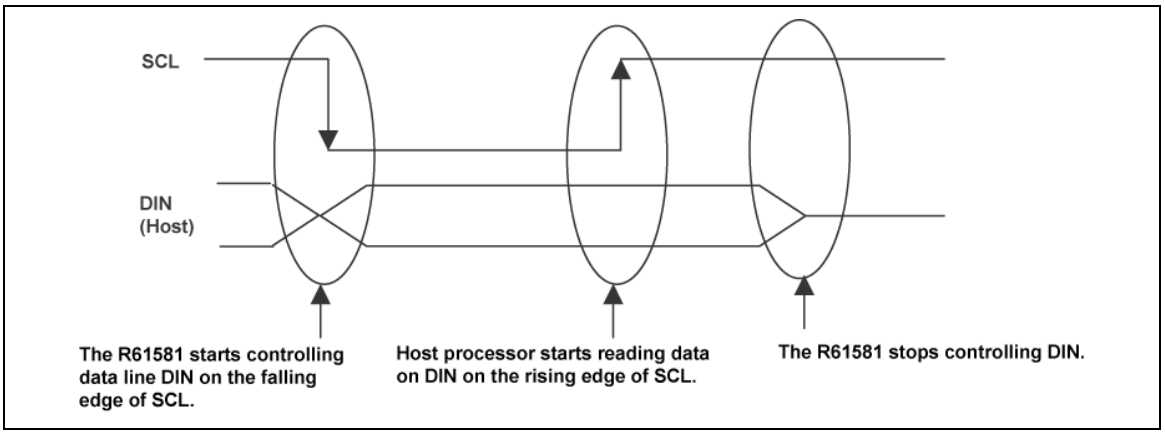


Figure 15 Serial Interface Write Cycle Sequence (Example)

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61581B0 via the interface between the R61581B0 and the host processor. Data are transmitted from the R61581B0 to the host processor via DIN on the falling edge of SCL. The host processor reads the data on the rising edge of SCL. See next figure for the read cycle sequence.



Note: SCL is not synchronous signal (can be halted).

Figure 16 Read Cycle Sequence

Read Command: 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 2Eh, 45h, A1h, BAh, BFh

The 1st byte of read data following a command, irrespective of parameter or frame memory data, is dummy.

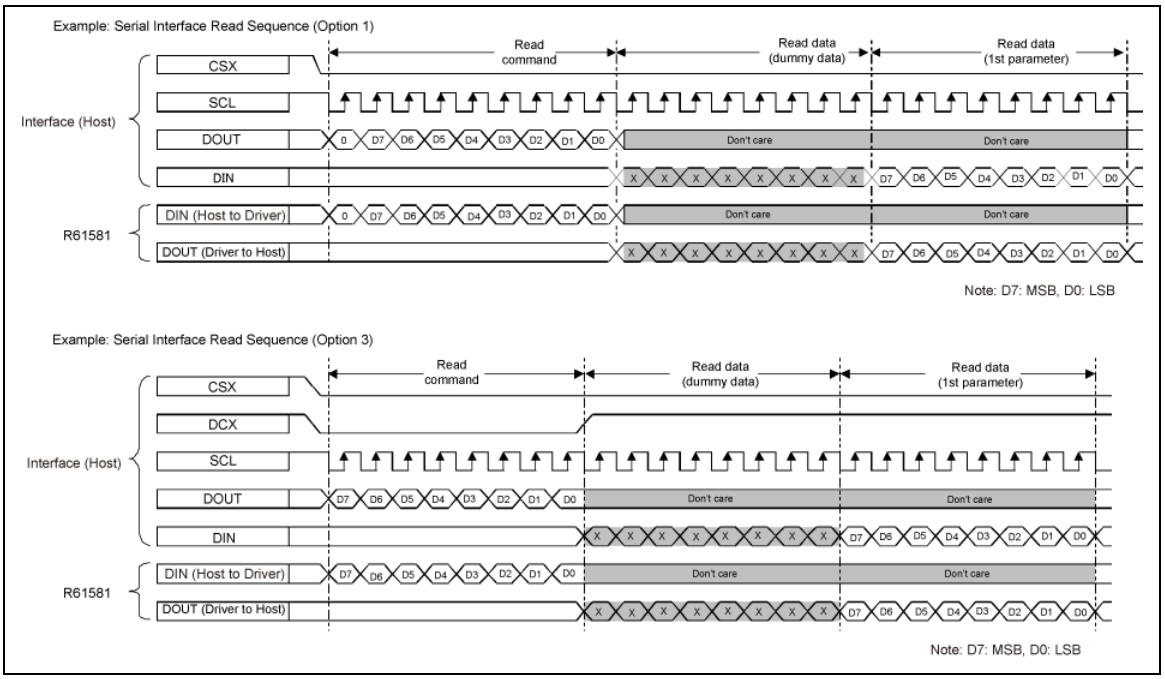


Figure 17 Serial Interface Read Cycle Sequence (Example)

Manufacturer Command Read (Read Mode In Command is Used): B0h, B1h, B3h, B4h, B8h, B9h, BCh, C0h, C1h, C3h, C4h, C8h, D0h, D1h, D2h, D4h, D8h, DAh, E0h, E1h

The 1st byte of read data following Read Mode In command (EFh) is dummy.

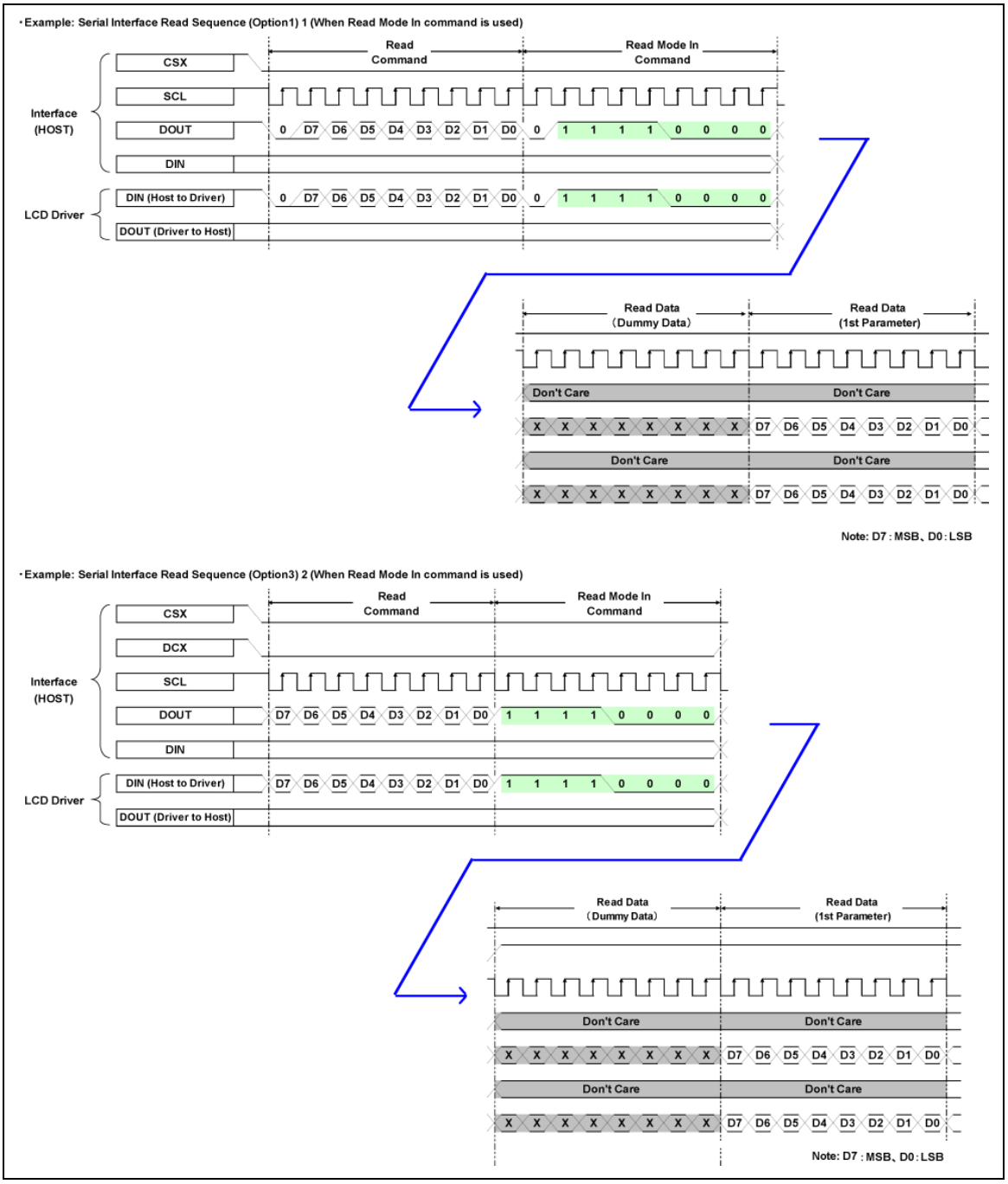


Figure 18 Serial Interface Read Cycle Sequence (Example 2)

Data Transfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the R61581B0, the command parameters sent to the R61581B0 before the break occurs are stored in the register of the R61581B0 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the R61581B0. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

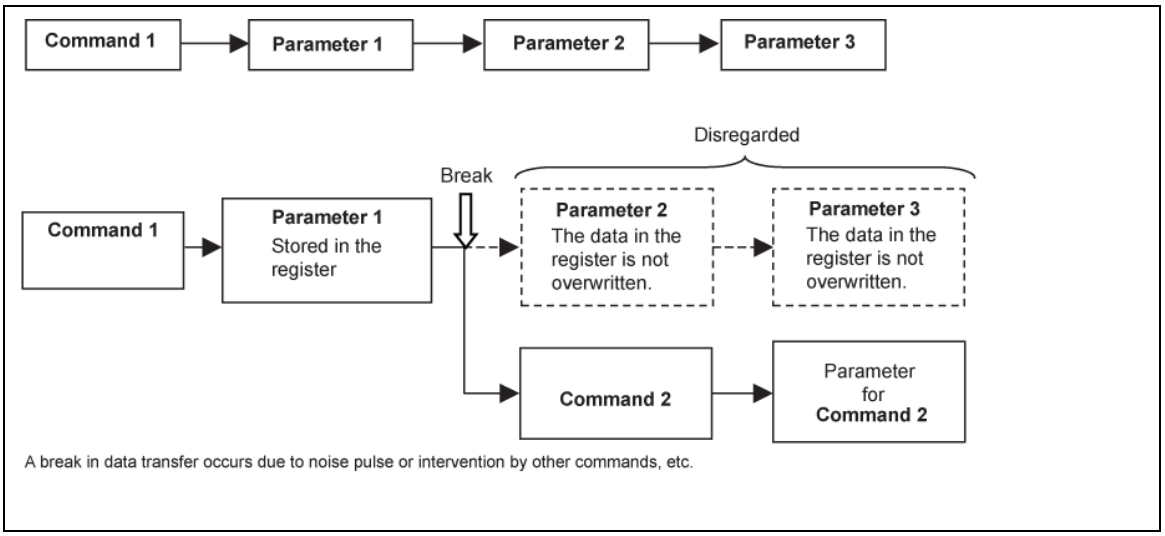


Figure 19

Data Transfer Pause

The R61581B0 does not support pause operation in Type C interface write and read operations. If transfer is stopped by setting CSX = “High” after command or parameter is transferred once, the next transfer (CSX = “Low”) should start from command.

DBI Data Format

The R61581B0 supports color formats shown in the table below. At least one color format is supported by each of Type B 18-/16-/9-/8-bit and Type C interface.

Table 10

Type	IM2-0	Data pin	color format	MIPI Spec.	R61581B0	Note
Type B	000	DB[17:0]	18bpp	Not defined	Yes	
	010	DB[15:0]	8bpp	Yes	No	
			12bpp	Yes	No	
			16bpp	Yes	Yes	
			18bpp (262,144-color Option 1)	Yes	Yes	
			18bpp (262,144-color Option 2)	Yes	Yes	
			24bpp (16,777,216-color Option 1)	Yes	Yes	Dither
			24bpp (16,777,216-color Option 2)	Yes	Yes	Dither
	001	DB[8:0]	18bpp	Yes	Yes	
	011	DB[7:0]	8bpp	Yes	No	
			12bpp	Yes	No	
			16bpp	Yes	Yes	
			18bpp	Yes	Yes	
			24bpp	Yes	Yes	Dither
Type C	101	DIN / DOUT	3bpp (8-color Option 1)	Yes	Yes	
			3bpp (8-color Option 2)	Yes	Yes	
			18bpp	Not defined	Yes	
			24bpp	Not defined	Yes	Dither
	111	DIN / DOUT	3bpp (8-color Option 1)	Yes	Yes	
			3bpp (8-color Option 2)	Yes	Yes	
			18bpp	Not Defined	Yes	
			24bpp	Not defined	Yes	Dither

Yes: Supported

No: Unsupported

DBI Type B Data Format

● Data Format for 18-Bit Interface (DB[17:0] is used. IM[2:0]=000)

	set pixel format	DFM	DB[17:0]																	
			[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Command Parameter Write	*	*											D7	D6	D5	D4	D3	D2	D1	D0
Command Parameter Read	*	*											D7	D6	D5	D4	D3	D2	D1	D0

	set pixel format	DFM	DB[17:0]																	
			[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read		*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

● Data Format for 16-Bit Interface (DB[15:0] is used. IM[2:0]=010)

	set pixel format	DFM	DB[17:0]																
			[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
Command Parameter Write	*	*									D7	D6	D5	D4	D3	D2	D1	D0	
Command Parameter Read	*	*									D7	D6	D5	D4	D3	D2	D1	D0	

	set pixel format	DFM	DB[15:0]																
			[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	
18bpp Frame Memory Write	3'h6	0	R1 [5]	R1 [4]	R1 [3]	R1 [2]	R1 [1]	R1 [0]			G1 [5]	G1 [4]	G1 [3]	G1 [2]	G1 [1]	G1 [0]			1st Trans
			B1 [5]	B1 [4]	B1 [3]	B1 [2]	B1 [1]	B1 [0]			R2 [5]	R2 [4]	R [3]	R2 [2]	R [1]	R2 [0]			2nd Trans
			G2 [5]	G2 [4]	G2 [3]	G2 [2]	G2 [1]	G2 [0]			B2 [5]	B2 [4]	B2 [3]	B2 [2]	B2 [1]	B2 [0]			3rd Trans
		1									R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			1st Trans
			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]			2nd Trans
24bpp Frame Memory Write (DITHER)	3'h7	0	R1 [7]	R1 [6]	R1 [5]	R1 [4]	R1 [3]	R1 [2]	R1 [1]	R1 [0]	G1 [7]	G1 [6]	G1 [5]	G1 [4]	G1 [3]	G1 [2]	G1 [1]	G1 [0]	1st Trans
			B1 [7]	B1 [6]	B1 [5]	B1 [4]	B1 [3]	B1 [2]	B1 [1]	B1 [0]	R2 [7]	R2 [6]	R2 [5]	R2 [4]	R2 [3]	R2 [2]	R2 [1]	R2 [0]	2nd Trans
			G2 [7]	G2 [6]	G2 [5]	G2 [4]	G2 [3]	G2 [2]	G2 [1]	G2 [0]	B2 [7]	B2 [6]	B2 [5]	B2 [4]	B2 [3]	B2 [2]	B2 [1]	B2 [0]	3rd Trans
		1									R1 [7]	R1 [6]	R1 [5]	R1 [4]	R1 [3]	R1 [2]	R1 [1]	R1 [0]	1st Trans
			G1 [7]	G1 [6]	G1 [5]	G1 [4]	G1 [3]	G1 [2]	G1 [1]	G1 [0]	B1 [7]	B1 [6]	B1 [5]	B1 [4]	B1 [3]	B1 [2]	B1 [1]	B1 [0]	2nd Trans
18bpp Frame Memory Read	*	0	r1 [5]	r1 [4]	r1 [3]	r1 [2]	r1 [1]	r1 [0]			g1 [5]	g1 [4]	g1 [3]	g1 [2]	g1 [1]	g1 [0]			1st Trans
			b1 [5]	b1 [4]	b1 [3]	b1 [2]	b1 [1]	b1 [0]			r2 [5]	r2 [4]	r2 [3]	r2 [2]	r2 [1]	r2 [0]			2nd Trans
			g2 [5]	g2 [4]	g2 [3]	g2 [2]	g2 [1]	g2 [0]			b2 [5]	b2 [4]	b2 [3]	b2 [2]	b2 [1]	b2 [0]			3rd Trans
		1									r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			1st Trans
			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]			2nd Trans

Figure 20

● Data Format for 9-Bit Interface (DB[8:0] is used. IM[2:0]=001)

	set pixel format	DFM	DB[8:0]									
			[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
Command Parameter Write	*	*		D7	D6	D5	D4	D3	D2	D1	D0	
Command Parameter Read	*	*		D7	D6	D5	D4	D3	D2	D1	D0	

	set pixel format	DFM	DB[8:0]									
			[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	1st Trans
			G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	2nd Trans
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	1st Trans
			g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	2nd Trans

● Data Format for 8-Bit Interface (DB[7:0] is used. IM[2:0]=011)

	set pixel format	DFM	DB[7:0]								
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
Command Parameter Write	*	*	D7	D6	D5	D4	D3	D2	D1	D0	
Command Parameter Read	*	*	D7	D6	D5	D4	D3	D2	D1	D0	

	set pixel format	DFM	DB[7:0]								
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	1st Trans
			G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	2nd Trans
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			1st Trans
			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			2nd Trans
			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]			3rd Trans
24bpp Frame Memory Write (DITHER)	3'h7	*	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1st Trans
			G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	2nd Trans
			B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	3rd Trans
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			1st Trans
			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			2nd Trans
			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]			3rd Trans

●Extended Format for 18bpp Data

set pixel format		EPF	Frame Memory Data (18bpp)																	
			r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	3'h5	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0 *1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0 *1
		2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1 *2	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1 *2
		2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

*1: R[4:0], B[4:0] = 5'h1F → r[5:0], b[5:0] = 6'hFF
*2: R[4:0], B[4:0] = 5'h00 → r[5:0], b[5:0] = 6'h00
Notes 1: The first Command Parameter Read and Frame Memory Read after read command is issued is invalid (dummy read).
2: Data are written to the Frame Memory when data for one pixel are input. In 2-pixel 3- transfer operation (16-bit I/F 18bpp Option1), the first and second pixels are written in the 2nd and 3rd transfers respectively.
3: If data transfer stops after 2nd transfer in 2-pixel 3-transfer operation, the first pixel data are written normally. This applies to the last address when number of pixel is odd according to window setting.
4: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

Figure 21

BGR Register Setting and Write/Read Data in the Frame Memory

System interface outputs write and read data in the same RGB order regardless of BGR register setting.

Example: 18-Bit Interface

● BGR = 0

	DB[17:0]																	
	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Write data	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

↓

	D[17:0]																	
	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Frame memory	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

↓

	DB[17:0]																	
	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Read data	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

● BGR = 1

	DB[17:0]																	
	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Write data	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

↓

	D[17:0]																	
	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Frame memory	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]

↓

	DB[17:0]																	
	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Read data	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

Figure 22

DBI Type C Data Format

● Data Format for Serial Interface Option1/Option3 (IM2-0=101/111)

	set pixel format	DFM	DB[7:0]								
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
Command Parameter Write	*	*	D7	D6	D5	D4	D3	D2	D1	D0	
Command Parameter Read	*	*	D7	D6	D5	D4	D3	D2	D1	D0	

● Extended Format for 18 bpp Data

	set pixel format	DFM	DB[7:0]								
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
3bpp Frame Memory Write	3'h1	0			R1 [0]	G1 [0]	B1 [0]	R2 [0]	G2 [0]	B2 [0]	
		1		R1 [0]	G1 [0]	B1 [0]		R2 [0]	G2 [0]	B2 [0]	
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			1st Trans
			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			2nd Trans
			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]			3rd Trans
24bpp Frame Memory Write	3'h7	*	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1st Trans
			G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	2nd Trans
			B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	3rd Trans
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			1st Trans
			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			2nd Trans
			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]			3rd Trans

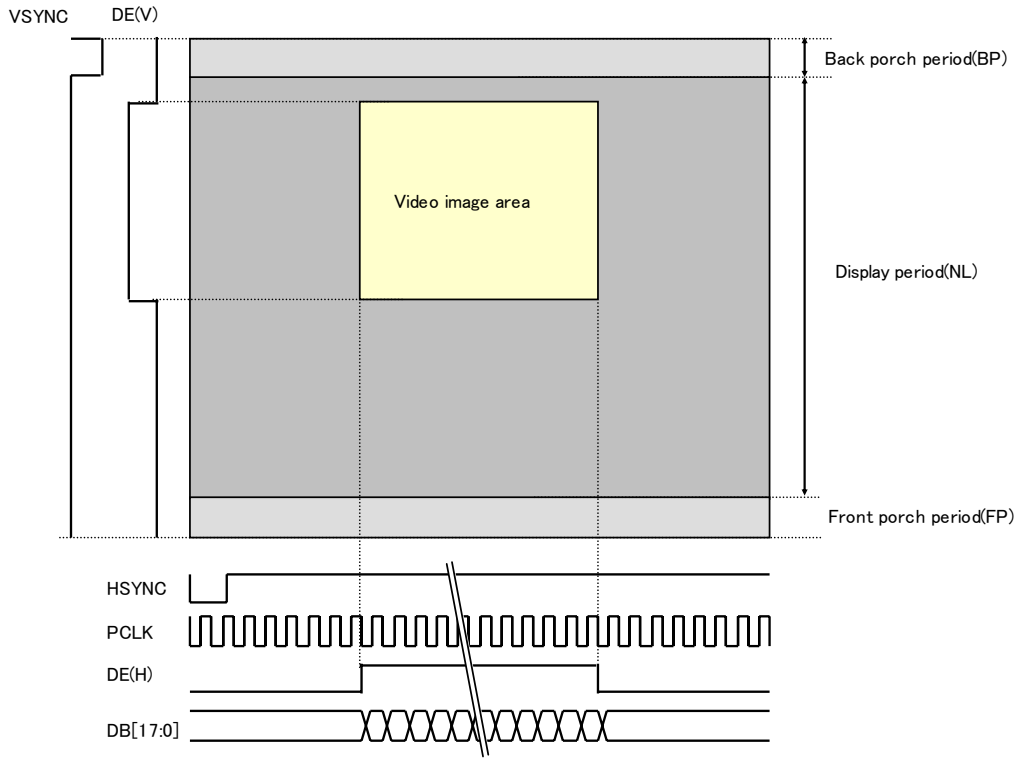
Notes 1: The first Command Parameter Read and Frame Memory Read after read command is issued is invalid (dummy read).
2: This page shows example with BGR=0. If BGR=1, allocation of R and B in the frame memory is swapped.

Figure 23

Display Pixel Interface (DPI)

Display Pixel Interface (DPI)

In Display Pixel Interface (DPI) operation, display operation is in synchronization with synchronization signals VSYNC, HSYNC and PCLK. By using Window Address Function in accordance with the cycle of frame memory write operation, the data are transferred only to the video image area so that the R61581B0 consumes only a small amount of power. In DPI operation, front and back porch periods must be made before and after the display period. Commands must be transferred via DBI Type B serial interface. DPI and DBI Type B cannot be selected simultaneously.



VSYNC: Frame synchronization signal. Specifies the start position of a frame.
HSYNC: Line synchronization signal. Specifies the start of a horizontal line.
PCLK: Pixel clock. Data is accepted at the rising edge of this signal.
DE: Data enable signal. DE=high means the R61581B0 is in data enable period.
DB[17:0]: Display data (RGB).

Back porch period(BP) BP≧2H.	Front porch period(FP) FP≧8H.
Display period (DP) NL=480H.	Number of line in 1frame period = FP+NL+BP.

Figure 24

DPI Timing

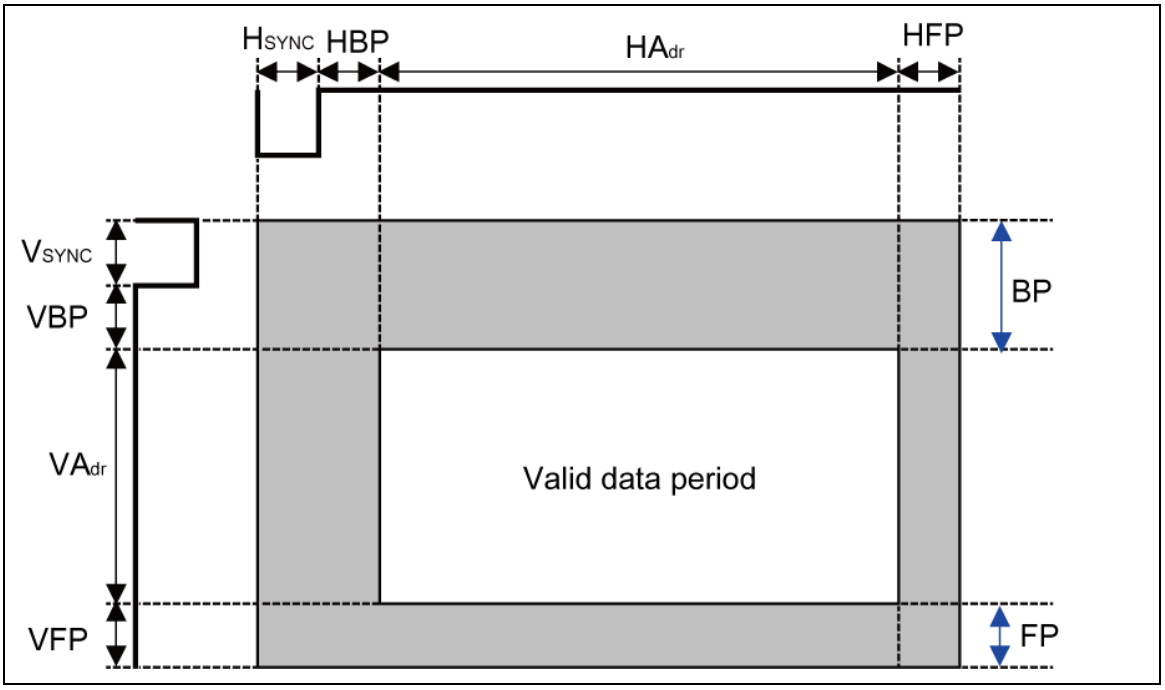


Figure 25

Table 11

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	2	10	16	1	PCLKCYC
Horizontal Back Porch	HBP	2	20	24	1	PCLKCYC
Horizontal Address	HAdr	—	320	—	1	PCLKCYC
Horizontal Front Porch	HFP	2	10	16	1	PCLKCYC
Vertical Synchronization	Vsync	1	2	4	1	Line
Vertical Back Porch	VBP	1	2	—	1	Line
Vertical Address	VAdr	—	480	—	1	Line
Vertical Front Porch	VFP	8	10	—	1	Line

Typical values are setting example when used with panel resolution 320 x 480 (HVGA), clock frequency 10.71MHz and frame frequency about 60Hz.

Note1: 1 Make sure that Vsync + VBP = BP, VFP = FP and VAdr = Number of lines specified by NL.
2 Make sure that Vsync + VBP + VFP + VAdr ≧ 490 Lines.
3 Make sure that (Number of PCLK per 1 line) ≥ (Number of RTN clock) × Division ratio (DIV) × (PCDIVL+PCDIVH) Setting example is as follows.

Setting Example for Display Control Clock in DPI Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing PCLK.

PCDIVH [3:0]: Number of PCLK during internal clock CLKD's high period. In units of 1 clock.
PCDIVL [3:0]: Number of PCLK during internal clock CLKD's low period. In units of 1 clock.

PCDIVH and PCDIVL, specifying PCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 785KHz is the smallest. Set PCDIVL = PCDIVH or PCDIVH - 1. Follow the restriction (Number of PCLK in 1H) ≥ (Number of RTN clock) * (Division ratio (DIV)) * (PCDIVL + PCDIVH).

Setting Example To set frame frequency to 60Hz:

Internal Clock

Internal Oscillation Clock: 785KHz
DIV=2'b0 (x 1/1)
RTN = 5'h19 (25 clocks)
FP=8'h8, BP=8'h8, NL=3B (480 lines)
→ **59.35Hz**

PCLK

HSYNC = 10CLK
HBP = 20CLK
HFP = 10CLK

60Hz x (8 + 480 + 8) lines x (10 + 20 + 320 + 10) clocks = 10.71MHz
PCLK frequency = 10.71MHz

10.71MHz / 785KHz = 13.64 → Set PCDIVH and PCDIVL so that PCLK is divided into 14.

10.71 / 14 = 765KHz
765KHz / 25 clocks / 496 lines = 61.7Hz

PCDIVH = 4'h7
PCDIVL = 4'h7

Video Image Display via DPI

The R61581B0 supports video image capable DPI and frame memory to store display data so that the driver has strong points such as

1. Window address function enabling data transfer for only video image area.
2. Data only for video image display area can be transferred.
3. Reduced amount of data transfer enables low power consumption operation as the system as a whole.
4. Still picture area is rewritten even in video image display period by using system interface together with DPI.

To access Frame Memory via System Interface (DBI) in DPI operation

Frame memory can be accessed via system interface in DPI operation as well. However in DPI operation, the frame memory is always written in synchronization with PCLK when DE = ”High”. Therefore, make sure to stop display data write operation via DPI to write data to frame memory via system interface. If RM = 0, the frame memory is accessed via system interface. To return to DPI operation, make write/read bus cycle time and then set RM = 1 and execute a write_memory_start command (2Ch) and then start frame memory access. If both interfaces are used to access the frame memory, write data are not guaranteed.

The following figure shows an example of video image display via DPI and display data rewrite in the still picture area via system interface.

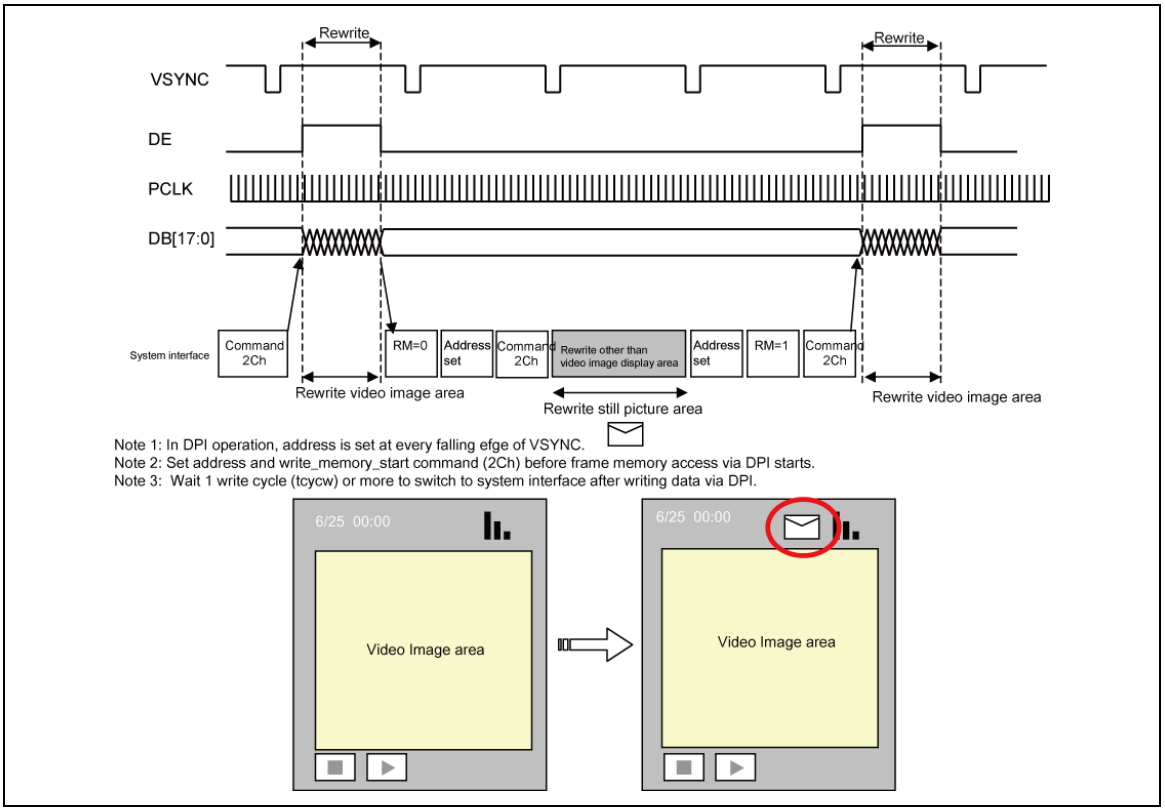


Figure 26

16-Bit DPI Connection

16-bit DPI is selected when set_pixel_format (3Ah) D[6:4] = 3'h5. Image is displayed in synchronization with synchronization signals VSYNC, HSYNC and PCLK. 16-bit RGB data (DB[15:0]) are transferred to internal frame memory in synchronization with data enable signal DE and display operation.

* Commands are set only via system interface (DBI Type C).

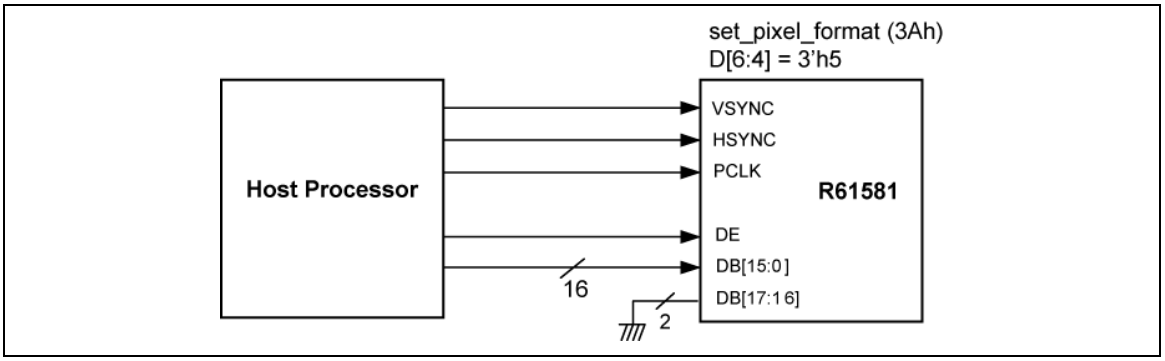


Figure 27

18-Bit DPI Connection

18-bit DPI is selected when set_pixel_format (3Ah) D[6:4] = 3'h6. Image is displayed in synchronization with synchronization signals VSYNC, HSYNC and PCLK. 18-bit RGB data (DB[17:0]) are transferred to internal frame memory in synchronization with data enable signal DE and display operation.

* Setting command is possible only via system interface (DBI Type C).

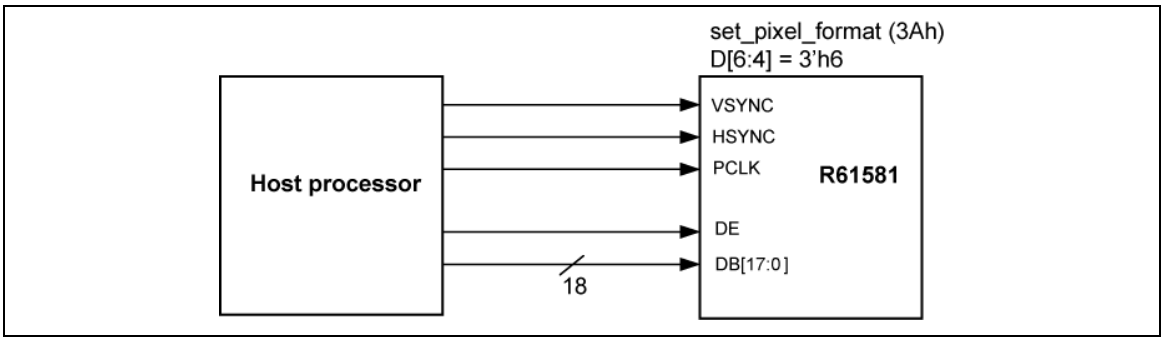


Figure 28

DPI Data Format

The R61581B0 supports color formats as below:

Table 12

set_pixel_format (3Ah) D[6:4]	Data pin	Color format	MIPI Spec.	R61581B0
3'h6	DB[17:0]	18bpp	Yes	Yes
3'h5	DB[15:0]	16bpp	Yes	Yes

Yes: Supported

No: Unsupported

See the next figure for connection of host professor and the R61581B0's pins.

●Pin Connection for 18-Bit Interface (DB[17:0] is used. set_pixel_format D[6:4]=3'h6. 18bpp)

Configuration 1

Host pin	D[23:0]																							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
							↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
LCD driver pin	DB[17:0]																							
							[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Configuration 2

Host pin	D[23:0]																							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
			R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0
			↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓
LCD driver pin	DB[17:0]																							
			[17]	[16]	[15]	[14]	[13]	[12]			[11]	[10]	[9]	[8]	[7]	[6]			[5]	[4]	[3]	[2]	[1]	[0]
			R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0

●Pin Connection for 16-Bit Interface (DB[15:0] is used. set_pixel_format D[6:4]=3'h5. 18bpp)

Configuration 1

Host pin	D[23:0]																							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
									R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
									↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
LCD driver pin	DB[15:0]																							
									[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
									R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Configuration 2

Host pin	D[23:0]																							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
				R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0
				↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	↓				↓	↓	↓	↓	↓
LCD driver pin	DB[15:0]																							
				[15]	[14]	[13]	[12]	[11]			[10]	[9]	[8]	[7]	[6]	[5]				[4]	[3]	[2]	[1]	[0]
				R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0

Configuration 3

Host pin	D[23:0]																							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
			R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0	
			↓	↓	↓	↓	↓				↓	↓	↓	↓	↓	↓			↓	↓	↓	↓	↓	
LCD driver pin	DB[15:0]																							
			[15]	[14]	[13]	[12]	[11]				[10]	[9]	[8]	[7]	[6]	[5]			[4]	[3]	[2]	[1]	[0]	
			R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0	

●Extended Format for 18 bpp Data

set_pixel_format	EPF	Frame Memory Data (18bpp)																	
		r5	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0
18bpp	*	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	2'h0	R4	R3	R2	R1	R0	0 *1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0 *1
	2'h1	R4	R3	R2	R1	R0	1 *2	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1 *2
	2'h2	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4

Figure 29

Note to DPI

a. In DPI operation, functions noted “disabled” in the table below are invalid.

Table 13

Function	External display interface	Internal display operation
Partial display function	Disabled	Enabled
Idle mode	Disabled	Enabled

b. It is necessary to supply VSYNC, HSYNC, PCLK, and DE all the time during DPI operation.

c. Panel control signal reference clock is PCLK in DPI operation unlike usual internal oscillation clock.

d. Make sure to follow mode switching sequence to transit from/to display by internal operation mode to/from display via external display interface.

e. The front porch period continues from the end of one frame period to the next VSYNC input during DPI operation.

f. DPI and DBI Type B (bus interface) cannot be selected simultaneously.

g. Address is set every frame on the falling edge of VSYNC during DPI operation.

h. Disable ENABLE to read/write instruction register via clock synchronous serial interface during DPI operation.

i. Make sure to follow transition sequence between internal clock operation and DPI display operation. Please execute the clock switch from the DPI operation to the internal clock operation in the state of sleep-in .

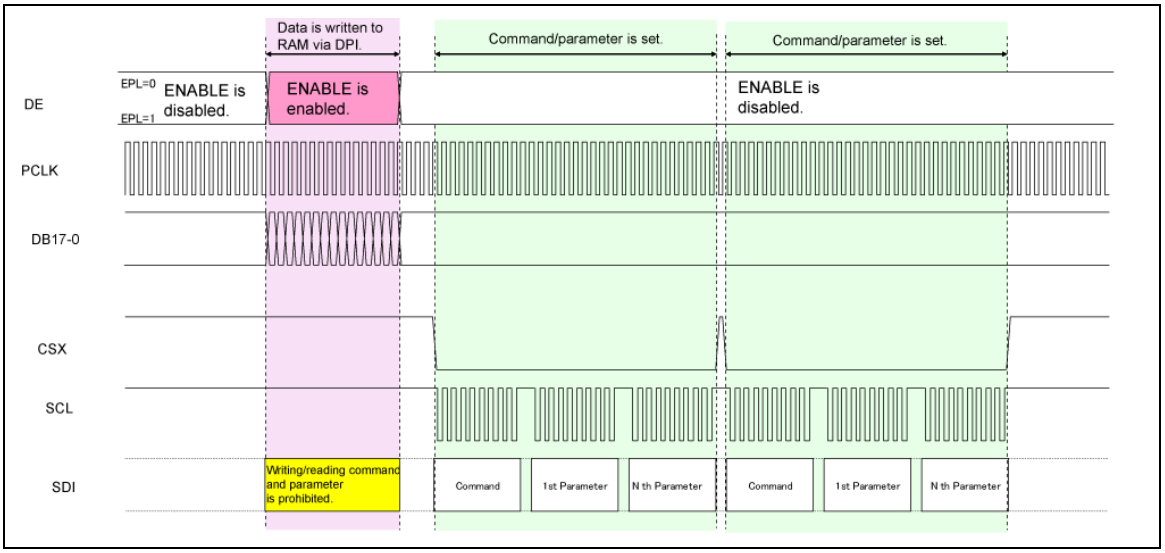


Figure 30

Transition Sequence between Internal Clock Operation and DPI Display Operation

From Internal Clock Operation to DPI Display Operation

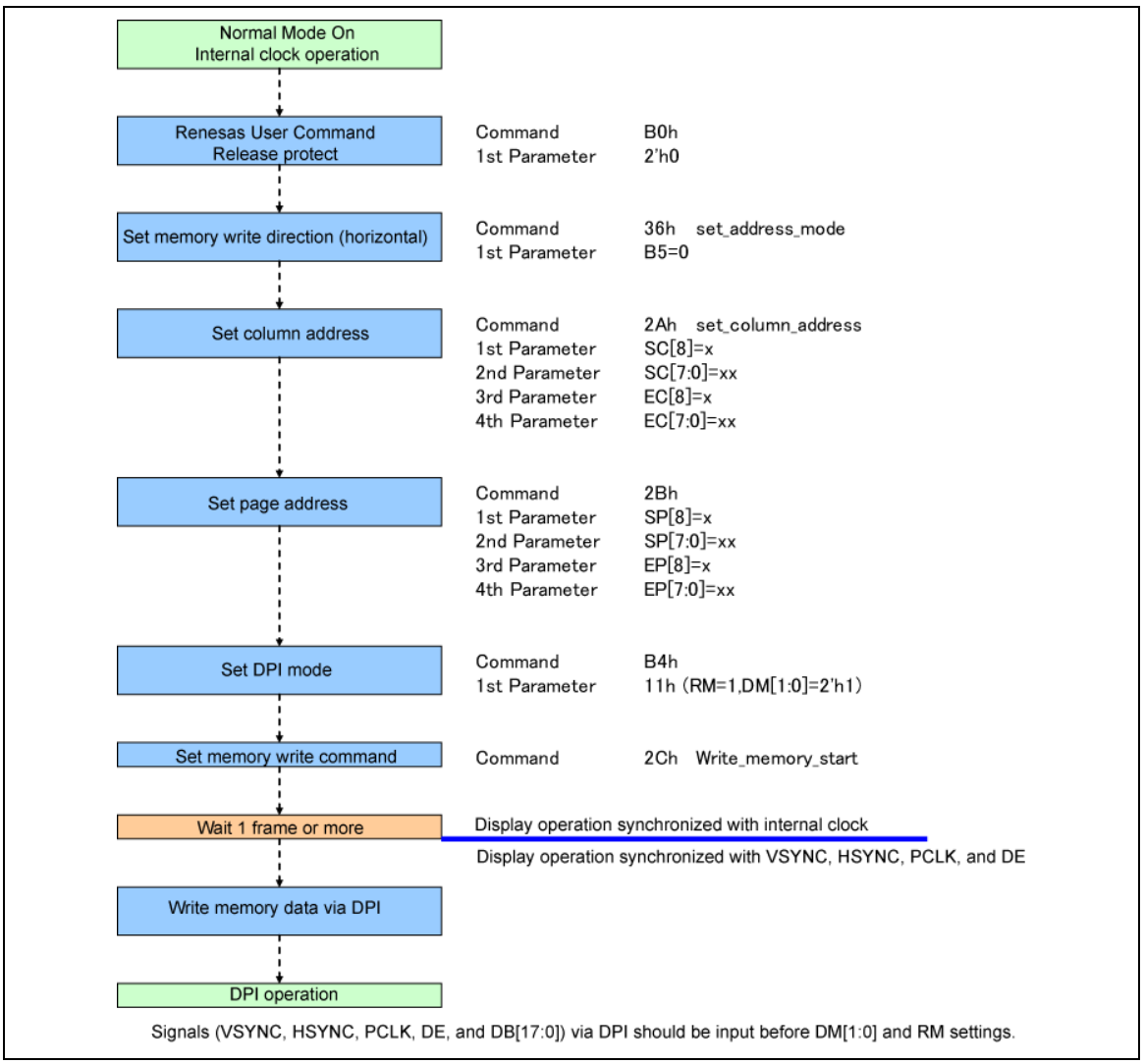


Figure 31

From DPI Display Operation to Internal Clock Operation

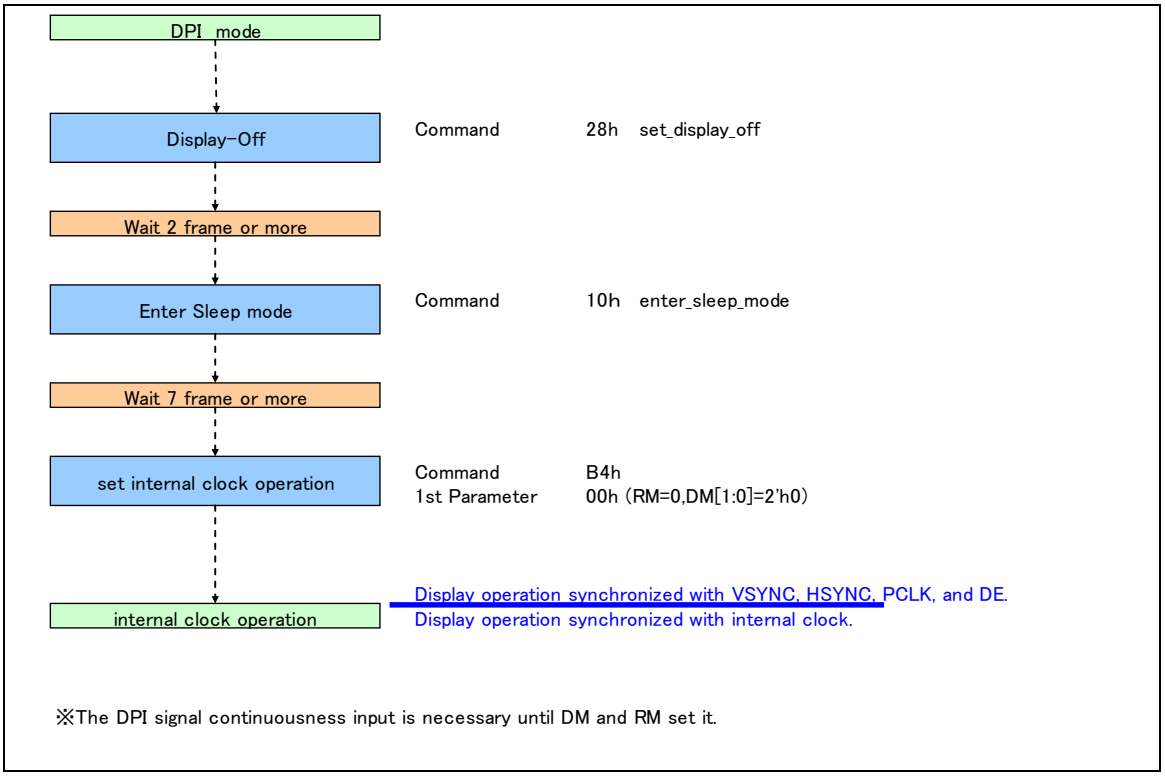


Figure 32

Command List

Table 14 User Command

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number of Parameter	MIPI DCS Type 1 Requirement	R61581B0 Implementation	Note
00h	nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
04h	read_DDB_start	R	5	No	Yes	
06h	get_red_channel	R	1	No	No	
07h	get_green_channel	R	1	No	No	
08h	get_blue_channel	R	1	No	No	
0Ah	get_power_mode	R	1	Yes	Yes	
0Bh	get_address_mode	R	1	Yes (Bit[7:0])	Yes (Bit[7:4], [0] only)	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes	1
0Eh	get_signal_mode	R	1	Yes	Yes	
0Fh	get_diagnostic _result	R	1	Bit7/6: Yes Bit5/4: Optional	Yes (Bit[6] Only)	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	Yes	Yes	
13h	enter_normal_mode	C	0	Yes	Yes	
20h	exit_invert_mode	C	0	Yes	Yes	
21h	enter_invert_mode	C	0	Yes	Yes	
26h	set_gamma_curve	W	1	Yes	No	1
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_address	W	4	Yes	Yes	
2Bh	set_page_address	W	4	Yes	Yes	

Table 15 User Command (continued)

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number of Parameter	MIPI DCS Type 1 Requirement	R61581B0 Implementation	Note
2Ch	write_memory_start	W	Variable	Yes	Yes	2
2Dh	write_LUT	W	Variable	Optional	No	
2Eh	read_memory_start	R	Variable	Yes	Yes	2
30h	set_partial_area	W	4	Yes	Yes	
33h	set_scroll_area	W	6	Yes	Yes	
34h	set_tear_off	C	0	Yes	Yes	
35h	set_tear_on	W	1	Yes	Yes	
36h	set_address_mode	W	1	Yes (Bit[7:0])	Yes (Bit[7:4], [0] only)	
37h	set_scroll_start	W	2	Yes	No	
38h	exit_idle_mode	C	0	Yes	Yes	
39h	enter_idle_mode	C	0	Yes	Yes	
3Ah	set_pixel_format	W	1	Yes	Yes	
3Ch	write_memory _continue	W	Variable	Yes	Yes	2
3Eh	read_memory _continue	R	Variable	Yes	Yes	2
44h	set_tear_scanline	W	2	Yes	Yes	
45h	get_scanline	R	2	Yes	Yes	
A1h	read_DDB_start	R	5	Yes	Yes	
A8h	read_DDB_continue	R	Variable	Yes	Yes	

Notes:
1. The R61581B0 supports one type of gamma curve specified by gamma adjustment register GC0. Therefore, D [2:0] bits (get_display_mode, 0Dh) are fixed at 0.
2. See “DBI Data Format” and “DPI Data Format” for details on data write to the frame memory and data read from the frame memory.

Table 16 Manufacturer Command

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number of Parameter	Category
B0h	Manufacturer Command Access Protect	W/R	1	Additional User Command
B1h	Low Power Mode Control	W/R	1	Additional User Command
B3h	Frame Memory Access and Interface Setting	W/R	4	Additional User Command
B4h	Display Mode and Frame Memory Write Mode Setting	W/R	1	Additional User Command
B8h	Backlight Control 1	W/R	18	
B9h	Backlight Control 2	W/R	5	
BAh	Backlight Control 3		1	
BFh	Device Code Read	R	4	
C0h	Panel Driving Setting	W/R	8	
C1h	Display Timing Setting for Normal Mode	W/R	4	
C2h	Display Timing Setting for Partial Mode	W/R	4	
C3h	Display Timing Setting for Idle Mode	W/R	4	
C4h	Source/VCOM/Gate Driving Timing Setting	W/R	4	
C6h	Interface Setting	W/R	1	
C8h	Gamma Set	W/R	20	
D0h	Power Setting (Common Setting)	W/R	4	
D1h	VCOM Setting	W/R	3	
D2h	Power Setting for Normal Mode	W/R	3	
D3h	Power Setting for Partial Mode	W/R	3	
D4h	Power Setting for Idle Mode	W/R	3	
DAh	DITHER Control	W/R	1	
E0h	NVM Access Control	W/R	3	
E1h	NVM Write Data Control	W/R	1	
EFh	Read Mode In	W	0	See note 3.
F0h-FFh	LSI Test Registers	W/R	Variable	

Note: 3. This command can be used only in DBI Type C operation.

Command Accessibility

In initial state, only User Command and Manufacturer Command Access Protect command (B0h) are accessible. Other commands are treated as nop.

Of Manufacturer Command (B0h-EFh) defined in the table below, additional User Commands (B1h-BFh) are accessible only when MCAP=2'h0 or 2'h2.

Other Manufacturer Commands (C0h-EFh) are accessible only when MCAP=2'h0. See MCAP command description for detail.

Table 17 User Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
00h	nop	Yes	Yes	Yes	Yes	Yes
01h	soft_reset	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
04h	read_DDB_start	Yes	Yes	Yes	Yes	Yes
0Ah	get_power_mode	Yes	Yes	Yes	Yes	Yes
0Bh	get_address_mode	Yes	Yes	Yes	Yes	Yes
0Ch	get_pixel_format	Yes	Yes	Yes	Yes	Yes
0Dh	get_display_mode	Yes	Yes	Yes	Yes	Yes
0Eh	get_signal_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
0Fh	get_diagnostic _result	Yes	Yes	Yes	Yes	Yes
10h	enter_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
11h	exit_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
12h	enter_partial_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
13h	enter_normal_mode	Yes	Yes	Yes	Yes	Yes
20h	exit_invert_mode	Yes	Yes	Yes	Yes	Yes
21h	enter_invert_mode	Yes	Yes	Yes	Yes	Yes
28h	set_display_off	Yes	Yes	Yes	Yes	Yes
29h	set_display_on	Yes	Yes	Yes	Yes	Yes
2Ah	set_column_address	Yes	Yes	Yes	Yes	Yes
2Bh	set_page_address	Yes	Yes	Yes	Yes	Yes

Table 18 User Command (continued)

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
2Ch	write_memory_start	Yes	Yes	Yes	Yes	Yes
2Eh	read_memory_start	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
30h	set_partial_area	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
34h	set_tear_off	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
35h	set_tear_on	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
36h	set_address_mode	Yes	Yes	Yes	Yes	Yes
38h	exit_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
39h	enter_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Ah	set_pixel_format	Yes	Yes	Yes	Yes	Yes
3Ch	write_memory_ continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Eh	read_memory_ continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
44h	set_tear_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
45h	get_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	No
A1h	read_DDB_start	Yes	Yes	Yes	Yes	Yes

Table 19 Manufacturer Command

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
B0h	Manufacturer Command Access Protect	Yes	Yes	Yes	Yes	Yes
B1h	Low Power Mode Control	No	No	No	No	Yes
B3h	Frame Memory Access and Interface Setting	Yes	Yes	Yes	Yes	Yes
B4h	Display Mode and Frame Memory Write Mode Setting	Yes	Yes	Yes	Yes	Yes
B8h	Backlight Control 1	Yes	Yes	Yes	Yes	Yes
B9h	Backlight Control 2	Yes	Yes	Yes	Yes	Yes
BAh	Backlight Control 3	Yes	Yes	Yes	Yes	No
BFh	Device Code Read	Yes	Yes	Yes	Yes	Yes
C0h	Panel Driving Setting	Yes	Yes	Yes	Yes	No
C1h	Display Timing Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
C2h	Display Timing Setting for Partial Mode	Yes	Yes	Yes	Yes	Yes
C3h	Display Timing Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
C4h	Source/VCOM/Gate Driving Timing Setting	Yes	Yes	Yes	Yes	Yes
C6h	Interface Setting	Yes	Yes	Yes	Yes	Yes
C8h	Gamma Set	Yes	Yes	Yes	Yes	Yes
D0h	Power Setting (Common Setting)	Yes	Yes	Yes	Yes	Yes
D1h	VCOM Setting	Yes	Yes	Yes	Yes	Yes
D2h	Power Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
D3h	Power Setting for Partial Mode	Yes	Yes	Yes	Yes	Yes
D4h	Power Setting for Idle Mode	Yes	Yes	Yes	Yes	Yes
DAh	DITHER Control	Yes	Yes	Yes	Yes	Yes

Table 20 Manufacturer Command (continued)

Operational Code (Hex)	Command	Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
E0h	NVM Access Control	Yes	Yes	Yes	Yes	No
E1h	set_write_DDB Control	Yes	Yes	Yes	Yes	Yes
EFh	Read Mode In	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
B0h-FFh (Except the above commands)	LSI Test Registers	No	No	No	No	No

Notes: 1. Commands may be accessed only when DM=0 (display operation is in synchronization with internal oscillation clock). Accessing these commands is disabled when DM=1 and DPI is selected.

2. Read Mode In command (EFh) can be used only in DBI Type C operation.

Default Modes and Values

Table 21 User Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	nop	None	N/A	N/A	N/A
01h	soft_reset	None	N/A	N/A	N/A
04h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)
		5th	FFh	FFh	FFh
0Ah	get_power_mode	1st	08h	08h	08h
0Bh	get_address_mode	1st	00h	No Change (Note1)	00h
0Ch	get_pixel_format	1st	66h	66h	66h
0Dh	get_display_mode	1st	00h	00h	00h
0Eh	get_signal_mode	1st	00h	00h	00h
0Fh	get_diagnostic _result	1st	00h	00h	00h
10h	enter_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
11h	exit_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
12h	enter_partial_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
13h	enter_normal_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
20h	exit_invert_mode	None	Invert Mode Off	Invert Mode Off	Invert Mode Off
21h	enter_invert_mode	None	Invert Mode Off	Invert Mode Off	Invert Mode Off
28h	set_display_off	None	Display Off	Display Off	Display Off
29h	set_display_on	None	Display Off	Display Off	Display Off
2Ah	set_column_address	1st/2nd SC[9:0]	000h	000h	000h
		3rd/4th EC[9:0]	13Fh	If set_address _mode B5=0 : 13Fh B5=1 : 1DFh	13Fh
2Bh	set_page_address	1st/2nd SP[9:0]	000h	000h	000h
		3rd/4th EP[9:0]	1DFh	If set_address _mode B5=0 : 1DFh B5=1 : 13Fh	1DFh

Table 22 User Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
2Ch	write_memory_start	all	Random Values	Not Cleared	Not Cleared
2Eh	read_memory_start	all	Random Values	Not Cleared	Not Cleared
30h	set_partial_area	1st/2nd SR[9:0]	000h	000h	000h
		3rd/4th ER[9:0]	1DFh	1DFh	1DFh
33h	set_scroll_area	1st/2nd TFA[9:0]	000h	000h	000h
		3rd/4th VSA[9:0]	1E0h	1E0h	1E0h
		4th/5th BFA[9:0]	000h	000h	000h
34h	set_tear_off	None	TE line output Off	TE line output Off	TE line output Off
35h	set_tear_on	1st	TE line output Off	TE line output Off	TE line output Off
36h	set_address_mode	1st	00h	No Change (Note1)	00h
37h	set_scroll_start	1st/2nd VSP[9:0]	000h	000h	000h
38h	exit_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39h	enter_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3Ah	set_pixel_format	1st	66h	66h	66h
3Ch	write_memory _continue	all	Random Values	Not Cleared	Not Cleared
3Eh	read_memory _continue	all	Random Values	Not Cleared	Not Cleared
44h	set_tear_scanline	1st/2nd STS[9:0]	000h	000h	000h
45h	get_scanline	1st/2nd GTS[9:0]	000h (invalid)	000h (invalid)	000h (invalid)
A1h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)
		5th	FFh	FFh	FFh
A8h	read_DDB_continue	-	Refer read_DDB_start	Refer read_DDB_start	Refer read_DDB_start

Note1) No Change from the value before soft_reset command.

Note2) Data is data loaded from building NVM into. When the VCM register value, Supplier ID, and Supplier Elective Data are written in NVM, the value becomes Default Value.

Table 23 Manufacturer Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
B0h	Manufacturer Command Access Protect	1st	MCAP=2'h3	No Change (Note1)	MCAP=2'h3
B1h	Low Power Mode Control	1st	DSTB=0 Sleep Mode On	DSTB=0 Sleep Mode On	DSTB=0 Sleep Mode On
B3h	Frame Memory Access and Interface setting	1st	WEMODE=0	No Change (Note1)	WEMODE=0
		2nd	TEI=3'h0	No Change (Note1)	TEI=3'h0
		3rd	DENC=3'h0	No Change (Note1)	DENC=3'h0
		4th	DFM=2'h0 EPF=2'h0	No Change (Note1)	DFM=2'h0 EPF=2'h0
B4h	Display Mode and Frame Memory Write Mode Setting	1st	RM=0 DM=2'h0	No Change (Note1)	RM=0 DM=2'h0
B8h	Backlight Control (1)	1st	BLCM=0 BLCON=0	No Change (Note1)	BLCM=0 BLCON=0
		2nd	THREW0=5'h00	No Change (Note1)	THREW0=5'h00
		3rd	THREW1=5'h00	No Change (Note1)	THREW1=5'h00
		4th	ULMTW0=5'h1F	No Change (Note1)	ULMTW0=5'h1F
		5th	ULMTW1=5'h1F	No Change (Note1)	ULMTW1=5'h1F
		6th	LLMTW0=5'h1F	No Change (Note1)	LLMTW0=5'h1F
		7th	LLMTW1=5'h1F	No Change (Note1)	LLMTW1=5'h1F
		8th	PITCHW=4'h0	No Change (Note1)	PITCHW=4'h0
		9th	CGAPW=5'h14	No Change (Note1)	CGAPW=5'h14
		10th	COEFK0=5'h0C	No Change (Note1)	COEFK0=5'h0C
		11th	COEFK1=5'h0C	No Change (Note1)	COEFK1=5'h0C
		12th	TBL3=8'h37	No Change (Note1)	TBL3=8'h37
		13th	TBL4=8'h5A	No Change (Note1)	TBL4=8'h5A
		14th	TBL5=8'h87	No Change (Note1)	TBL5=8'h87
		15th	TBL6=8'hBE	No Change (Note1)	TBL6=8'hBE
		16th	CTRL_SEL0= 2'h0	No Change (Note1)	CTRL_SEL0= 2'h0
		17th	CTRL_SEL1= 2'h0	No Change (Note1)	CTRL_SEL1= 2'h0
		18th	DGAP=2'h0	No Change (Note1)	DGAP=2'h0

Table 24 Manufacturer Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
B9h	Backlight Control (2)	1st	LEDON=0 PWMON=0	No Change (Note1)	LEDON=0 PWMON=0
		2nd	BDCV=8'h00	No Change (Note1)	BDCV=8'h00
		3rd	PWMDIV=8'h00	No Change (Note1)	PWMDIV=8'h00
		4th	DIMON=0 LEDPWMPOL=0 LEDPWME=0 PWMWM=0	No Change (Note1)	DIMON=0 LEDPWMPOL=0 LEDPWME=0 PWMWM=0
BAh	Backlight Control (3)	1st	RDPWM=8'h00	RDPWM=8'h00	RDPWM=8'h00
BFh	Device Code Read	1st	8'h01	8'h01	8'h01
		2nd	8'h22	8'h22	8'h22
		3rd	8'h15	8'h15	8'h15
		4th	8'h81	8'h81	8'h81
C0h	Panel Driving Setting	1st	SS=0,BGR=0 GS=0,SM=0 REV=0	No Change (Note1)	SS=0,BGR=0 GS=0,SM=0 REV=0
		2nd	NL=6'h3B	No Change (Note1)	NL=6'h3B
		3rd	SCN=6'h00	No Change (Note1)	SCN=6'h00
		4th	PTV=0 BLV=1	No Change (Note1)	PTV=0 BLV=1
		5th	PTS=3'h0 PTDC=0 NDL=0	No Change (Note1)	PTS=3'h0 PTDC=0 NDL=0
		6th	ISC=4'h1 PTG=0	No Change (Note1)	ISC=4'h1 PTG=0
		7th	NW=2'h0 BLS=0	No Change (Note1)	NW=2'h0 BLS=0
		8th	PCDIVL=3'h3 PCDIVH=3'h4	No Change (Note1)	PCDIVL=3'h3 PCDIVH=3'h4
C1h	Display Timing Setting for Normal Mode	1st	BC0=1	No Change (Note1)	BC0=1
		2nd	RTN0=6'h19 DPI_OFF=0	No Change (Note1)	RTN0=6'h19 DPI_OFF=0
		3rd	BP0=8'h08	No Change (Note1)	BP0=8'h08
		4th	FP0=8'h08	No Change (Note1)	FP0=8'h08
C2h	Display Timing Setting for Partial Mode	1st	BC1=1	No Change (Note1)	BC1=1
		2nd	RTN1=6'h19	No Change (Note1)	RTN1=6'h19
		3rd	BP1=8'h08	No Change (Note1)	BP1=8'h08
		4th	FP1=8'h08	No Change (Note1)	FP1=8'h08
C3h	Display Timing Setting for Idle Mode	1st	BC2=1	No Change (Note1)	BC2=1
		2nd	RTN2=6'h19	No Change (Note1)	RTN2=6'h19
		3rd	BP2=8'h08	No Change (Note1)	BP2=8'h08
		4th	FP2=8'h08	No Change (Note1)	FP2=8'h08

Table 25 Manufacturer Command (continued)

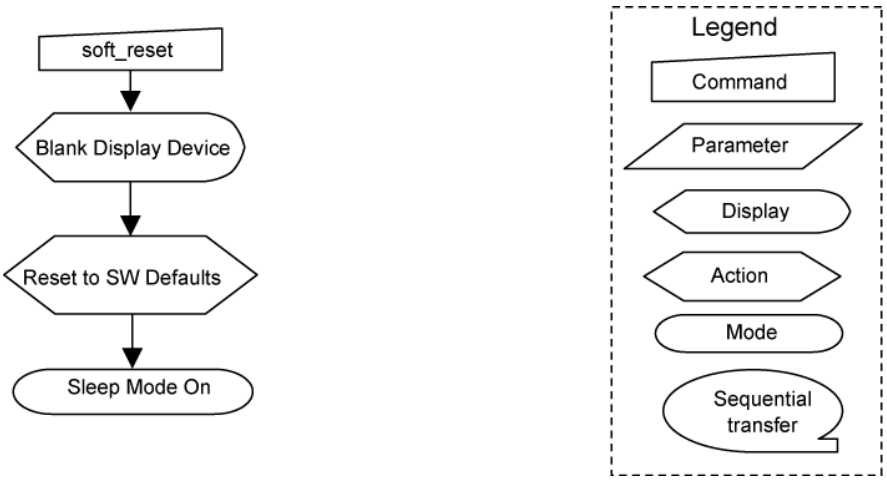
Operational Code (Hex)	Command	Parameters	Default Modes and Values (Hex)		
			After Power-on	After SW Reset	After HW Reset
C4h	Source/VCOM/Gate Driving Timing Setting	1st	NOW=3'h1 SDT=3'h1	No Change (Note1)	NOW=3'h1 SDT=3'h1
		2nd	MCP=3'h1	No Change (Note1)	MCP=3'h1
		3rd	VEM=2'h3 VEQW=3'h1	No Change (Note1)	VEM=2'h3 VEQW=3'h1
		4th	SPCW=3'h1	No Change (Note1)	SPCW=3'h1
C6h	Interface Setting	1st	VSPL=1'h1 HSPL=1'h0 EPL=1'h0 DPL=1'h1	No Change (Note1)	VSPL=1'h1 HSPL=1'h0 EPL=1'h0 DPL=1'h1
C8h	Gamma Set	1st-18th	All "0"	No Change (Note1)	All "0"
D0h	Power Setting for Common	1st	WCVC=0 WCVRH=0 WCBT=0	No Change (Note1)	WCVC=0 WCVRH=0 WCBT=0
		2nd	VC=3'h0	No Change (Note1)	VC=3'h0
		3rd	VRH=5'h00	No Change (Note1)	VRH=5'h00
		4th	BT=3'h0 BTH=3'h0 BTMODE=0	No Change (Note1)	BT=3'h0 BTH=3'h0 BTMODE=0
D1h	VCOM Setting	1st	WCVCM=0 WCVDV=0	No Change (Note1)	WCVCM=0 WCVDV=0
		2nd	NVM value	NVM value	NVM value
		3rd	NVM value	NVM value	NVM value
D2h	Power Setting for Normal Mode	1st	AP0=2'h3	No Change (Note1)	AP0=2'h3
		2nd	DC00=3'h4 DC10=3'h2	No Change (Note1)	DC00=3'h4 DC10=3'h2
		3rd	DC30=3'h4	No Change (Note1)	DC30=3'h4
D3h	Power Setting for Partial Mode	1st	AP1=2'h3	No Change (Note1)	AP1=2'h3
		2nd	DC01=3'h4 DC11=3'h2	No Change (Note1)	DC01=3'h4 DC11=3'h2
		3rd	DC31=3'h2	No Change (Note1)	DC31=3'h2
D4h	Power Setting for Idle Mode	1st	AP2=2'h3	No Change (Note1)	AP2=2'h3
		2nd	DC02=3'h4 DC12=3'h2	No Change (Note1)	DC02=3'h4 DC12=3'h2
		3rd	DC32=3'h2	No Change (Note1)	DC32=3'h2
DAh	DITHER Setting	1st	DITHERON=0 SAT_LOW=0 PTN_SEL=0 OFSY=2'h0 OFSX=2'h0	No Change (Note1)	DITHERON=0 SAT_LOW=0 PTN_SEL=0 OFSY=2'h0 OFSX=2'h0
E0h	NVM Access Control	1st	NVAE=0	No Change (Note1)	NVAE=0
		2nd	FTT=0	No Change (Note1)	FTT=0
		3rd	VERIFLGER=0 VERIFLGWR=0 TEM=0	No Change (Note1)	VERIFLGER=0 VERIFLGWR=0 TEM=0
E1h	NVM Write Date Control	1st	WCDDB=0	No Change (Note1)	WCDDB=0
EFh	Read Mode In	1st	N/A	N/A	N/A

User Command

nop : 00h

00h	nop												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00h
Parameter	None												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read. X = Don't Care												
Restriction	-												
Flow Chart	-												

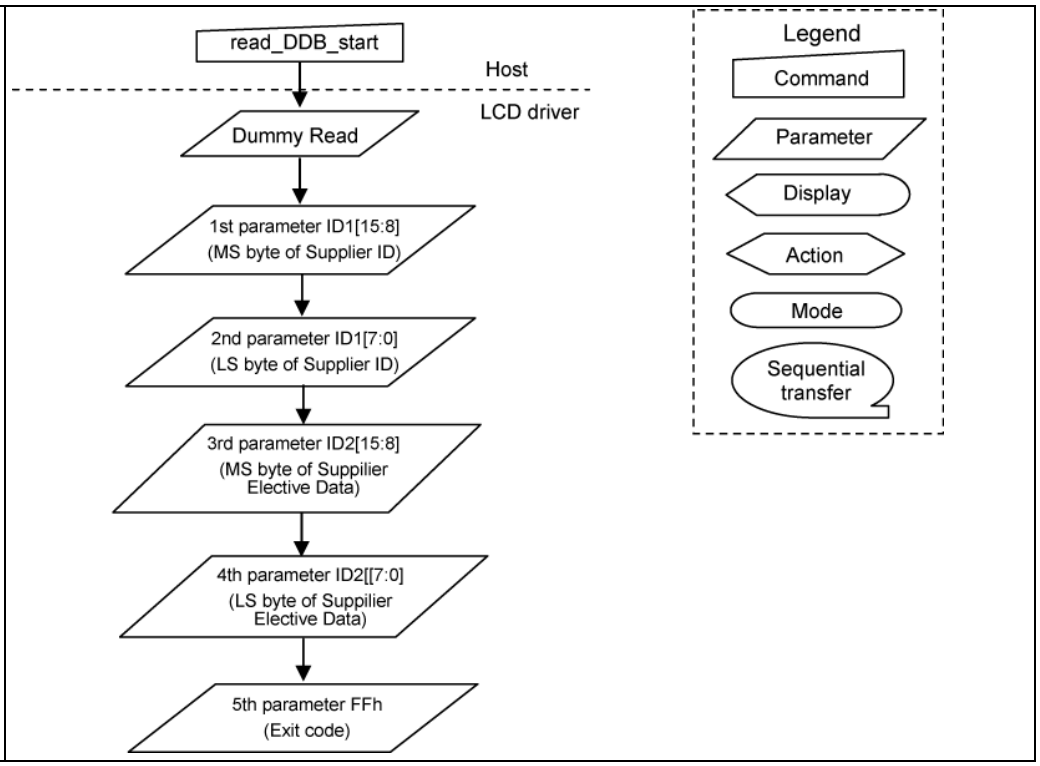
soft_reset: 01h

01H	**soft_reset**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01h
Parameter	None												
Description	The display module performs a software reset. Commands and parameters are written with their SW Reset default values. (See “Default Modes and Values”.) Note: The Frame Memory contents are unaffected by this command. X = Don’t care												
Restriction	If a soft_reset is sent when the display module is in Sleep Mode, the host processor must wait 120 milliseconds before sending an exit_sleep_mode command. soft_reset should not be sent during exit_sleep_mode sequence. No new command setting is allowed until the R61581B0 enters the Sleep Mode. See “State & Command sequence” for sequence to enter Sleep Mode. If a soft_reset is sent when the display module is in Sleep Mode, data in NVM are read. No new command setting is inhibited when data are read (5ms).												
Flow Chart													

read_DDB_start: 04h

04h	read_DDB_start												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	0	1	0	0	04h
Dummy parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	1	↑	1	X	1	1	1	1	1	1	1	1	FFh
Description	The command returns information from the display module as follows: 1st parameter: upper byte (ID1[15:8]) of Supplier ID 2nd parameter: lower byte (ID[7:0]) of Supplier ID 3rd parameter: Supplier Elective Data (ID2[15:8]) 4th parameter: Supplier Elective Data (ID2[7:0]) 5th parameter: Exit Code (FFh) Supplier ID and Supplier Elective Data stored in internal NVM are read. Read values are the same as ones read by read_DDB_start (A1h) command. read_DDB_continue (A8h) command is not affected. X=Don't care												
Restriction	-												

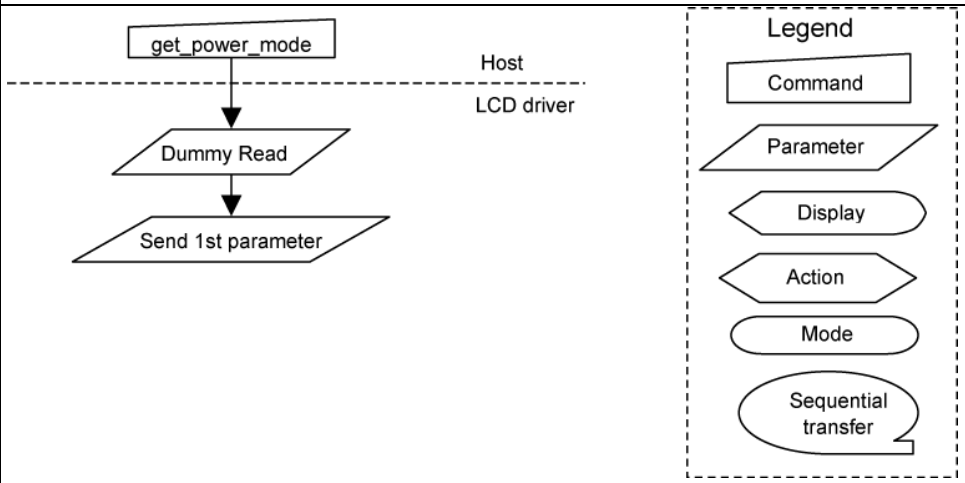
Flow Chart


read_DDB_start
Host
LCD driver
Dummy Read
1st parameter ID1[15:8]
(MS byte of Supplier ID)
2nd parameter ID1[7:0]
(LS byte of Supplier ID)
3rd parameter ID2[15:8]
(MS byte of Suppilier
Elective Data)
4th parameter ID2[[7:0]
(LS byte of Suppilier
Elective Data)
5th parameter FFh
(Exit code)
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

get_power_mode: 0Ah

0Ah	get_power_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	0	1	0	0Ah
1st parameter	1	↑	1	X	0	IDMON	PTLON	SLPOUT	NORON	DSPON	0	0	XXh
Description	The display module returns the current power mode.												

Bit	Description	Comment	Command list Symbol
D7	Reserved	Set to “0”	-
D6	Idle Mode On/Off		IDMON
D5	Partial Mode On/Off		PTLON
D4	Sleep Mode On/Off		SLPOUT
D3	Display Normal Mode On/Off		NORON
D2	Display On/Off		DSPON
D1	Reserved	Set to “0”	-
D0	Reserved	Set to “0”	-

0Ah	**get_power_mode**
	• Bit D7 – Not defined This bit is not applicable. Set to “0”. • Bit D6 – Idle Mode On/Off ‘0’ = Idle Mode Off. ‘1’ = Idle Mode On. • Bit D5 – Partial Mode On/Off ‘0’ = Partial Mode Off. ‘1’ = Partial Mode On. • Bit D4 – Sleep Mode On/Off ‘0’ = Sleep Mode On ‘1’ = Sleep Mode Off • Bit D3 – Display Normal Mode On/Off ‘0’ = Display Normal Mode Off ‘1’ = Display Normal Mode On • Bit D2 – Display On/Off ‘0’ = Display is Off ‘1’ = Display is On • Bit D1 – Not Defined This bit is not applicable. Set to “0”. • Bit D0 – Not Defined This bit is not applicable. Set to “0”. X = Don’t care.
Restriction	-
Flow chart	

get_address_mode: 0Bh

0Bh	get_address_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	0	1	1	0Bh
1st parameter	1	↑	1	X	B7	B6	B5	B4	0	0	0	B0	XXh

Description

The display module returns the current status of the display as described in the table below. This command setting depends on set_address_mode (36h). For B4, B3, and B0, please refer to "Appendix" for each mode.

Bit	Description	Comment	Command list symbol
D7	Page Address Order		B7
D6	Column Address Order		B6
D5	Page/Column Order		B5
D4	Line Address Order		B4
D3	RGB/BGR Order	Set to "0"	
D2	Display Data Latch Order	Set to "0"	
D1	Reserved	Set to "0"	
D0	Switching between Common outputs and Frame Memory		B0

- Bit D7 - Page Address Order

'0' = Top to Bottom (When set_address_mode D7 = '0')
'1' = Bottom to Top (When set_address_mode D7 = '1')

- Bit D6 – Column Address Order

'0' = Left to Right (When set_address_mode D6 = '0')
'1' = Right to Left (When set_address_mode D6 = '1')

- Bit D5 – Page/Column Order

'0' = Normal Mode (When set_address_mode D5 = '0')
'1' = Reverse Mode (When set_address_mode D5 = '1')

Note: See "Host Processor to Memory Write/Read Direction" and "Memory Access Control: 36h" for D7 to D5 bits.

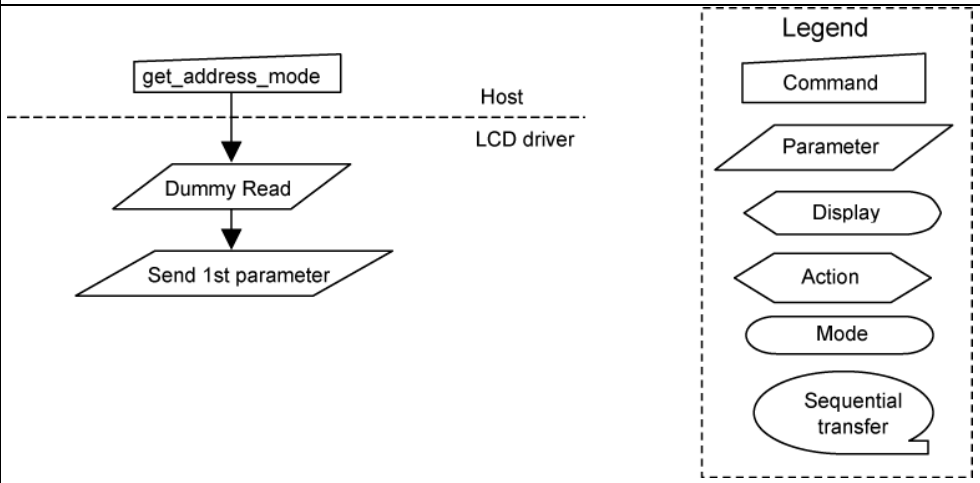
- Bit D4 – Line Address Order

'0' = LCD Refresh Top to Bottom (When set_address_mode D4 = '0')
'1' = LCD Refresh Bottom to Top (When set_address_mode D4 = '1')

Note: See "Memory Access Control (36h)" for D4 bit.

- Bit D3 – RGB/BGR Order

This bit is not applicable. Set to "0" (Not supported).

0Bh	**get_address_mode**
Description	• Bit D2 – Display Data latch Data Order This bit is not applicable. Set to “0” (Not supported). • Bit D1 – Reserved This bit is not applicable. Set to “0” (Not supported). • Bit D0 – Switching between Common outputs and Frame Memory ‘0’ = Reading direction from Frame Memory to Common Outputs is identical with writing direction. ‘1’ = Reading direction from Frame Memory to Common Outputs is reverse of writing direction. X = Don’t care.
Restriction	-
Flow Chart	

Note: See “”State Transition Diagram” for display mode transition.

get_pixel_format: 0Ch

0Ch	get_pixel_format												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	1	0	0	0Ch
1st parameter	1	↑	1	X	0	D6	D5	D4	0	D2	D1	D0	XXh

Description

This command indicates the current status of the display as described in the table below. This command setting depends on set_pixel_format (3Ah).

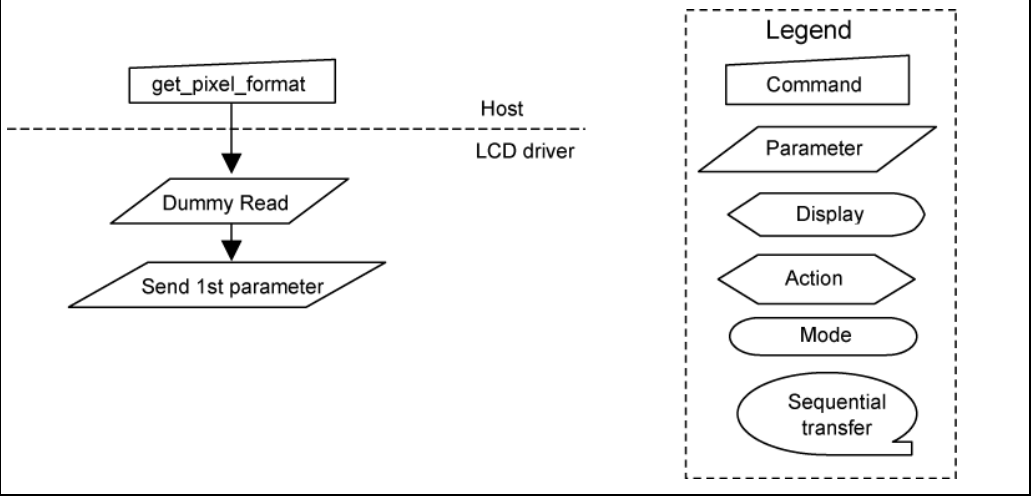
Bit	Description	Comment
D7	DPI Pixel format	Set to "0"
D6	(RGB Interface Color Format)	D6
D5		D5
D4		D4
D3	DBI Pixel Format	Set to "0"
D2	(Control Interface Color Format)	D2
D1		D1
D0		D0

- Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)
- Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection)
- Bit D7 and D3 – These bits are not applicable. So they are set to "0". See description of command set_pixel_format (3Ah).

Control Interface Color Format	D6/D2	D5/D1	D4/D0	
Setting inhibited	0	0	0	-
3 bits/pixel (8 colors)	0	0	1	DBI Type C
Setting inhibited	0	1	0	-
Setting inhibited	0	1	1	-
Setting inhibited	1	0	0	-
16 bits/pixel (65,536 colors)	1	0	1	DBI Type B (16/8 bits)
18 bits/pixel (262,144 colors)	1	1	0	DBI Type B DBI Type C
24 bits/pixel (16,777,216 colors)	1	1	1	DBI Type B (16/8 bits) DBI Type C

Note: When the Setting inhibited bits are set, undesirable image will be displayed on the panel.

x = Don't care.

0Ch	get_pixel_format
	

get_display_mode: 0Dh

0Dh	get_display_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	1	0	1	0Dh
1st parameter	1	↑	1	X	VSSON	0	DSPINVON	0	0	0	0	0	XXh

Description

The display module returns the current status of the display as described in the table below.

Bit	Description	Comment	Command list symbol
D7	Vertical Scrolling Status		VSSON
D6	Reserved	Set to “0”	
D5	Inversion ON/OFF		DSPINVON
D4	Reserved	Set to “0”	
D3	Reserved	Set to “0”	
D2	Gamma Curve Selection	Set to “0”	
D1	Gamma Curve Selection	Set to “0”	
D0	Gamma Curve Selection	Set to “0”	

- Bit D7 – Vertical Scrolling status

  ‘0’ = Vertical scrolling is Off.
  ‘1’ = Vertical Scrolling is On.

- Bit D6 – Reserved

  This bit is not applicable. Set to “0”.

- Bit D5 – Inversion On/Off

  ‘0’ = Inversion is Off.
  ‘1’ = Inversion is On.

- Bit D4, D3 – Reserved

  These bits are not applicable. Set to “0”.

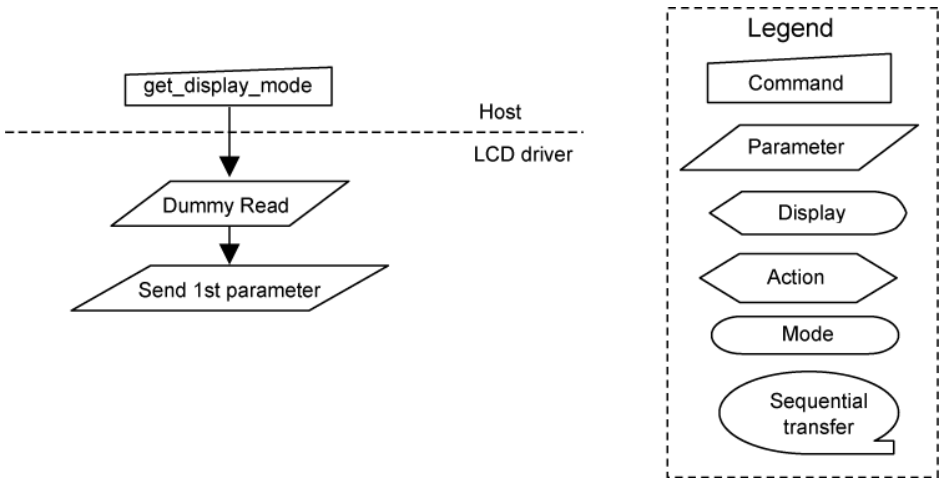
- Bit D2, D1, D0 – Gamma Curve Selection

  These bits are not applicable. Set to “0”.

X = Don’t care

Restriction

-

0Dh	get_display_mode
Flow Chart	

get_signal_mode: 0Eh

0Eh	**get_signal_mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	1	1	0	0Eh
1st parameter	1	↑	1	X	TEON	TELOM	0	0	0	0	0	0	XXh

Description

The display module returns the Display Signal Mode as described in the table below.

Bit	**Description**	**Comment**	**Command list symbol**
D7	Tearing Effect line ON/OFF		TEON
D6	Tearing Effect line Output Mode		TELOM
D5	Reserved	Set to “0”	-
D4	Reserved	Set to “0”	-
D3	Reserved	Set to “0”	-
D2	Reserved	Set to “0”	-
D1	Reserved	Set to “0”	-
D0	Reserved	Set to “0”	-

- Bit D7 – Tearing Effect Line On/Off

  ‘0’ = Tearing Effect Line Off
  ‘1’ = Tearing Effect On

- Bit D6 – Tearing Effect Line Output Mode (See “set_tear_on: 35h”).

  ‘0’ = Mode1
  ‘1’ = Mode2

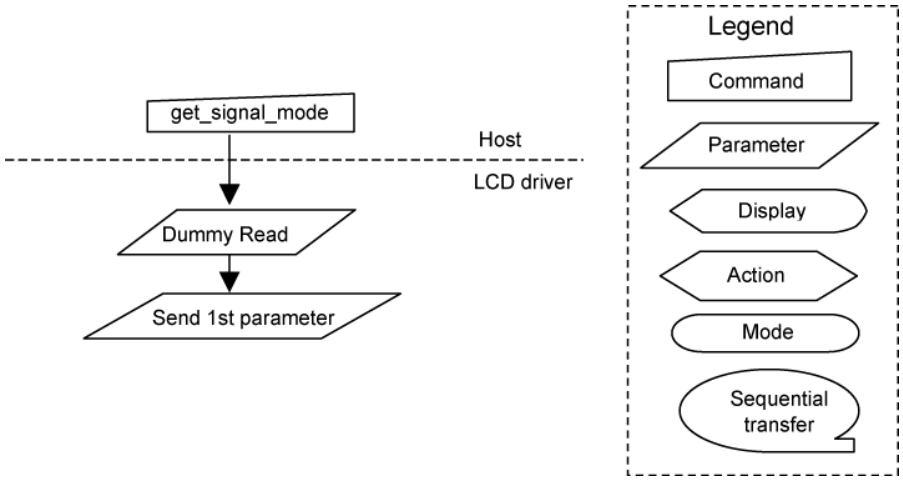
- Bit D5-D0 – Reserved

  These bits are not applicable. Set to “0”.

X = Don’t care

Restriction

-

0Eh	get_signal_mode
Flow Chart	

get_diagnostic_result:0Fh

0Fh	get_diagnostic_result												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	0	1	1	1	1	0Fh
1st Parameter	0	↑	1	X	0	FUN CD	0	0	0	0	0	0	XXh

Description

Bit	Description	Comment	Command List Symbol
D7	Register Loading Detection	Set to 0	
D6	Functionality Detection		FUNCD
D5	Chip Attachment Detection	Set to 0	-
D4	Display Glass Break Detection	Set to 0	-
D3	Reserved	Set to 0	-
D2	Reserved	Set to 0	-
D1	Reserved	Set to 0	-
D0	Reserved	Set to 0	-

The display module returns the self-diagnostic results following the exit_sleep_mode (11h) as shown in the table above.

- Bit D7 – Register Loading Detection

This bit is not applicable. Set to “0”.

- Bit D6 – Functionality Detection

Note: See Self-Diagnostic Function for D6.

- Bit D5 – Chip Attachment Detection

This bit is not applicable. Set to “0”.

- Bit D4 –Display Glass Break Detection

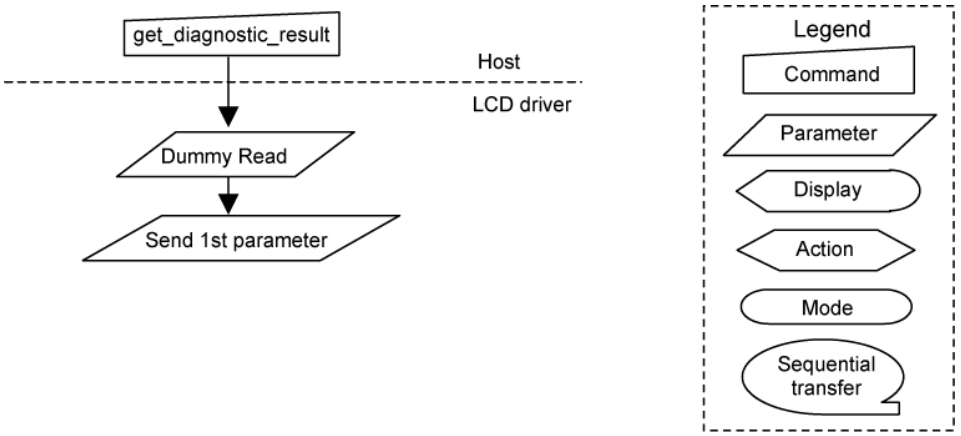
This bit is not applicable. Set to “0”.

- Bit D3, D2, D1, D0 – Reserved

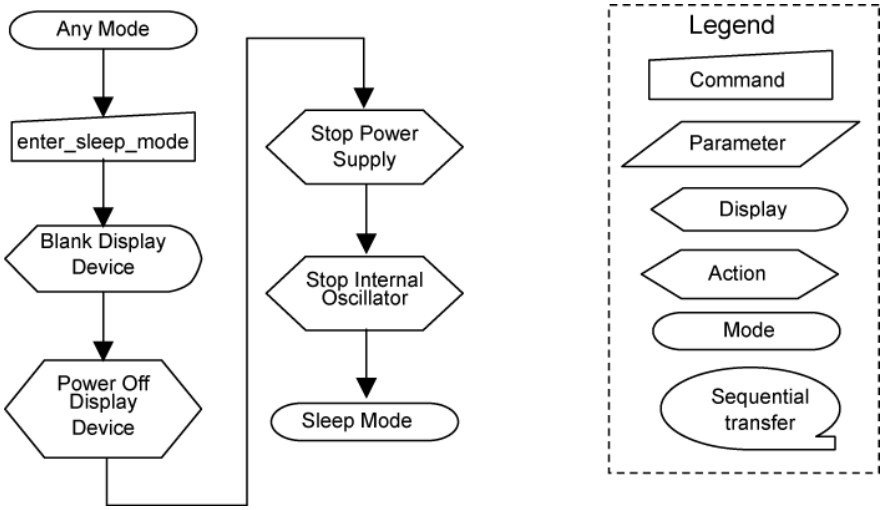
Set to 0.

X = Don’t care

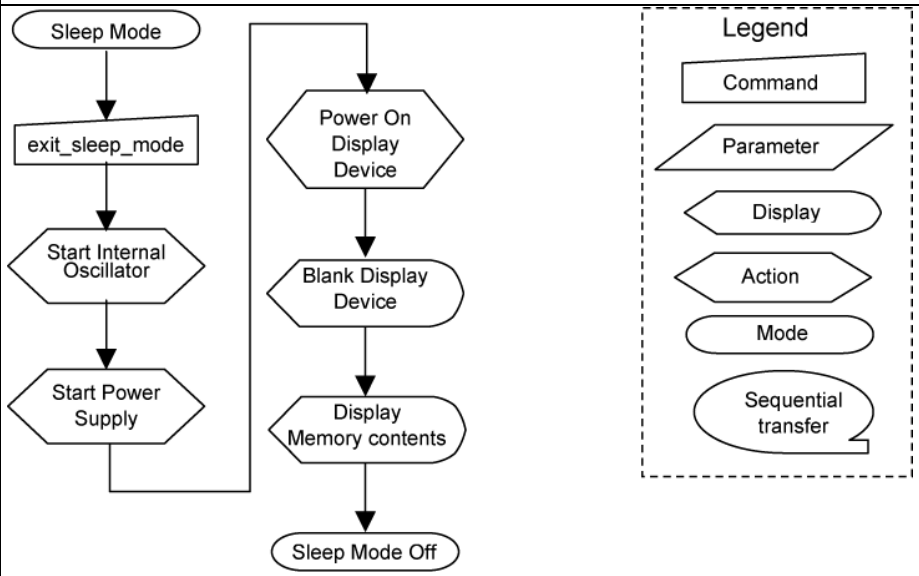
Restriction: -

0Fh	get_diagnostic_result
Flow Chart	

enter_sleep_mode: 10h

10h	enter_sleep_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	1	0	0	0	0	10h
Parameter	None												
Description	This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. See “State & Command sequence” for Sleep In sequence. DBI remains operational and the memory maintains its contents. See State Transition Diagram for each stage of transition. X = Don’t care												
Restriction	This command has no effect when the module is already in Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted. Sending a new command is prohibited while the R61581B0 performs either power supply OFF sequencer or blank scan.												
Flow Chart													

exit_sleep_mode: 11h

11h	exit_sleep_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	1	0	0	0	1	11h
Parameter	None												
Description	This command causes the display module to exit Sleep mode. DC/DC converter, internal oscillation and panel scanning start. See “State & Command sequence” for exit_sleep_mode. See State Transition Diagram for each stage of transition. X = Don’t care												
Restriction	This command shall not cause any visual effect on display device when the display module is not in Sleep mode. No new command setting is allowed during power supply ON sequence. Operation may continue for more than 120msec due to power supply ON sequence setting. Do not send any command also in this case. The host processor must wait 120 milliseconds after sending an enter_sleep_mode command before sending an exit_sleep_mode command. The display runs the self-diagnostic function after this command is received. When exit_sleep command is sent, data is read from NVM. No new command setting is allowed while data is being read (5ms).												
Flow Chart													

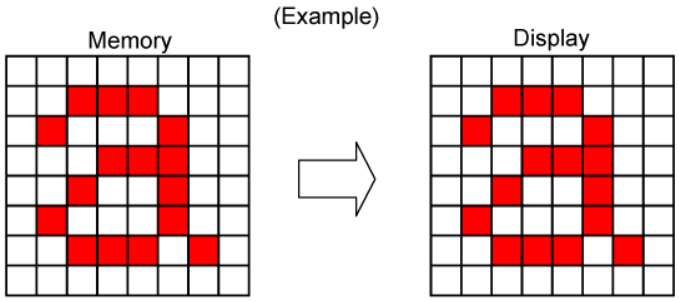
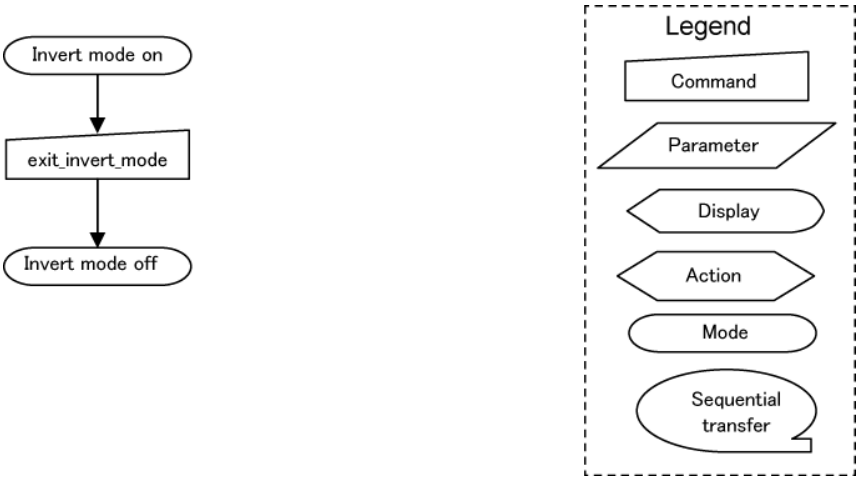
enter_partial_mode: 12h

12h	enter_partial_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12h
Parameter	None												
Description	This command causes the display module to enter the Partial mode. The Partial mode window is described by the set_partial_area command (30h). To leave Partial mode, the enter_normal_mode (13h) should be written. X = Don't care Note: When a command breaks in the middle of frame period in Normal mode, the command is enabled from the next frame period.												
Restriction	This command has no effect when the module is already in Partial mode.												
Flow Chart	See "set_partial_area: 30h".												

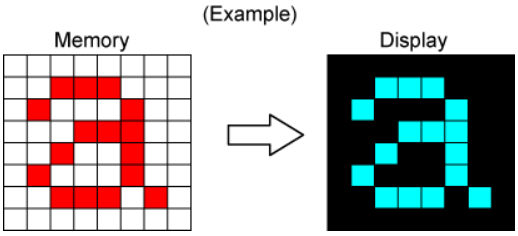
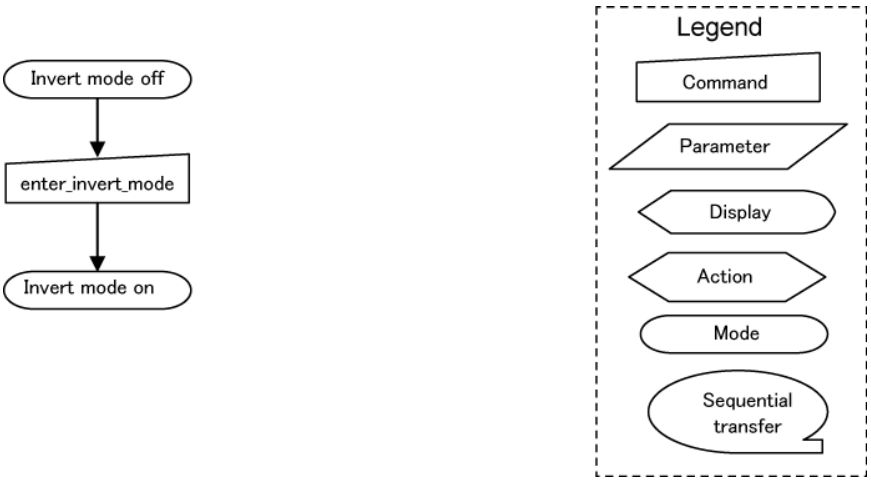
enter_normal_mode: 13h

13h	enter_normal_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	0	1	0	0	1	1	13h
Parameter	None												
Description	This command causes the display module to enter the Normal mode. Normal mode means Partial mode is off. X = Don't care Note: When a command breaks in the middle of frame period in Partial Mode, that command becomes valid from the next frame period.												
Restriction	This command has no effect when Normal mode is already active.												
Flow Chart	See the descriptions of commands set_partial_area (30h) when using this command.												

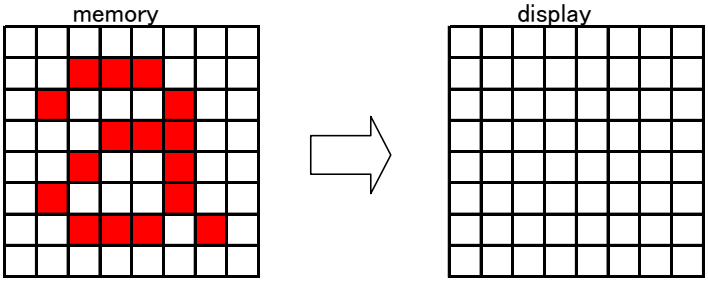
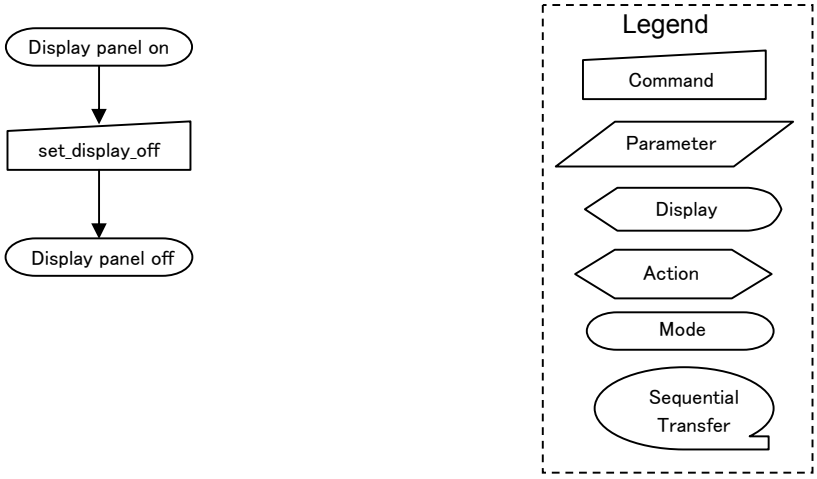
exit_invert_mode: 20h

20h	exit_invert_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	0	0	0	0	20h
Parameter	None												
Description	This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.  X = Don't care												
Restriction	This command has no effect when the module is already in Inversion is off.												
Flow Chart	 												

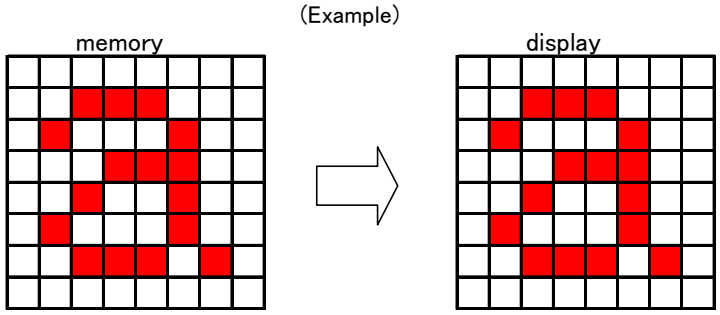
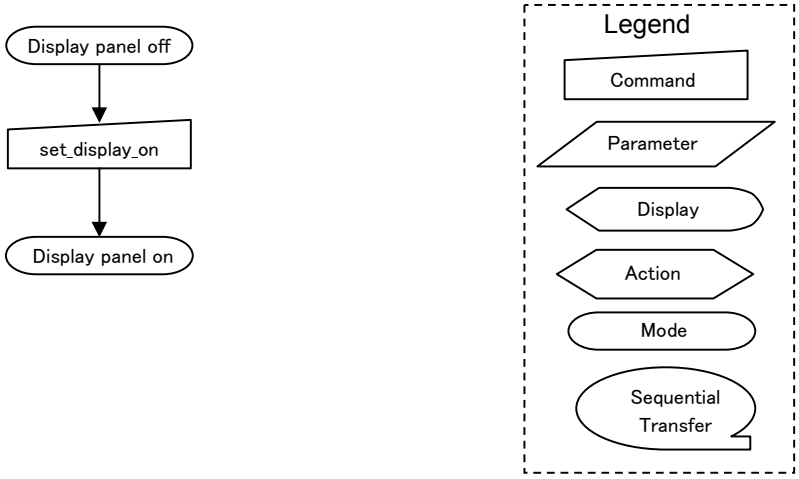
enter_invert_mode: 21h

21h	enter_invert_mode												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	0	0	0	1	21h
Parameter	None												
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. All bits send from the frame memory to the display invert. No status bits are changed.  X = Don't care												
Restriction	This command has no effect when the display module is already inverting the display image.												
Flow Chart	 												

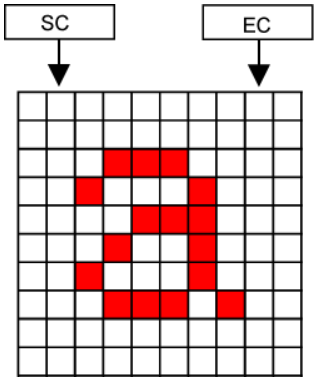
set_display_off: 28h

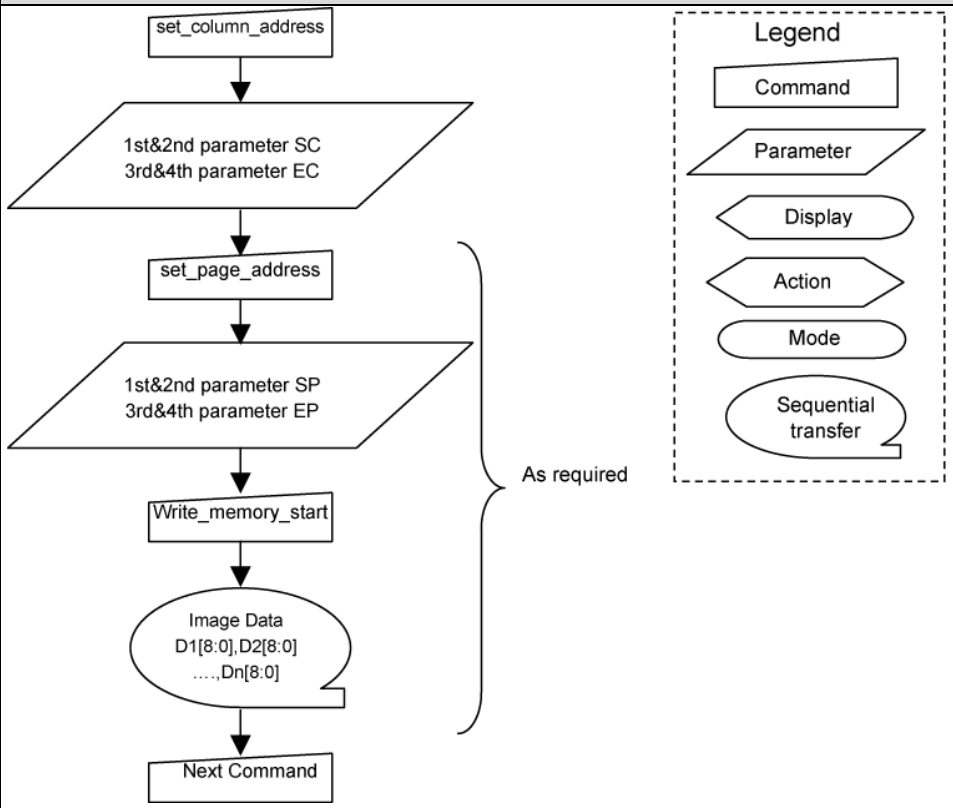
28h	set_display_off												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	0	0	0	28h
Parameter	None												
Description	This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example)  For DISPOFF mode selection, see “Panel Driving Setting: C0h”. X = Don’t care												
Restriction	This command has no effect when the display panel is already off.												
Flow Chart	 												

set_display_on: 29h

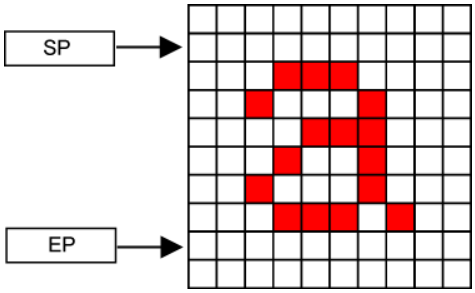
29h	set_display_on												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	0	1	0	0	1	29h
Parameter	None												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.  X = Don't care												
Restriction	This command has no effect when the display panel is already on.												
Flow Chart	 												

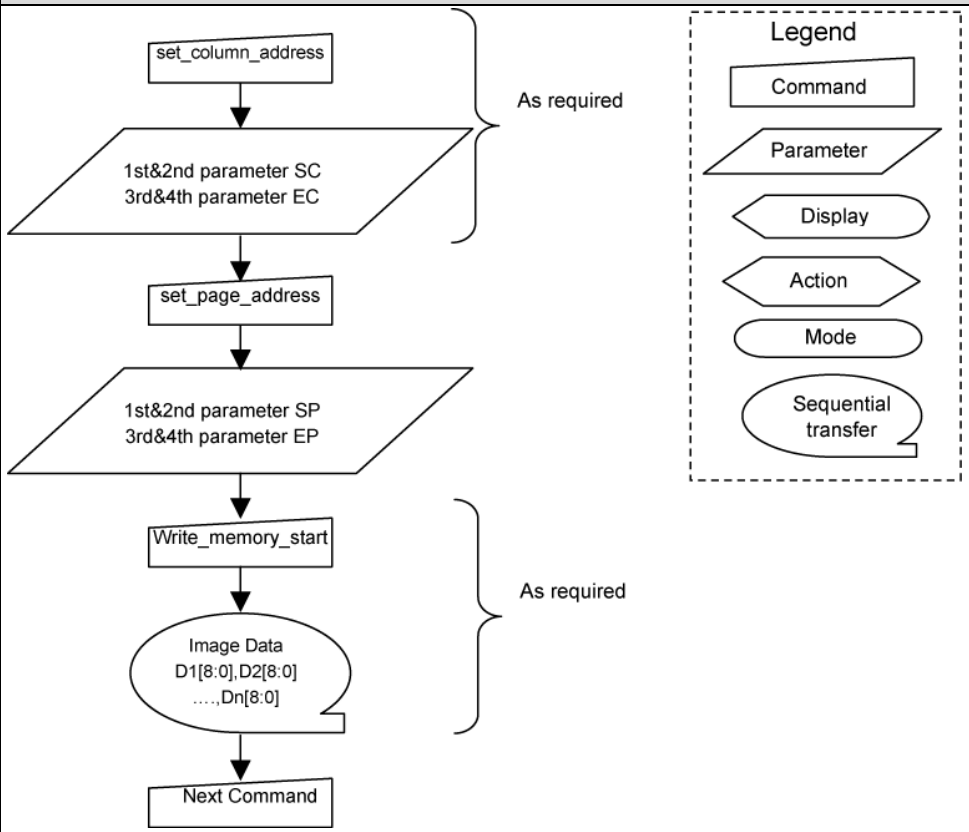
set_column_address: 2Ah

2Ah	**set_column_address**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	0	1	0	2Ah
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	SC[8]	XXh
2nd parameter	1	1	↑	X	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	XXh
3rd parameter	1	1	↑	X	0	0	0	0	0	0	0	EC[8]	XXh
4th parameter	1	1	↑	X	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	XXh
Description	This command defines the column extent of the frame memory accessed by the host processor. The values of SC[8:0] and EC[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed. Example  X=Don't care.												
Restriction	SC [8:0] must be equal to or less than EC[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SC[8:0] or EC[8:0] > 1DFh • If set_address_mode B5 = 1: SC[8:0] or EC[8:0] > 13Fh												

2Ah	**set_column_address**
Flow Chart	

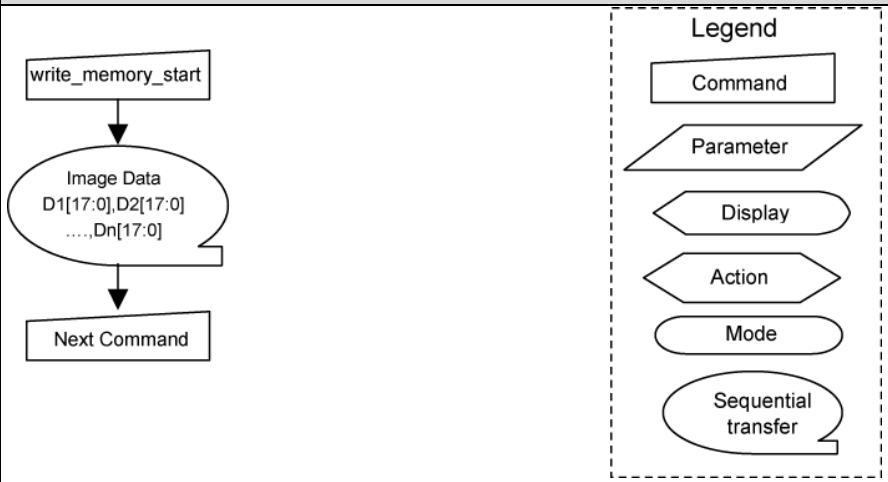
set_page_address: 2Bh

2Bh	**set_page_address**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	0	1	1	2Bh
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	SP[8]	XXh
2nd parameter	1	1	↑	X	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	XXh
3rd parameter	1	1	↑	X	0	0	0	0	0	0	0	EP[8]	XXh
4th parameter	1	1	↑	X	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	XXh
Description	This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed. The values of SP[8:0] and EP[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. Example  X = Don't care												
Restriction	SP[8:0] must always be equal to or less than EP[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance. Note: The parameters are disregarded in following cases. • If set_address_mode B5 = 0: SP[8:0] or EP[8:0] > 1DFh • If set_address_mode B5 = 1: SP[8:0] or EP[8:0] > 0EFh												

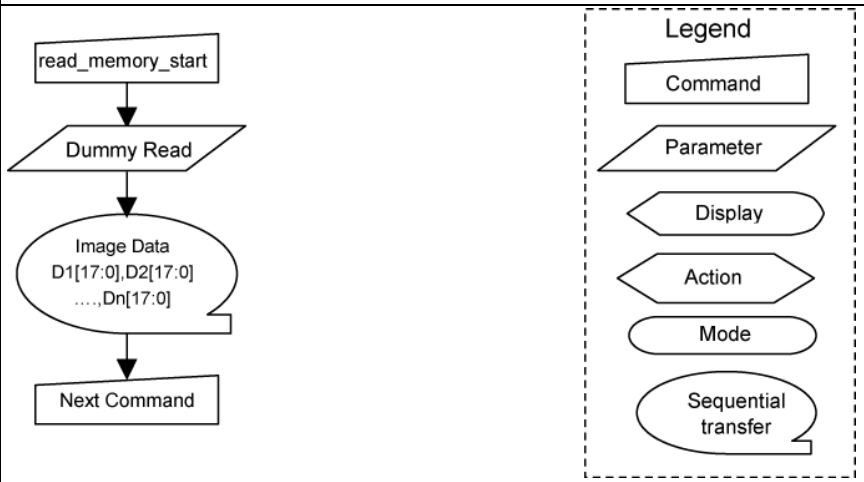
2Bh	**set_page_address**
Flow Chart	

write_memory_start: 2Ch

2Ch	write_memory_start												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	1	0	0	2Ch
1st pixel data	1	1	↑	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
: :	1	1	↑	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth pixel data	1	1	↑	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data 1 is stored in frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If Frame Memory Access and Interface setting (B3h) WEMODE = 0: If the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. If Frame Memory Access and Interface setting (B3h) WEMODE = 1 When the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are set to the Start Column and Start Page respectively. Then subsequent data are written to the frame memory. Sending any other command will stop writing to the frame memory. See "DBI Data Format" and "DPI Data Format" for write data formats in DBI Type B 18-/16-/9-/8-bit bus interface, Type C serial interface, and DPI. X=Don't care.												
Restriction	In all color modes, there are no restrictions on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.												

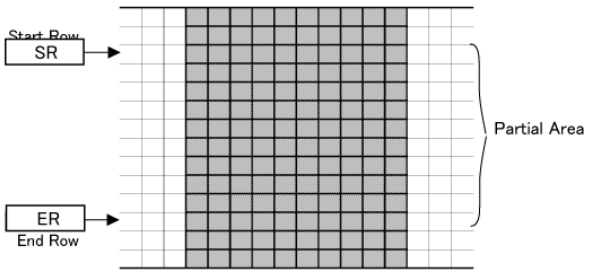
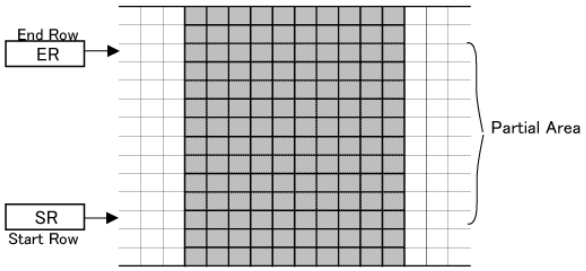
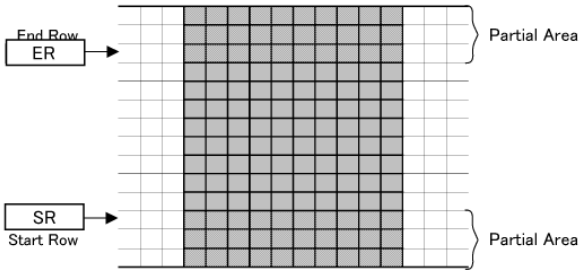
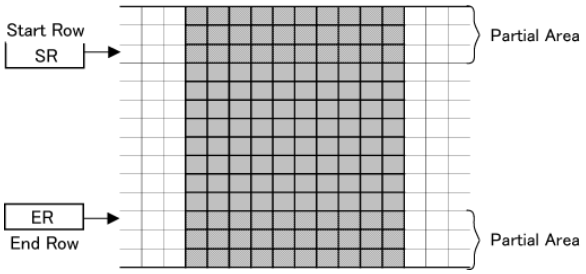
2Ch	write_memory_start
Flow Chart	

read_memory_start: 2Eh

2Eh	read_memory_start												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	0	1	1	1	0	2Eh
1st pixel data	1	↑	1	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
:	1	↑	1	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth pixel data	1	↑	1	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the frame memory to the host processor. No status bits are changed. If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively. After pixel data I are read from the frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction". If read operation continued after (EP, EC) data are read, the last data (EP, EC) continue to be read. Any other written command stops frame memory read. See "DBI Data Format" and "DPI Data Format" for write data formats in DBI Type B 18-/16-/9-/8-bit bus interface, Type C serial interface, and DPI. X = Don't care.												
Restriction	In all color modes, the Frame read is always 24 bits so there is no restriction on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.												
Flow Chart													

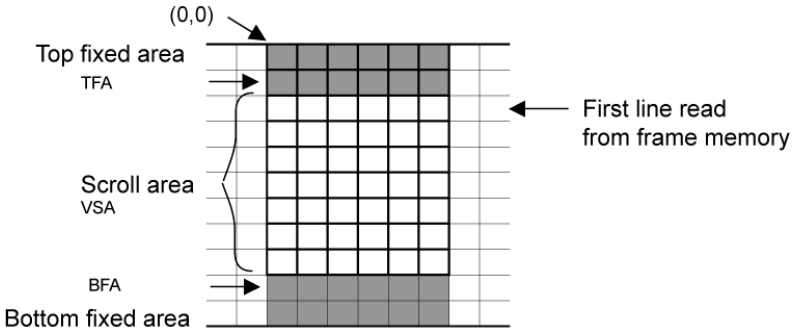
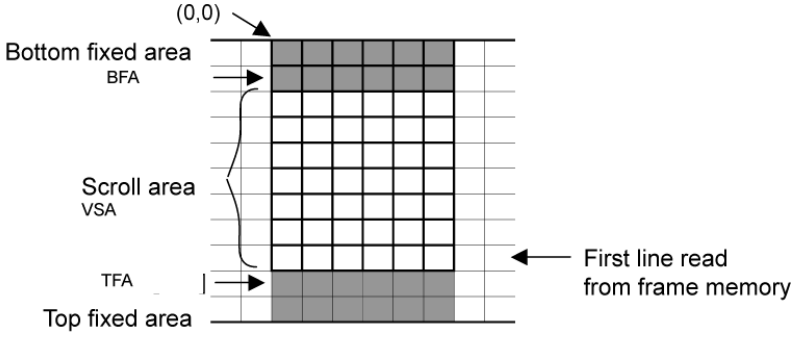
set_partial_area: 30h

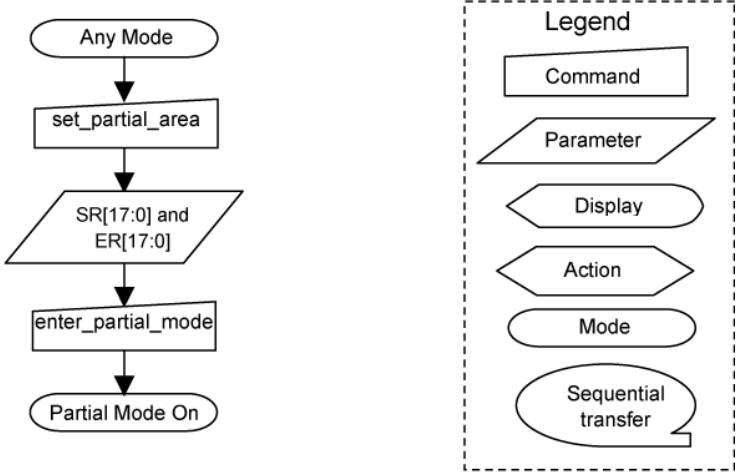
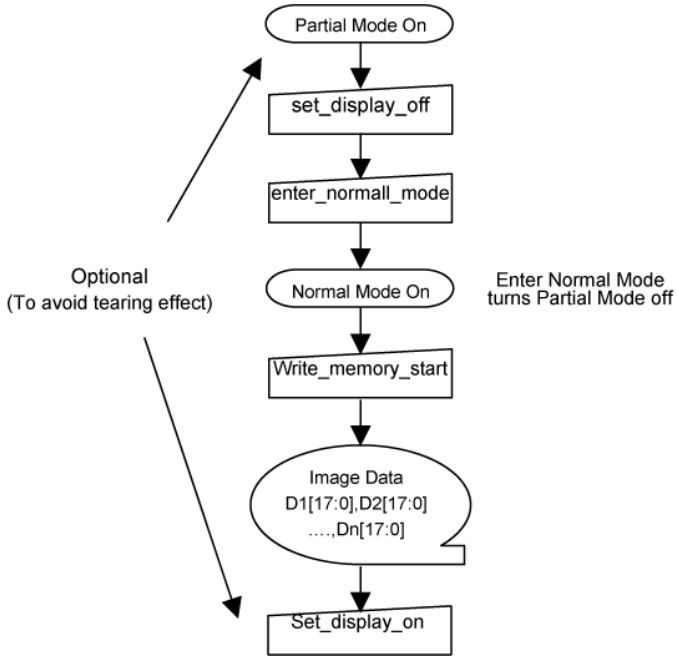
30h	set_partial_area												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	0	0	0	0	30h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	SR[8]	000h … 1AFh
2nd parameter	1	1	↑	X	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	
3rd parameter	1	1	↑	X	0	0	0	0	0	0	0	ER[8]	000h … 1AFh
4th parameter	1	1	↑	X	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	

30h	**set_partial_area**
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. End Row > Start Row (set_address_mode(36h) B4=0)  End Row > Start Row(set_address_mode(36h) B4=1)  End Row < Start Row (set_address_mode(36h) B4=0)  End Row < Start Row (set_address_mode(36h) B4=1)  If End Row = Start Row, the partial area will be one row deep. X = Don't care.
Restriction	-

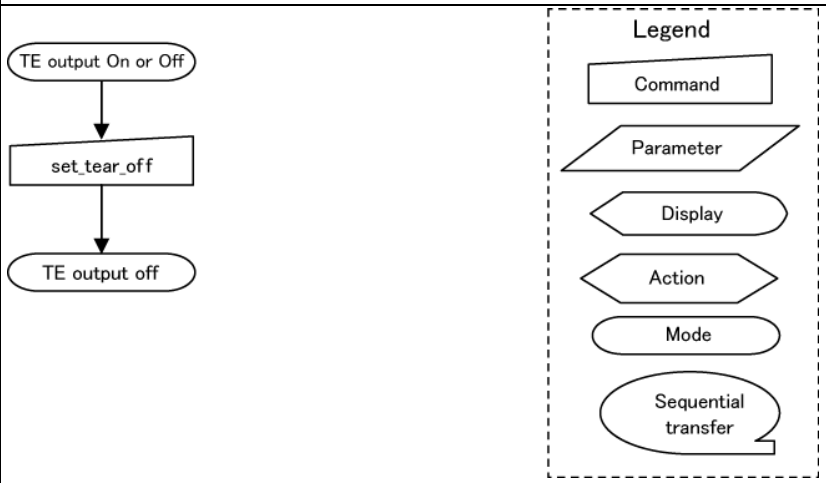
set_scroll_area: 33h

33h	set_scroll_area												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	0	0	1	1	33h
1st parameter	1	1	↑	X	0	0	0	0	0	0	0	TFA [8]	000h … 140h
2nd parameter	1	1	↑	X	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA [3]	TFA [2]	TFA [1]	TFA [0]	
3rd parameter	1	1	↑	X	0	0	0	0	0	0	0	VSA [8]	000h … 140h
4th parameter	1	1	↑	X	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	
5th parameter	1	1	↑	X	0	0	0	0	0	0	0	BFA [8]	000h … 140h
6th parameter	1	1	↑	X	BFA [7]	BFA [6]	BFA [5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	

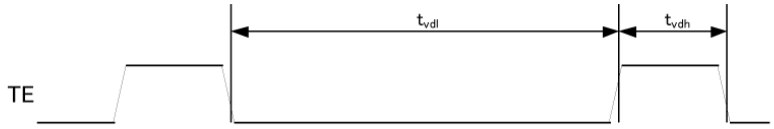
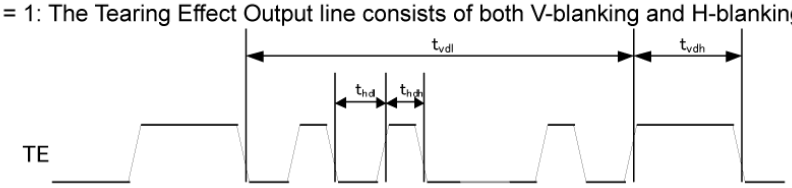
33h	**set_scroll_area**
Description	This command defines the display module's Vertical Scrolling Area. If set_address_mode (36h) B4 = 0: The 1st and 2nd parameters TFA[8:0] describe the Top Fixed Area in number of lines from the top of the frame memory. The 3rd and 4th parameters VSA[8:0] describe the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of Vertical Scrolling Area starts immediately after the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately the top most line of the Bottom Fixed Area. The 5th and 6th parameters BFA[8:0] describe the Bottom Fixed Area in number of lines from the top of the frame memory. Set the number of lines from the bottom of the frame memory. TFA, VSA and BFA refer to the frame memory line pointer.  If set_address_mode (36h) B4 = 1: The 1st and 2nd parameters TFA[8:0] describe the Top Fixed Area in number of lines from the bottom of the frame memory. The 3rd and 4th parameters VSA[8:0] describe the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of Vertical Scrolling Area starts immediately after the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately the top most line of the Bottom Fixed Area. The 5th and 6th parameters BFA[8:0] describe the Bottom Fixed Area in number of lines from the top of the frame memory. Set the number of lines from the bottom of the frame memory. TFA, VSA and BFA refer to the frame memory line pointer.  TFA, VSA and BFA refer to the frame memory line pointer.

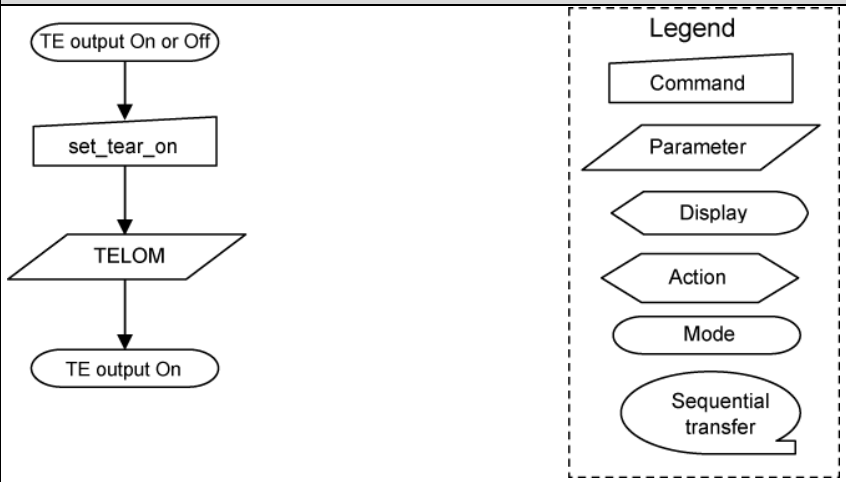
33h	**set_scroll_area**
Restriction	The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages). (max. 480 lines) In Vertical Scroll Mode, set_address_mode B5 should be set to '0' and this only affects the Frame Memory Write.
Flow Chart	1. To enter Partial mode  2. To exit Partial mode 

set_tear_off: 34h

34h	**set_tear_off**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	0	1	0	0	34h
Parameter	None												
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already off.												
Flow Chart													

set_tear_on: 35h

35h	**set_tear_on**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	0	1	0	1	35h
1st parameter	1	1	↑	X	X	X	X	X	X	X	X	TELOM	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Refresh order). The Tearing Effect Line On has one parameter, TELON that describes the Tearing Effect Output Line mode. See TE Pin Output Signal for detail. TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only. The Tearing Effect Output line shall be high during vertical blanking period.  TELOM = 1: The Tearing Effect Output line consists of both V-blanking and H-blanking information.  **tvdl** **Number of lines set by NL** **tvdh** **Number of lines set by BP + Number of lines set by FP** **thdl** **3 clocks (based on internal operation clock)** **thdh** **Number of clocks set by RTN – 3 clocks (based on internal operation clock)** Note: The Tearing Effect Output line shall be active low when the display module is in Sleep mode. X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already ON. Changes in parameter TELOM is enabled from the next frame period.												

35h	set_tear_on
Flow Chart	

set_address_mode: 36h

36h	**set_address_mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	0	0	0	1	1	0	1	1	0	36h
1st parameter	1	1	↑	X	B7	B6	B5	B4	0	0	0	B0	XXh

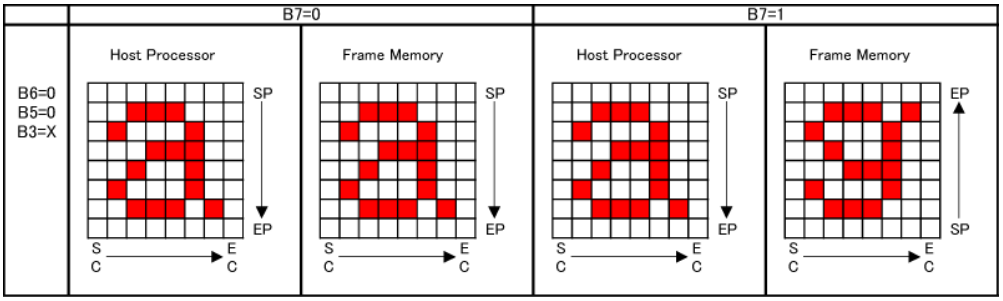
Description

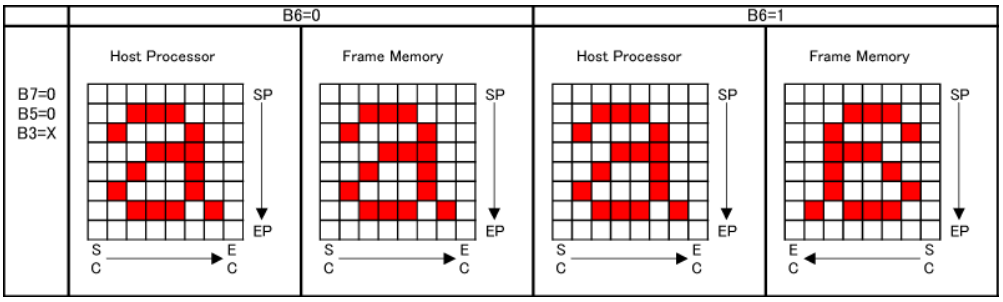
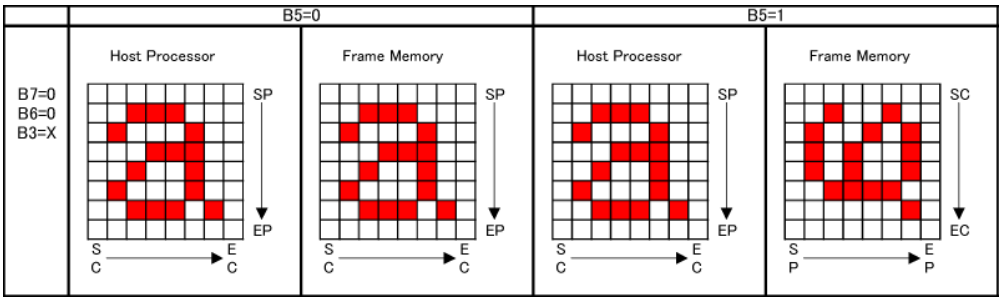
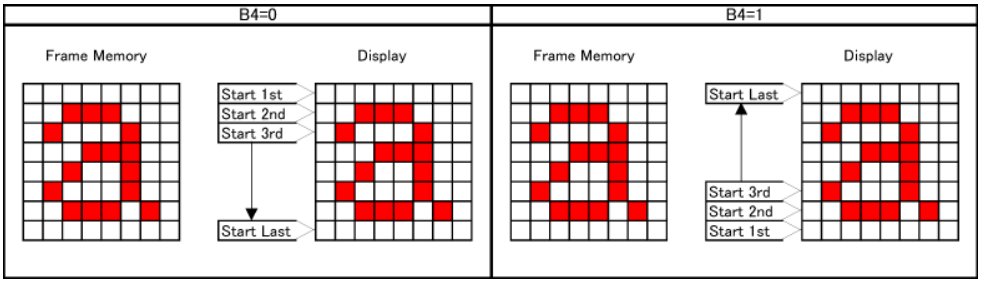
This command sets read/write scanning direction of frame memory. No status bits are changed.

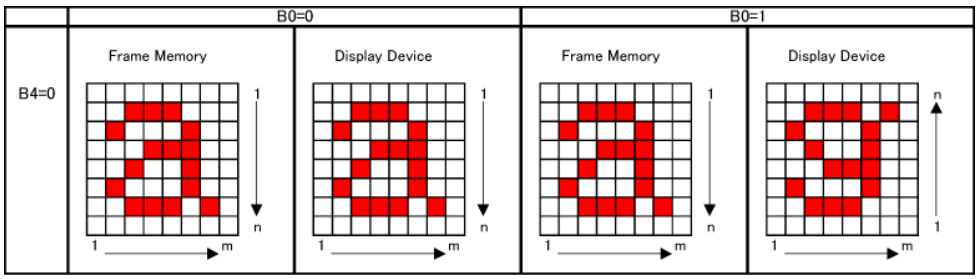
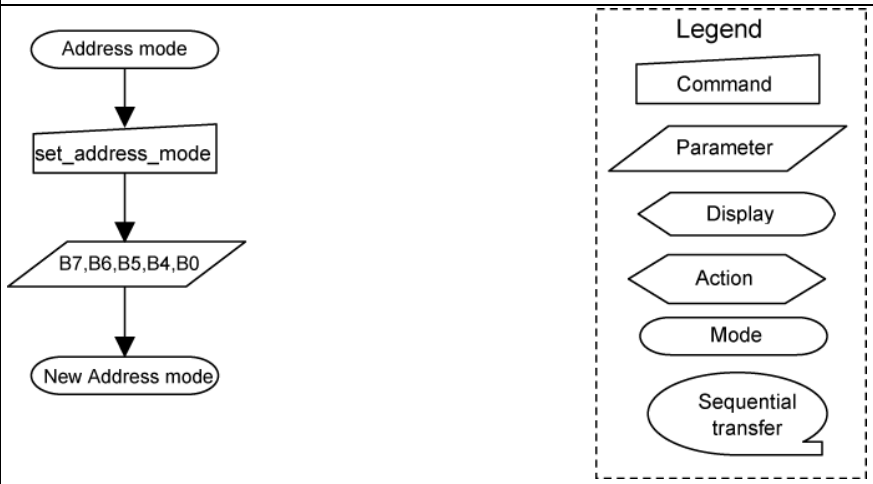
Bit	**Description**	**Comment**	**Symbol**
D7	Page Address Order		B7
D6	Column Address Order		B6
D5	Page/Column Addressing Order		B5
D4	Display Device Line Refresh Order		B4
D3	RGB/BGR Order	Don't care	-
D2	Display Data Latch Data Order	Don't care	-
D1	Flip Horizontal	Don't care	-
D0	Flip Vertical		B0

- Bit B7 - Page Address Order

'0' = Top to Bottom
'1' = Bottom to Top

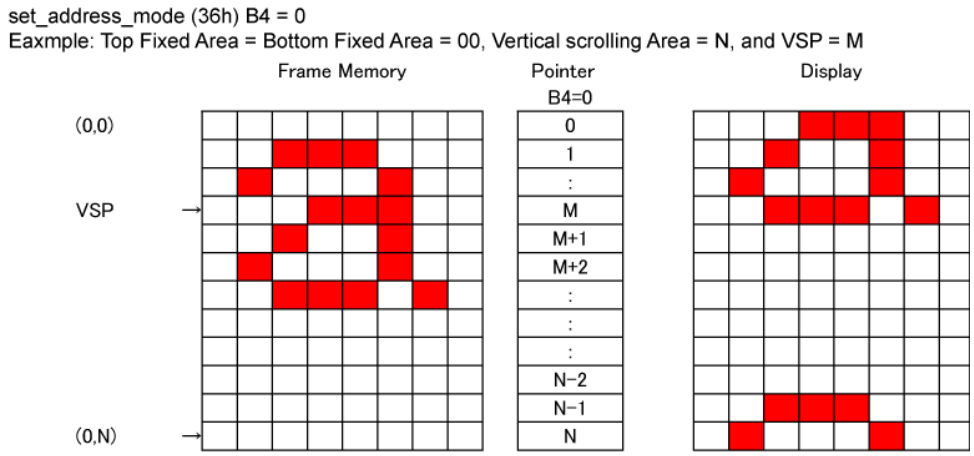
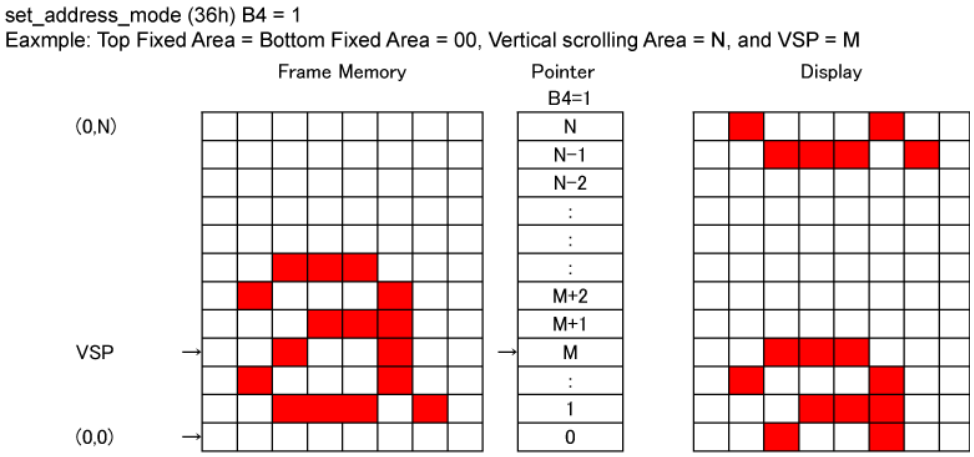


36h	**set_address_mode**
Description	• Bit B6 - Column Address Order '0' = Left to Right '1' = Right to Left  • Bit B5 – Page/Column Addressing Order '0' = Normal Mode '1' = Reverse Mode  For bits B7 to B5, see "Frame Memory." • Bit B4 – Display Device Line Refresh Order '0' = LCD Refresh Top to Bottom '1' = LCD Refresh Bottom to Top (Memory reading and gate scanning directions invert simultaneously.) 

36h	**set_address_mode**
Description	• Bit B3 – RGB/BGR order This bit is not applicable. Set to “0”. (not supported) • Bit B2 – Display Data Latch Data Order This bit is not applicable. Set to “0”. (not supported) • Bit B1 – Flip Horizontal This bit is not applicable. Set to “0”. (not supported) • Bit B0 – Flip Vertical ‘0’ = Normal ‘1’ = Flipped (Gate scanning direction inverts.)  X = Don’t care
Restriction	-
Flow Chart	

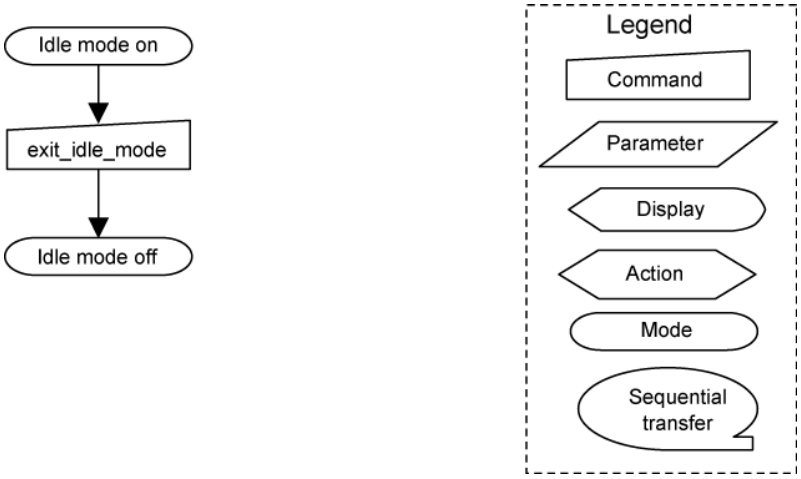
set_scroll_start: 37h

37h	set_scroll_start												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37h
1st parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP [8]	000h … 13Fh
2nd parameter	1	1	↑	x	VSP [7]	VSP [6]	VSP [5]	VSP [4]	VSP [3]	VSP [2]	VSP [1]	VSP [0]	

37h	**set_scroll_start**
Description	This command is used together with set_scroll_area (33h). The set_scroll_start command has one parameter, VSP (Vertical Scroll Pointer). VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area as illustrated below:   Note: When a new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect. X = Don't care

Restriction	Since the value of the Vertical Scrolling Pointer is absolute with reference to the Frame Memory, it must not enter the fixed area (defined by set_scroll_area (33h)). Otherwise, an undesirable image will be displayed on the panel although the command will be accepted.
Flow Chart	See set_scroll_area (33h) description.

exit_idle_mode: 38h

38h	**exit_idle_mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	0	0	0	38h
Parameter	None												
Description	This command causes the display module to exit Idle mode. LCD can display up to maximum 262,144 colors. If the operation of the R61581B0 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cycle can be adjusted for every display mode (Normal, Partial, Normal + Idle, Partial + Idle modes). See description of the manufacturer commands C1h-C3h's 1st to 3rd parameters for detail. If the operation of the R61581B0 is in synchronization with internal oscillation clock (DM=0), the current in amplifier and step-up clock cycle can be adjusted for different display modes (Normal, Partial, Normal + Idle, Partial + Idle modes). See description of the manufacturer commands D2-D4h's 1st and 2nd parameters for detail. X = Don't care												
Restriction	This command has no effect when the display module is not in Idle mode.												
Flow Chart													

enter_idle_mode: 39h

39h	**enter_idle_mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	0	0	1	39h
Parameter	None												

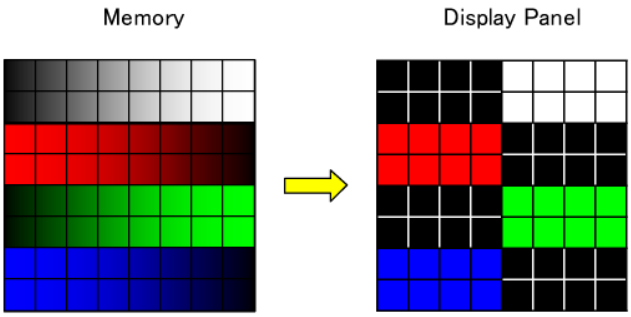
Description

This command causes the display module to enter Idle mode. In Idle mode, color expression is reduced. Eight color depth data are displayed using MSB of each R, G and B color components in the Frame Memory. In this mode, only grayscale levels V0 and V63 are used and power supplies for other levels V1-V62 are halted, reducing power consumption.

If the operation of the R61581B0 is in synchronization with internal oscillation clock (DM=0), the frame rate and liquid crystal alternating cycle can be adjusted for every display mode (Normal/Partial, and Idle (Normal/Partial) modes). See description of the manufacturer commands C1h-C3h's 1st - 3rd parameters for detail.

Also, the current in amplifier and step-up clock cycle can be adjusted for different display modes (Normal/Partial, and Idle (Normal/Partial) modes). See description of the manufacturer commands D2-D4h's 1st and 2nd parameters for detail.

It is possible to reduce power consumption by optimizing settings for Idle Mode.

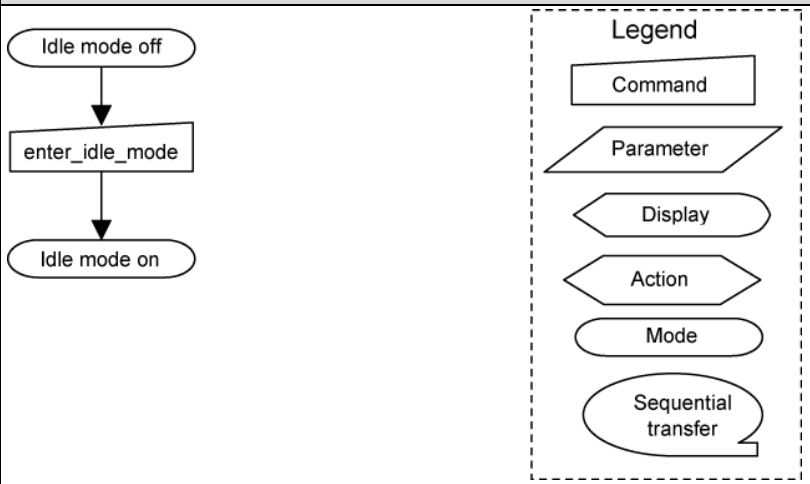


Memory Contents vs. Display Color			
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	0 X X X X X	0 X X X X X	0 X X X X X
Blue	0 X X X X X	0 X X X X X	0 X X X X X
Red	1 X X X X X	1 X X X X X	1 X X X X X
Magenta	1 X X X X X	1 X X X X X	1 X X X X X
Green	0 X X X X X	0 X X X X X	0 X X X X X
Cyan	0 X X X X X	0 X X X X X	0 X X X X X
Yellow	1 X X X X X	1 X X X X X	1 X X X X X
White	1 X X X X X	1 X X X X X	1 X X X X X

X = Don't care

Restriction

This command has no effect when module is already in Idle mode.

39h	enter_idle_mode
Flow Chart	

set_pixel_format: 3Ah

3Ah	set_pixel_format												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	0	1	0	3Ah
1st parameter	1	1	↑	X	0	D6	D5	D4	0	D2	D1	D0	XXh

Description

This command is used to define the format of RGB picture data, which are to be transferred via the DBI/DPI. The formats are shown in the following table:

Bit D[6:4] – DPI Pixel Format (RGB Interface Color Format Selection)

Bit D[2:0] – DBI Pixel Format (Control Interface Color Format Selection)

Bit D7 and D3 – These bits are not applicable. Set to “0”.

Control Interface Color Format	D6/D2	D5/D1	D4/D0	
Setting inhibited	0	0	0	-
3 bits/pixel (8 colors)	0	0	1	DBI Type C
Setting inhibited	0	1	0	-
Setting inhibited	0	1	1	-
Setting inhibited	1	0	0	-
16 bits/pixel (65,536 colors)	1	0	1	DBI Type B (16 bits/8 bitis)
18 bits/pixel (262,144 colors)	1	1	0	DBI Type B DBI Type C
24 bits/pixel (16,777,216 colors) DITHER pixel format	1	1	1	DBI Type B (16 bits/8 bits) DBI Type C

See “DBI Data Format” and “DPI Data Format” for each type of interfaces.

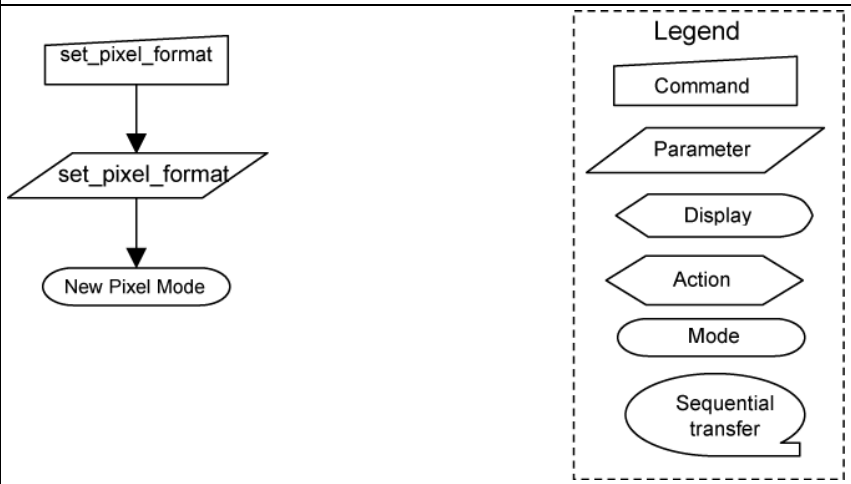
Note: When the bits settings are disabled are set, undesirable image will be displayed on the panel.

X = Don’t care

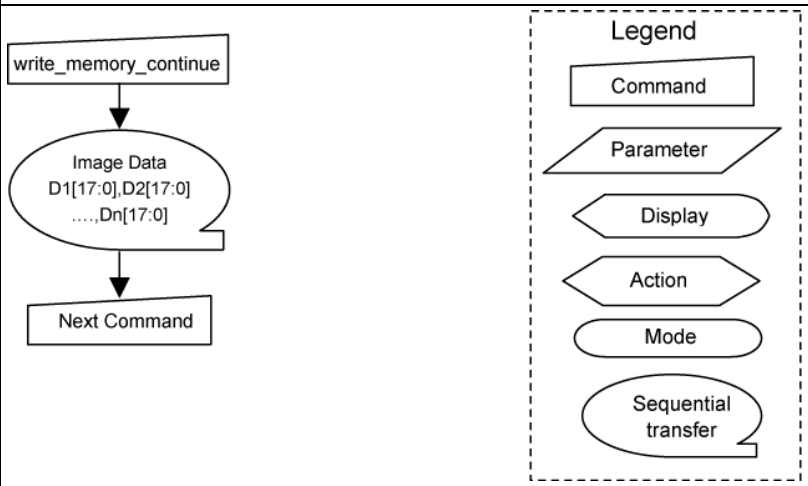
Restriction

There is no visible effect until the frame memory is written.

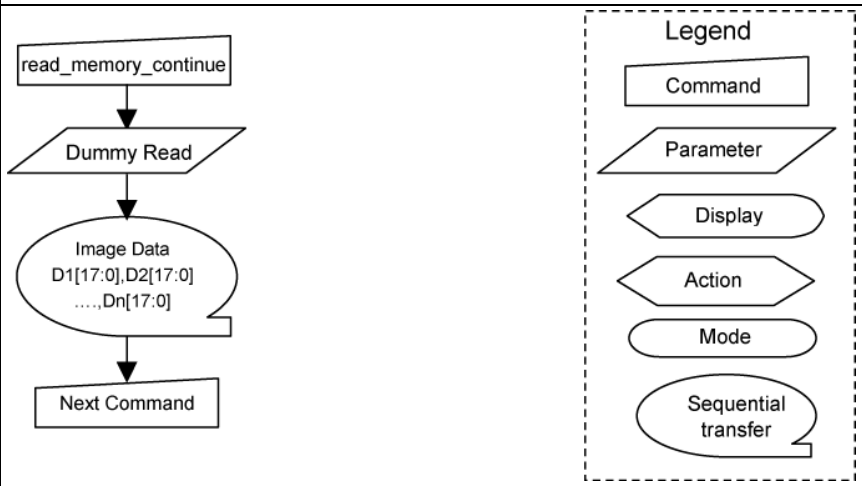
Flow Chart



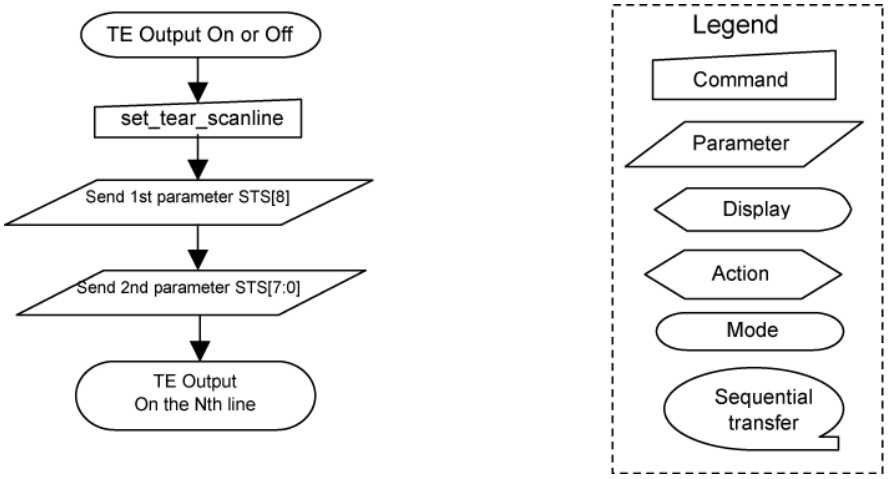
write_memory_continue: 3Ch

3Ch	write_memory_continue												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3Ch
1st parameter	1	1	↑	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
:	1	1	↑	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth parameter	1	1	↑	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Frame Memory Access and Interface setting (B3h): WEMODE = 0 If the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored. Frame Memory Access and Interface setting (B3h): WEMODE = 1 When the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are reset to the Start Column/Start Page positions, and the subsequent data are written to the frame memory. X=Don't care												
Restriction	If write_memory_continue command is executed without setting set_column_address (2Ah), set_page_address (2Bh), and set_address_mode (36h), there is no guarantee that data are correctly written to the frame memory.												
Flow Chart													

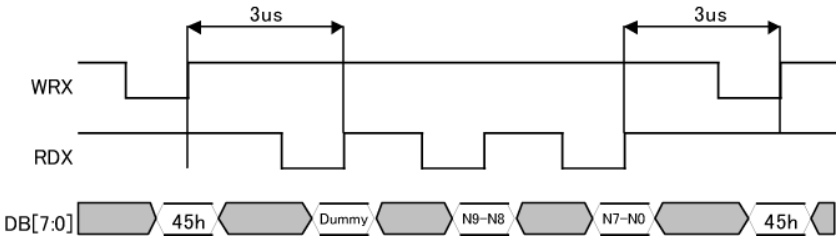
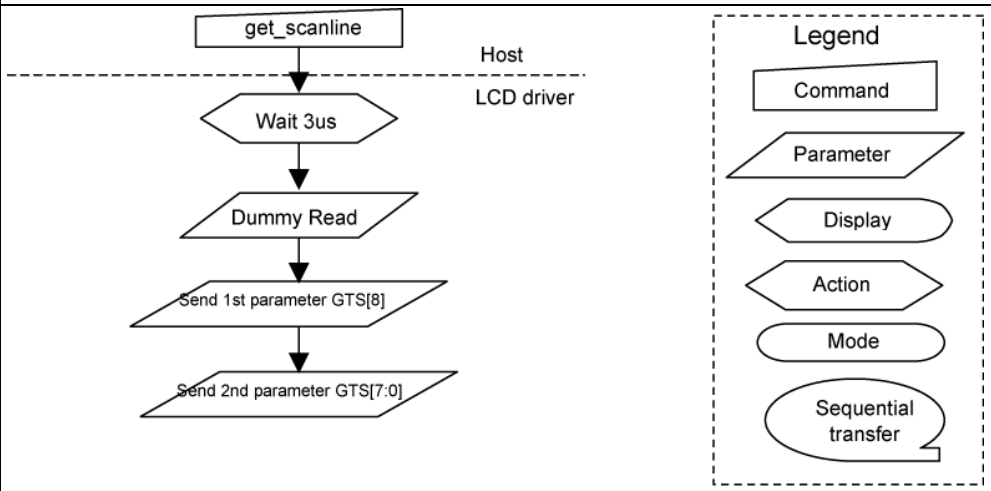
read_memory_continue: 3Eh

3Eh	read_memory_continue												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	0	1	1	1	1	1	0	3Eh
1st Pixel data	1	↑	1	D1 [17:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h … 3FFh
:	1	↑	1	Dx [17:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h … 3FFh
Nth Pixel data	1	↑	1	Dn [17:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h … 3FFh
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the location following the previous read_memory_continue or read_memory_start command. If read operation is executed after (EP. EC) is read, the last data (EP, EC) continue to output. After pixel data 1 are written to frame memory (SC, SP), address counter's direction differs depending on setting of set_address_mode (36h)'s Bits 5, 6, 7. See "Host Processor to Memory Write/Read Direction". X = Don't care												
Restriction	In any color mode, format returned by read_memory_continue is always 18 bits so there is no restriction on the length of parameter.												
Flow Chart													

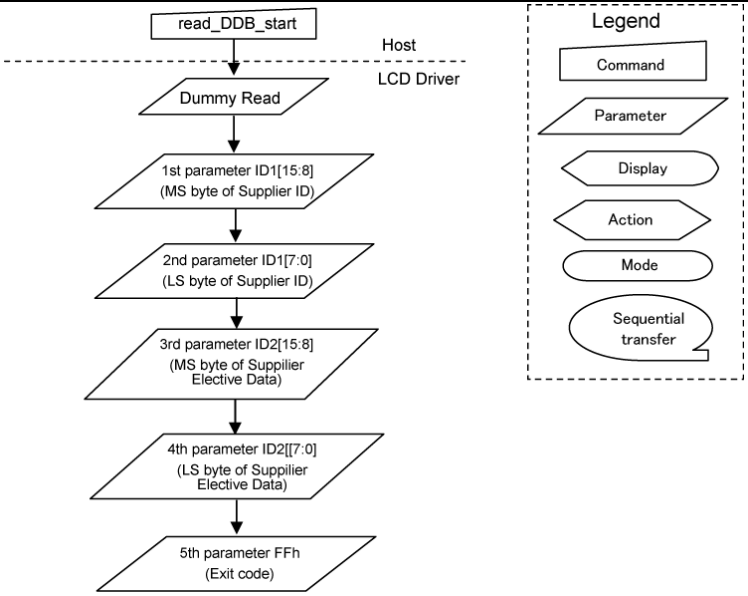
set_tear_scanline:44h

44h	**set_tear_scanline**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	X	0	0	0	0	0	0	0	STS [8]	0Xh
2nd Parameter	1	1	↑	X	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	XXh
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N defined by STS [8:0]. TE line is unaffected by change in B4 bit of set_address_mode command. See figure in "TE Pin Output Signal". X =don't care.												
Restriction	The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame. Setting is disabled when TELOM=1 of set_tear_on (35h). Make sure that STS [8:0] ≤ NL (number of line) + 1.												
Flow Chart													

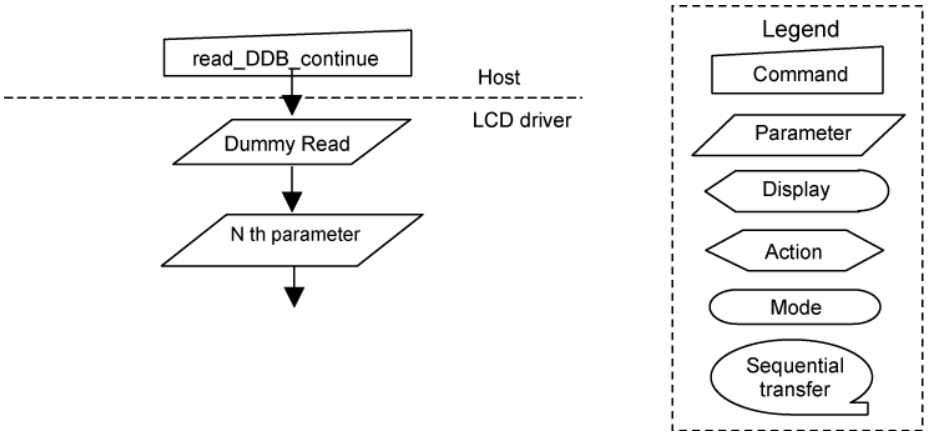
get_scanline: 45h

45h	**get_scanline**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	0	1	0	0	0	1	0	1	45h
1st parameter	1	↑	1	X	0	0	0	0	0	0	0	GTS [8]	0Xh
2nd parameter	1	↑	1	X	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	XXh
Description	The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back porch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined. X = Don't care												
Restriction	After get_line command is input, it takes 3μs or more to read it. After parameters are read, wait 3μs or more to input this command again.  												
Flow Chart	 												

read_DDB_start: A1h

A1h	**read_DDB_start**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	0	0	0	0	1	A1h
Dummy Parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	1	↑	1	X	1	1	1	1	1	1	1	1	FFh
Description	The command returns information from the display module as follows: 1st parameter: upper byte of Supplier ID (ID1[15:8]) 2nd parameter: lower byte of Supplier ID (ID1[7:0]) 3rd parameter: Supplier Elective Data (ID2[15:8]) 4th parameter: Supplier Elective Data (ID2[7:0]) 5th parameter: Exit Code (FFh) Supplier ID and Supplier Elective Data stored in internal NVM is read. X=Don't care												
Restriction	-												
Flow Chart													

read_DDB_continue: A8h

A8h	**read_DDB_continue**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	0	1	0	0	0	A8h
Dummy Parameter	1	↑	1	X	X	X	X	X	X	X	X	X	XXh
1st Parameter	1	↑	1	X	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	XXh
2nd Parameter	1	↑	1	X	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	XXh
3rd parameter	1	↑	1	X	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	XXh
4th parameter	1	↑	1	X	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	XXh
5th parameter	1	↑	1	X	1	1	1	1	1	1	1	1	FFh
Description	This command continues read operation from the position the operation is halted by read_DDB_continue or read_DDB_start. For the position that information is returned, see read_DDB_start (A1h). X=Don't care												
Restriction	To fix the position that information is returned, execute read_DDB_start command and parameter read operation at least once before read_DDB_continue command. If they are not executed, the value returned by read_DDB_continue command is invalid.												
Flow Chart													

Manufacturer Command

Additional User Command

MCAP: Manufacturer Command Access Protect (B0h)

B0h	MCAP(Manufacturer Command Access Protect)												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	0	0	0	0	B0h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	MCAP[1]	MCAP[0]	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

MCAP[1:0]

The R61581B0 is required to release Access Protect before inputting a Manufacturer Command. This command releases parameters so that Manufacturer Command inputs are enabled. When the conditions to release Protect, as shown in the table below, are met, Manufacturer Command inputs are enabled.

MCAP [1]	MCAP [0]	User Command	Manufacturer Command		
		00h-0Fh	B0h	B1-BFh	C0h-FFh
0	0	Yes	Yes	Yes	Yes
0	1	Setting Inhibited			
1	0	Yes	Yes	Yes	No
1	1	Yes	Yes	No	No

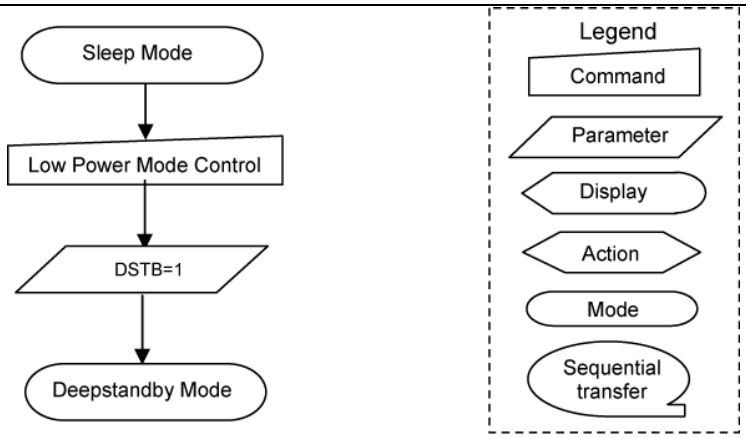
Yes: Accessing is enabled (Protect Off)
No: Accessing is disabled (Protect On)

Once the R61581B0 enables Manufacturer Command inputs, it keeps the state until MCAP[1:0] is written so that the R61581B0 enters Protect ON state again.

Restriction

After H/W Reset or exiting Deep Standby Mode, accessing a Manufacturer Command is restricted so that Manufacture Commands B1h-BFh inputs are identified as nop command.

Low Power Mode Control (B1h)

B1h	Low Power Mode Control												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	0	0	0	1	B1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	DSTB	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read This command is used to enter the Deep Standby Mode. **DSTB** The Deep Standby Mode is entered when DSTB=1. Internal logic power supply circuit (VDD) is turned down enabling low power consumption. In the Deep Standby mode, data stored in the Frame Memory and the Instructions are not retained. Rewrite them after the Deep Standby mode is exited. See Deep Standby Mode IN/EXIT Sequence in "State and Command Sequence".												
Restriction	-												
Flow Chart													

Frame Memory Access and Interface Setting (B3h)

B3h	Frame Memory Access and Interface Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	1	B3h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	WEMODE	0	XXh
2nd Parameter	1	#A	#B	X	0	0	0	0	0	TEI [2]	TEI [1]	TEI [0]	XXh
3rd Parameter	1	#A	#B	X	0	0	0	0	0	DENC [2]	DENC [1]	DENC [0]	XXh
4th Parameter	1	#A	#B	X	0	0	EPF [1]	EPF [0]	0	0	0	DFM	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

WEMODE

After frame memory write operation reaches to the end of window address area, the next write start position is selected.

WEMODE = 0: The write start position is not reset to the start of window address, and the subsequent data are disregarded. (Default)
WEMODE = 1: The write start position is reset to the start of window address area to overwrite the subsequent data to the previous data.

TEI [2:0]
The bit is used to define interval between outputs of TE signal. Set in accordance with update cycle and transfer rate of the display data.

TEI[2]	TEI[1]	TEI[0]	Interval
0	0	0	Every frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other setting			Setting inhibited

-Description

DENC [2:0]

The bit is used to define Frame Memory write cycle in DPI operation. Set in accordance with update cycle of the display data.

DENC [2]	DENC [1]	DENC [0]	Frame Memory Write Cycle
0	0	0	Every frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	3 frames
1	0	0	4 frames
1	0	1	5 frames
1	1	0	6 frames
1	1	1	7 frames

EPF[1:0]

This bit is used to set data format when 16bpp (R,G,B) data are converted to 18bpp (r,g,b) stored in internal frame memory (18bpp).

EPF is enabled when one of

1 DBI Type B 16-bit interface (set_pixel_format (3Ah) D[2:0]=3'h5)
2 DBI Type B 8-bit interface (set_pixel_format (3Ah) D[2:0]=3'h5)
3 DPI 16-bit interface (set_pixel_format (3Ah) D[6:4]=3'h5)
is selected. EPF is disabled in other interface operation.

Description

EPF[1:0]	16bpp (R, G, B) → 18bpp (r, g, b)
2'h0	"0" is written to the LSB. r[5:0]={R[4:0], 1'h0} g[5:0]={G[5:0]} b[5:0]={B[4:0], 1'h0} Note that the data are converted as follows: R[4:0], B[4:0]=5'h1F → r, b[5:0]=6'h3F G[5:0]=6'h3F → g[5:0]=6'h3F
2'h1	"1" is written to the LSB. r[5:0]={R[4:0], 1'h1} g[5:0]={G[5:0]} b[5:0]={B[4:0], 1'h1} Note that the data are converted as follows: R[4:0], B[4:0]=5'h0 → r, b[5:0]=6'h00 G[5:0]=6'h0 → g[5:0]=6'h00
2'h2	The MSB value is written to the LSB. r[5:0]={R[4:0], R[4]} g[5:0]={G[5]:0} b[5:0]={B[4:0], B[4]}
2'h3	Setting inhibited

DFM

The bit is used to define image data write/read format to the Frame Memory in DBI Type B 16 bit bus interface and DBI Type C serial interface operation. See "DBI Data Format" for details.

Display Mode and Frame Memory Write Mode Setting (B4h)

B4h	Display Mode and Frame Memory Write Mode Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	1	0	0	B4h
1st Parameter	1	#A	#B	X	0	0	0	RM	0	0	DM[1]	DM[0]	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

RM

The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation. RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting RM.

RM	Interface to access Frame Memory
0	DBI
1	DPI

See "Display Pixel Interface" for the sequence.

DM[1:0]

The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DIP signal. Note that switching between VSYNC and DPI operation is prohibited.

DM[1]	DM[0]	Display mode
0	0	Internal oscillation clock
0	1	DPI signal
1	0	VSYNC signal
1	1	Setting inhibited

Backlight Control 1 (B8h)

B8h	Backlight Control 1												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	0	0	0	B8h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	BLCM	BLCON	XXh
2nd parameter	1	#A	#B	X	0	0	0	THREW0[4]	THREW0[3]	THREW0[2]	THREW0[1]	THREW0[0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	THREW1[4]	THREW1[3]	THREW1[2]	THREW1[1]	THREW1[0]	XXh
4th parameter	1	#A	#B	X	0	0	ULMTW0[5]	ULMTW0[4]	ULMTW0[3]	ULMTW0[2]	ULMTW0[1]	ULMTW0[0]	XXh
5th parameter	1	#A	#B	X	0	0	ULMTW1[5]	ULMTW1[4]	ULMTW1[3]	ULMTW1[2]	ULMTW1[1]	ULMTW1[0]	XXh
6th parameter	1	#A	#B	X	0	0	LLMTW0[5]	LLMTW0[4]	LLMTW0[3]	LLMTW0[2]	LLMTW0[1]	LLMTW0[0]	XXh
7th parameter	1	#A	#B	X	0	0	LLMTW1[5]	LLMTW1[4]	LLMTW1[3]	LLMTW1[2]	LLMTW1[1]	LLMTW1[0]	XXh
8th parameter	1	#A	#B	X	0	0	0	0	PITCHW[3]	PITCHW[2]	PITCHW[1]	PITCHW[0]	XXh
9th parameter	1	#A	#B	X	0	0	0	CGAPW[4]	CGAPW[3]	CGAPW[2]	CGAPW[1]	CGAPW[0]	XXh
10th parameter	1	#A	#B	X	0	0	0	COEFK0[4]	COEFK0[3]	COEFK0[2]	COEFK0[1]	COEFK0[0]	XXh
11th parameter	1	#A	#B	X	0	0	0	COEFK1[4]	COEFK1[3]	COEFK1[2]	COEFK1[1]	COEFK1[0]	XXh
12th parameter	1	#A	#B	X	TBL3[7]	TBL3[6]	TBL3[5]	TBL3[4]	TBL3[3]	TBL3[2]	TBL3[1]	TBL3[0]	XXh
13th parameter	1	#A	#B	X	TBL4[7]	TBL4[6]	TBL4[5]	TBL4[4]	TBL4[3]	TBL4[2]	TBL4[1]	TBL4[0]	XXh
14th parameter	1	#A	#B	X	TBL5[7]	TBL5[6]	TBL5[5]	TBL5[4]	TBL5[3]	TBL5[2]	TBL5[1]	TBL5[0]	XXh
15th parameter	1	#A	#B	X	TBL6[7]	TBL6[6]	TBL6[5]	TBL6[4]	TBL6[3]	TBL6[2]	TBL6[1]	TBL6[0]	XXh
16th parameter	1	#A	#B	X							CTRL_SEL0[1]	CTRL_SEL0[0]	XXh
17th parameter	1	#A	#B	X							CTRL_SEL1[1]	CTRL_SEL1[0]	XXh
18th parameter	1	#A	#B	X							DGAP[1]	DGAP[0]	XXh

Note: Make sure that BLC function is turned off (DB0 of the 1st parameter: BLCON=0) when changing parameter values of B8h.

Write #A="1" #B="↑"
Read #A="↑" #B="1" & Insert dummy read

BLCM

The bit is used to select BLC mode. There are two sets of bits for each of THREW, ULMTW, LLMTW, and COEFK and registers, enabling different settings for different display images.

BLCM	BLC mode	Enabled register			
0	Mode 0	THREW0 [4:0]	ULMTW0 [5:0]	LLMTW0 [5:0]	COEFK0 [4:0]
1	Mode 1	THREW1 [4:0]	ULMTW1 [5:0]	LLMTW1 [5:0]	COEFK1 [4:0]

BLCON

The bit is used to turn the BLC function ON/OFF.

BLCON	BLC function
0	OFF
1	ON

The BLC function is disabled in Idle Mode On and Display Invert Mode On. Use BLC function (BLCON = 1) in Idle Mode Off and Display Invert Mode Off.

THREW0[4:0], THREW1[4:0]

The bits are used to specify percentage from the threshold to grayscale number 63 in the total of grayscale data. This is the ratio (percentage) of the maximum number of pixels that makes display image white (= data "63") to the total of pixels by image processing.

Percentage of pixels =

Number of pixels with the grayscale from the threshold to grayscale No. 63/ Number of all pixels

THREW0 is enabled when BLCM=0.

THREW1 is enabled when BLCM=1.

THREW0[4:0] THREW1[4:0]	Percentage of pixels	THREW0[4:0] THREW1[4:0]	Percentage of pixels
5'h00	0%	5'h10	32%
5'h01	2%	5'h11	34%
5'h02	4%	5'h12	36%
5'h03	6%	5'h13	38%
5'h04	8%	5'h14	40%
5'h05	10%	5'h15	42%
5'h06	12%	5'h16	44%
5'h07	14%	5'h17	46%
5'h08	16%	5'h18	48%
5'h09	18%	5'h19	50%
5'h0A	20%	5'h1A	52%
5'h0B	22%	5'h1B	54%
5'h0C	24%	5'h1C	56%
5'h0D	26%	5'h1D	58%
5'h0E	28%	5'h1E	60%
5'h0F	30%	5'h1F	62%

Note: Make sure that BLC function is turned off (DB0 of the 1st parameter: BLCON=0) when changing parameter values on B8h and switching BLC modes (DB1 of the 1st parameter: BLCM).

ULMTW0[5:0], ULMTW1[5:0]

The possible maximum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale.

ULMTW0 is enabled when BLCM=0.
ULMTW1 is enabled when BLCM=1.

The maximum value can be set in the range of 0 to 63.

ULMTW0[5:0] ULMTW1[5:0]	Maximum gray scale (Frame memory data)
6'h00	6'h00
6'h01	6'h01
6'h02	6'h02
6'h03	
:	:
6'h3B	6'h3B
6'h3C	6'h3C
6'h3D	6'h3D
6'h3E	6'h3E
6'h3F	6'h3F

LLMTW0[5:0], LLMTW1[5:0]

The possible minimum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale.

LLMTW0 is enabled when BLCM=0.
LLMTW1 is enabled when BLCM=1.

The minimum value can be set in the range of 0 to 63.

LLMTW0[5:0] LLMTW1[5:0]	Minimum gray scale (Frame memory data)
6'h00	6'h00
6'h01	6'h01
6'h02	6'h02
6'h03	
:	:
6'h3B	6'h3B
6'h3C	6'h3C
6'h3D	6'h3D
6'h3E	6'h3E
6'h3F	6'h3F

Note: LLMTW0[5:0] and LLMTW1[5:0] values are restricted according to COEFK0/1 values. See COEFK0/1 descriptions (B8h) for details.

PITCHW[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one eighth of the grayscale. Make sure that CGAPW[4:0] ≥ PITCHW[3:0].

PITCHW[3:0]	Amount of change (grayscale)
4'h0	Setting inhibited
4'h1	1/8 of grayscale
4'h2	1/4 of grayscale
4'h3	3/8 of grayscale
4'h4	1/2 of grayscale
4'h5	5/8 of grayscale
4'h6	3/4 of grayscale
4'h7	7/8 of grayscale
4'h8	1 grayscale
4'h9	9/8 of grayscale
4'hA	5/4 of grayscale
4'hB	11/8 of grayscale
4'hC	3/2 of grayscale
4'hD	13/8 of grayscale
4'hE	7/4 of grayscale
4'hF	15/8 of grayscale

CGAPW[4:0]

The difference of the two grayscales counted by the threshold counter is set in units of one eighth of the grayscale. Make sure that CGAPW[4:0] ≥ PITCHW[3:0].

CGAPW[4:0]	Grayscale difference	CGAPW[4:0]	Grayscale difference
5'h00	Setting inhibited	5'h10	2 gray scales
5'h01	1/8 of gray scale	5'h11	17/8 of gray scale
5'h02	1/4 of gray scale	5'h12	9/4 of gray scale
5'h03	3/8 of gray scale	5'h13	19/8 of gray scale
5'h04	1/2 of gray scale	5'h14	5/2 of gray scale
5'h05	5/8 of gray scale	5'h15	21/8 of gray scale
5'h06	3/4 of gray scale	5'h16	11/4 of gray scale
5'h07	7/8 of gray scale	5'h17	23/8 of gray scale
5'h08	1 gray scale	5'h18	3 gray scales
5'h09	9/8 of gray scale	5'h19	25/8 of gray scale
5'h0A	5/4 of gray scale	5'h1A	13/4 of gray scale
5'h0B	11/8 of gray scale	5'h1B	27/8 of gray scale
5'h0C	3/2 of gray scale	5'h1C	7/2 of gray scale
5'h0D	13/8 of gray scale	5'h1D	29/8 of gray scale
5'h0E	7/4 of gray scale	5'h1E	15/4 of gray scale
5'h0F	15/8 of gray scale	5'h1F	31/8 of gray scale

COEFK0[4:0], COEFK1[4:0]

These registers set the range of the grayscale that prevent display image from being white, according to the ratio of the grayscale mentioned here to the grayscale number that makes data white.

COEFK0[4:0] COEFK1[4:0]	Range of gray scale preventing image from being white	LLMTW* Min.	COEFK0[4:0] COEFK1[4:0]	Range of gray scale preventing image from being white	LLMTWx Min.
5'h00	0%	6'h00	5'h10	100.00%	6'h20
5'h01	6.25%	6'h04	5'h11	Setting inhibited	-
5'h02	12.50%	6'h07	5'h12	Setting inhibited	-
5'h03	18.75%	6'h0A	5'h13	Setting inhibited	-
5'h04	25.00%	6'h0D	5'h14	Setting inhibited	-
5'h05	31.25%	6'h0F	5'h15	Setting inhibited	-
5'h06	37.50%	6'h12	5'h16	Setting inhibited	-
5'h07	43.75%	6'h14	5'h17	Setting inhibited	-
5'h08	50.00%	6'h15	5'h18	Setting inhibited	-
5'h09	56.25%	6'h17	5'h19	Setting inhibited	-
5'h0A	62.50%	6'h19	5'h1A	Setting inhibited	-
5'h0B	68.75%	6'h1A	5'h1B	Setting inhibited	-
5'h0C	75.00%	6'h1B	5'h1C	Setting inhibited	-
5'h0D	81.25%	6'h1D	5'h1D	Setting inhibited	-
5'h0E	87.50%	6'h1E	5'h1E	Setting inhibited	-
5'h0F	93.75%	6'h1F	5'h1F	Setting inhibited	-

Note: LLMTW0[5:0] and LLMTW1[5:0] values are restricted as above table according to COEFK0[4:0] and COEFK1[4:0] values. Make sure to follow the above minimum LLMTW*[5:0] setting to each COEFK[4:0] value.

TBL3[7:0], TBL4[7:0], TBL5[7:0], TBL6[7:0]

The reference value used for interpolation calculation in gamma table are set by TBL*.

TBL*[7:0]	8-bit reference value
8'h00	8'h00
8'h01	8'h01
8'h02	8'h02
8'h03	8'h03
:	:
8'hFB	8'hFB
8'hFC	8'hFC
8'hFD	8'hFD
8'hFE	8'hFE
8'hFF	8'hFF

CTRL_SEL1[1:0], CTRL_SEL0[1:0]

These registers select a controller specifying a threshold grayscale value (Dth) and an operation mode corresponding to the controller.

CTRL_SEL0[1:0] CTRL_SEL1[1:0]	Mode
2'b00	Video image mode
2'b01	Still image mode
2'b10	Setting inhibited
2'b11	Setting inhibited

DGAP[1:0]

This register sets a difference between two threshold grayscale values (Dth) used in a still image mode controller by the grayscale. Dth may change, depending on whether this difference exceeds a hysteresis width or not due to change in image. If a difference between Dth before change in image and Dth after the change in image is within a hysteresis width, Dth does not change. If this difference exceeds a hysteresis width, Dth changes.

DGAP[1:0]	Hysteresis width
2'b00	1 gray scale
2'b01	2 gray scales
2'b10	3 gray scales
2'b11	4 gray scales

Backlight Control 2 (B9h)

B9h	Backlight Control 2												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	0	0	1	B9h
1st Parameter	1	#A	#B	X	0	0	0	0	0	0	LED ON	PWM ON	XXh
2nd Parameter	1	#A	#B	X	BDCV [7]	BDCV[6]	BDCV[5]	BDCV [4]	BDCV[3]	BDCV [2]	BDCV [1]	BDCV [0]	XXh
3rd Parameter	1	#A	#B	X	PWMDIV [7]	PWM DIV [6]	PWM DIV [5]	PWM DIV [4]	PWM DIV [3]	PWM DIV [2]	PWM DIV [1]	PWM DIV [0]	XXh
4th Parameter	1	#A	#B	X	0	0	0	PWMWM	LEDPWME	LED PWM POL	0	DIM ON	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

LEDON

The value written in the LEDON register becomes LEDON signal and it is output.

When LED is controlled by this product, it is useful.

PWMWM, PWMON

PWMWM = 0: Controls On/Off of the PWM output according to Display On/Off state.

PWMWM = 1: Controls On/Off of the PWM output according to PWMON setting. Note that LEDPWM is OFF when in Sleep Mode regardless of PWMON value.

PWMWM setting can be changed only in Sleep Mode On.

LEDPWME

LEDPWM pin output enable bit. In the system configuration using no LEDPWM pin, set the bit to 0. In the system configuration using LEDPWM pin, set the bit to 1. This setting can be changed only in Sleep Mode On.

LEDPWME	PWMWM	PWMON	BLCON	RDPWM	LEDPWM output
0	0	*	0	BDCV	0%
			1	BLC*BDCV	0%
	1	0	0	0%	0%
			1	Setting inhibited	Setting inhibited
		1	0	BDCV	0%
			1	BLC*BDCV	0% (note 2)
1	0	*	0	BDCV	BDCV (note 1)
			1	BLC*BDCV	BLC*BDCV (note 1)
	1	0	0	0%	0%
			1	Setting inhibited	Setting inhibited
		1	0	BDCV	BDCV
			1	BLC*BDCV	BLC*BDCV (note 2)

Notes: 1. If PWMWM = 0, On/Off of the PWM output is automatically controlled according to display ON/Off state.
Display Off: Sleep Mode On + set_display_off
Display On: sleep Mode Off + set_display_on
2. If PWMWM = 1, RDPWM and LEDPWM outputs cause BDCV value to be read during Display Off.

BDCV[7:0]

PWM signal's width is selected from 256 values between 8'hFF and 8'h00 when LED is adjusted externally. The setting is enabled even when BLCON=0.

BDCV[7:0]	**Amount of light**
8'h00	None (0%)
8'h01	1/255
8'h02	2/255
8'h03	3/255
:	:
8'hFE	254/255
8'hFF	255/255 (100%)

PWMDIV[7:0]

The bit is used to define frequency of PWM signal that is output from LEDPWM pin.

PWMDIV[7:0]	LEDPWM frequency	PWMDIV[7:0]	LEDPWM frequency
8’h00	40.0 KHz	8'h10-8'h1E	Setting inhibited
8'h01	20.0 KHz	8'h1F	1.25 KHz
8'h02	13.3 KHz	8'h20-8'h3E	Setting inhibited
8'h03	10.0 KHz	8'h3F	0.62 KHz
8'h04-8'h06	Setting inhibited	8'h40-8'h7E	Setting inhibited
8'h07	5.00 KHz	8'h7F	0.31 KHz
8'h08-8'h0E	Setting inhibited	8'h80-8'hFE	Setting inhibited
8'h0F	2.50 KHz	8'hFF	0.16 KHz

Note: The values in the table above show the typical. There shall be variance of maximum ±7% in the actual operation.

LEDPWMPOL

The bit is used to define polarity of LEDPWM signal.

LEDPWPOL	LEDPWM pin	
	Lit period	Non-lit period
0	High	Low
1	Low	High

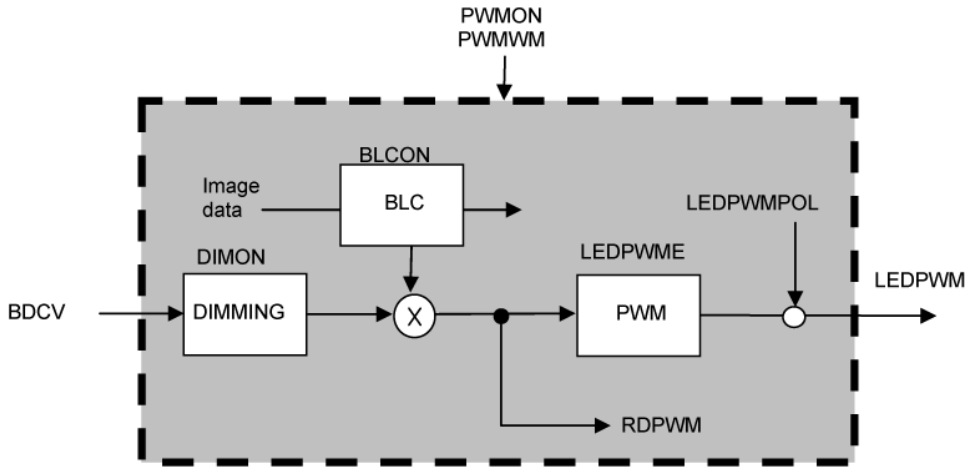
DIMON

DIMON bit is used to enable / disable LEDPWM’s DIMMING function.

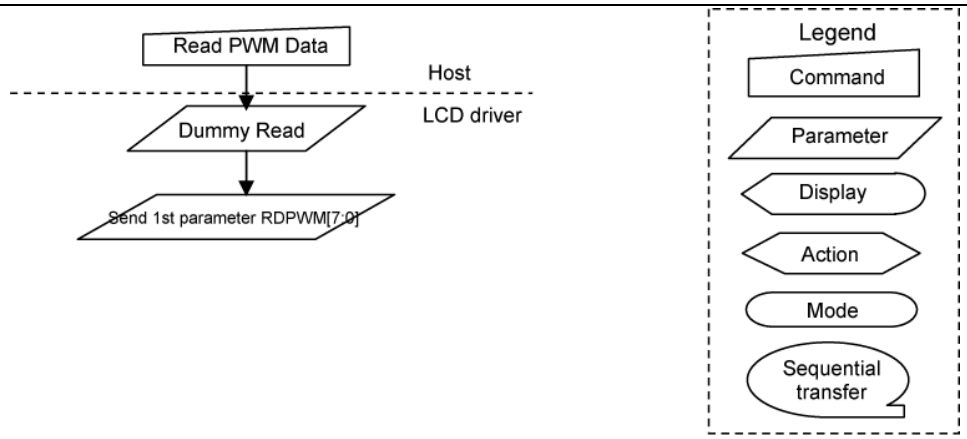
The bit is used to control change in brightness (change in LEDPWM signal) when BCDV register is rewritten or LEDPWM pin is turned on. This setting is enabled only in Sleep Mode On.

DIMON	DIMMING function	Brightness
0	OFF	Changes immediately
1	ON	Changes gradually in approximately 500ms.

Note: This bit is applied to BDCV register setting and not to brightness change by the BLC function.



Backlight Control 3 (BAh)

BAh	Backlight Control 3 (Read PWM Data)												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	0	1	0	BAh
1st parameter	1	↑	1	X	RDPWM [7]	RDPWM [6]	RDPWM [5]	RDPWM [4]	RDPWM [3]	RDPWM [2]	RDPWM [1]	RDPWM [0]	XXh
Description	The command is used to read LED brightness data for LEDPWM signal. X = Don't care												
Flow Chart													
Restriction	Data read is disabled when in the Sleep mode.												

Device Code Read (BFh)

BFh	Device Code Read												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	0	1	1	1	1	1	1	BFh
1st Parameter	1	↑	1	X	0	0	0	0	0	0	0	1	01h
2nd Parameter	1	↑	1	X	0	0	1	0	0	0	1	0	22h
3rd Parameter	1	↑	1	X	0	0	0	1	0	1	0	1	15h
4th Parameter	1	↑	1	X	1	0	0	0	0	0	0	1	81h
Description	The parameters are used to read the information as follows. 1st parameter: Returns the upper byte "01h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 2nd parameter: Returns the lower byte "22h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 3rd parameter: Returns the upper byte "15h" of product code of this LSI. 4th parameter: Returns the lower byte "81h" of product code of this LSI. X = Don't care												
Restriction	-												

Panel Control

Panel Driving Setting (C0h)

C0h	Panel Driving Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	0	C0h
1st parameter	1	#A	#B	X	0	0	0	REV	SM	GS	BGR	SS	XXh
2nd parameter	1	#A	#B	X	0	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	XXh
3rd parameter	1	#A	#B	X	0	0	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	XXh
4th parameter	1	#A	#B	X	0	0	0	0	0	0	BLV	PTV	XXh
5th parameter	1	#A	#B	X	0	0	0	NDL	PTDC	PTS [2]	PTS [1]	PTS [0]	XXh
6th parameter	1	#A	#B	X	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	XXh
7th parameter	1	#A	#B	X	0	0	0	0	BLS	0	0	NW	XXh
8th parameter	1	#A	#B	X	0	PC DIVH [2]	PC DIVH [1]	PC DIVH [0]	0	PC DIVL [2]	PC DIVL [1]	PC DIVL [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read												

Description

REV

The grayscale is reversed by setting REV = 1. This enables the R61581B0 to display the same image from the same set of data on both normally white and black panels. The source output level during the retrace period and non-lit display period is determined by register settings, BLS and NDL, respectively.

REV	Frame Memory data	Source output level in display area	
		Positive polarity	Negative polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

SM

SM=0: Left/right interchanging scan
SM=1: Left/right one-side scan

GS

GS=0: Forward scan
GS=1: Reverse scan

The R61581B0 allows changing gate driver assignment and the scan mode by combination of SM and GS bits. Set these bits in accordance with the configuration of the module. For details, see "Scan Mode Setting".

BGR

The bit is used to reverse 18-bit write data in the Frame Memory from RGB to BGR. Set in accordance with arrangement of color filters.

BGR=0: Data are written to the Frame Memory in the order of RGB. (Default)
BGR=1: Data are written to the Frame Memory in the order of BGR.

SS

The bit is used to select the shifting direction of the source driver output. Set in accordance with mounting position of the R61581B0 to the panel.

SS=0: S1 to S960 (Default)
SS=1 S960 to S1

To change the RGB order, set SS and BGR bit.

SS=0, BGR=0: RGB
SS=1, BGR=1: BGR

Description

NL[5:0]

These bits set the number of lines to drive the LCD to in units of 8 lines in the range from 400 to 480 lines. The frame memory address mapping is not affected by the number of NL[5:0]. The number of lines should be set according to the panel size.

NL[5:0]	Number of drive line
6'h00-6'h30	Setting inhibited
6'h31	400 lines
6'h32	408 lines
6'h33	416 lines
6'h34	424 lines
6'h35	432 lines
6'h36	440 lines
6'h37	448 lines
6'h38	456 lines
6'h39	464 lines
6'h3A	472 lines
6'h3B	480 lines
6'h3C-6'h3F	Setting inhibited

NL when the DPI interface is used is made 480 lines.

SCN[5:0]

The bit is used to set scanning start position.

SCN[5:0]	Scanning start position (N: Number of line(s) defined by NL[6:0])			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G[1]	G[(N)]	G[1]	G[(2N – 480)]
6'h01	G[9]	G[(N+8)]	G[16]	G[(2N – 464)]
6'h02	G[17]	G[(N+16)]	G[33]	G[(2N – 448)]
6'h03	G[25]	G[(N+24)]	G[49]	G[(2N – 432)]
6'h04	G[33]	G[(N+32)]	G[65]	G[(2N – 416)]
6'h05	G[41]	G[(N+40)]	G[81]	G[(2N – 400)]
6'h06	G[49]	G[(N+48)]	G[97]	G[(2N – 384)]
6'h07	G[57]	G[(N+56)]	G[113]	G[(2N – 368)]
6'h08	G[65]	G[(N+64)]	G[129]	G[(2N – 352)]
6'h09	G[73]	G[(N+72)]	G[145]	G[(2N – 336)]
6'h0A	G[81]	G[(N+80)]	G[161]	G[(2N – 320)]
6'h0B-6'h2F	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

Description

To set SCN, follow the restriction below:

SM	GS	Restriction
0	0	(Scanning start position -1) + (Number of line (NL bit)) ≤ 480
0	1	Scanning start position ≤ 480
1	0	(Scanning start position -1)/2 + (Number of line (NL bit)) ≤ 480
1	1	Scanning start position ≤ 480

NW

This bit sets the number of lines for inversion liquid crystal drive by line inversion waveform (BCn=1, Display Timing Setting for Normal Mode (C1h), Display Timing Setting for Partial Mode (C2h), and Display Timing Setting for Idle Mode (C3h)). The polarity of waveform inverts in every 1 or 2 line(s).

NW	Number of line(s)
0	1 line
1	2 lines

BLV

The bit selects line or frame inversion during the retrace period.

BLV=0: line inversion is selected for the retrace period when line inversion is selected by BCn=1, C1h~C3h.

BLV=1: Frame inversion is selected for the retrace period.

BCn	BLV	Retrace period
0	-	Frame inversion
1	0	Line inversion
	1	Frame inversion

PTV

The bit is used to define inversion in the non-lit display area.

PTV=1: frame inversion is selected for the non-lit display area when line inversion is selected (BCn=1).

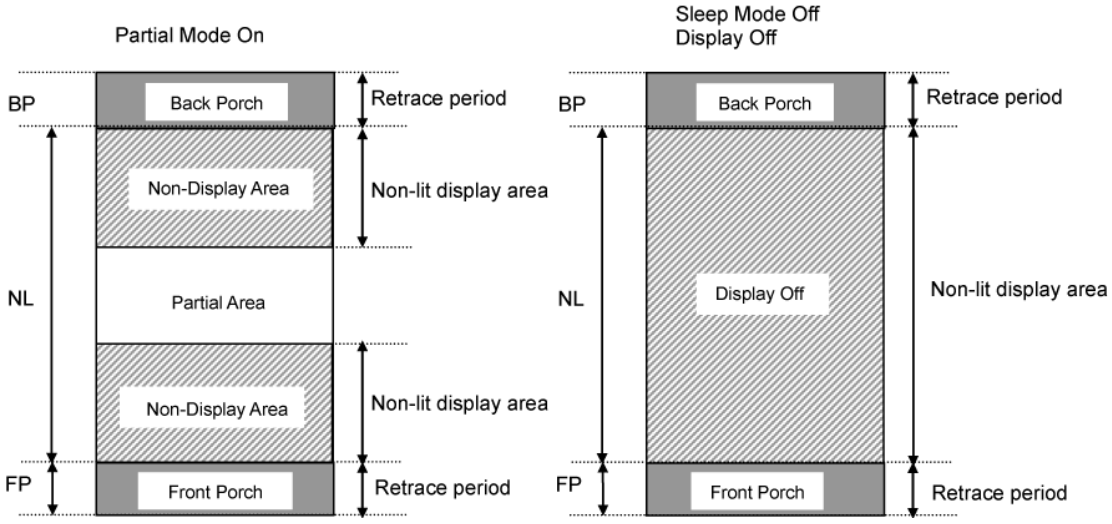
BCn	PTV	Inversion in non-lit display area
0	*	Frame inversion
1	0	Line inversion
	1	Frame inversion

“Retrace period” means back and front porches.

“Non-lit display area” means:

Non-display area other than the Partial Area defined by SR[8:0] and ER[8:0].
Display area when Sleep mode is off and the display operation is off.

Description



BLS

The bit is used to source output level in the Retrace Period. The polarity of grayscale voltage in the Retrace period is inverted.

	Retrace Period	
BLS	**Positive polarity**	**Negative polarity**
0	V63	V0
1	V0	V63

NDL

The bit is used to define source output level in the non-lit display area. The polarity of grayscale voltage is inverted.

	Non-lit display area	
NDL	**Positive polarity**	**Negative polarity**
0	V63	V0
1	V0	V63

PTS[2:0], PTDC

The bit is used to define low-power consumption operation. PTS[1:0] defines output level in the retrace period and the non-lit display area. PTS[2] defines the operation of the grayscale amplifier and the step-up clock frequency.

Description

PTS[2]	PTS[1:0]	Source output level in non-lit display area (Note) Positive polarity	Negative polarity	Grayscale amplifier in non-lit display area
0	00	V63	V0	V0 to V63
	01	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)
	10	GND	GND	V0 to V63
	11	Hi-z	Hi-z	V0 to V63
1	00	V63	V0	V0,V63
	01	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)
	10	GND	GND	V0,V63
	11	Hi-z	Hi-z	V0,V63

Note: The polarity of the source output level in non-lit display period is set by NDL (C0h). The polarity of the source output level during the retrace period is defined by BLS (C0h). If PTDC=1, step-up operation may not be executed properly depending on CD0h and RTNn values.

PTDC

The bit is used to define low power consumption operation. PTDC defines step-up clock frequency in the retrace period and the non-lit display area. See Step-up clock frequency (DC0n, DC1n, DC3n) register for details.

Note: The polarity of the source output level in non-lit display period is set by NDL (C0h). The polarity of the source output level during the retrace period is defined by BLS (C0h). If PTDC=1, step-up operation may not be executed properly depending on DC0n, DC1n, DC3n and RTNn values.

PTG

The bit is used to select gate scan mode in non-lit display area.

PTG	Gate output in non-lit display area
0	Normal scan
1	Interval scan

Note: Set BCn=0 and select frame inversion in interval scan operation.

Description

ISC[3:0]

The bit is used to set gate interval scan when PTG bit sets interval scan in non-lit display area. The scan interval is always of odd number. The polarity of liquid crystal drive waveform is inverted in the same timing as the interval scan.

ISC[3:0]	Scan interval	ISC[3:0]	Scan interval
4'h0	Setting inhibited	4'h8	17 frames
4'h1	3 frames	4'h9	19 frames
4'h2	5 frames	4'hA	21 frames
4'h3	7 frames	4'hB	23 frames
4'h4	9 frames	4'hC	25 frames
4'h5	11 frames	4'hD	27 frames
4'h6	13 frames	4'hE	29 frames
4'h7	15 frames	4'hF	31 frames

PCDIVH[3:0]/PCDIVL[3:0]

When the R61581B0's display operation is synchronized with PCLK (DM=1, DPI), internal clock for display operation switches from internal oscillation clock to PCLKD. The bits are used to define the division ratio of PCLKD to PCLK.

PCDIVH defines the number of PCLK in PCLKD=High period in units of 1 clock.
PCDIVL defines the number of PCLK in PCLKD=Low period in units of 1 clock.

PCDIVH[3:0] PCDIVL[3:0]	Number of clocks	PCDIVH[3:0] PCDIVL[3:0]	Number of clocks
4'h0	Setting inhibited	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clocks
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Set PCDIVL=PCDIVH or PCDIVH-1.

Also, set PCDIVH and PCDIVL so that PCLKD frequency becomes the closest to internal oscillation clock frequency 785KHz.

See "Setting Example for Display Control Clock in DPI Operation" for details in setting the bits.

Display Timing Setting for Normal Mode (C1h)
Display Timing Setting for Partial Mode (C2h)
Display Timing Setting for Idle Mode (C3h)

C1h	**Display Timing Setting for Normal Mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	0	1	C1h
1st Parameter	1	#A	#B	X	0	0	0	0	BC0	0	DIV0 [1]	DIV0 [0]	XXh
2nd Parameter	1	#A	#B	X	0	0	0	RTN 0[4]	RTN 0 [3]	RTN 0[2]	RTN 0[1]	RTN 0[0]	XXh
3rd Parameter	1	#A	#B	X	BP0 [7]	BP0 [6]	BP0 [5]	BP0 [4]	BP0 [3]	BP0 [2]	BP0 [1]	BP0 [0]	XXh
4th Parameter	1	#A	#B	X	FP0 [7]	FP0 [6]	FP0 [5]	FP0 [4]	FP0 [3]	FP0 [2]	FP0 [1]	FP0 [0]	XXh
C2h	**Display Timing Setting for Partial Mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	1	0	C2h
1st Parameter	1	#A	#B	X	0	0	0	0	BC1	0	DIV1 [1]	DIV1 [0]	XXh
2nd Parameter	1	#A	#B	X	0	0	0	RTN 1[4]	RTN 1[3]	RTN 1[2]	RTN 1[1]	RTN 1[0]	XXh
3rd Parameter	1	#A	#B	X	BP1 [7]	BP1 [6]	BP1 [5]	BP1 [4]	BP1 [3]	BP1 [2]	BP1 [1]	BP1 [0]	XXh
4th Parameter	1	#A	#B	X	FP1 [7]	FP1 [6]	FP1 [5]	FP1 [4]	FP1 [3]	FP1 [2]	FP1 [1]	FP1 [0]	XXh
C3h	**Display Timing Setting for Idle Mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	0	1	1	C3h
1st Parameter	1	#A	#B	X	0	0	0	0	BC2	0	DIV2 [1]	DIV2 [0]	XXh
2nd Parameter	1	#A	#B	X	0	0	0	RTN 2[4]	RTN 2[3]	RTN 2[2]	RTN 2[1]	RTN 2[0]	XXh
3rd Parameter	1	#A	#B	X	BP2 [7]	BP2 [6]	BP2 [5]	BP2 [4]	BP2 [3]	BP2 [2]	BP2 [1]	BP2 [0]	XXh
4th Parameter	1	#A	#B	X	FP2 [7]	FP2 [6]	FP2 [5]	FP2 [4]	FP2 [3]	FP2 [2]	FP2 [1]	FP2 [0]	XXh

Description

Write #A="1" #B="↑"
Read #A="↑" #B="1" & Insert dummy read

Timings can be defined separately for different modes.
C1h: Enabled in Normal Mode On, Idle Mode Off.
C2h: Enabled in Partial Mode On, Idle Mode Off.
C3h: Enabled in Normal Mode On, Idle Mode On and Partial Mode On, Idle Mode On

BCn

These bits define liquid crystal drive waveform inversion.

BCn = 0: Frame inversion waveform is selected.
BCn = 1: Line inversion waveform is selected.

For details, see "Line Inversion AC Drive".

DIVn[1:0]

These bits set the division ratio of the internal clock frequency (DIVn). The frame frequency can be changed by DIV bit and RTNn (defining the number of clocks in 1 line period).

The R61581B0's internal operation is synchronized with the clock divided by the division ratio set by DIV bits.

Also, reference clock width in the source delay time, VCOM inversion point gate non-overlap period settings and so on changes in accordance with DIVn setting.

For details, see "Frame Frequency Adjustment Function".

DIVn[1:0]	Division ratio of internal operation clock
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Frame frequency calculation

Frame frequency (f_{FRM}) = {fosc / (Clock per line × division ratio × (NL + FP + BP))} [Hz]

fosc: Internal clock frequency (785 kHz)
Clocks per line: RTN bit
Division ratio: DIV bit
Number of drive line(s) on the panel: NL bit
Front porch (FP): FP bit
Back porch (BP): BP bit

RTNn[4:0]

These bits set the number of clocks in 1 line period.

RTNn[4:0]	Clocks per line	RTNn[4:0]	Clocks per line	RTNn[4:0]	Clocks per line
5'h00-5'h0F	Setting inhibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

DPI_OFF

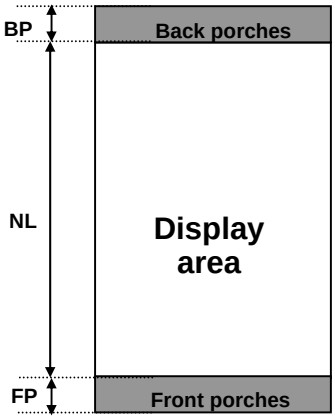
Set this bit for transition from DPI display operation to internal clock operation during DPI operation. For details, see "Transition Sequence between Internal Clock Operation and DPI Display Operation."

Description

FPn, BPn

These parameters define the retrace period (i.e. front and back porches) which appears before and after the display area. DPn bits define number of front porch lines while BPn bits define number of back porch lines.

FPn[7:0], BPn[7:0]	Number of front porch lines	Number of back porch lines
8'h00	Setting inhibited	Setting inhibited
8'h01	Setting inhibited	Setting inhibited
8'h02	Setting inhibited	Setting inhibited
8'h03	Setting inhibited	Setting inhibited
8'h04	4 lines	4 lines
8'h05	5 lines	5 lines
8'h06	6 lines	6 lines
8'h07	7 lines	7 lines
8'h08	8 lines	8 lines
8'h09	9 lines	9 lines
8'h0A	10 lines	10 lines
8'h0B	11 lines	11 lines
8'h0C	12 lines	12 lines
8'h0D	13 lines	13 lines
8'h0E	14 lines	14 lines
8'h0F	15 lines	15 lines
:	:	:
8'h7F	127 lines	127 lines
8'h80	128 lines	128 lines
8'h81	Setting inhibited	Setting inhibited
:	:	:
8'hFF	Setting inhibited	Setting inhibited



Restriction	Set the BP and FP bits as follows. Make sure that the total of lines set by the BP and FP bits is an even number.		
	BP ≥ 4 lines	FP ≥ 4 lines	FP + BP ≤ 256 lines

Display_Setting commands (C1h, C2h, and C3h) can be set according to display mode.

Table 26 Display Mode and Valid Register Setting

Display mode	Operation clock (DIV)	Clocks per line (RTN)	Back Porch (BP)	Front Porch (FP)	VCOM inversion cycle (BC)
(Normal mode) + Idle mode off	C1h: DIV0	C1h: RTN0	C1h: BP0	C1h: FP0	C1h: BC0
(Partial mode) + Idle mode off	C2h: DIV1	C2h: RTN1	C2h: BP1	C2h: FP1	C2h: BC1
Idle mode on + (Normal/Partial mode off)	C3h: DIV2	C3h: RTN2	C3h: BP2	C3h: FP2	C3h: BC2

Source/VCOM/Gate Driving Timing Setting (C4h)

C4h	Source/VCOM/Gate Driving Timing Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	#A	#B	X	0	SDT [2]	SDT [1]	SDT [0]	0	NOW [2]	NOW [1]	NOW [0]	XXh
2nd Parameter	1	#A	#B	X	0	0	0	0	0	MCP [2]	MCP [1]	MCP [0]	XXh
3rd Parameter	1	#A	#B	X	0	VEQW[2]	VEQW [1]	VEQW [0]	0	0	VEM [1]	VEM [0]	XXh
4th Parameter	1	#A	#B	X	0	0	0	0	0	SPCW [2]	SPCW [1]	SPCW [0]	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

SDT [2:0]

The bit is used to set the source output alternating position in 1 line period.

SDT[2:0]	Source output alternating position	SDT[2:0]	Source output alternating position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h and C3h).

NOW[2:0]

These bits set the gate output start position (non-overlap period) in 1 line period.

NOW[2:0]	Gate output start position	NOW[2:0]	Gate output start position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h and C3h).

Description

MCP [2:0]

The bit is used to set the VCOM output alternating position in 1 line period.

MCP[2:0]	VCOM alternating position	MCP[2:0]	VCOM alternating position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, C2h, and C3h).

VEQW[2:0]

These bits define VCOM equalize period.

VEQW[2:0]	VCOM equalize period	VEQW[2:0]	VCOM equalize period
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn.

VEM[1:0]

VEM[0]: VCOMH equalize switch
VEM[0] = 1: When VCOMH level falls from VCOMH to VCOML level, the level first falls to the GND level and then to the VCOML level.

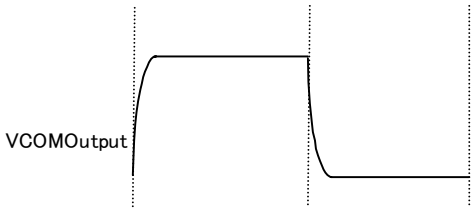
VEM[1]: VCOML equalize switch
VEM[1] = 1: When VCOMH level rises from VCOML level to VCOMH level, the level first goes up to the VCI level and then to the VCOMH level.

These bits reduce power consumption during VCOM drive period. In using this function, make sure VCI < VCOMH, GND > VCOML.

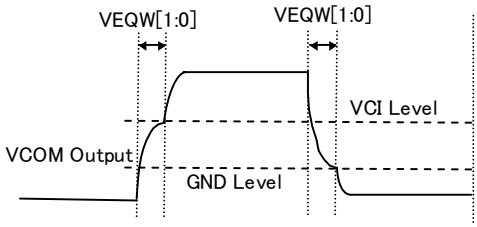
VEM[1:0]	Operation
2'h0	Setting inhibited
2'h1	Setting inhibited
2'h2	Setting inhibited
2'h3	VCOMH/VCOML equalize

When enabling VCOM function to reduce power consumption, check the display quality on the panel and effectiveness of power saving.

Description



i) VEQW[1:0]＝0h



ii) VEQW[1:0]≠0h,VEM[1:0]=3h

SPCW[2:0]

The bit is used to set source pre-charge period in 1 line period. Pre-charge period is set by SPCW[2:0] starting from the source output alternating position defined by SDT [2:0]. Source output is precharged only on the line where liquid crystal waveform inverts.

This function realizes power consumption reduction depending on image data. Check actual image quality and effect on the panel.

SPCW[2:0]	Source precharge Period
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVn (C1h, C2h, and C3h).

Interface Setting (C6h)

C6h	Interface Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	0	1	1	0	C6h
1st Parameter	1	#A	#B	X	0	0	0	VSPL	HSPL	0	EPL	DPL	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B="1" & Insert dummy read **VSPL** This bit sets the signal polarity of VSYNC pin. VSPL = 0: Low active. VSPL = 1: High active. **HSPL** This bit sets the signal polarity of HSYNC pin. HSPL = 0: Low active. HSPL = 1: High active. **EPL** This bit sets the signal polarity of ENABLE pin. EPL = 0: When ENABLE is set to 0, writing data to DB[17:0] pins is enabled. When ENABLE is set to 1, data is not written to DB[17:0] pins. EPL = 1: When ENABLE is set to 1, writing data to DB[17:0] pins is enabled. When ENABLE is set to 0, data is not written to DB[17:0] pins. **DPL** This bit sets the signal polarity of DOTCLK pin. DPL = 0: Data is input on the rising edge of DOTCLK. DPL = 1: Data is input on the falling edge of DOTCLK.												

Gamma Control

Gamma Set (C8h)

C8h	Gamma Set												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	0	1	0	0	0	C8h
1st parameter	1	1	↑	X	0	0	0	PR0P 00[4]	PR0P 00[3]	PR0P 00[2]	PR0P 00[1]]	PR0P 00[0]	XXh
2nd parameter	1	1	↑	X	0	0	0	PR0P 01[4]	PR0P 01[3]	PR0P 01[2]	PR0P 01[1]]	PR0P 01[0]	XXh
3rd parameter	1	1	↑	X	0	0	0	PR0P 02[4]	PR0P 02[3]	PR0P 02[2]	PR0P 02[1]	PR0P 02[0]	XXh
4th parameter	1	1	↑	X	PR0P 04[3]	PR0P 04[2]	PR0P 04[1]	PR0P 04[0]	PR0P 03[3]	PR0P 03[2]	PR0P 03[1]	PR0P 03[0]	XXh
5th parameter	1	1	↑	X	0	0	0	0	PR0P 05[3]	PR0P 05[2]	PR0P 05[1]	PR0P 05[0]	XXh
6th parameter	1	1	↑	X	0	0	0	PR0P 06[4]	PR0P 06[3]	PR0P 06[2]	PR0P 06[1]	PR0P 06[0]	XXh
7th parameter	1	1	↑	X	0	0	0	PR0P 07[4]	PR0P 07[3]	PR0P 07[2]	PR0P 07[1]	PR0P 07[0]	XXh
8th parameter	1	1	↑	X	0	0	0	PR0P 08[4]	PR0P 08[3]	PR0P 08[2]	PR0P 08[1]	PR0P 08[0]	XXh
9th parameter	1	1	↑	X	0	0	PIR0P 1[1]	PIR0P 1[0]	0	0	PIR0P 0[1]	PIR0P 0[0]	XXh
10th parameter	1	1	↑	X	0	0	PIR0P 3[1]	PIR0P 3[0]	0	0	PIR0P 2[1]	PIR0P 2[0]	XXh
11th parameter	1	1	↑	X	0	0	0	PR0N 00[4]	PR0N 00[3]	PR0N 00[2]	PR0N 00[1]	PR0N 00[0]	XXh
12th parameter	1	1	↑	X	0	0	0	PR0N 01[4]	PR0N 01[3]	PR0N 01[2]	PR0N 01[1]	PR0N 01[0]	XXh
13th parameter	1	1	↑	X	0	0	0	PR0N 02[4]	PR0N 02[3]	PR0N 02[2]	PR0N 02[1]	PR0N 02[0]	XXh
14th parameter	1	1	↑	X	PR0N 04[3]	PR0N 04[2]	PR0N 04[1]	PR0N 04[0]	PR0N 03[3]	PR0N 03[2]	PR0N 03[1]	PR0N 03[0]	XXh
15th parameter	1	1	↑	X	0	0	0	0	PR0N 05[3]	PR0N 05[2]	PR0N 05[1]	PR0N 05[0]	XXh
16th parameter	1	1	↑	X	0	0	0	PR0N 06[4]	PR0N 06[3]	PR0N 06[2]	PR0N 06[1]	PR0N 06[0]	XXh
17th parameter	1	1	↑	X	0	0	0	PR0N 07[4]	PR0N 07[3]	PR0N 07[2]	PR0N 07[1]	PR0N 07[0]	XXh
18th parameter	1	1	↑	X	0	0	0	PR0N 08[4]	PR0N 08[3]	PR0N 08[2]	PR0N 08[1]	PR0N 08[0]	XXh

19th parameter	1	1	↑	X	0	0	PIR0 N1[1]	PIR0 N1[0]	0	0	PIR0 N0[1]	PIR0 N0[0]	XXh
20th parameter	1	1	↑	X	0	0	PIR0 N3[1]	PIR0 N3[0]	0	0	PIR0 N2[1]	PIR0 N2[0]	XXh
Description	See “Gamma Correction Function” for detailed description of the parameters.												

Power Control

Power Setting (Common Setting) (D0h)

D0h	Power Setting (Common Setting)												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	0	D0h
1st parameter	1	#A	#B	X	0	0	0	0	0	WCBT	WCVRH	WCVC	XXh
2nd parameter	1	#A	#B	X	0	0	0	0	0	VC [2]	VC [1]	VC [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	VRH [4]	VRH [3]	VRH [2]	VRH [1]	VRH [0]	XXh
4th parameter	1	#A	#B	X	BTMODE	BTH [2]	BTH [1]	BTH [0]	0	BT [2]	BT [1]	BT [0]	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

WCVC

WCVC=1: Used to enable write to VC[2:0].
WCVC=0: Used to disable write to VC[2:0].

WCVRH

WCVRH =1: Used to enable write to VRH[4:0].
WCVRH =0: Used to disable write to VRH[4:0].

WCBT

WCBT=1: Used to enable write to BTMODE, BTH[2:0], and BT[2:0].
WCBT=0: Used to disable write to BTMODE, BTH[2:0], and BT[2:0].

VC[2:0]

The bit defines voltage level VCI1.

VC[2:0]	VCI1 (Step-up reference voltage)
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	2.88V
3'h3	2.76V
3'h4	2.64V
3'h5	2.52V
3'h6	2.40V
3'h7	VCI

Note: 1. VCI1 ≤ VCI.

Note 2: When VCI is 3V or less, VC should be set to 3'h7. Also, apply the electrical potential VCI directly to VCI1.

Description

VRH[4:0]

Sets VREG voltage from 1.6 x VCIR to 1.975 x VCIR. Set the VC and VRH bits so that VREG≤DDVDH-0.5V.

VRH[4:0]	VREG	VRH[4:0]	VREG
5'h00	Halt (Hi-z)	5'h17	VCIR x 1.775
5'h01-5'h0F	Setting inhibited	5'h18	VCIR x 1.800
5'h10	VCIR x 1.600	5'h19	VCIR x 1.825
5'h11	VCIR x 1.625	5'h1A	VCIR x 1.850
5'h12	VCIR x 1.650	5'h1B	VCIR x 1.875
5'h13	VCIR x 1.675	5'h1C	VCIR x 1.900
5'h14	VCIR x 1.700	5'h1D	VCIR x 1.925
5'h15	VCIR x 1.725	5'h1E	VCIR x 1.950
5'h16	VCIR x 1.750	5'h1F	VCIR x 1.975

BTMODE

Chooses a register used to set a step-up factor according to VCOM output level.

VCOM output	BTMODE = 0	BTMODE = 1
VCOMH	BT[2:0]	BTH[2:0]
VCOML	BT[2:0]	BT[2:0]

BT[2:0], BTH[2:0]

The bit sets a step-up factor according to selected voltage level. Smaller step-up factor leads to less power consumption.

BT[2:0], BTH[2:0]	DDVDH	VCL	VGH	VGL
3'h0	VCI1 x 2 [x 2]	-VCI1 [x -1]	Setting inhibited	
3'h1			DDVDH×3 [x 6]	-(VCI1+DDVDH×2) [x –5]
3'h2				-(DDVDH×2) [x –4]
3'h3				-(VCI1+DDVDH) [x –3]
3'h4			Setting inhibited	
3'h5			VCI1+DDVDH×2 [x 5]	-(VCI1+DDVDH×2) [x –5]
3'h6				-(DDVDH×2) [x –4]
3'h7				-(VCI1+DDVDH) [x –3]

Note: The step-up factors for VCI1 are shown in the brackets [].

VCOM Setting (D1h)

D1h	VCOM Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	0	1	D1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	WC VDV	WC VCM	XXh
2nd parameter	1	#A	#B	X	0	VCM [6]	VCM [5]	VCM [4]	VCM [3]	VCM [2]	VCM [1]	VCM [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	VDV [4]	VDV [3]	VDV [2]	VDV [1]	VDV [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **WCVCM** WCVCM=1: Used to enable write to VCM[6:0]. To set NVM write data, write 1 in WCVCM. WCVCM=0: Used to disable write to VCM[6:0]. Values loaded from NVM are retained even if this parameter is written. **WCVDV** WCVDV =1: Used to enable write to VDV[4:0]. To set NVM write data, write 1 in WCVDV. WCVDV =0: Used to disable write to VDV[4:0]. Values loaded from NVM are retained even if this parameter is written. **VCM[6:0]** The bit is used to set VCOMH voltage when VCOMR=1 within the range of VREG x 0.492 ~ 1.000. For details, see VCM setting table. **VDV[4:0]** The bit is used to set VCOM alternating amplitude within the range of VREG x 0.70 ~ 1.32. See VDV setting table.												

Description

VCM setting table

VCM[6:0]	VCOMH	VCM[6:0]	VCOMH
7’h00	VREG × 0.492	7’h30	VREG × 0.684
7’h01	VREG × 0.496	7’h31	VREG × 0.688
7’h02	VREG × 0.500	7’h32	VREG × 0.692
7’h03	VREG × 0.504	7’h33	VREG × 0.696
7’h04	VREG × 0.508	7’h34	VREG × 0.700
7’h05	VREG × 0.512	7’h35	VREG × 0.704
7’h06	VREG × 0.516	7’h36	VREG × 0.708
7’h07	VREG × 0.520	7’h37	VREG × 0.712
7’h08	VREG × 0.524	7’h38	VREG × 0.716
7’h09	VREG × 0.528	7’h39	VREG × 0.720
7’h0A	VREG × 0.532	7’h3A	VREG × 0.724
7’h0B	VREG × 0.536	7’h3B	VREG × 0.728
7’h0C	VREG × 0.540	7’h3C	VREG × 0.732
7’h0D	VREG × 0.544	7’h3D	VREG × 0.736
7’h0E	VREG × 0.548	7’h3E	VREG × 0.740
7’h0F	VREG × 0.552	7’h3F	VREG × 0.744
7’h10	VREG×0.556	7’h40	VREG×0.748
7’h11	VREG×0.560	7’h41	VREG×0.752
7’h12	VREG×0.564	7’h42	VREG×0.756
7’h13	VREG×0.568	7’h43	VREG×0.760
7’h14	VREG×0.572	7’h44	VREG×0.764
7’h15	VREG×0.576	7’h45	VREG×0.768
7’h16	VREG×0.580	7’h46	VREG×0.772
7’h17	VREG×0.584	7’h47	VREG×0.776
7’h18	VREG×0.588	7’h48	VREG×0.780
7’h19	VREG×0.592	7’h49	VREG×0.784
7’h1A	VREG×0.596	7’h4A	VREG×0.788
7’h1B	VREG×0.600	7’h4B	VREG×0.792
7’h1C	VREG×0.604	7’h4C	VREG×0.796
7’h1D	VREG×0.608	7’h4D	VREG×0.800
7’h1E	VREG×0.612	7’h4E	VREG×0.804
7’h1F	VREG×0.616	7’h4F	VREG×0.808
7’h20	VREG×0.620	7’h50	VREG×0.812
7’h21	VREG×0.624	7’h51	VREG×0.816
7’h22	VREG×0.628	7’h52	VREG×0.820
7’h23	VREG×0.632	7’h53	VREG×0.824
7’h24	VREG×0.636	7’h54	VREG×0.828
7’h25	VREG×0.640	7’h55	VREG×0.832
7’h26	VREG×0.644	7’h56	VREG×0.836
7’h27	VREG×0.648	7’h57	VREG×0.840
7’h28	VREG×0.652	7’h58	VREG×0.844
7’h29	VREG×0.656	7’h59	VREG×0.848
7’h2A	VREG×0.660	7’h5A	VREG×0.852
7’h2B	VREG×0.664	7’h5B	VREG×0.856
7’h2C	VREG×0.668	7’h5C	VREG×0.860
7’h2D	VREG×0.672	7’h5D	VREG×0.864
7’h2E	VREG×0.676	7’h5E	VREG×0.868
7’h2F	VREG×0.680	7’h5F	VREG×0.872

Description

VCM setting table

VCM[6:0]	VCOMH	VCM[6:0]	VCOMH
7'h60	VREG×0.876	7'h70	VREG×0.940
7'h61	VREG×0.880	7'h71	VREG×0.944
7'h62	VREG×0.884	7'h72	VREG×0.948
7'h63	VREG×0.888	7'h73	VREG×0.952
7'h64	VREG×0.892	7'h74	VREG×0.956
7'h65	VREG×0.896	7'h75	VREG×0.960
7'h66	VREG×0.900	7'h76	VREG×0.964
7'h67	VREG×0.904	7'h77	VREG×0.968
7'h68	VREG×0.908	7'h78	VREG×0.972
7'h69	VREG×0.912	7'h79	VREG×0.976
7'h6A	VREG×0.916	7'h7A	VREG×0.980
7'h6B	VREG×0.920	7'h7B	VREG×0.984
7'h6C	VREG×0.924	7'h7C	VREG×0.988
7'h6D	VREG×0.928	7'h7D	VREG×0.992
7'h6E	VREG×0.932	7'h7E	VREG×0.996
7'h6F	VREG×0.936	7'h7F	VREG×1.000

VDV setting table

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	VREG × 0.70	5'h10	VREG×1.02
5'h01	VREG × 0.72	5'h11	VREG×1.04
5'h02	VREG × 0.74	5'h12	VREG×1.06
5'h03	VREG × 0.76	5'h13	VREG×1.08
5'h04	VREG × 0.78	5'h14	VREG×1.10
5'h05	VREG × 0.80	5'h15	VREG×1.12
5'h06	VREG × 0.82	5'h16	VREG×1.14
5'h07	VREG × 0.84	5'h17	VREG×1.16
5'h08	VREG × 0.86	5'h18	VREG×1.18
5'h09	VREG × 0.88	5'h19	VREG×1.20
5'h0A	VREG × 0.90	5'h1A	VREG×1.22
5'h0B	VREG × 0.92	5'h1B	VREG×1.24
5'h0C	VREG × 0.94	5'h1C	VREG×1.26
5'h0D	VREG × 0.96	5'h1D	VREG×1.28
5'h0E	VREG × 0.98	5'h1E	VREG×1.30
5'h0F	VREG × 1.00	5'h1F	VREG×1.32

Note: Make sure that VCOM amplitude is 6.0V or less.

Power Setting for Normal Mode (D2h)
Power Setting for Partial Mode (D3h)
Power Setting for Idle Mode (D4h)

D2h	**Power Setting for Normal Mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	0	D2h
1st parameter	1	#A	#B	X	0	1	1	0	0	0	AP0 [1]	AP0 [0]	XXh
2nd parameter	1	#A	#B	X	0	DC10 [2]	DC10 [1]	DC10 [0]	0	DC00 [2]	DC00 [1]	DC00 [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DC30 [2]	DC30 [1]	DC30 [0]	XXh
D3h	**Power Setting for Partial Mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	0	1	1	D3h
1st parameter	1	#A	#B	X	0	1	1	0	0	0	AP1 [1]	AP1 [0]	XXh
2nd parameter	1	#A	#B	X	0	DC11 [2]	DC11 [1]	DC11 [0]	0	DC01 [2]	DC01 [1]	DC01 [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DC31 [2]	DC31 [1]	DC31 [0]	XXh
D4h	**Power Setting for Idle Mode**												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	0	1	0	0	D4h
1st parameter	1	#A	#B	X	0	1	1	0	0	0	AP2 [1]	AP2 [0]	XXh
2nd parameter	1	#A	#B	X	0	DC12 [2]	DC12 [1]	DC12 [0]	0	DC02 [2]	DC02 [1]	DC32 [0]	XXh
3rd parameter	1	#A	#B	X	0	0	0	0	0	DC32 [2]	DC32 [1]	DC32 [0]	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read Power control is defined for each mode. D2h is enabled in Normal Mode On and Idle Mode Off. D3h is enabled in Partial Mode On and Idle Mode Off. D4h is enabled in Normal Mode On, Idle Mode On, Partial Mode On, and Idle Mode On.												

Description

APn[1:0]

These bits adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current will enhance the drivability of the LCD, however more current will be consumed. Adjust the constant current taking the trade-off between the display quality and the current consumption into account.

APn[1:0]	**Constant current in operational amplifier in LCD power supply circuit**
2'h0	Halt operational amplifier and step-up circuits
2'h1	0.5
2'h2	0.75
2'h3	1

The values represent the ratios of constant current in respective APn[1:0] settings to the constant current when APn[1:0] is set to 2'h3.

DC0n[2:0]

These bits are used to set the step-up clock frequency of the step-up circuit that generates DDVDH.

DC0n[2:0]	**Step-up clock frequency (f_{DCDC1})**	
	PTDC = 1'b0	**PTDC = 1'b1**
3'h0	f_{OSC}/8	f_{OSC}/10
3'h1	f_{OSC}/10	f_{OSC}/12
3'h2	f_{OSC}/12	f_{OSC}/16
3'h3	f_{OSC}/16	f_{OSC}/20
3'h4	f_{OSC}/20	f_{OSC}/24
3'h5	f_{OSC}/24	f_{OSC}/32
3'h6	The step up circuit halts	The step up circuit halts
3'h7	f_{OSC}/32	f_{OSC}/32

Description

DC1n[2:0]

These bits are used to define the step-up clock frequency of the step-up circuit that generates VGH and VGL.

DC1n	Step-up clock frequency (f_{DCDC2})
3'h0	Line frequency / 2
3'h1	Line frequency / 4
3'h2	Line frequency / 8
3'h3	Line frequency / 16
3'h4	Line frequency / 32
3'h5	Setting inhibited
3'h6	The step-up circuit halts
3'h7	Setting inhibited

DC3n[2:0]

These bits are used to define the step-up clock frequency of the step-up circuit that generates VCL.

DC30[2:0] DC32[2:0]	Step-up clock frequency (f_{DCDC3})
3'h0	$f_{OSC}/8$
3'h1	$f_{OSC}/10$
3'h2	$f_{OSC}/12$
3'h3	$f_{OSC}/16$
3'h4	$f_{OSC}/20$
3'h5	$f_{OSC}/24$
3'h6	Setting inhibited
3'h7	$f_{OSC}/32$

Step-up clock operation is synchronized with display operation. A division ratio is reset at the start of a line.

DITHER Setting (DAh)

DAh	DITHER Setting												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	0	1	1	0	1	0	DAh
1st parameter	1	#A	#B	X	OFSX[1]	OFSX[0]	OFSY[1]	OFSY[0]	0	PTN_SEL	SAT_LOW	DITHER_ON	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B="1" & Insert dummy read

OFSX[1:0]

This bit sets horizontal movement of a dither pattern according to coordinates of display data.

OFSX[1:0]	Horizontal movement
2'h0	0 (Default)
2'h1	+1
2'h2	+2
2'h3	+3

OFSY[1:0]

This bit sets vertical movement of a dither pattern according to coordinates of display data.

OFSY[1:0]	Vertical movement
2'h0	0 (Default)
2'h1	+1
2'h2	+2
2'h3	+3

PTN_SEL

This bit sets a dither pattern.

PTN_SEL	Dither pattern
1'h0	2 x 2 (Size)
1'h1	4 x 4 (Size)

SAT_LOW

This bit regards some grayscales to lower grayscales as follows.

SAT_LOW	Grayscale
1'h0	Higher grayscale; grayscales 252 to 255 are regarded as grayscale 63.
1'h1	Lower grayscale; grayscales 0 to 3 are regarded as grayscale 0)

DITHER_ON

When this bit is enabled, it performs dither processing on image data written to frame memory. Dither processing is enabled only when 24bpp color format is selected. Dither processing is performed to display a large number of colors by using a small number of colors.

NVM Control

NVM Access Control (E0h)

E0h	NVM Access Control												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	0	E0h
1st parameter	1	#A	#B	0	0	0	0	0	0	0	0	NVAE	XXh
2nd parameter	1	#A	#B	X	0	FTT	CALB	0	0	0	0	0	XXh
3rd parameter	1	#A	#B	X	0	0	0	TEM	0	0	VERIFLGWR	VERIFLGER	XXh

Description

Write #A="1" #B="↑"

Read #A="↑" #B=" 1" & Insert dummy read

NVAE

The bit is used to enable access to NVM when NVAE=1.

CALB

When CALB=1, all data on the NVM are read to be updated onto the corresponding registers. CALB=0 is returned when loading is finished. Execute D0h command after executing CALB. Set CALB when display is off.

FTT

NVM control register. When FTT=1, NVM write/erase is triggered. The bit is set to 0 when NVM write/erase verifies operation is finished.

VERIFLGER

This bit is used for data read only. Data write to this bit is ignored. Data erase and erase verify are executed before performing a data write. This bit is written according to the result of the erase verify.

If erase verify result is good: VERIFLGER=1
If erase verify result is not good: VERIFLGER=0

VERIFLGWR

This bit is used for data read only. Data write to this bit is ignored. Data write and write verify are executed after a data erase. This bit is written according to the result of the write verify.

If write verify result is good: VERIFLGWR=1
If write verify result is not good: VERIFLGWR=0

TEM

TE is used to output the result of automatic NVM write data verify.

TEM	TE output
1'h0	Tearing Effect
1'h1	TE = 0 The write data was not correct. TE = 1 The write data was correct.

NVM Write Data Control (E1h)

E1h	NVM write Data Control												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	0	0	0	1	E1h
1st parameter	1	#A	#B	X	0	0	0	0	0	0	0	WCD DB	XXh
Description	Write #A="1" #B="↑" Read #A="↑" #B=" 1" & Insert dummy read **WCDDB** WCDDB=1: Used to enable write to Supplier ID1[15:0] and ID2 [15:0]. To set NVM write data, write 1 in WCDDB. WCDDB=0: Used to disable write to Supplier ID1[15:0] and ID2[15:0]. Values loaded from NVM are retained even if this parameter is written.												

Interface Control

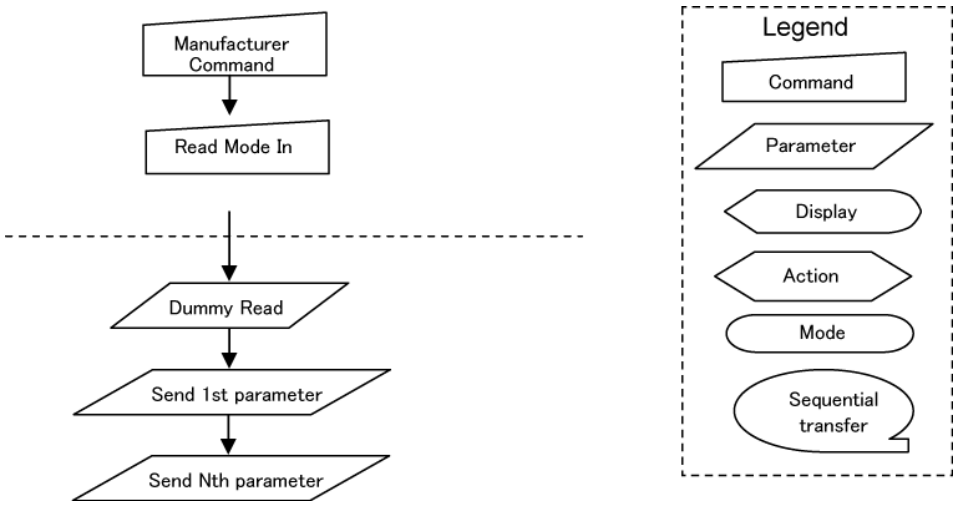
Read Mode In (EFh)

EFh	Read Mode In (EFh)												
	DCX	RDX	WRX	DB[17:8]	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	0	1	↑	X	1	1	1	0	1	1	1	1	EFh

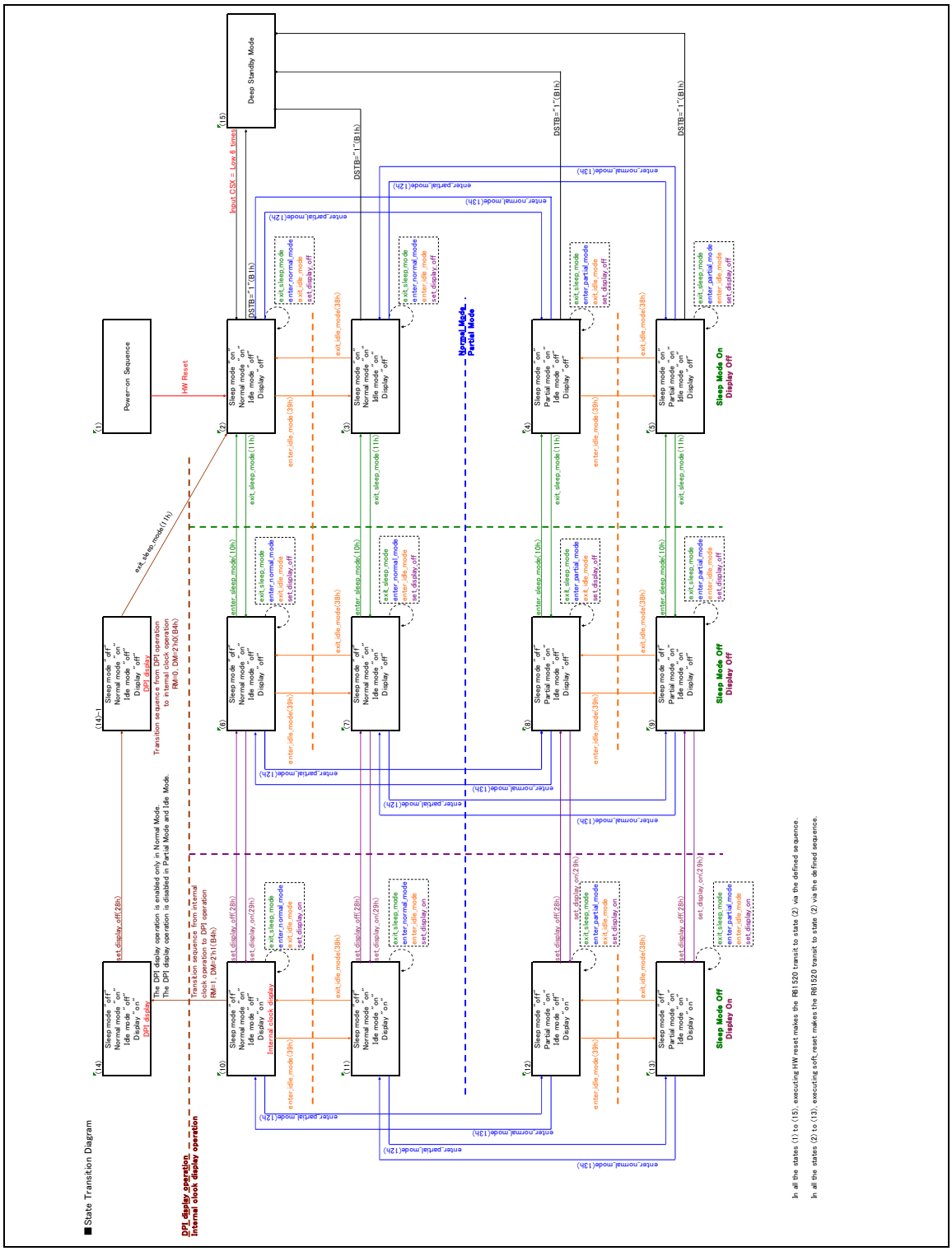
Description

This command is used to read registers that can be written/read by Manufacturer Command in DBI Type C operation. When this command is set, the R61581B0 enters read mode. When CSX is set to High, the R61581B0 exits read mode. When CSX is set to Low after that, the R61581B0 enters write mode. See the table below for whether Read Mode In command is required.

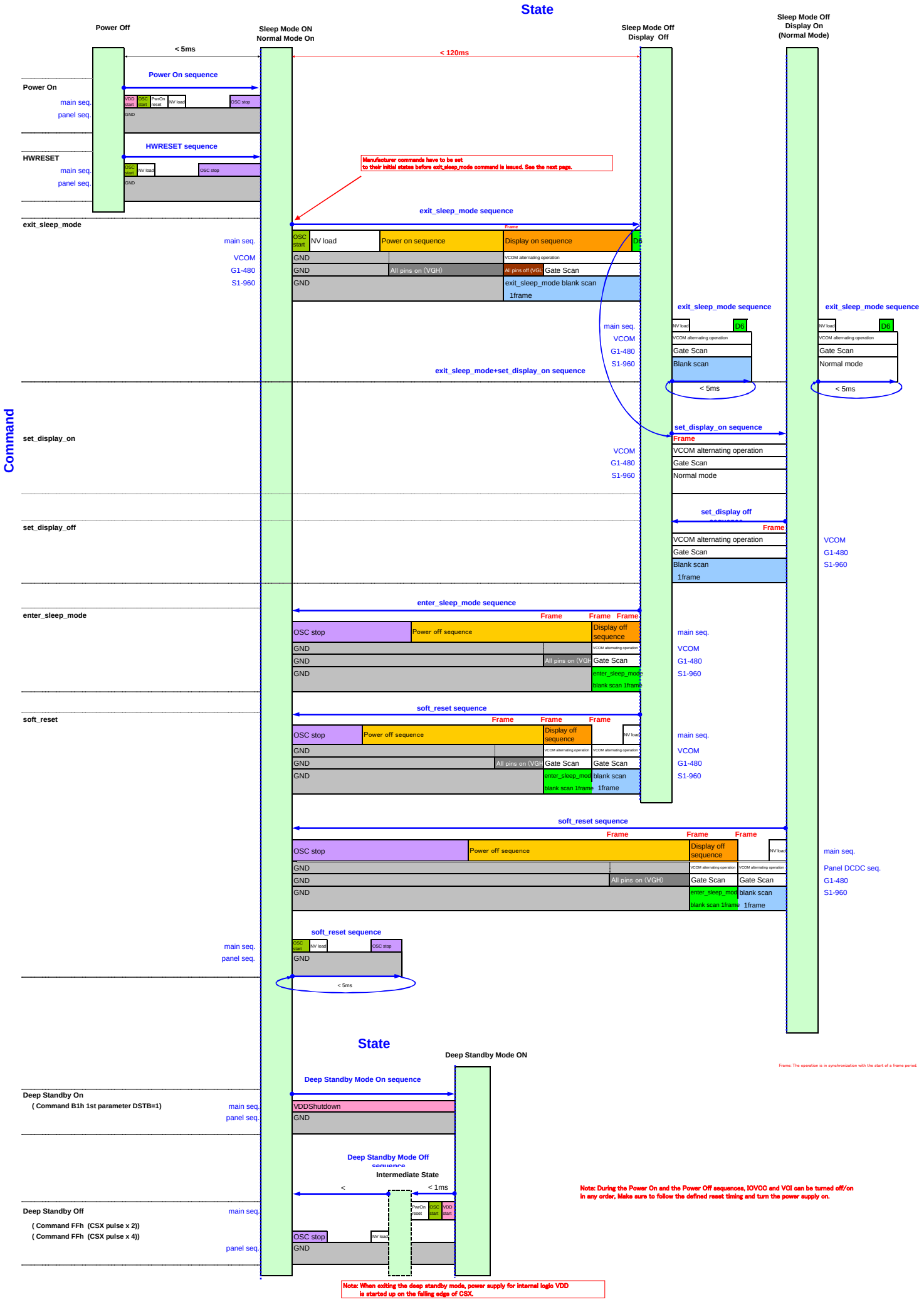
Operational code (Hex)	Command	Whether Read Mode In command is required
B0h	Manufacturer Command Access Protect	Yes
B1h	Low Power Mode Control	Yes
B3h	Frame Memory Access and Interface Setting	Yes
B4h	Display Mode and Frame Memory Write Mode Setting	Yes
B8h	Backlight Control 1	Yes
B9h	Backlight Control 2	Yes
BAh	Backlight Control 3	No
BFh	Device Code Read	No
C0h	Panel Drive Setting	Yes
C1h	Display Timing Setting for Normal/Partial Mode	Yes
C2h	Display Timing Setting for Partial Mode	Yes
C3h	Display Timing Setting for Idle Mode	Yes
C4h	Source/VCOM Gate Driving Timing Setting	Yes
C6h	Interface Setting	Yes
C8h	Gamma Set	Yes
D0h	Power Setting (Common Setting)	Yes
D1h	VCOM Setting	Yes
D2h	Power Setting for Normal Mode	Yes
D3h	Power Setting for Partial Mode	Yes
D4h	Power Setting for Idle Mode	Yes
D8h	Sequence Control	Yes
DAh	DITHER Setting	Yes
E0h	NVM Access Control	Yes
EFh	Read Mode In	-

EFh	Read Mode In
Flow Chart	

State Transition Diagram



■ R61581 State & Command sequence



Power/Display On/Off Sequence Examples

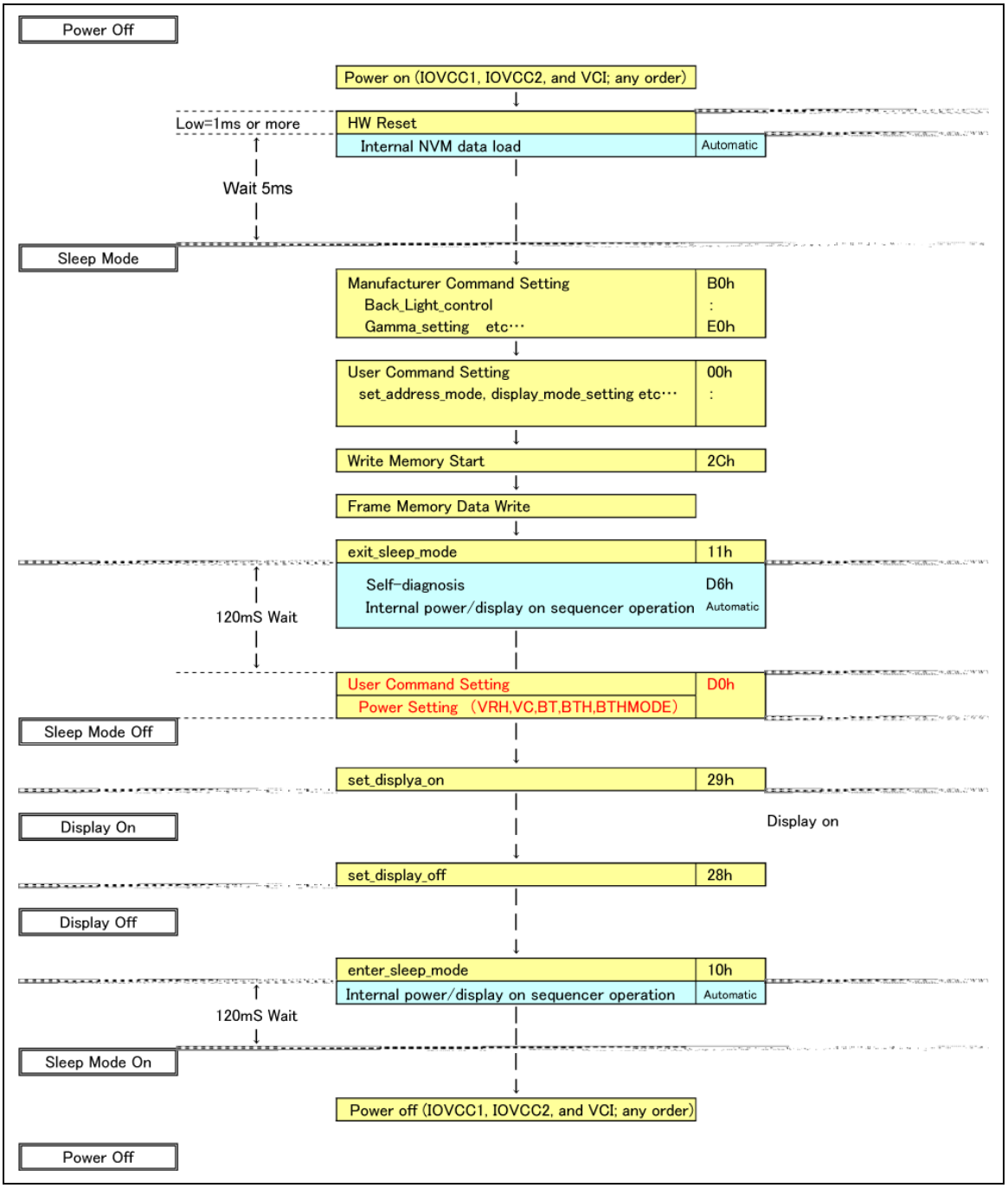


Figure 32

Deep Standby Mode On/Off Sequence Examples

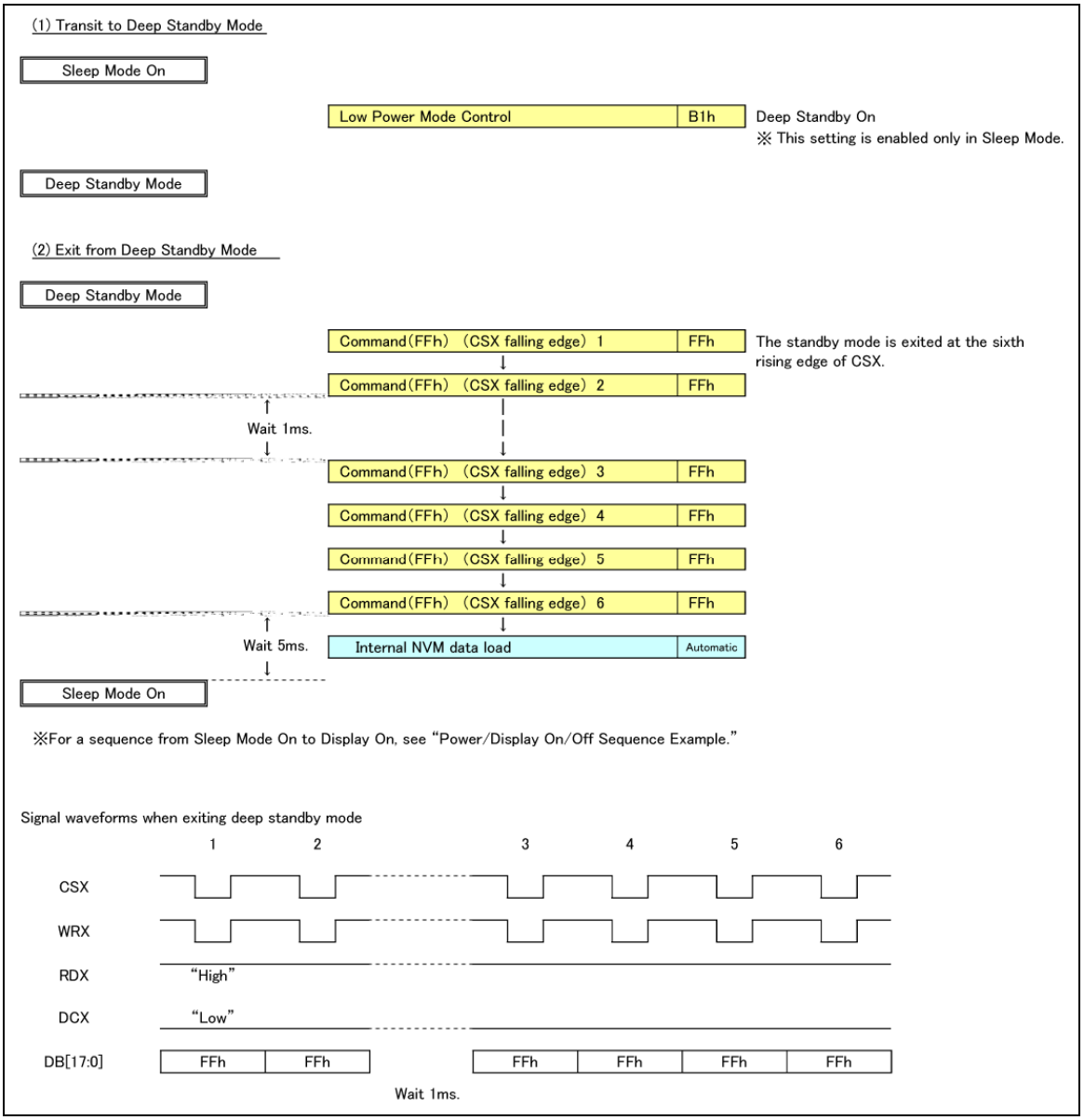


Figure 33

Reset

The R61581B0 initial internal setting is done with a RESET input. During the RESET period, no access, whether it is command write or frame memory data write operation, is accepted. The source driver unit and the power supply circuit unit are also reset to the respective initial states when RESET signal is inputted to the R61581B0.

1. Initial state of command

   The initial state of command is shown in Default Modes and Values table in Command List. See "Default Modes and Values." The command setting is initialized to the default value when executing a Hardware Reset.

2. Frame Memory data initial state

   The Frame Memory data is not automatically initialized by inputting RESET. It needs to be initialized by software during Display Off period.

3. Input/output pin initial state

Table 27

Pin name	Input/Output Pin Initial State
DB[17:0]	Hi-Z
DOUT	Hi-Z
TE	GND
LEDPWM	GND
VDD	1.5V
VCI1	Hi-Z
C11P/C11M	Hi-Z/Hi-Z
C12P/C12M	Hi-Z/Hi-Z
C13P/C13M	Hi-Z/GND
C21P/C21M	VCI/GND
C22P/C22M	VCI/GND

Pin name	Input/Output Pin Initial State
VREG	VGS
VCOML	GND
VCOMH	VCI (DDVDH)
VCL	GND
VGL	GND
VGH	VCI
DDVDH	VCI
VCOM	GND
S[960:1]	GND
G[480:1]	GND

Frame Memory

The frame memory retains image data of up to 345,600 bytes (480 x 320 x 18 bits).

Address Mapping from Memory to Display

Normal Display On or Partial Mode On

In this mode, a content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 01DFh is displayed.

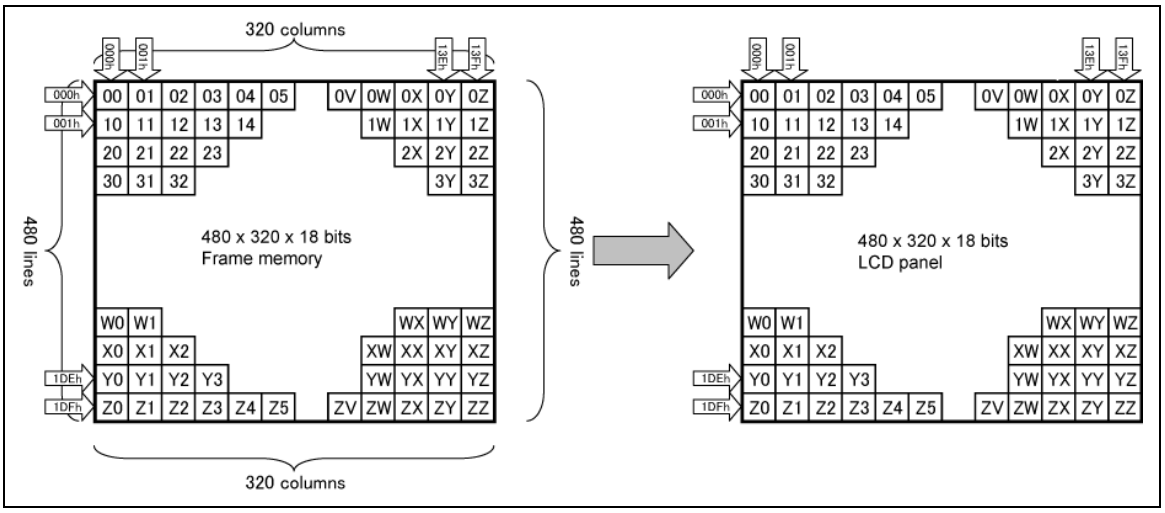


Figure 34

Vertical Scroll Example

Case 1: TFA+VSA+BFA≠NL

If such an setting is made, the command will be accepted but an undesirable image will be displayed.

Case 2: TFA+VSA+BFA = NL (Rolling scrolling)

Example 2-a: when TFA = 0, VSA = 480, BFA = 0 and VSP = 40

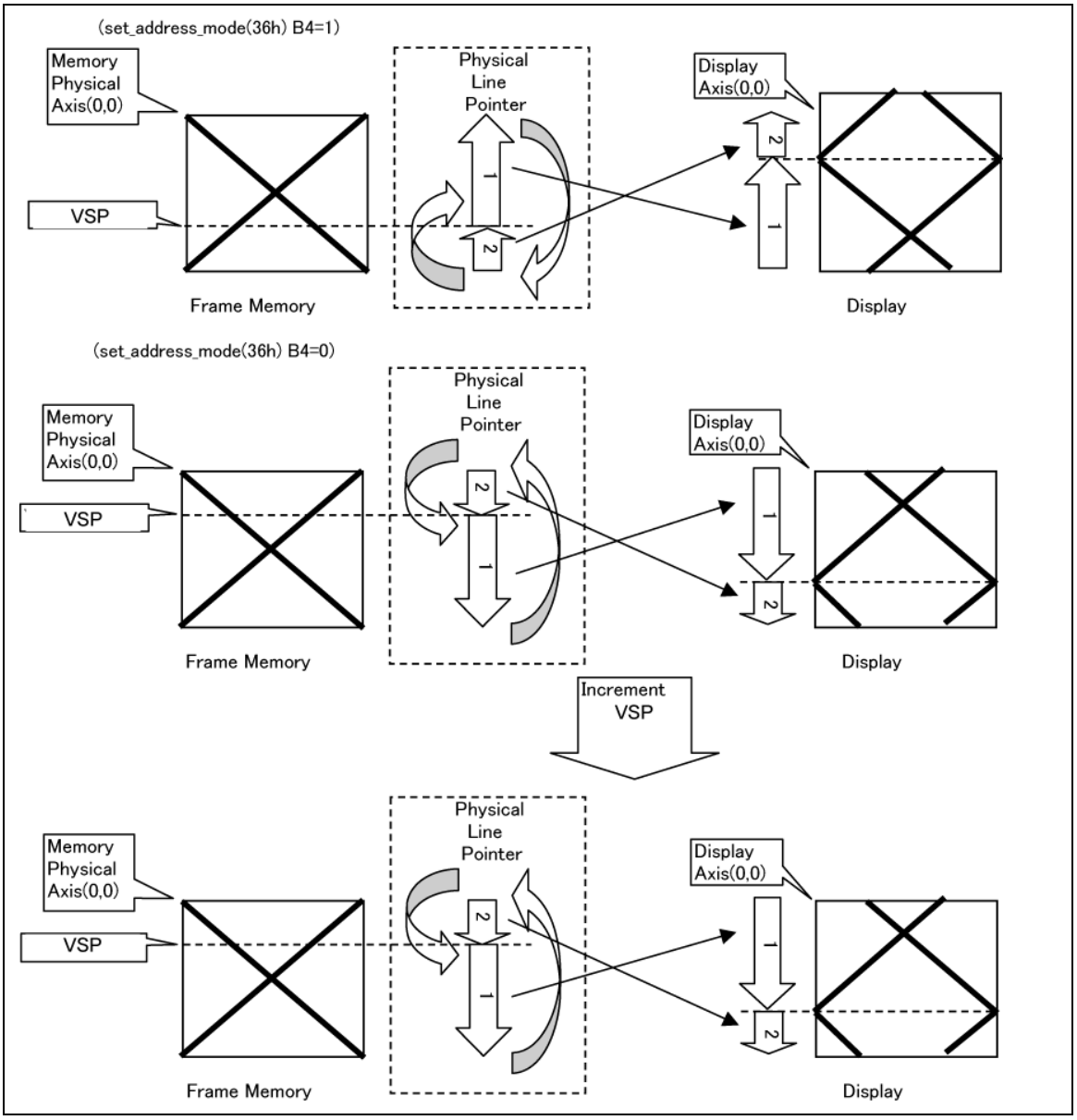


Figure 35

Example 2-b: when TFA = 30, VSA = 370, BFA = 0 and VSP = 80

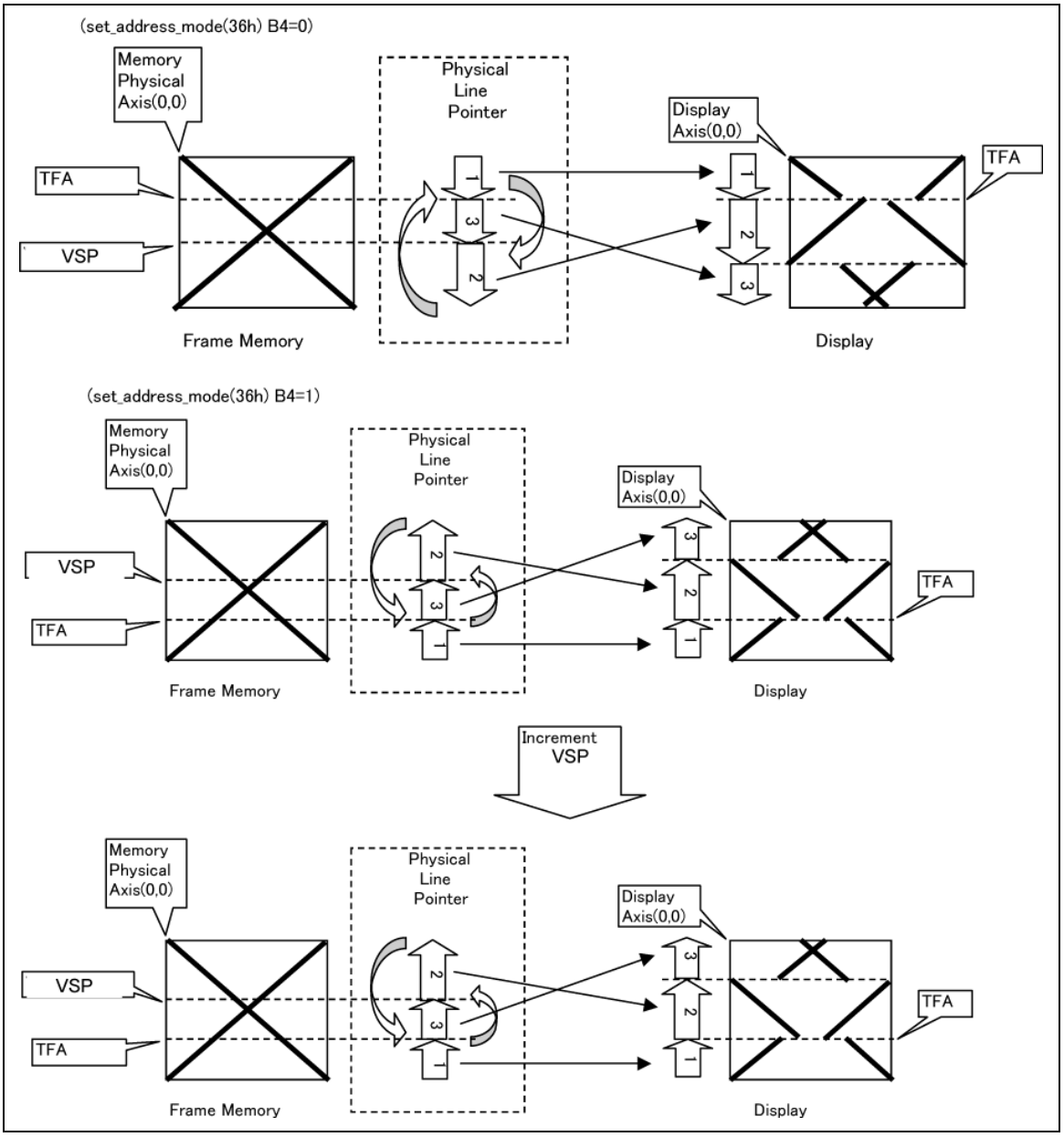


Figure 36

Write/Read Direction from/to Host Processor

Below figure illustrates data stream from the host processor.

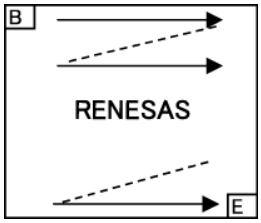


Figure 37

The data is written in the order illustrated above. The Counter which dictates write position on the physical memory is controlled by "set_address_mode (36h)" command Bits B5, B6, B7 as illustrated below.

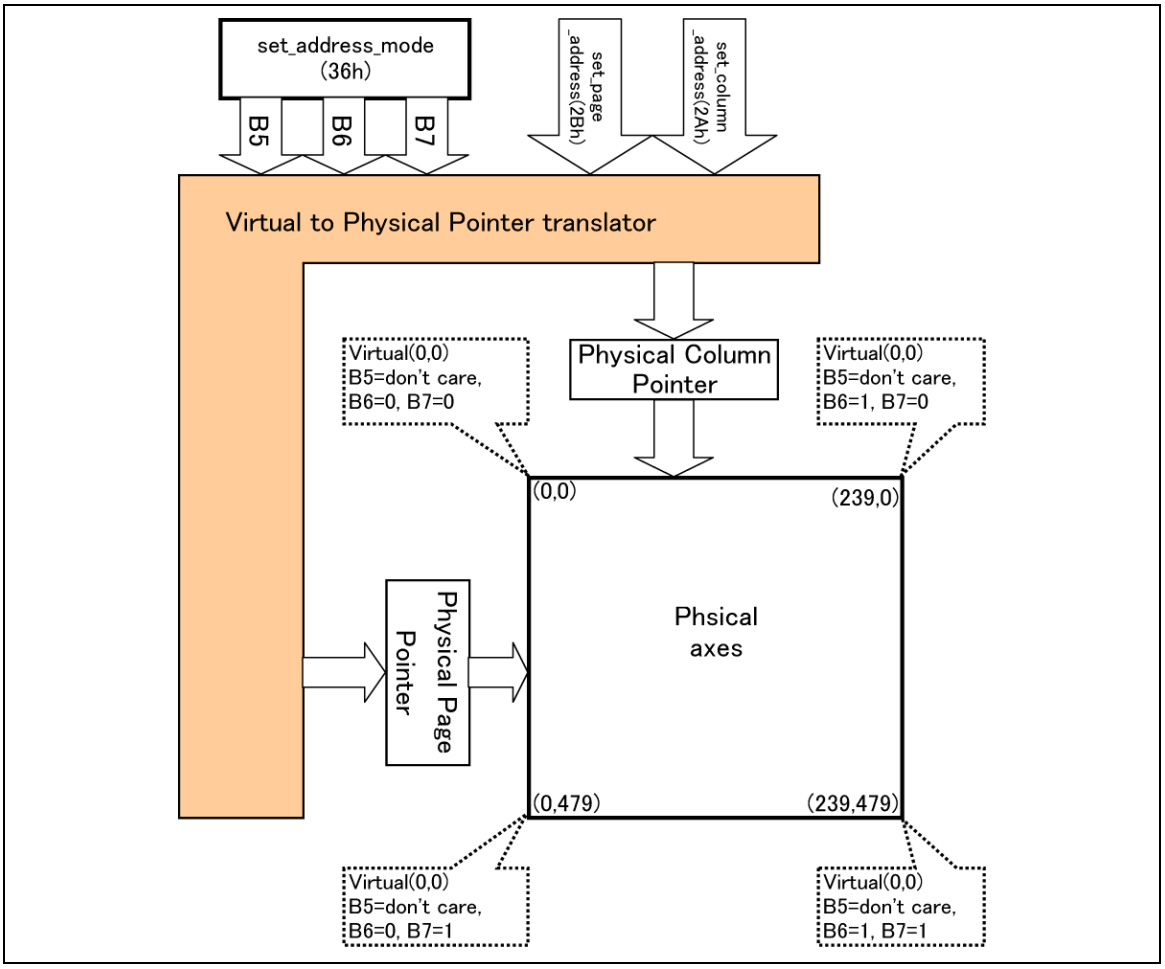


Figure 38

Table 28

B5	B6	B7	Column Address	Page Address
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

For each image orientation, the controls on the column and page counters apply as below.

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by set_address_mode (36h) bits B7, B6 and B5. The write order for each pixel unit is as follows.

Table 29

D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Table 30

Condition	Column counter	Page counter	Note
When commands write_memory_start (2Ch) and read_memory_start (2Eh) are received.	Back to Start Column	Back to Start Page	
Execute Pixel Read/Write	Increment by 1	No change	
When column counter value is larger than ”End Column”	Back to Start Column	Increment by 1	
When column counter value is larger than ”End Column” and page counter value is larger than “End Page”	STOP	STOP	Entry Mode(B3h) WEMODE=0
	Back to Start Column	Back to Start Page	Entry Mode(B3h) WEMODE=1

One pixel unit represents 1 column and 1 page counter value on the Frame Memory. See the next page for the resultant image for each orientation setting.

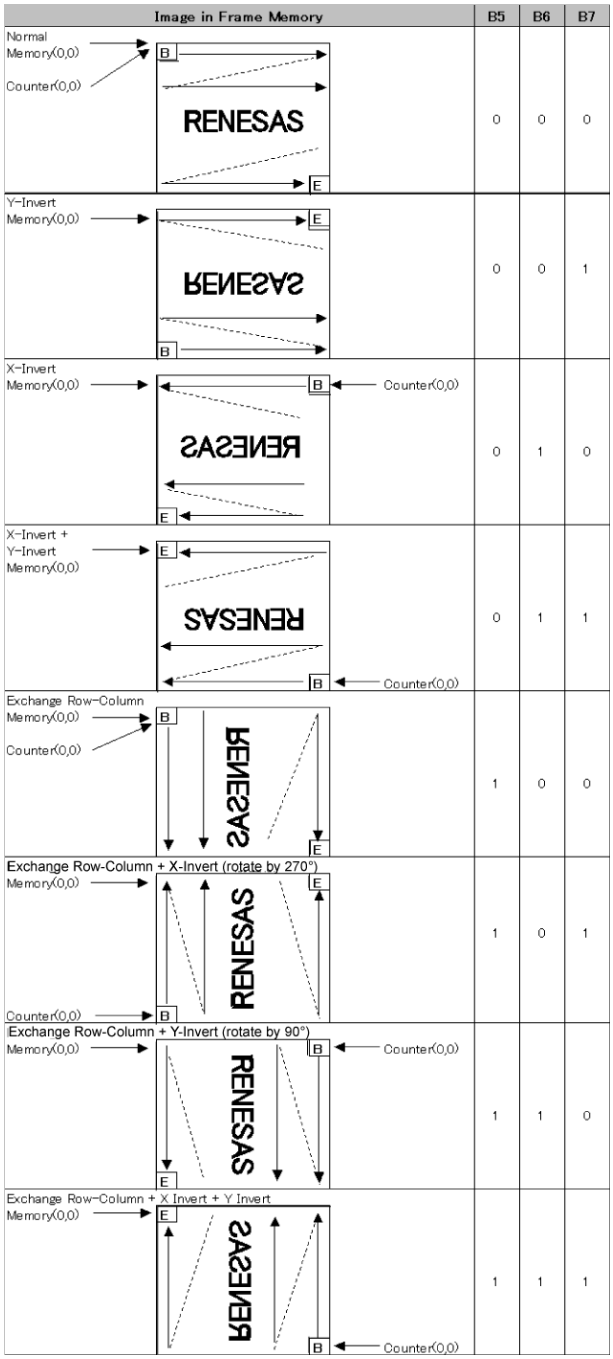


Image in Frame Memory
B5
B6
B7
Normal
Memory(0,0)
Counter(0,0)
RENESAS
0 0 0
Y-Invert
Memory(0,0)
0 0 1
X-Invert
Memory(0,0)
Counter(0,0)
0 1 0
X-Invert +
Y-Invert
Memory(0,0)
0 1 1
Exchange Row-Column
Memory(0,0)
Counter(0,0)
1 0 0
Exchange Row-Column + X-Invert (rotate by 270°)
Memory(0,0)
Counter(0,0)
1 0 1
Exchange Row-Column + Y-Invert (rotate by 90°)
Memory(0,0)
Counter(0,0)
1 1 0
Exchange Row-Column + X Invert + Y Invert
Memory(0,0)
Counter(0,0)
1 1 1

Figure 39

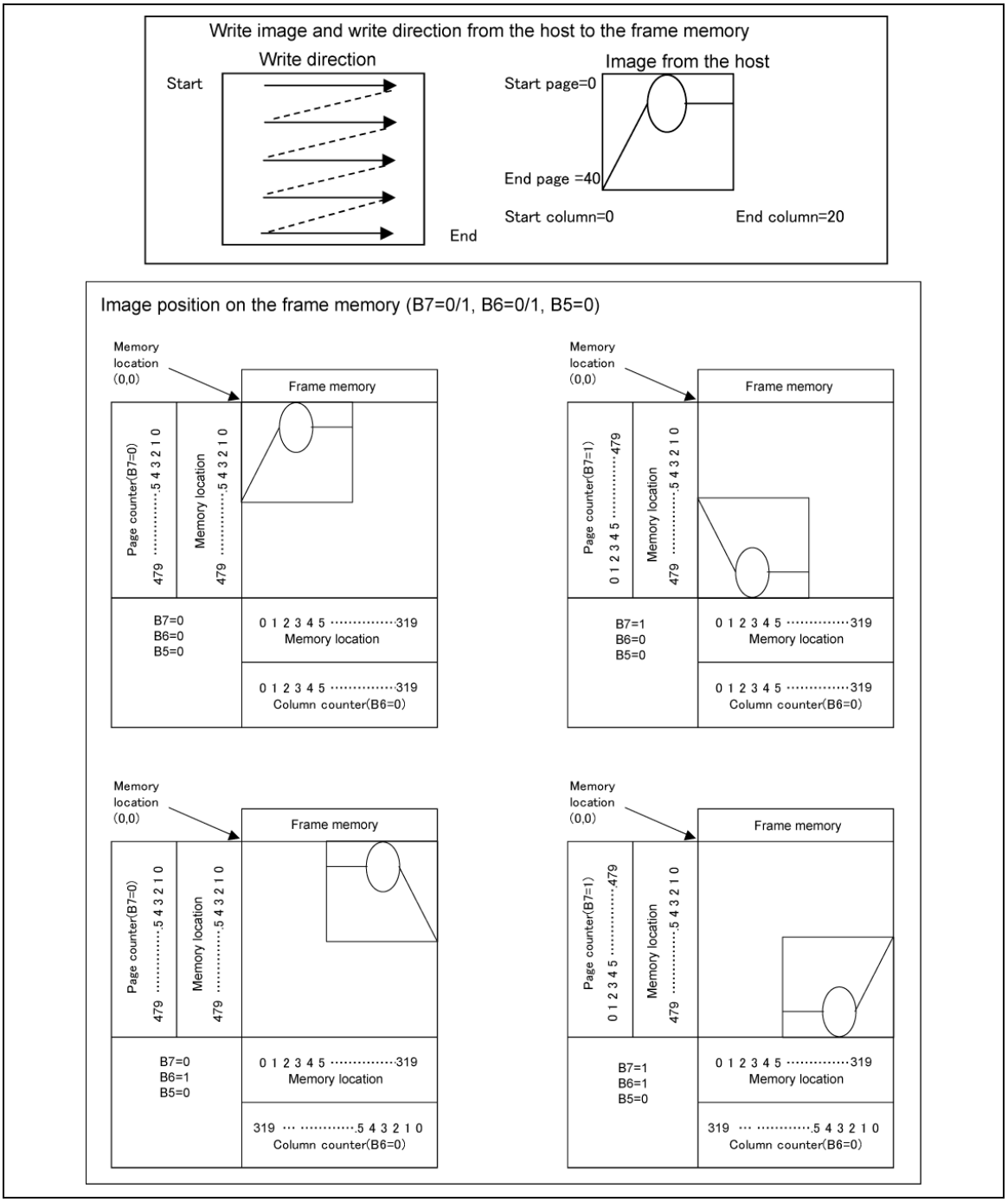

Write image and write direction from the host to the frame memory
Write direction
Start
End
Image from the host
Start page=0
End page =40
Start column=0
End column=20
Image position on the frame memory (B7=0/1, B6=0/1, B5=0)
Memory location (0,0)
Frame memory
Page counter(B7=0)
479 ·····5 4 3 2 1 0
Memory location
479 ·····5 4 3 2 1 0
B7=0
B6=0
B5=0
0 1 2 3 4 5 ·····319
Memory location
0 1 2 3 4 5 ·····319
Column counter(B6=0)
Memory location (0,0)
Frame memory
Page counter(B7=1)
0 1 2 3 4 5 ·····479
Memory location
479 ·····5 4 3 2 1 0
B7=1
B6=0
B5=0
0 1 2 3 4 5 ·····319
Memory location
0 1 2 3 4 5 ·····319
Column counter(B6=0)
Memory location (0,0)
Frame memory
Page counter(B7=0)
479 ·····5 4 3 2 1 0
Memory location
479 ·····5 4 3 2 1 0
B7=0
B6=1
B5=0
0 1 2 3 4 5 ·····319
Memory location
319 ··· ·····5 4 3 2 1 0
Column counter(B6=0)
Memory location (0,0)
Frame memory
Page counter(B7=1)
0 1 2 3 4 5 ·····479
Memory location
479 ·····5 4 3 2 1 0
B7=1
B6=1
B5=0
0 1 2 3 4 5 ·····319
Memory location
319 ··· ·····5 4 3 2 1 0
Column counter(B6=0)

Figure 40

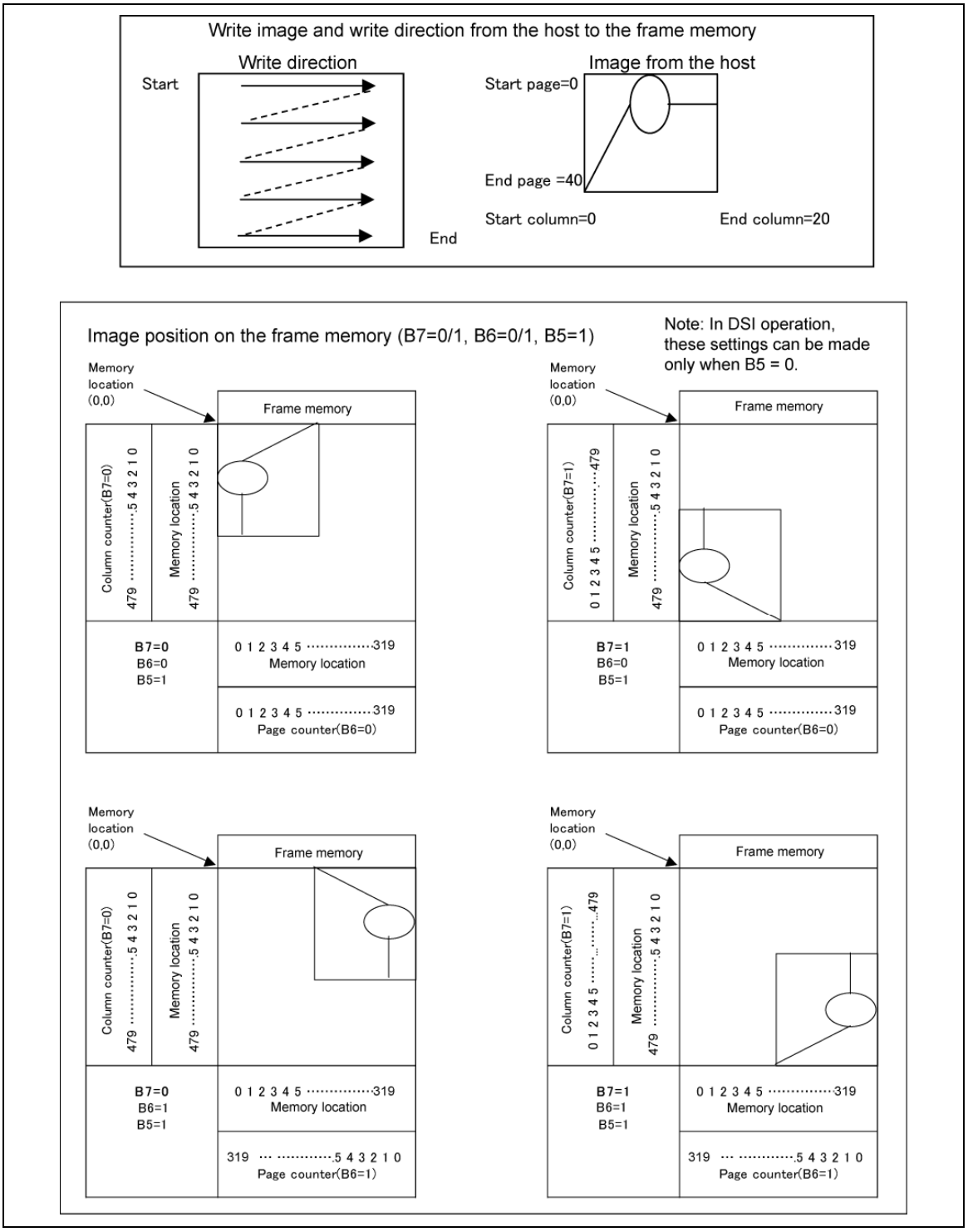

Write image and write direction from the host to the frame memory
Write direction
Start
End
Image from the host
Start page=0
End page =40
Start column=0
End column=20
Image position on the frame memory (B7=0/1, B6=0/1, B5=1)
Note: In DSI operation, these settings can be made only when B5 = 0.
Memory location (0,0)
Frame memory
Column counter(B7=0)
Column counter(B7=1)
Memory location
B7=0 B6=0 B5=1
B7=1 B6=0 B5=1
B7=0 B6=1 B5=1
B7=1 B6=1 B5=1
0 1 2 3 4 5 ·····319
Memory location
Page counter(B6=0)
319 ··· ·····5 4 3 2 1 0
Page counter(B6=1)

Figure 41

Self-Diagnostic Functions

The R61581B0 supports the self-diagnostic functions. Set get_diagnostic_result (0Fh) 1st parameter's D6 bit as following flow chart.

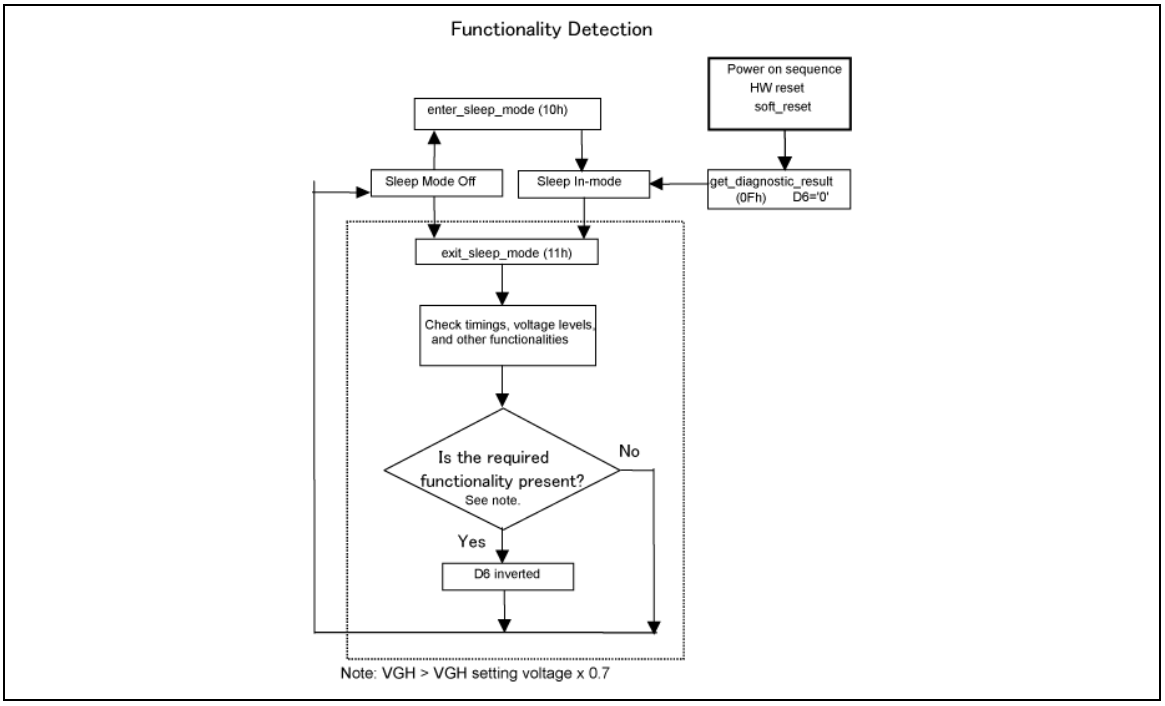


Figure 42

Functionality Detection

The exit_sleep_mode command is a trigger for the Functionality Detection function. If VGH level is VGH setting value x 0.7 or greater, the step-up circuit is regarded as operating properly, then bit D6 of the SDR register is inverted.

Dynamic Backlight Control Function

The R61581B0 supports BLC (backlight control) function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The display image is dynamically controlled by BLC function. The availability of this function ranges from moving picture such as TV image to still picture such as menu. The histogram of display data is analyzed by BLC function, according to the brightness range of backlight set by parameters. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image.

Note 1: The BLC setting is enabled by BLCON bit setting (B8h: Backlight Control).

Note 2: The effect of BLC function on power efficiency and display quality depends on image data and the setting. Check display quality on the panel.

Note 3: The BLC function is disabled in Idle Mode On and Display Invert Mode On. Use BLC function (BLCON = 1) in Idle Mode Off and Display Invert Mode Off.

- Control backlight dynamically according to the image histogram.
- PWM pin for LED backlight adjustment
- PWM signal control register set by the host processor. Backlight dimmer is adjusted by calculating internally decided PWM value and maximum PWM value from the host processor.

System Configuration

1. The PWM signal is used to directly control the R61581B0 and LED driver IC. The LED driver IC is controlled entirely via the R61581B0.

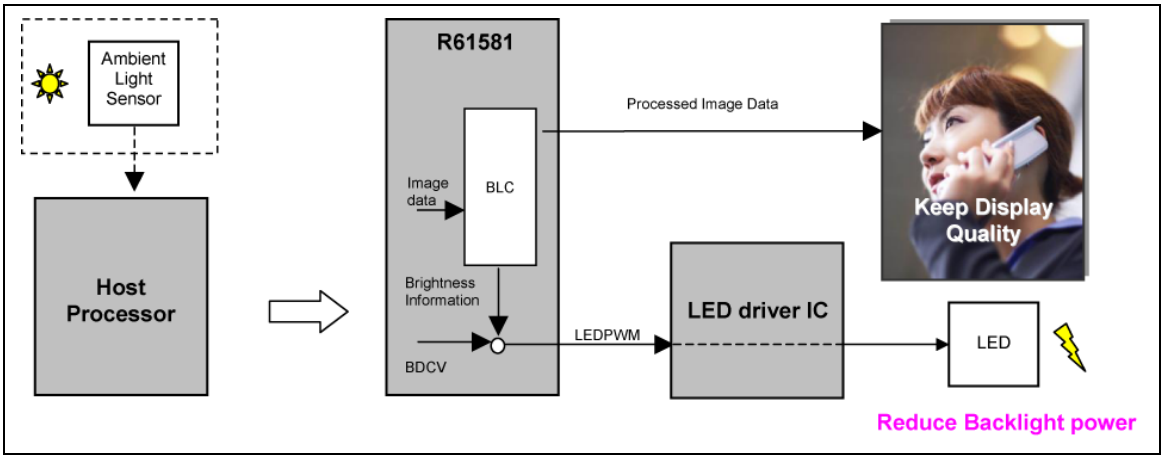


Figure 43

2. The host processor reads LED brightness information internally generated by BLC processing from the R61581B0 via MIPI DBI. Then, the LED driver IC is controlled from the host processor. There is the time difference between brightness adjustment by PWM and displaying data processed from the R61581B0. Check the effect on the image.

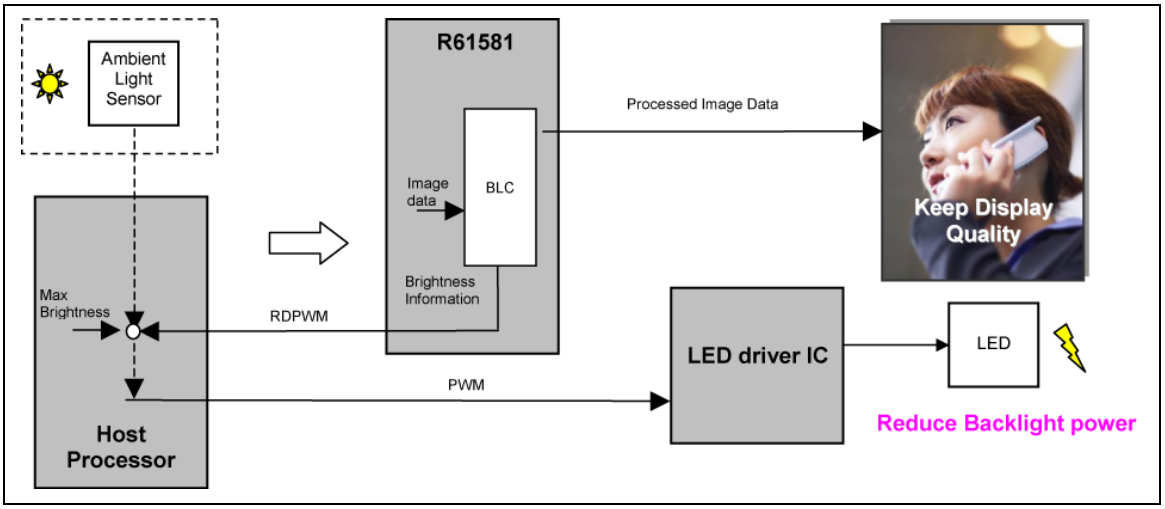


Figure 44

BLC Parameter Setting

The backlight control function has the following two functions.

- Image processing and backlight control processing
- Retain the grayscale of the display image that is turned into white

These functions are set by the following parameters.

(1) BLC operating threshold (THREW)

(2) Set the amount of change of a threshold grayscale value (Dth) per frame (PITCHW)

(3) Difference between two grayscale values counted by the histogram counter (CGAPW)

(4) Backlight brightness adjustment range (ULMTW and LLMTW)

(5) Gamma conversion table (TBL_MIN, TBLx[7:0])

(6) Interpolation to prevent display image from being white (COEFK)

(1) THREW[4:0]

This parameter sets the ratio (percentage) of the maximum number of pixels that makes display image white (= data "63") to the total of pixels by image processing. The ratio can be set from 0 to 62% in units of two percent. After this parameter sets the number of pixels that makes display image white, a threshold grayscale value (Dth) that makes display image white is set so that the number of the pixels set by this parameter does not change.

To reduce the power by about 30 percent, set the above ratio to thirty percent (THREW = 5'h0F). When the value set by this parameter exceeds the range of Dth mentioned later, the priority is given to the range of a threshold grayscale value (Dth).

According to the relationship between a threshold grayscale value (Dth) and gamma conversion table (see (5)), the rate of backlight brightness reduction (= the rate of power reduction) and image correction factor are set.

- The larger THREW value tends to enhance the effect of reducing backlight power, and increases the image correction factor. In this case, the effect on display image increases (See note 1).
- The smaller THREW value tends to reduce the effect of reducing backlight power, and decreases the image correction factor. In this case, the effect on display image decreases (See note 1).

Notes: 1. the tendency for backlight power reduction and the effect on image by BLC function depend on image data. Check display quality.
2. The histogram analysis result is enabled from the next frame.

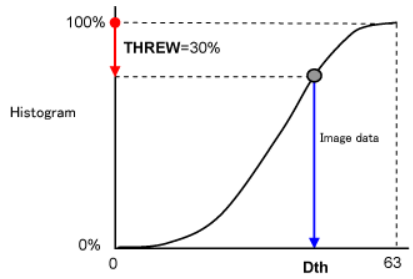


Figure 45

(2) PITCHW[3:0]

This parameter sets the amount of change of a threshold grayscale value (Dth) that makes display image white per frame in units of one half of the grayscale. When the target (Dth_t) is changed by the histogram change of input image including video image, this parameter can adjust the amount of changing a threshold grayscale value (Dth). So, this parameter is effective in reducing sharp change of backlight brightness.

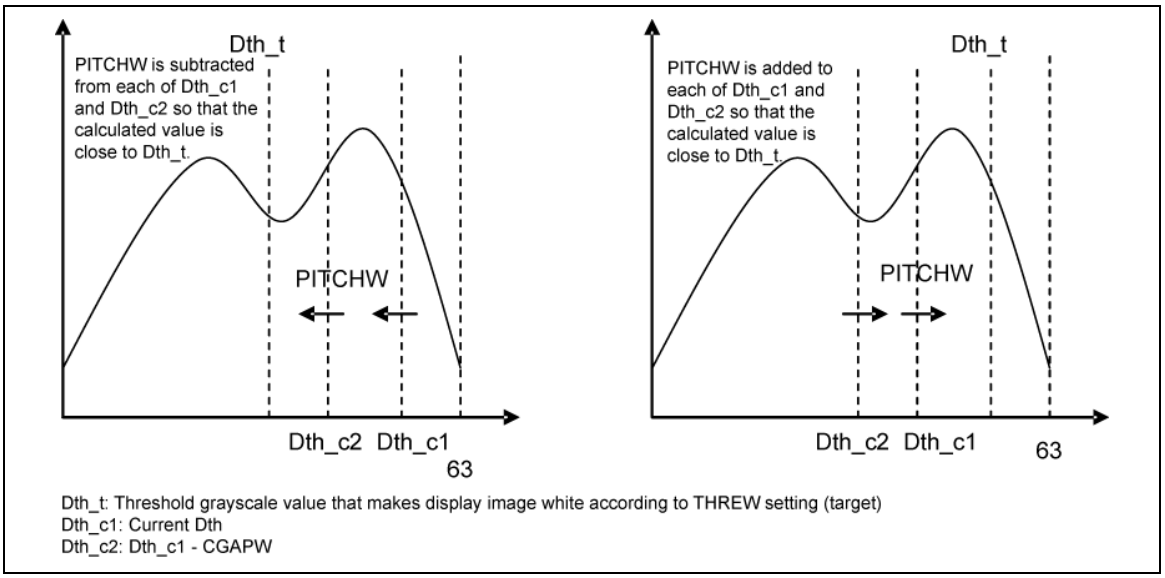


Figure 46

(3) CGAPW[4:0]

The difference of the two grayscales (Dth_c1 and Dth_c2) counted by the present threshold counter is set in units of one half of the grayscale. This parameter is effective in slowing the change of a threshold grayscale value (Dth). So, the speed of the change of Dth is adjusted to reduce subtle change and flicker.

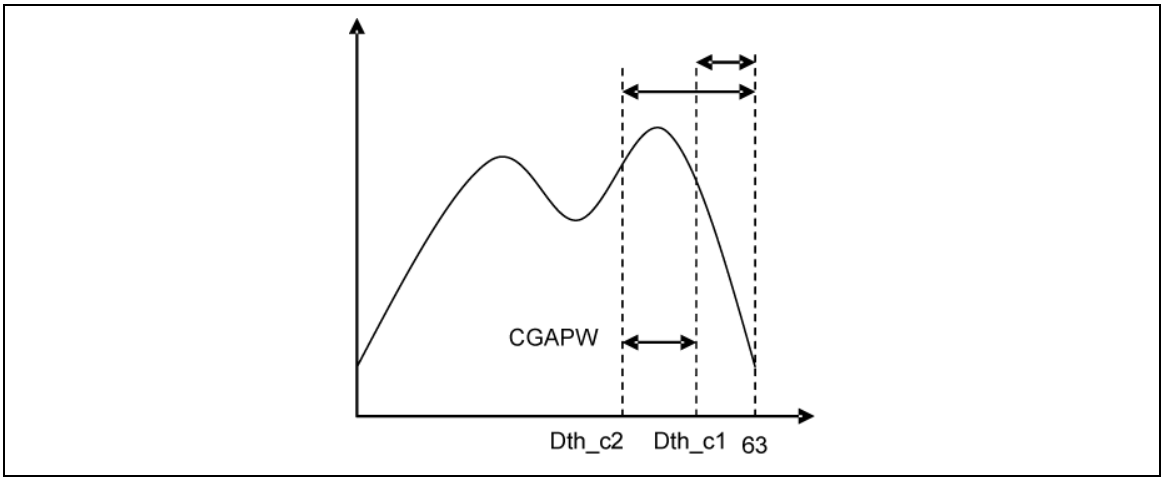


Figure 47

(4) ULMTW[5:0], LLMTW[5:0]

The possible range of a threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. ULMTW and LLMTW set the maximum grayscale and the minimum grayscale, respectively. Dth can be changed within the range set by ULMTW and LLMTW.

When there is no effect in saving power consumption due to a large number of pixels displaying white color, that is, in a case such as GUI, the R61581B0 can save power consumption by setting ULMTW lower than the maximum grayscale if saving power consumption precedes the display quality.

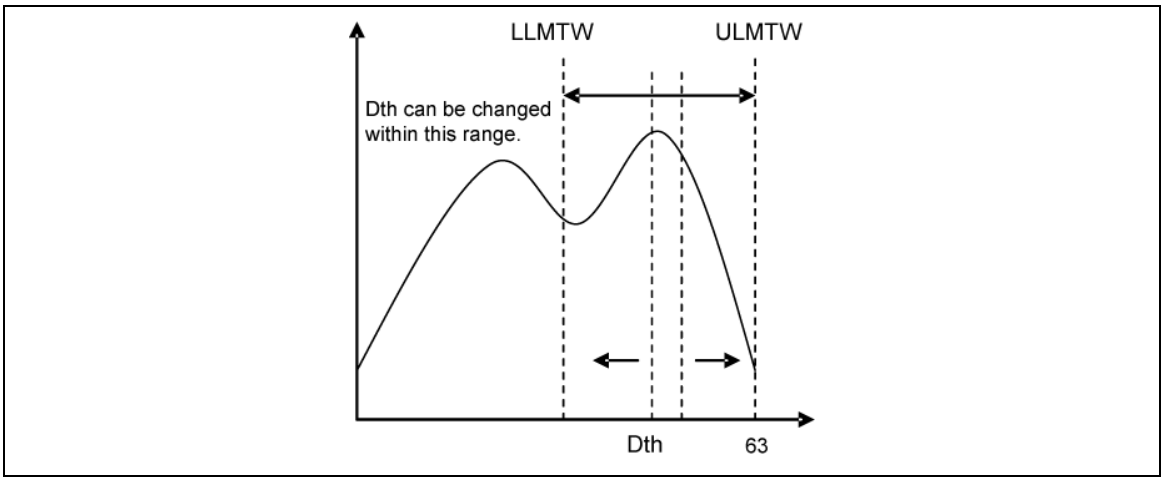


Figure 48

(5) TBL*[7:0]

The reference values used for interpolation calculation in gamma table are set by 8-bit TBL*[7:0]. Interpolation is performed as follows. First, four grayscale values are specified by TBL*[7:0]. Then, the output data corresponding to the input data to thirty one grayscale values specified at even interval between the adjacent two grayscale values of the nine grayscale values specified by TBL*[7:0] is calculated by linear interpolation.

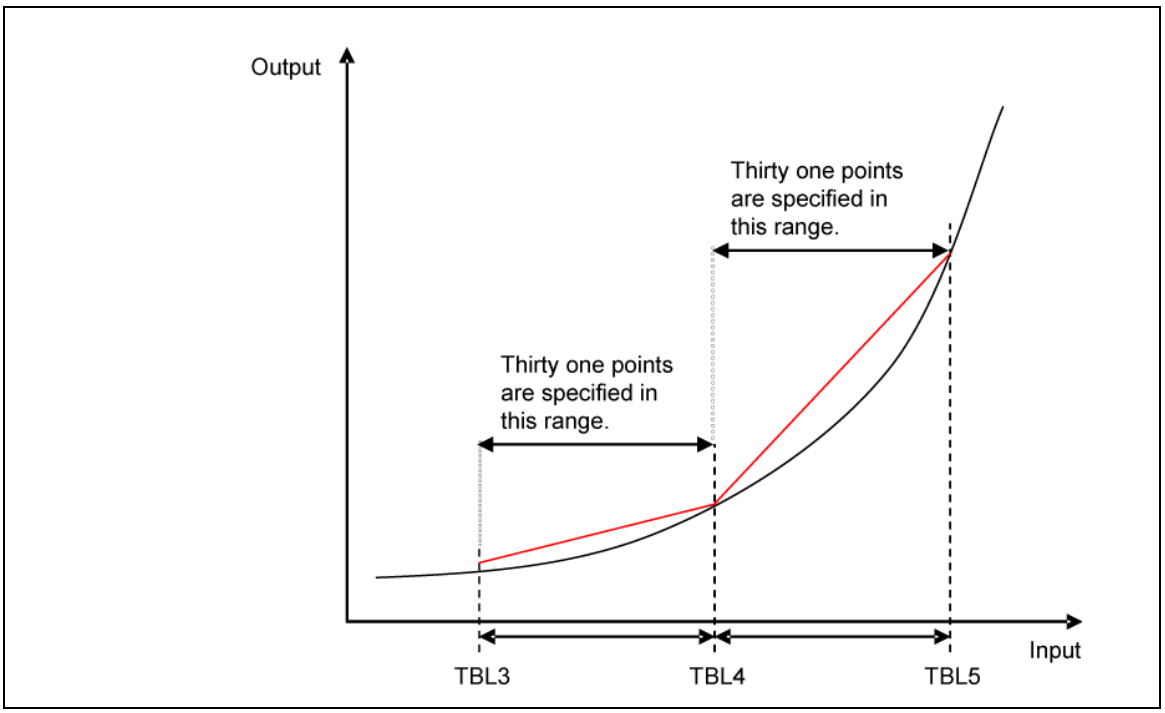


Figure 49

The table setting value is calculated by the following formula according to panel gamma value.

Table setting value = 255 x (table input grayscale / 255) ^ gamma

As the input table grayscale, the above calculation formula is applied to the five grayscale values (grayscales 127, 159, 191, and 223) to calculate the table values. The table value is set as TBL*. The following table is applied to the case that gamma is set to 2.2.

Table 31

Register	TBL3	TBL4	TBL5	TBL6
Table input grayscale	127	159	191	223
Table setting value	55	90	135	190

(6) COEFK[4:0]

This register sets the range of the grayscale that prevent display image from being white, according to the ratio of the grayscale mentioned here to the grayscale number that makes data white. The ratio can be set from 0 percent to 100 percent. The first grayscale (S) that starts grayscale interpolation to prevent display image from being white is calculated by this register and Dth. Then, the number of grayscales between this grayscale (S) and the maximum grayscale is calculated by interpolation function, and it is used as image processing pixel value.

The larger COEFK[4:0] setting value increases the number of grayscales available in interpolation and relatively decreases the contrast between interpolation sections. As a result, the gamma value changes, and then, the brightness decreases. Also, the color of the section changes. In interpolation factor, there is a trade-off between contrast between interpolation section and the interpolation that the gamma value changes.

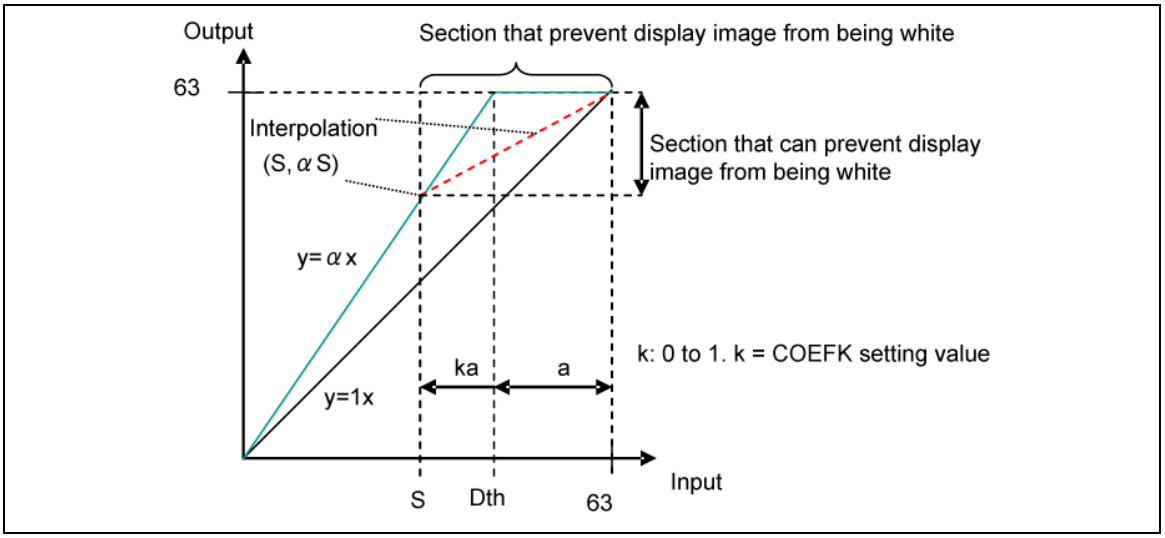


Figure 50

PWM Signal Setting

The PWM signal is output from the LEDPWM pin according to BDCV[7:0] bit settings and brightness information (8 bits) output from BLC control circuit.

PWM output specification (LEDPWMPOL = 0)

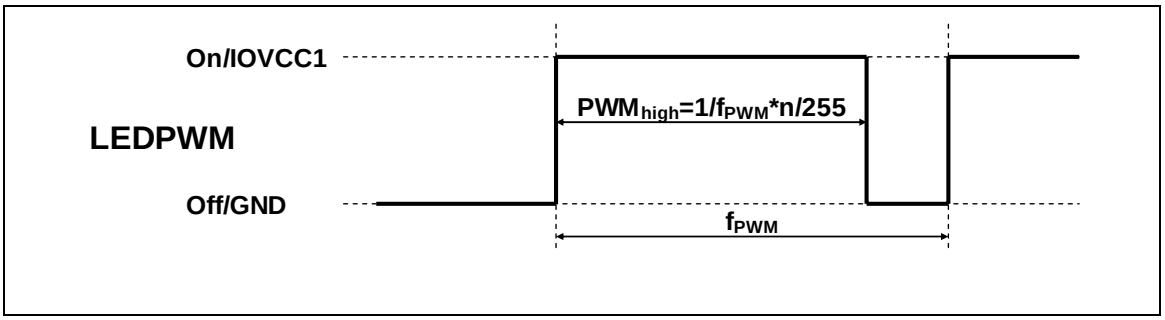
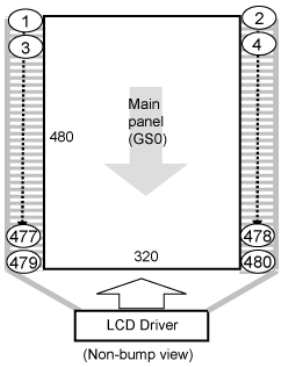
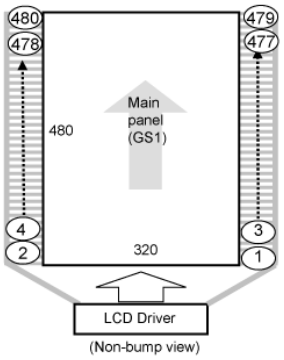
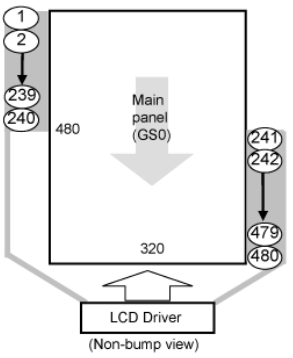
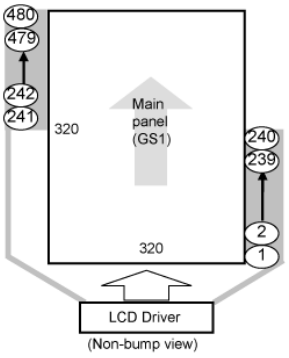


Figure 51

Note: The values in the table above show the typical. There shall be variance of maximum +/-7% in the actual operation.

Scan Mode Setting

The R61581B0 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the R61581B0 and the LCD panel.

SM	Scan direction	
0	Left/right interchanging forward scan (GS=0)  Scan order G[1] → G[2] → G[3] ..... G[478] → G[479] → G[480]	Left/right interchanging reverse scan (GS=1)  Scan order G[480] → G[479] → G[478] ..... G[3] → G[2] → G[1]
1	Left/right one-side forward scan (GS=0)  Scan order G[1] → G[3]....G[477] → G[479] → G[2] → G[4]....G[478] → G[480]	Left/right one-side reverse scan (GS=1)  Scan order G[480] → G[478].... → G[4] → G[2] → G[479] → G[477]....G[3] → G[1]

Note: The numbers in the circles in the figure show the order of scan.

Figure 52

Frame Frequency Adjustment Function

The R61581B0 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting Display Timing Setting (RTN bits) without changing the oscillation frequency.

It is possible to set a low frame frequency for saving power consumption when displaying a still picture and set a high frame frequency when displaying video image.

Also, the R61581B0 has frame-frequency adjustment parameters which can set frame frequency according to display modes (Normal, partial and Idle modes).

Relationship between the Liquid Crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be changed by setting the number of clocks per 1 line period (RTN).

Equation for calculating frame frequency

$$FrameFrequency = \frac{fosc}{NumberofClocks/line \times (NL + FP + BP)}[Hz]$$

fosc: Internal operation clock frequency (785kHz)
Number of clocks per line: RTN
Division ratio: DIV
Line: number of lines to drive the LCD: NL
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when Maximum Frame Frequency = 60 Hz

fosc : 785 kHz
Number of lines: 480 lines
1H period: 26 clock cycles (RTN[4:0] = “11010”)
Division ratio of operating clock: 1/1
Front porch: 8 lines
Back porch: 8 lines

$$\therefore f_{FLM} = \frac{785kHz}{26clocks \times \frac{1}{1} \times (480 + 8 + 8)} \approx 60Hz$$

In the conditions described here, the frame frequency can be changed as follows by setting RTN and DIV. (NL = 480 lines, BP = 8 lines, FP = 8 lines, fosc = 785kHz).

Line Inversion AC Drive

The R61581B0, in addition to frame-inversion liquid crystal alternating current drive, supports line inversion alternating current drive.

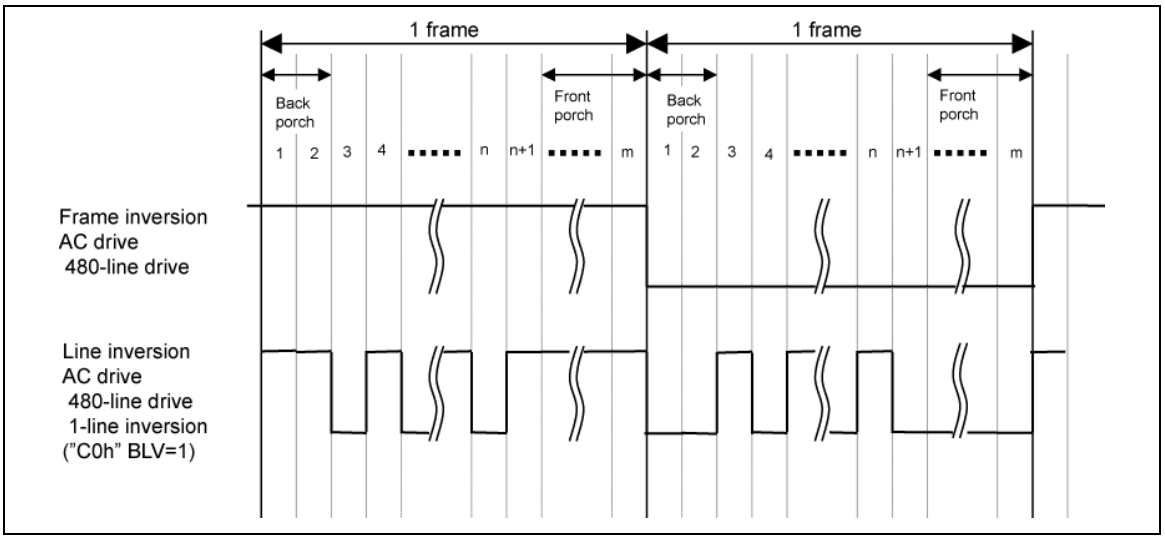


Figure 53

Alternating Timing

The following figure illustrates the liquid-crystal polarity inversion timing of different LCD driving methods.

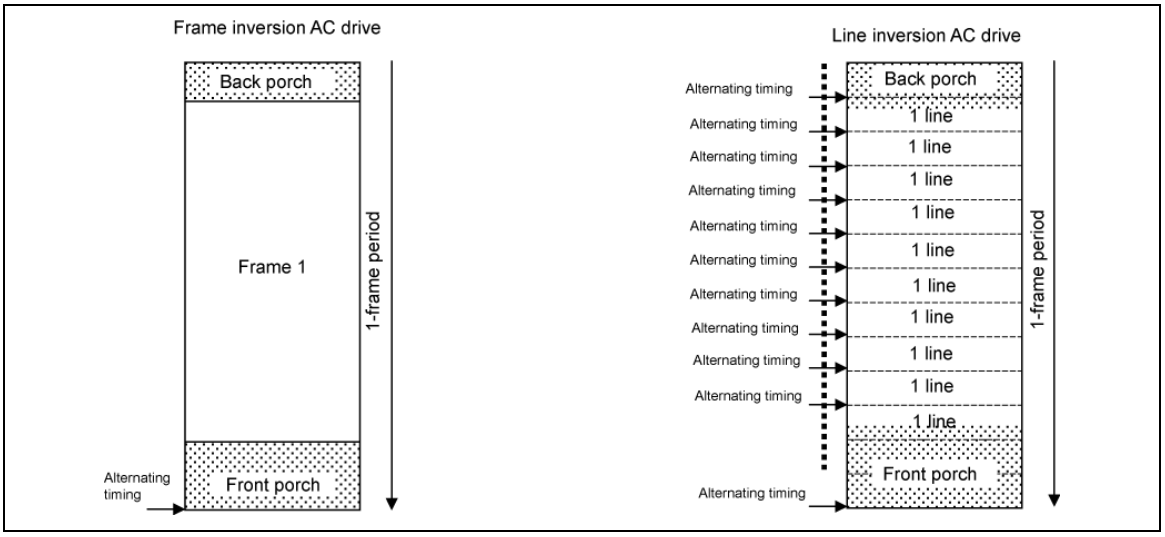


Figure 54

TE Pin Output Signal

Tearing Effect Line signal can be output from TE pin as frame memory data transfer synchronous signals. TE signal is trigger for frame memory write operation to enable data transfer in synchronization with the scanning operation. Tearing Effect Output signal is turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

Table 32

TEON (represents status of 35h command)	TELOM (35h1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode1)
1	1	TE (Mode2)

Tearing Effect signal mode is defined by TELOM, D0 parameter of set_tear_on (35h).

Write TELOM=0 when using DSI TE report function.

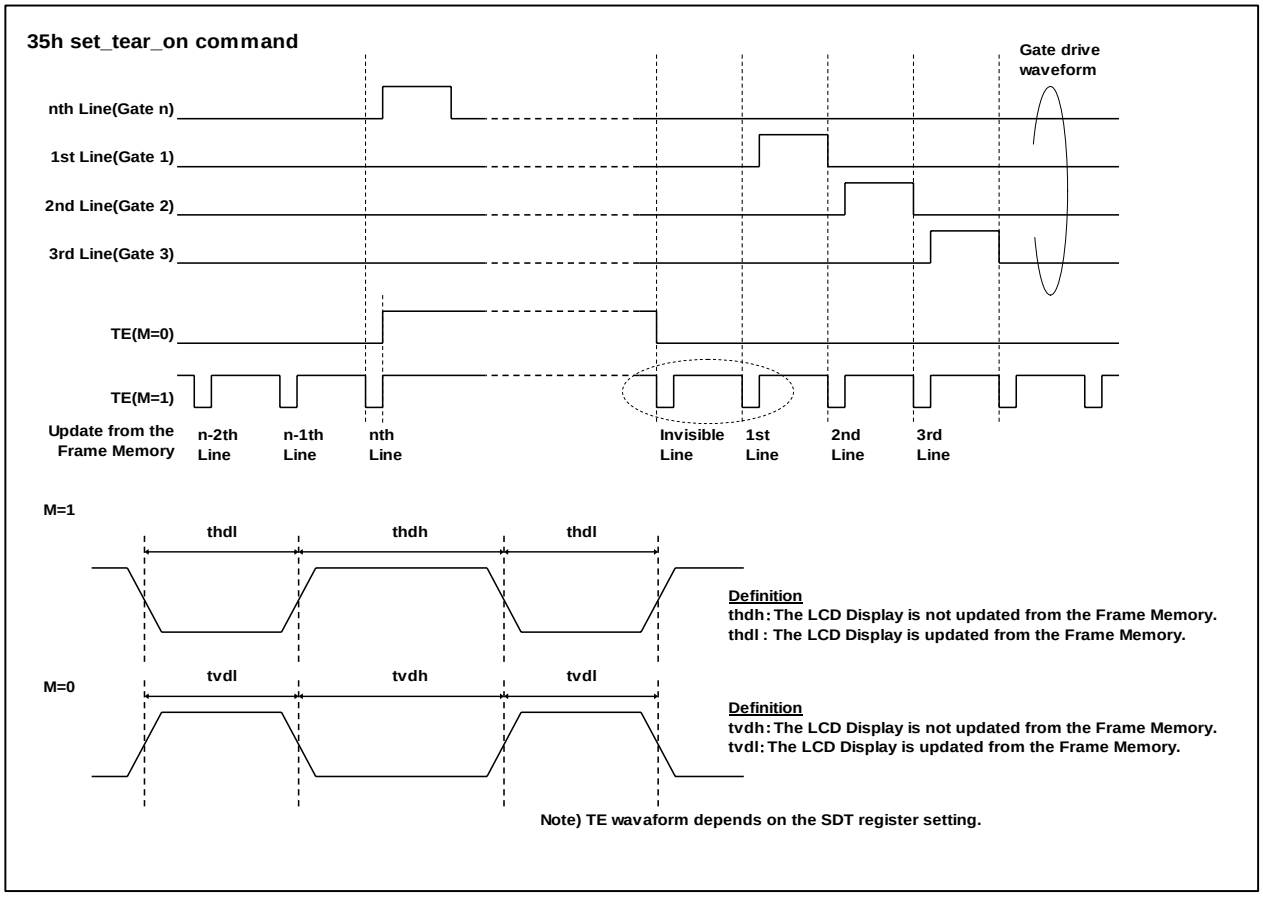


Figure 55

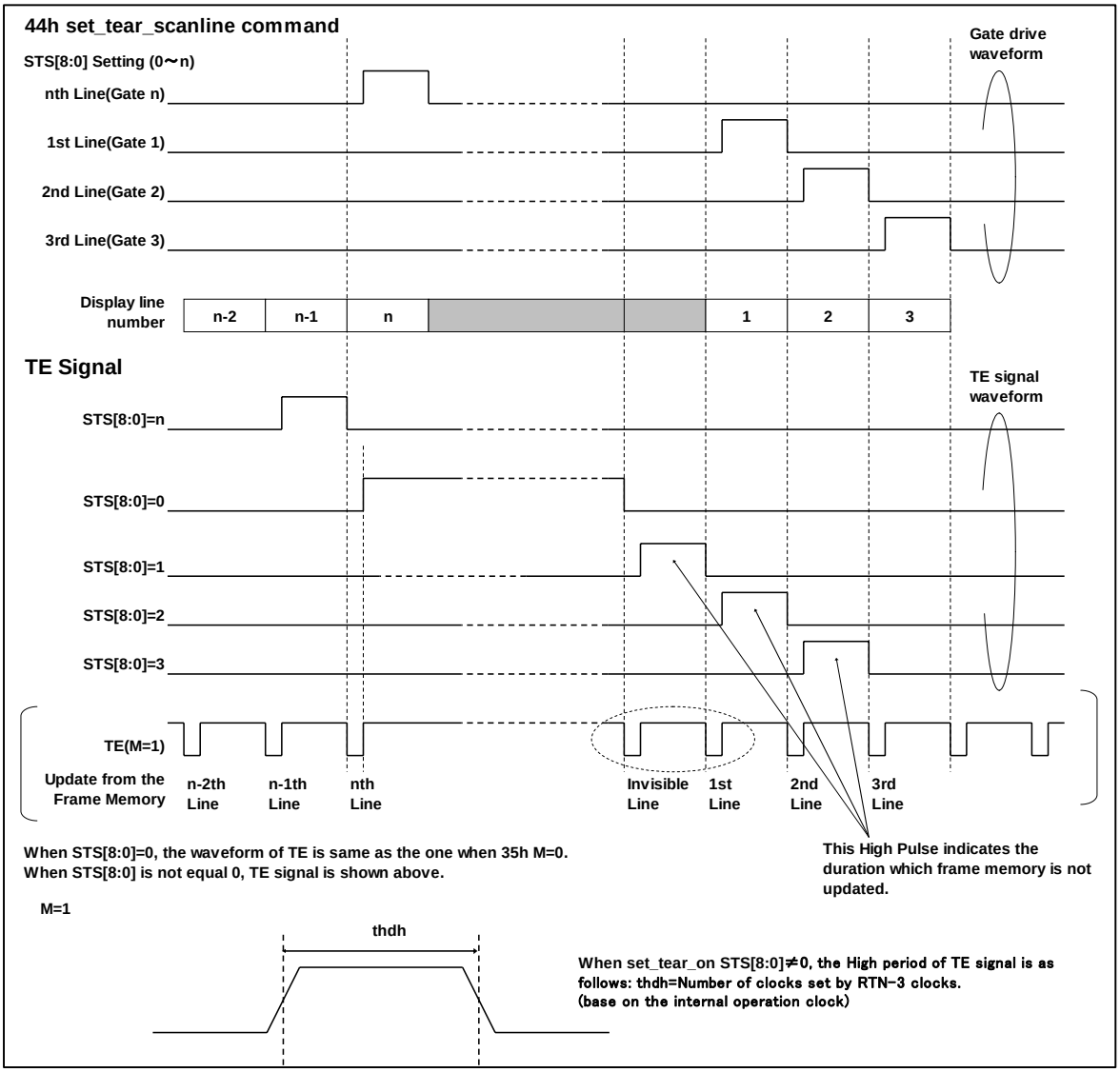

44h set_tear_scanline command
STS[8:0] Setting (0～n)
Gate drive waveform
nth Line(Gate n)
1st Line(Gate 1)
2nd Line(Gate 2)
3rd Line(Gate 3)
Display line number
n-2
n-1
n
1
2
3
TE Signal
TE signal waveform
STS[8:0]=n
STS[8:0]=0
STS[8:0]=1
STS[8:0]=2
STS[8:0]=3
TE(M=1)
Update from the Frame Memory
n-2th Line
n-1th Line
nth Line
Invisible Line
1st Line
2nd Line
3rd Line
When STS[8:0]=0, the waveform of TE is same as the one when 35h M=0.
When STS[8:0] is not equal 0, TE signal is shown above.
This High Pulse indicates the duration which frame memory is not updated.
M=1
thdh
When set_tear_on STS[8:0]≠0, the High period of TE signal is as follows: thdh=Number of clocks set by RTN-3 clocks.
(base on the internal operation clock)

Figure 56

Display-Synchronous Data Transfer Using TE Signal

The R61581B0 enables data transfer in synchronization with the display scan by writing data to the internal frame memory using the TE signal as the trigger.

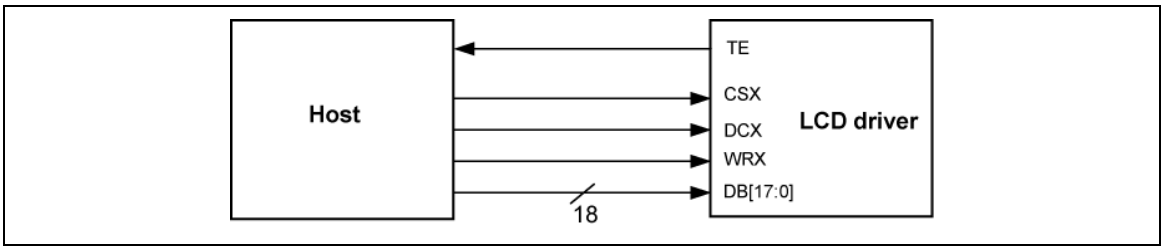


Figure 57 Interface Example for Display-Synchronous Data Transfer

By writing data to the internal Frame Memory at faster than calculated minimum speed, it becomes possible to rewrite the video image data without flickering the display and display video image via system interface. The display data is written in the Frame Memory so that the R61581B0 rewrites the data only within the video image area and minimize the number of data transfer required to display video image.

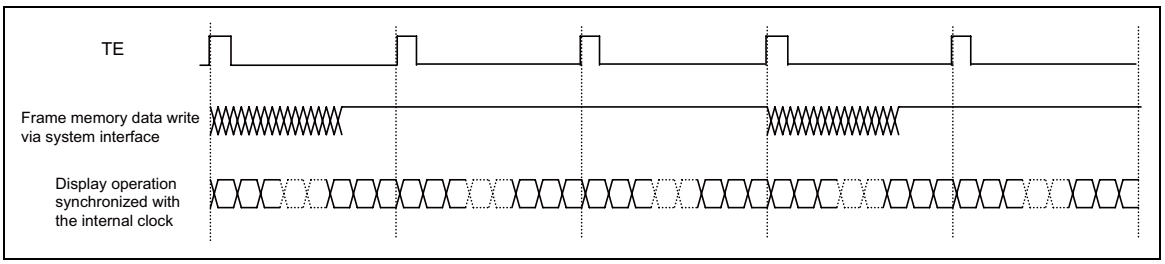


Figure 58 Video Image Data Write with TE

When transferring data using TE as the trigger, there are restrictions in setting the minimum Frame Memory data write speed and the minimum internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz] = Frame frequency × (Display lines (NL) + Front porch (FP) + Back porch (BP)) × Clocks per 1H (RTN) × Variances

Frame memory write speed (min.) [Hz] >
240 × Display lines (NL) / {(FP + BP + Display lines (NL) – Margins) × Division ratio (DIV) × Clocks per 1H (RTN) × 1/ fosc}

Note: When frame memory write operation is not started right after the rising edge of TE, the time from the rising edge of TE until the start of frame memory write operation must also be taken into account.

An example of calculating the minimum frame memory writing speed and internal clock frequency for writing data in synchronization with display operation.

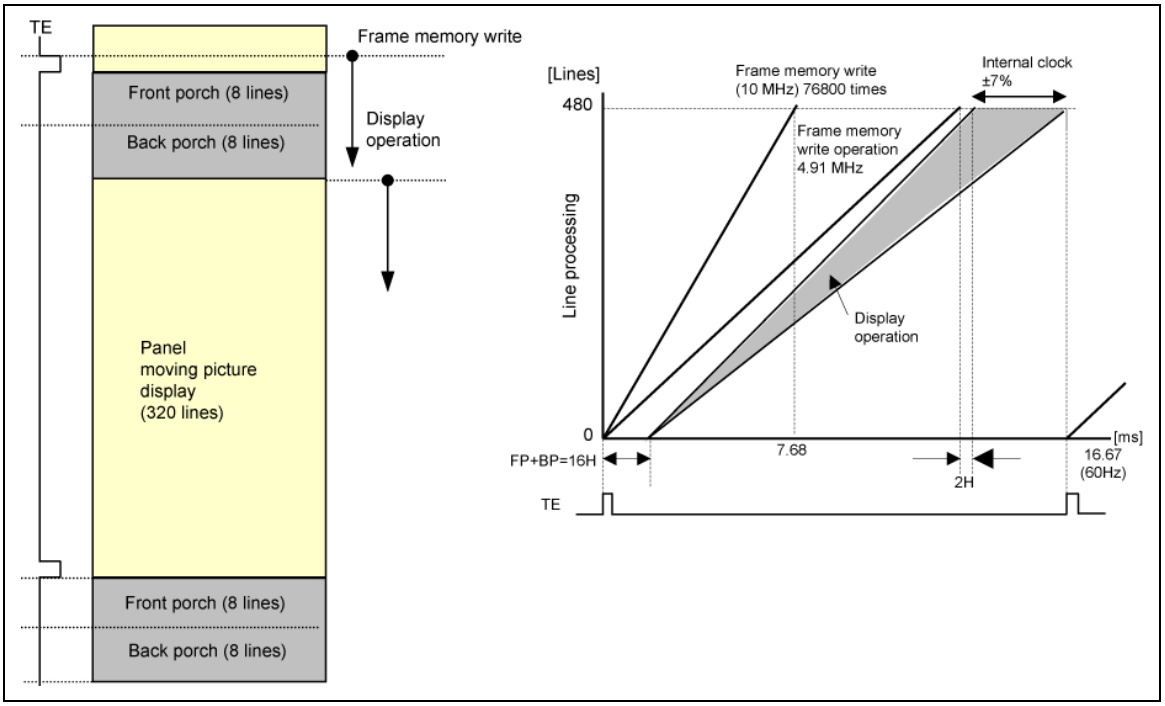


Figure 59

Liquid Crystal Panel Interface Timing

Liquid Crystal Panel Interface Timing in Internal Clock Operation

The following figure shows the timing of DPI and liquid crystal panel interface signals in DPI operation.

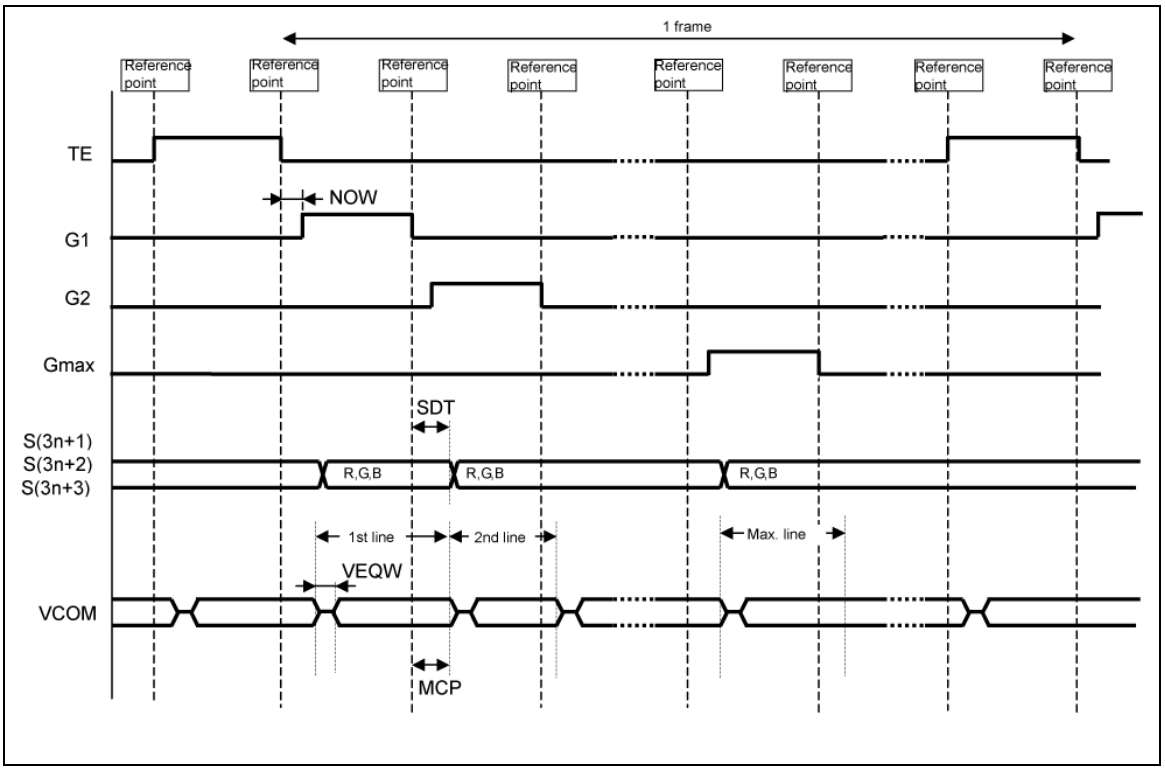


Figure 60

VCOM and source output alternating positions are defined separately.

Notes 1. The shown TE waveform has values M=0, set_tear_scanline STS[8:0]=1.
2. In the VCOM waveform shown in the above figure, BCn=1, BLV=1.

Setting range
MCP[2:0]: 1 to 7clks
SDT[2:0]: 1 to 7clks
NOW[2:0]: 1 to 7clks
Units: 1clk

Liquid Crystal Panel Interface Timing in DPI Operation

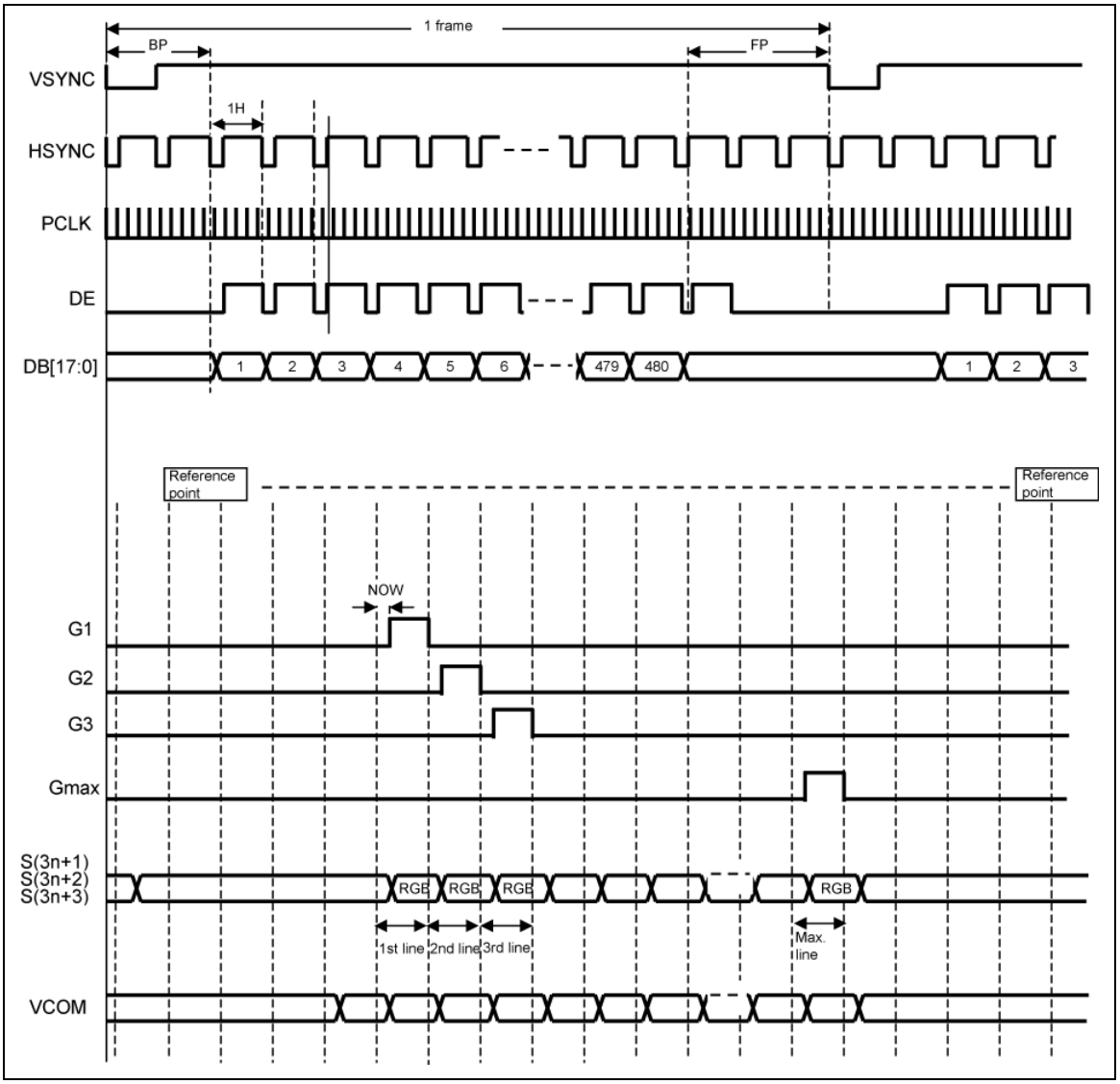


Figure 61

Note: In the VCOM waveform shown in the above figure, BCn=1, BLV=1.

Gamma Correction Function

γ Correction Function

The R61581B0 supports γ-correction function to make the optimal colors according to the characteristics of the panel. The R61581B0 has registers for positive and negative polarities to allow different settings.

γ Correction Circuit

The following figure shows the γ-correction circuit. According to the settings of variable resistors R0 to R8, the voltage the level of which is the difference is between VREG1OUT and VGS is evenly divided into 8 grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62 and V63). The other 42 grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see "Grayscale Voltage Calculation Formula".

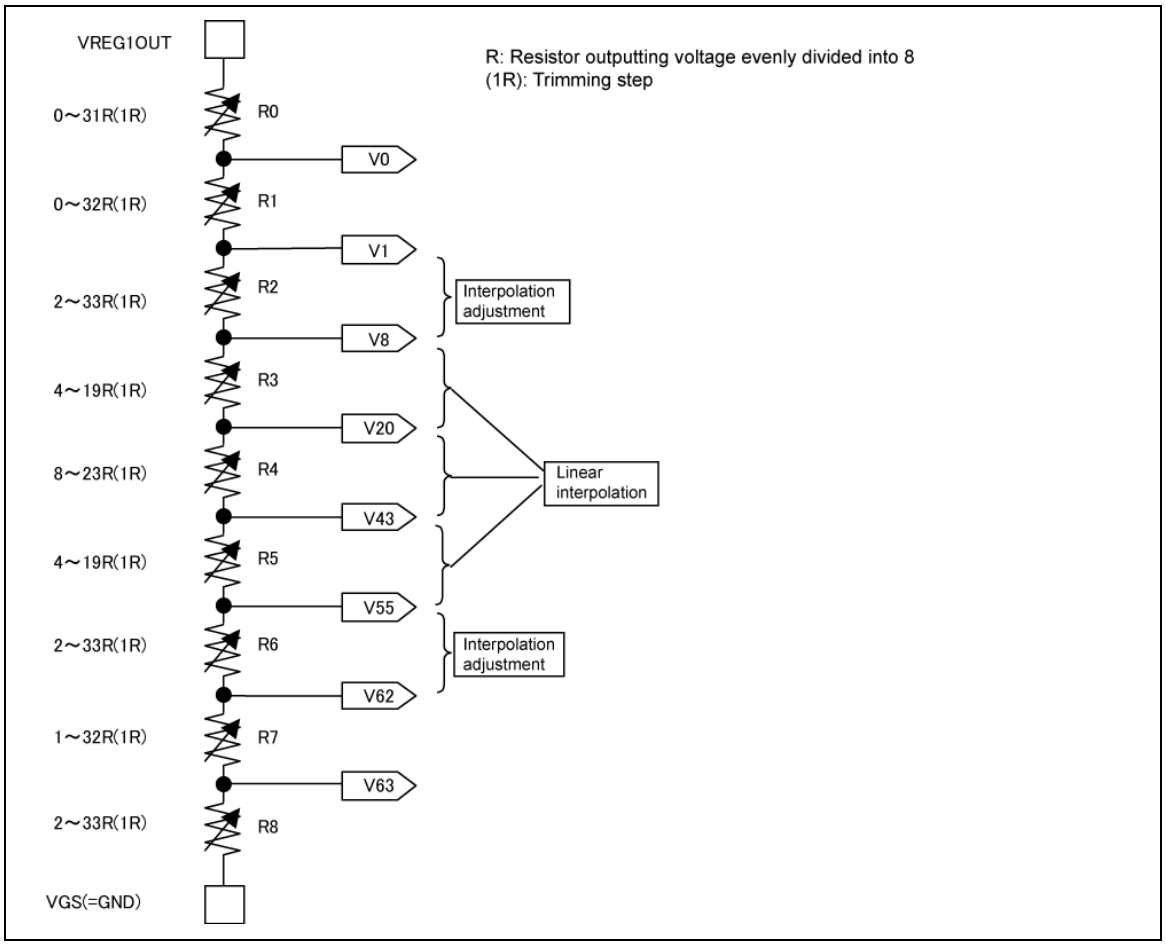


Figure 62

γ Correction Registers

The γ-correction registers include 42-bit reference level adjustment registers per R, G, and B dots (positive polarity and negative polarity) and 8-bit interpolation adjustment registers.

Reference Level Adjustment Registers

Table 33 Reference Level Adjustment Registers

Resistor	Gamma Set	
	Positive polarity	Negative polarity
R0	PR0P00[4:0]	PR0N00[4:0]
R1	PR0P01[4:0]	PR0N01[4:0]
R2	PR0P02[4:0]	PR0N02[4:0]
R3	PR0P03[3:0]	PR0N03[3:0]
R4	PR0P04[3:0]	PR0N04[3:0]
R5	PR0P05[3:0]	PR0N05[3:0]
R6	PR0P06[4:0]	PR0N06[4:0]
R7	PR0P07[4:0]	PR0N07[4:0]
R8	PR0P08[4:0]	PR0N08[4:0]

Table 34 Reference Level Adjustment Registers and Resistors

Resistor	Register		Resistance	Resistor	Register		Resistance
	Name	Value			Name	Value	
R0	PR**0[4:0]	5'h00	0R	R5	PR**5[3:0]	4'h0	4R
		5'h01	1R			4'h1	5R
		5'h02	2R			4'h2	6R
		⋮	⋮			⋮	⋮
		5'h1F	31R			4'hF	19R
R1	PR**1[4:0]	5'h00	1R	R6	PR**6[4:0]	5'h00	2R
		5'h01	2R			5'h01	3R
		5'h02	3R			5'h02	4R
		⋮	⋮			⋮	⋮
		5'h1F	32R			5'h1F	33R
R2	PR**2[4:0]	5'h00	2R	R7	PR**7[4:0]	5'h00	1R
		5'h01	3R			5'h01	2R
		5'h02	4R			5'h02	3R
		⋮	⋮			⋮	⋮
		5'h1F	33R			5'h1F	32R
R3	PR**3[3:0]	4'h0	4R	R8	PR**8[4:0]	5'h00	2R
		4'h1	5R			5'h01	3R
		4'h2	6R			5'h02	4R
		⋮	⋮			⋮	⋮
		4'hF	19R			5'h1F	33R
R4	PR**4[3:0]	4'h0	8R				
		4'h1	9R				
		4'h2	10R				
		⋮	⋮				
		4'hF	23R				

Note: ** indicates 0P/0N.

Interpolation Registers

Table 35 Interpolation Registers

Interpolation adjustment	Gamma Set	
	Positive polarity	Negative polarity
V2 ~ V7	PI0P0[1:0]	PI0N0[1:0]
	PI0P1[1:0]	PI0N1[1:0]
V56 ~ V61	PI0P2[1:0]	PI0N2[1:0]
	PI0P3[1:0]	PI0N3[1:0]

Table 36 Interpolation factor for V2 to V7

(See "Grayscale Voltage Calculation Formula" for IPV* level)

PI**0[1:0]	PI**1[1:0]	IPV2	IPV3	IPV4	IPV5	IPV6	IPV7
2'h0	2'h0	81%	67%	52%	39%	26%	13%
	2'h1	78%	61%	43%	33%	22%	11%
	2'h2	73%	52%	31%	23%	15%	8%
	2'h3	72%	50%	28%	21%	14%	7%
2'h1	2'h0	80%	68%	56%	42%	28%	14%
	2'h1	76%	62%	48%	36%	24%	12%
	2'h2	70%	52%	35%	26%	17%	9%
	2'h3	69%	50%	31%	23%	16%	8%
2'h2	2'h0	78%	70%	61%	46%	30%	15%
	2'h1	74%	63%	53%	39%	26%	13%
	2'h2	66%	53%	39%	29%	20%	10%
	2'h3	64%	50%	36%	27%	18%	9%
2'h3	2'h0	78%	70%	63%	47%	31%	16%
	2'h1	73%	64%	54%	41%	27%	14%
	2'h2	65%	53%	41%	31%	20%	10%
	2'h3	63%	50%	37%	28%	19%	9%

Table 37 Interpolation Factor for V56 to V61

PI**3[1:0]	PI**2[1:0]	IPV56	IPV57	IPV58	IPV59	IPV60	IPV61
2'h0	2'h0	87%	74%	61%	48%	33%	19%
	2'h1	89%	78%	67%	57%	39%	22%
	2'h2	92%	85%	77%	69%	48%	27%
	2'h3	93%	86%	79%	72%	50%	28%
2'h1	2'h0	86%	72%	58%	44%	32%	20%
	2'h1	88%	76%	64%	52%	38%	24%
	2'h2	91%	83%	74%	65%	48%	30%
	2'h3	92%	84%	77%	69%	50%	31%
2'h2	2'h0	85%	70%	54%	39%	30%	22%
	2'h1	87%	74%	61%	47%	37%	26%
	2'h2	90%	80%	71%	61%	47%	34%
	2'h3	91%	82%	73%	64%	50%	36%
2'h3	2'h0	84%	69%	53%	38%	30%	22%
	2'h1	86%	73%	59%	46%	36%	27%
	2'h2	90%	80%	69%	59%	47%	35%
	2'h3	91%	81%	72%	63%	50%	37%

Note: ** indicates 0P / 0N / 1P / 1N / 2P / 2N.

Grayscale Voltage Calculation Formulas

Table 38 Grayscale Voltage Calculation Formula

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	ΔV x Σ(R1 ~ R8)/SUMR	V32	V43 + (V20 − V43) x 11/23
V1	ΔV x Σ(R2 ~ R8)/SUMR	V33	V43 + (V20 − V43) x 10/23
V2	V8 + (V1 − V8) x IPV2	V34	V43 + (V20 − V43) x 9/23
V3	V8 + (V1 − V8) x IPV3	V35	V43 + (V20 − V43) x 8/23
V4	V8 + (V1 − V8) x IPV4	V36	V43 + (V20 − V43) x 7/23
V5	V8 + (V1 − V8) x IPV5	V37	V43 + (V20 − V43) x 6/23
V6	V8 + (V1 − V8) x IPV6	V38	V43 + (V20 − V43) x 5/23
V7	V8 + (V1 − V8) x IPV7	V39	V43 + (V20 − V43) x 4/23
V8	ΔV x Σ(R3 ~ R8)/SUMR	V40	V43 + (V20 − V43) x 3/23
V9	V20 + (V8 − V20) x 11/12	V41	V43 + (V20 − V43) x 2/23
V10	V20 + (V8 − V20) x 10/12	V42	V43 + (V20 − V43) x 1/23
V11	V20 + (V8 − V20) x 9/12	V43	ΔV x Σ(R5 ~ R8)/ SUMR
V12	V20 + (V8 − V20) x 8/12	V44	V55 + (V43 − V55) x 11/12
V13	V20 + (V8 − V20) x 7/12	V45	V55 + (V43 − V55) x 10/12
V14	V20 + (V8 − V20) x 6/12	V46	V55 + (V43 − V55) x 9/12
V15	V20 + (V8 − V20) x 5/12	V47	V55 + (V43 − V55) x 8/12
V16	V20 + (V8 − V20) x 4/12	V48	V55 + (V43 − V55) x 7/12
V17	V20 + (V8 − V20) x 3/12	V49	V55 + (V43 − V55) x 6/12
V18	V20 + (V8 − V20) x 2/12	V50	V55 + (V43 − V55) x 5/12
V19	V20 + (V8 − V20) x 1/12	V51	V55 + (V43 − V55) x 4/12
V20	ΔV x Σ(R4 ~ R8)/SUMR	V52	V55 + (V43 − V55) x 3/12
V21	V43 + (V20 − V43) x 22/23	V53	V55 + (V43 − V55) x 2/12
V22	V43 + (V20 − V43) x 21/23	V54	V55 + (V43 − V55) x 1/12
V23	V43 + (V20 − V43) x 20/23	V55	ΔV x Σ(R6 ~ R8)/SUMR
V24	V43 + (V20 − V43) x 19/23	V56	V62 + (V55 − V62) x IPV56
V25	V43 + (V20 − V43) x 18/23	V57	V62 + (V55 − V62) x IPV57
V26	V43 + (V20 − V43) x 17/23	V58	V62 + (V55 − V62) x IPV58
V27	V43 + (V20 − V43) x 16/23	V59	V62 + (V55 − V62) x IPV59
V28	V43 + (V20 − V43) x 15/23	V60	V62 + (V55 − V62) x IPV60
V29	V43 + (V20 − V43) x 14/23	V61	V62 + (V55 − V62) x IPV61
V30	V43 + (V20 − V43) x 13/23	V62	ΔV x (R7 + R8)/SUMR
V31	V43 + (V20 − V43) x 12/23	V63	ΔV x R8/SUMR

Note: Make sure that
ΔV = VREG1OUT – VGS
SUMR = Σ(R0 ~ R8) ≥ 70R.
V63 ≥ 0.2V

Frame Memory Data and the Grayscale Voltage

Table 39

Frame memory data	Grayscale Voltage				Frame memory data	Grayscale Voltage			
	REV = 1		REV = 0			REV = 1		REV = 0	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity		Positive polarity	Negative polarity	Positive polarity	Negative polarity
6'h00	V0	V63	V63	V0	6'h20	V32	V31	V31	V32
6'h01	V1	V62	V62	V1	6'h21	V33	V30	V30	V33
6'h02	V2	V61	V61	V2	6'h22	V34	V29	V29	V34
6'h03	V3	V60	V60	V3	6'h23	V35	V28	V28	V35
6'h04	V4	V59	V59	V4	6'h24	V36	V27	V27	V36
6'h05	V5	V58	V58	V5	6'h25	V37	V26	V26	V37
6'h06	V6	V57	V57	V6	6'h26	V38	V25	V25	V38
6'h07	V7	V56	V56	V7	6'h27	V39	V24	V24	V39
6'h08	V8	V55	V55	V8	6'h28	V40	V23	V23	V40
6'h09	V9	V54	V54	V9	6'h29	V41	V22	V22	V41
6'h0A	V10	V53	V53	V10	6'h2A	V42	V21	V21	V42
6'h0B	V11	V52	V52	V11	6'h2B	V43	V20	V20	V43
6'h0C	V12	V51	V51	V12	6'h2C	V44	V19	V19	V44
6'h0D	V13	V50	V50	V13	6'h2D	V45	V18	V18	V45
6'h0E	V14	V49	V49	V14	6'h2E	V46	V17	V17	V46
6'h0F	V15	V48	V48	V15	6'h2F	V47	V16	V16	V47
6'h10	V16	V47	V47	V16	6'h30	V48	V15	V15	V48
6'h11	V17	V46	V46	V17	6'h31	V49	V14	V14	V49
6'h12	V18	V45	V45	V18	6'h32	V50	V13	V13	V50
6'h13	V19	V44	V44	V19	6'h33	V51	V12	V12	V51
6'h14	V20	V43	V43	V20	6'h34	V52	V11	V11	V52
6'h15	V21	V42	V42	V21	6'h35	V53	V10	V10	V53
6'h16	V22	V41	V41	V22	6'h36	V54	V9	V9	V54
6'h17	V23	V40	V40	V23	6'h37	V55	V8	V8	V55
6'h18	V24	V39	V39	V24	6'h38	V56	V7	V7	V56
6'h19	V25	V38	V38	V25	6'h39	V57	V6	V6	V57
6'h1A	V26	V37	V37	V26	6'h3A	V58	V5	V5	V58
6'h1B	V27	V36	V36	V27	6'h3B	V59	V4	V4	V59
6'h1C	V28	V35	V35	V28	6'h3C	V60	V3	V3	V60
6'h1D	V29	V34	V34	V29	6'h3D	V61	V2	V2	V61
6'h1E	V30	V33	V33	V30	6'h3E	V62	V1	V1	V62
6'h1F	V31	V32	V32	V31	6'h3F	V63	V0	V0	V63

Power Supply Generating Circuit

The following figure shows the configuration of LCD drive voltage generating circuit of the R61581B0.

Power Supply Circuit Connection Example 1

VCI level is adjusted internally by the VCI1 output circuit.

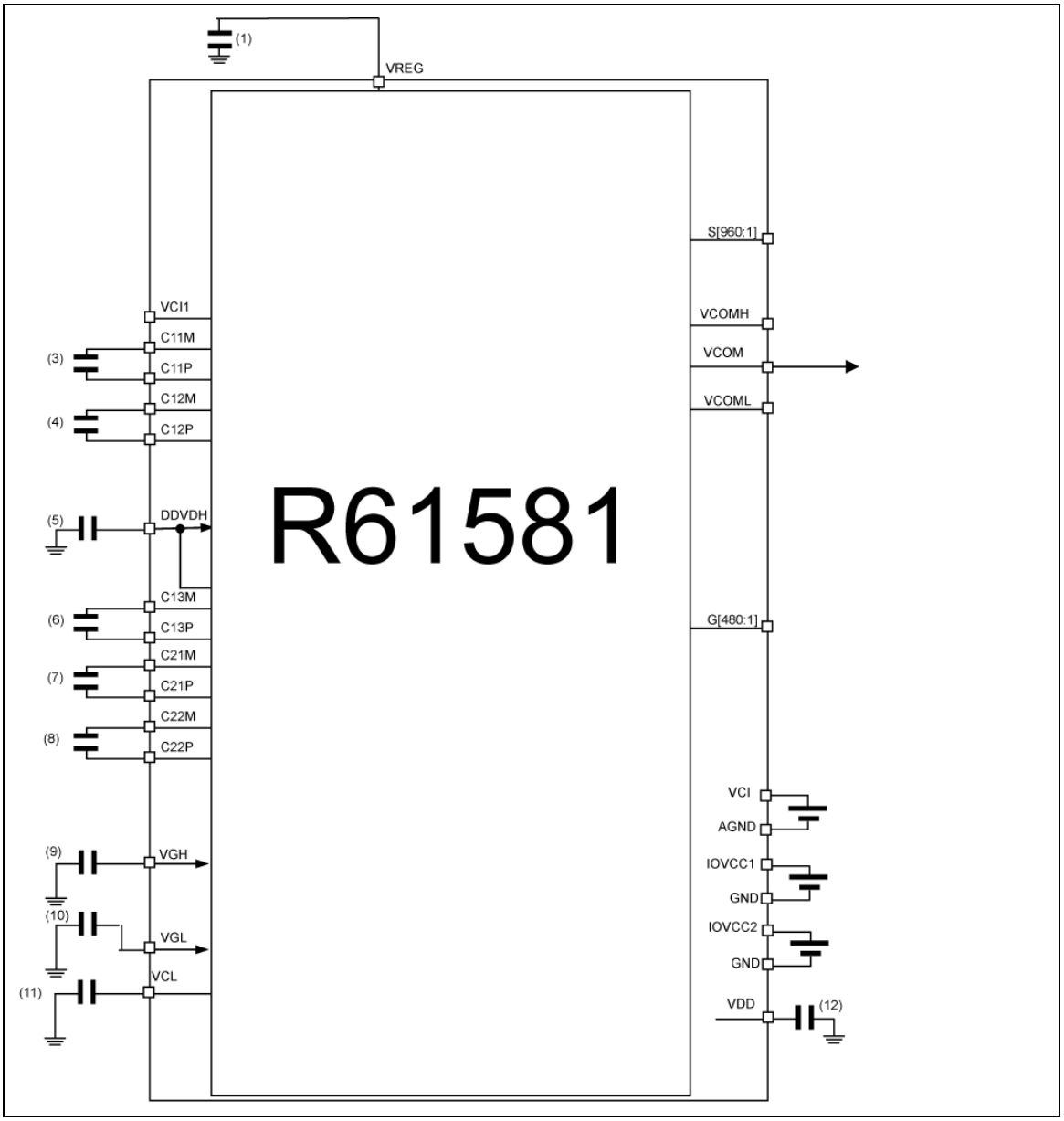


Figure 63

Power Supply Circuit Connection Example 2 (VCI Voltage is directly Input to VCI1 Pins)

The electrical potential VCI is directly applied to VCI1. In this case, the VCI1 level cannot be adjusted internally (see note), but step-up operation becomes more effective. (Only when VCI=3.0V or less)

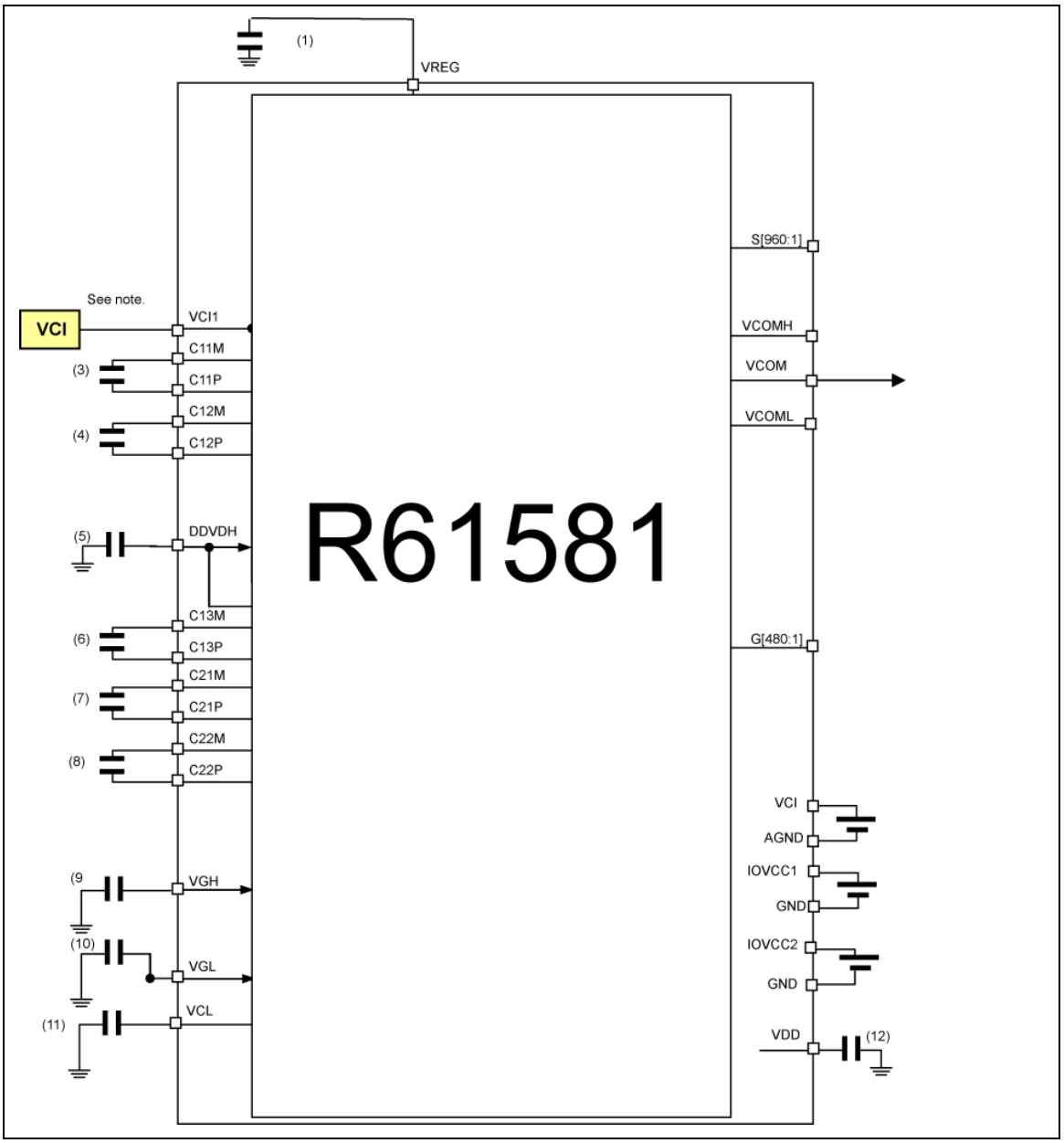


Figure 64

Note: When the VCI level is directly applied to VCI1, set VC[2:0] (D0h: the 2nd parameter) to 3'h7. Capacitor connected to VCI1 is not required.

Specifications of External Elements Connected to the Power Supply Circuit

The following table shows specifications of external elements connected to the R61581B0's power supply circuit. The numbers of the connection pins correspond to the numbers shown in Configuration of Power Supply Circuit.

Table 40 Capacitor Connected to LCD Power Supply Circuit

Capacity	Recommended voltage	Pins to connect
1μF (B characteristics)	6V	(1)VREG, (3)C11P/M, (4) C12P/M, (6)C13P/M, (11)VCL, (12)VDD, (13)VCOMH, (14)VCOML
	10V	(5)DDVDH, (7)C21P/M, (8)C22P/M
	25V	(9)VGH, (10)VGL

Note: (2) VCI1, (13) VCOMH, and (14) VCOML will be removed.

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61581B0 and the relationship between TFT display application voltage waveforms and electrical potential.

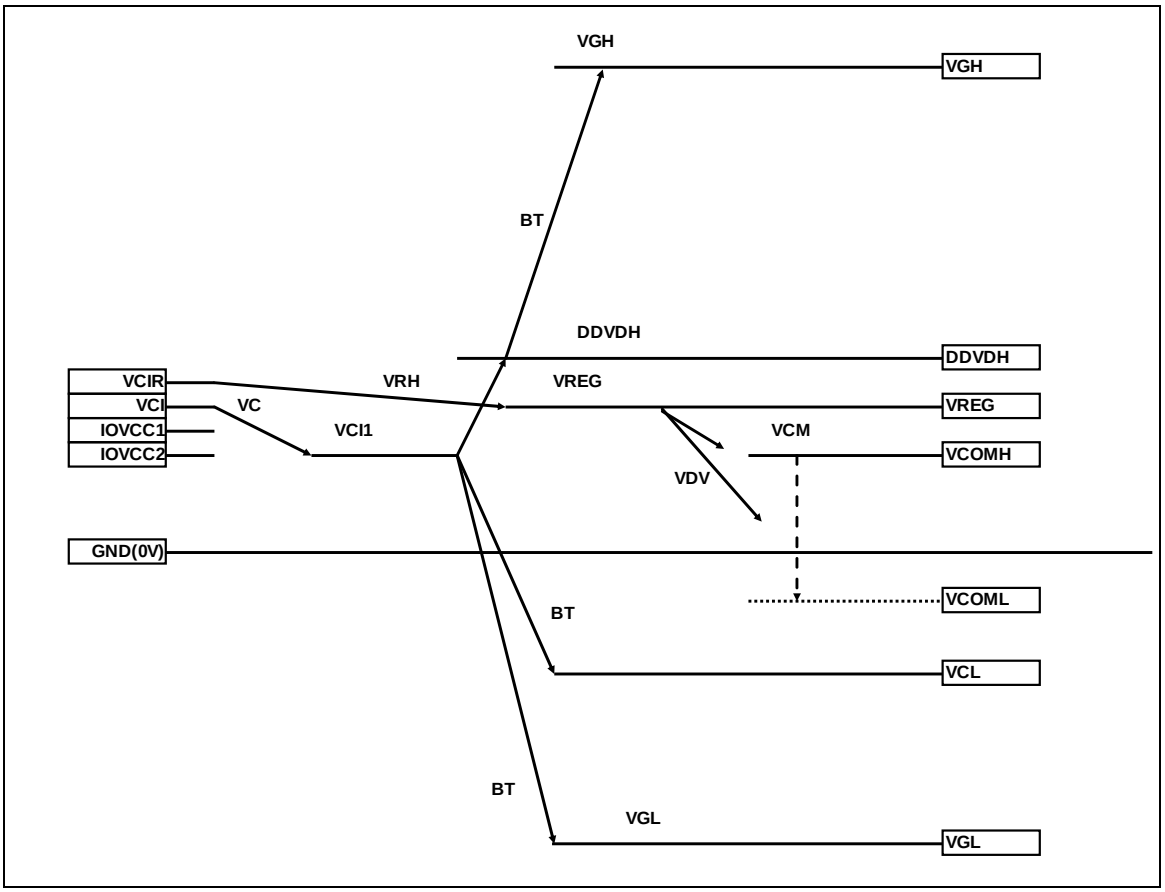


Figure 65

Note: The DDVDH, VGH, VGL, VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at respective outputs. When the alternating cycle of VCOM is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

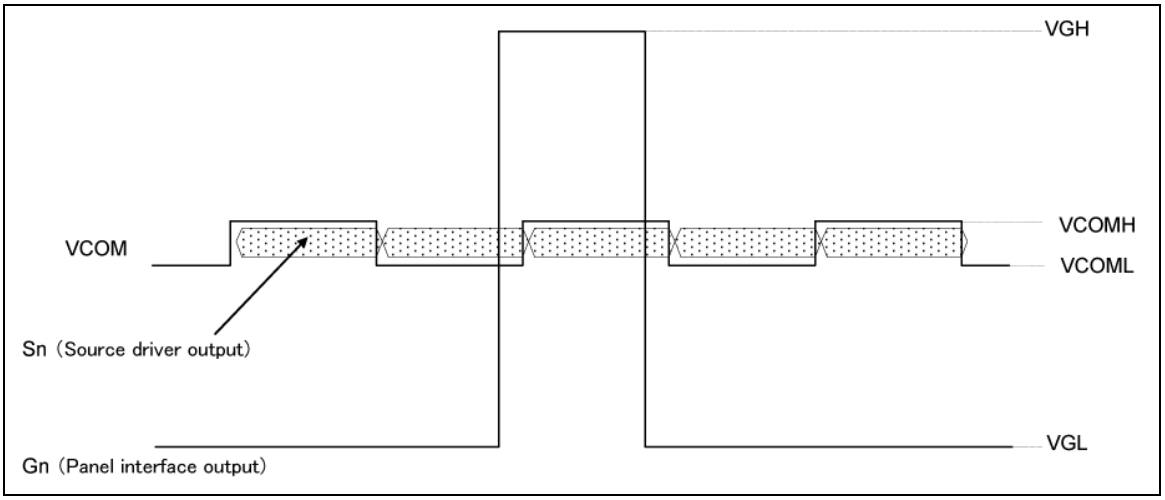


Figure 66 Voltage Application to TFT Display

NVM Control

The R61581B0 incorporates 59-bit NVM for user's use.

- 7 bits are for VCOM adjustment (VCM register value is stored)
- 5 bits are for VCOM alternating amplitude adjustment (VDV register value is stored)
- 32 bits are for Supplier ID (read by read_DDB_start)

To write, read and erase data from/to the NVM, follow the sequences below. Data on the NVM is loaded to internal registers automatically when the sequences are performed.

Power On sequence

HW RESET sequence

soft_reset sequence

Data stored in the NVM is retained permanently even if power supply is turned off.

Table 41

Operation mode	Power supply voltage		Time	Temperature
Write/Erase	VCI	2.50 ~ 3.30V	500ms	25°C±5°C
	IOVCC1	1.65 ~ 3.3V		

Note: NVM data rewrite (erase-write) operation should be performed up to 5 times per address.

NVM Load (Register Resetting) Sequence

Data on the NVM is loaded either automatically or by setting a command.

During the following sequence, the data written to the NVM is automatically loaded to the internal register.

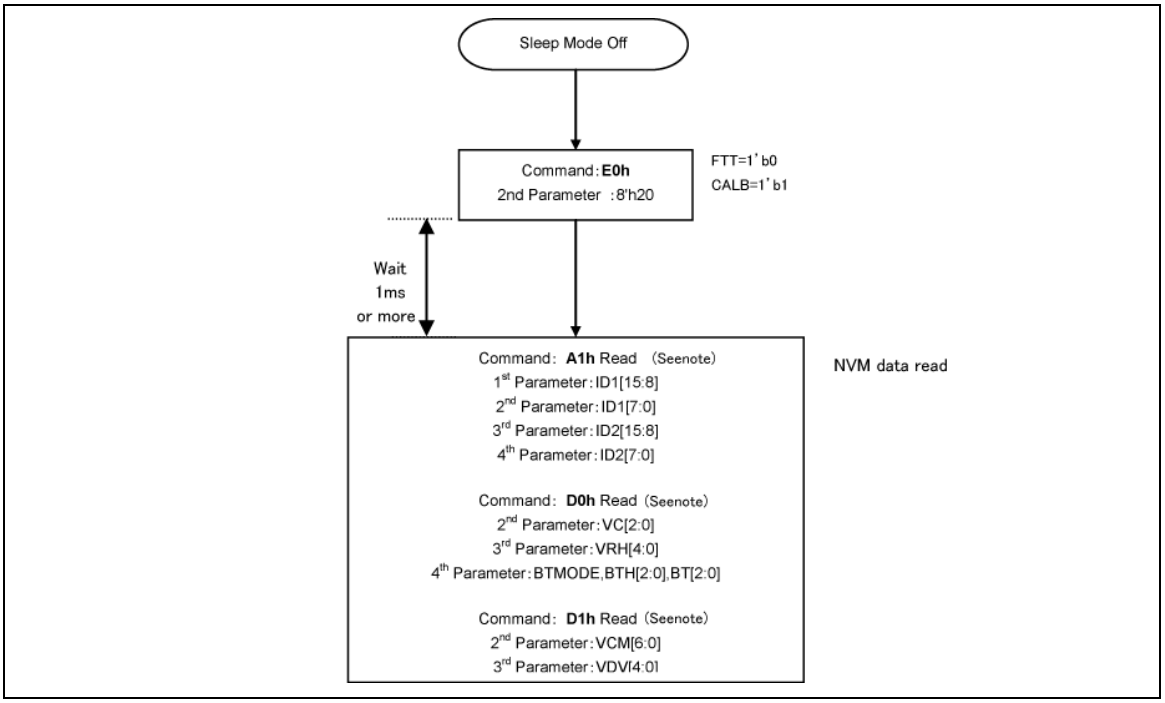


Figure 67 NVM Load (Register Resetting) Sequence

Note: In DBI Type C operation, see Manufacturer Command read sequence using Read Mode In command.

NVM Write Sequence

Defined 16 bit data is written to the selected address. When "1" is written to these bits, the bits are set to "1". If the data is erased from the bit, the bit is returned to "0". The bit to which data is not written should be set to "0".

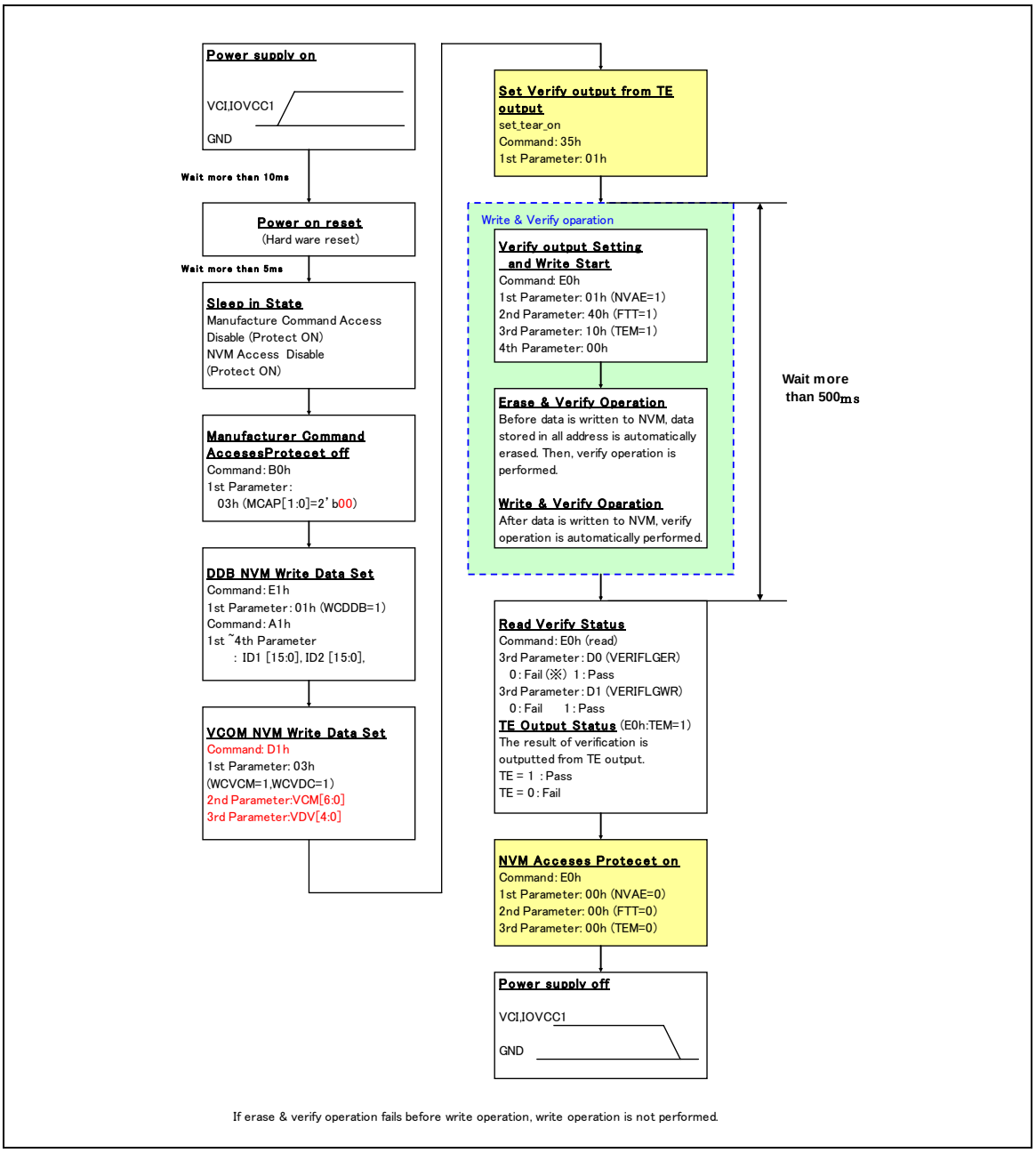


Figure 68

Absolute Maximum Rating

Table 42

Item	Symbol	Unit	Ratings	Note
Power supply voltage 1	IOVCC1/IOVCC2	V	-0.3 ~ +4.6	1, 2
Power supply voltage 2	VCI – AGND	V	-0.3 ~ +4.6	1, 3
Power supply voltage 3	DDVDH – AGND	V	-0.3 ~ +6.5	1, 4
Power supply voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power supply voltage 5	AGND– VGL	V	-0.3 ~ +13.0	1, 5
Power supply voltage 6	VGH– VGL	V	-0.3 ~ +30.0	1
Power supply voltage 7	VCI – VCL	V	-0.3 ~ +6.5	1, 6
Input voltage	Vt	V	-0.3 ~ IOVCC1 + 0.3	1
Operating Temperature	Topr	°C	-40 ~ +85	1, 7
Storage Temperature	Tstg	°C	-55 ~ +110	1

Notes: 1. If the LSI is used beyond the absolute maximum ratings, it may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of the LSI is not guaranteed if it is used in the conditions above the limits and it may lead to malfunction.

2. Make sure (High) IOVCC1/2 ≥ GND (Low).
3. Make sure (High) VCI ≥ AGND (Low).
4. Make sure (High) DDVDH ≥ AGND (Low).
5. Make sure (High) AGND ≥ VGL (Low).
6. Make sure (High) VCI ≥ VGL (Low).
7. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Electrical Characteristics

DC Characteristics

Table 43 (IOVCC1 = 1.65V ~ 3.3V, Ta = -40°C ~ +85°C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input "High" level voltage 1 Interface pin (except RESX)	V_{IH1}	V	IOVCC1=1.65V ~ 3.3V	0.80× IOVCC1	-	IOVCC1	1,2
Input "Low" level voltage 1 Interface pin (except RESX)	V_{IL1}	V	IOVCC1=1.65V ~ 3.3V	0	-	0.20× IOVCC1	1, 2
Input "High" level voltage 2 RESX	V_{IH2}	V	IOVCC1=1.65V ~ 3.3V	0.90× IOVCC1	-	IOVCC1	1,2
Input "Low" level voltage 2 RESX	V_{IL2}	V	IOVCC1=1.65V ~ 3.3V	0	-	0.10× IOVCC1	1,2
Output "High" level voltage 1 (DB[17:0], TE, LEDPWM)	V_{OH1}	V	IOVCC1=1.65V ~ 3.3V, IOH=-0.1mA	0.8× IOVCC1	-	-	1
Output "Low" level voltage 1 (DB[17:0], TE, LEDPWM)	V_{OL1}	V	IOVCC1=1.65V ~ 3.3V, IOL=0.1mA	-	-	0.20× IOVCC1	1
Input/Output leakage current from bus interface pin	I_{LI}	μA	Vin=0 ~ IOVCC1	-1	-	1	4
Current consumption (IOVCC1-GND) Normal Mode, BLC OFF (262,144-color display operation)	I_{OP1}	μA	480-line drive, IOVCC1=1.80V, VCI=2.80V, fFRM=60Hz, Ta=25°C, Frame memory data: 18'h00000, BLCON=0	-	500	700	5, 6
Current consumption (IOVCC1-GND) Idle Mode (64-line drive, partial display operation)	I_{op2}	μA	64-line drive, partial display operation, IOVCC1=1.80V, VCI=2.80V, fFRM=40Hz, Ta=25°C, BC2=0, Frame memory data: 18h'00000, BLCON=0	-	500	700	5, 6
Current consumption (IOVCC1-GND) Normal Mode, BLC ON (262,144-color display operation)	I_{OP3}	μA	480-line drive, IOVCC1=1.80V, VCI=2.80V, fFRM=60Hz, Ta=25°C, Frame memory data: 18'h00000, BLCON=1	-	650	850	5, 6
Current consumption (IOVCC1-GND) Sleep IN Mode	I_{ST}	μA	IOVCC1=1.8V, Ta=25°C	-	50	250	5, 6
Current consumption (IOVCC1-GND) Deep Standby Mode	I_{DST}	μA	IOVCC1=1.8V, Ta=25°C	-	0.1	1.0	5, 6

Current consumption (IOVCC1-GND) Frame memory access mode	I_{RAM}	mA	IOVCC1=1.80V, VCI=2.80V, tCYCW=70ns, Ta=25°C, Consecutive frame memory access during display operation. 8 bit x 2 transfers, Write data: 18'h00000	-	1.8	4.0	5, 6
LCD power supply current (VCI-AGND) 262,144-color display operation (Normal Mode + Idle Mode Off)	Ici1	mA	IOVCC1=1.8V, VCI=2.8V, 480-line drive, fFRM=60Hz, Ta=25°C, Frame memory data: 18'h00000, DIV0=2'h0, RTN0=5'h1A REV=0, BC0=0, FP0=8'h8, BP0=8'h8, VC=3'h4, BT=3'h2, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h4, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0, PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2), No load on the panel, BLCON=0	-	3.2	5.0	5, 6

LCD power supply current (VCI-AGND) 8-color (64-line partial display operation) (Partial Mode + Idle Mode On)		Ici2	mA	IOVCC1=1.8V, VCI=2.8V, 64-line partial display, fFRM=40Hz, Ta=25°C, Frame memory data: 18'h00000, DIV2=2'h1, RTN2=5'h14, REV=0, BC2=0, FP2=8'h8, BP2=8'h8, VC=3'h4, BT=3'h2, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP2=2'h3, DC02=3'h4, DC12=3'h2, DC32=3'h4, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0, PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0, (*: 0, 1, 2), No load on the panel, BLCON=0	-	0.8	1.5	5, 6
Output voltage deviation	V0~ V63	ΔVO	mV	–	-	-	40	7
Average output voltage variance		ΔVΔ	mV	—	-35	-	+35	8

Step-up Circuit Characteristics

Table 44

Item		Unit	Test Condition	Min.	Typ.	Max.	Note
Step-up output voltage	DDVDH	V	IOVCC1=1.8V, VCI =2.8V, Ta=25°C, DIV*=2'h1, RTN*=5'h11, VC=3'h4, BT=3'h2, AP*=2'h3, DC0*=3'h4, DC1*=3'h2, DC3*=3'h4, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, No load on the panel, Iload1=-3 [mA]	4.98	5.13	-	-
	VGH	V	IOVCC1=1.8V, VCI =2.8V, Ta=25°C, DIV*=2'h1, RTN*=5'h11, VC=3'h4, BT=3'h2, AP*=2'h3, DC0*=3'h4, DC1*=3'h2, DC3*=3'h4, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL =1[uF]/B characteristics, No load on the panel, Iload2=-100[uA],	14.84	15.20	-	-
	VGL	V	IOVCC1=1.8V, VCI =2.8V, Ta=25°C, DIV*=2'h1, RTN*=5'h11, VC=3'h4, BT=3'h2, AP*=2'h3, DC0*=3'h4, DC1*=3'h2, DC3*=3'h4, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL =1[uF]/B characteristics, No load on the panel, Iload3=+100[uA]	-	-10.10	-9.60	-
	VCL	V	IOVCC1=1.8V, VCI =2.8V, Ta=25°C, DIV*=2'h1, RTN*=5'h11, VC=3'h4, BT=3'h2, AP*=2'h3, DC0*=3'h4, DC1*=3'h2, DC3*=3'h4, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL =1[uF]/B characteristics, No load on the panel, Iload4=+1000[uA]	-	-2.34	-2.04	-

Internal Reference Voltage

Table 45

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Internal reference voltage	VCIR	V	IOVCC1 = 2.5V ~ 3.3V Ta = -40°C ~ +85°C	-	2.53	-	-

Power Supply Voltage Range (Ta=-40°C ~ +85°C, GND=AGND=0V)

Table 46

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Power supply voltage	IOVCC1	V	Ta = -40°C ~ +85°C	1.65	1.8/2.8	3.3	-
Power supply voltage	IOVCC2	V		2.5	3.0	3.3	
Power supply voltage	VCI	V		2.5	2.8	3.3	-

Output Voltage Range

Table 47

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Grayscale, VCOM reference voltage	VREG	V	Ta = -40°C ~ +85°C GND=AGND=0V	-	-	DDVDH-0.5	-
Source driver		V		GND+0.2	-	VREG	-
VCOMH output	VCOMH	V		3.0	-	VREG	-
VCOML output	VCOML	V		VCL+0.5	-	0.0	-
VCOM amplitude		V		-	-	6.0	-
Step-up output voltage	DDVDH	V		4.5	-	6.0	-
Step-up output voltage	VGH	V		10.0	-	18.0	-
Step-up output voltage	VGL	V		-13.0	-	-4.5	-
Step-up output voltage	VCL	V		-3.0	-	-1.9	-
Voltage between VCI and VCL		V		-	-	6.0	-
Voltage between VGH and VGL		V		-	-	28.0	-

AC Characteristics (IOVCC1=1.65V ~ 3.30V, Ta=-40°C ~ +85°C: Note 1)

Clock Characteristics

Table 48

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
RC oscillation clock	fosc	kHz	IOVCC1=1.8V, 25°C	730	785	840

DBI Type B (18-/16-/9-/8-Bit) Timing Characteristics

Table 49 1-, 3/2-, 2-, 3- Transfer, IOVCC1=1.65V ~ 3.30V

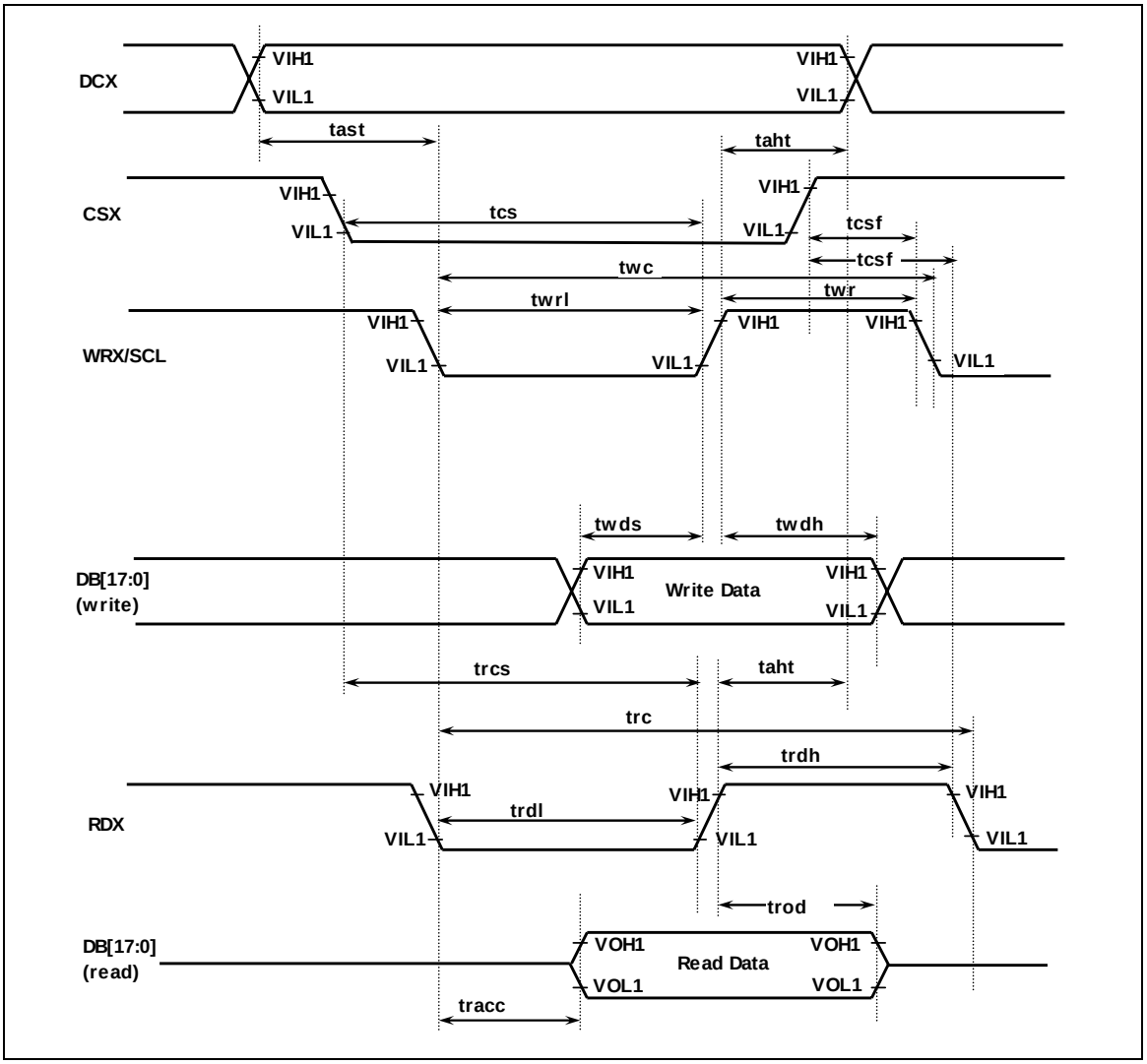
Item		Symbol		Unit	Test Condition	Min.	Max.
Address setup time		DCX	tast	ns		0	-
Address hold time (Write/Read)			taht	ns		10	-
Chip select setup time (Write)		CSX	tcs	ns		30	-
Chip select setup time (Read)			trcs	ns		170	-
Chip select wait time (Write)			tcsfw	ns		20	-
Chip select wait time (Read)			tcsfr	ns		20	
1 transfer	Write cycle time	WRX	twc1	ns		60	-
	Write control pulse ”High” period		twrh1	ns		30	-
	Write control pulse ”Low” period		twrl1	ns		30	-
3/2 transfers 2 transfers	Write cycle time		twc2	ns		40	-
	Write control pulse ”High” period		twrh2	ns		20	-
	Write control pulse ”Low” period		twrl2	ns		20	-
3 transfers	Write cycle time		twc3	ns		40	-
	Write control pulse ”High” period		twrh3	ns		20	-
	Write control pulse ”Low” period		twrl3	ns		20	-
Read cycle time		RDX	trc	ns		450	-
Read control pulse ”High” period			trdh	ns		250	-
Read control pulse ”Low” period			trdl	ns		170	-
Write data setup time		DB[17:0]	twds	ns	CL Max.30pF Min.8pF	15	-
Write data hold time			twdh	ns		20	-
Read access time			tracc	ns		10	150
Output disable time			trod	ns		10	-

Note: 1 transfer: (1)16-bit I/F 16 bits/pixel, (2)18-bit I/F 18 bits/pixel

3/2 transfers: (1)16-bit I/F 18 bits/pixel Option1

2 transfers: (1) 8-bit I/F 16 bits/pixel, (2) 9-bit I/F 18 bits/pixel

3 transfers: (1) 8-bit I/F 18 bits/pixel, (2)18-bit I/F 18 bits/pixel Option2



- **Figure A DBI Type B (16-/ 18-Bit, 8-/9-Bit Timing) Bus Timing**

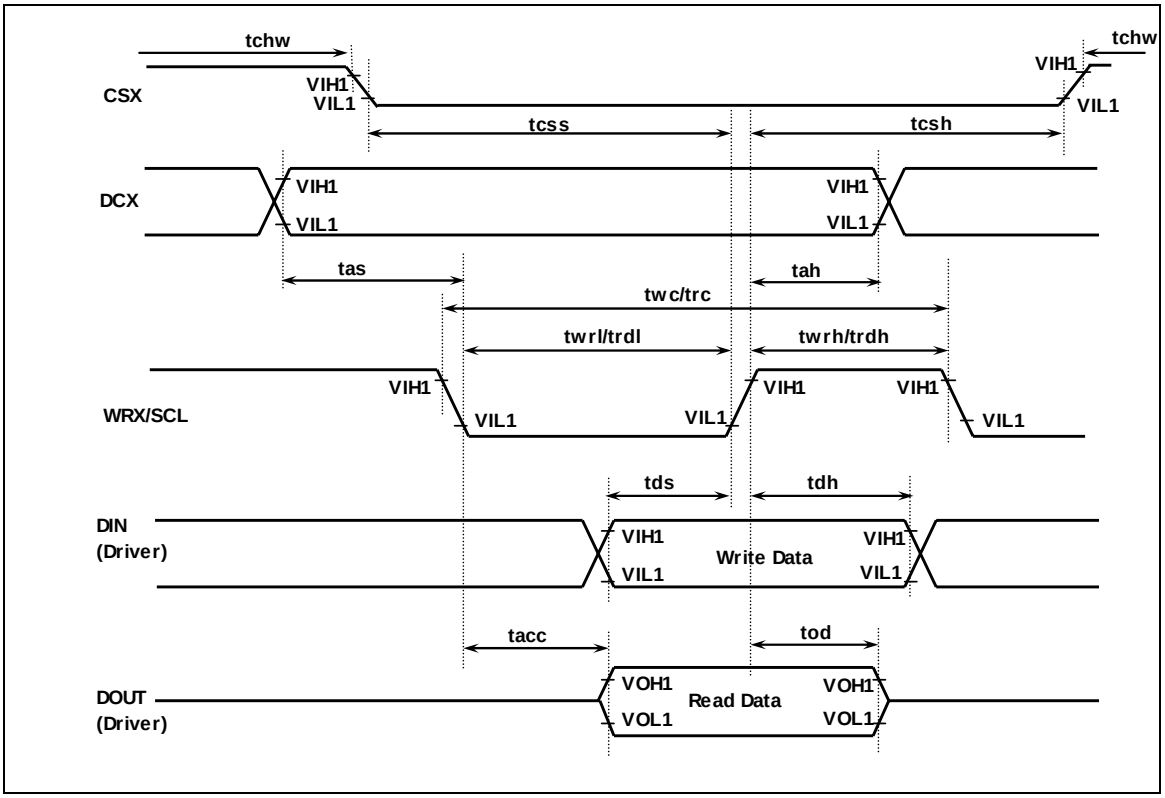
Note: Unused DB[17:0] pins shall be fixed to “IOVCC1” or “GND”.

DBI Type C Timing Characteristics

Table 50 IOVCC1=1.65V ~ 3.30V

Item	Symbol		Unit	Test Condition	Min.	Max.
Chip select setup time	CSX	tcss	ns		40	-
Chip select hold time		tcsh	ns		40	-
Chip select “High” pulse width		tchw	ns		100	
Address setup time	DCX	tas	ns		10	-
Address hold time (Write/Read)		tah	ns		10	-
Write cycle time	WRX/SCL (Write)	twc	ns		100	-
WRX/SCL ”High” period (Write)		twrh	ns		40	-
WRX/SCL ”Low” period (Write)		twrl	ns		40	-
Read cycle time	WRX/SCL (Read)	trc	ns		300	-
WRX/SCL ”High” period (Read)		trdh	ns		120	-
WRX/SCL ”Low” period (Read)		trdl	ns		120	-
Data setup time	DIN	tds	ns		30	-
Data hold time		tdh	ns		30	-
Access time	DOUT	tacc	ns	CL Max.30pF Min.8pF	-	110
Output disable time		tod	ns		10	-

Note: The address setup time and address hold time are defined only in Option 3.

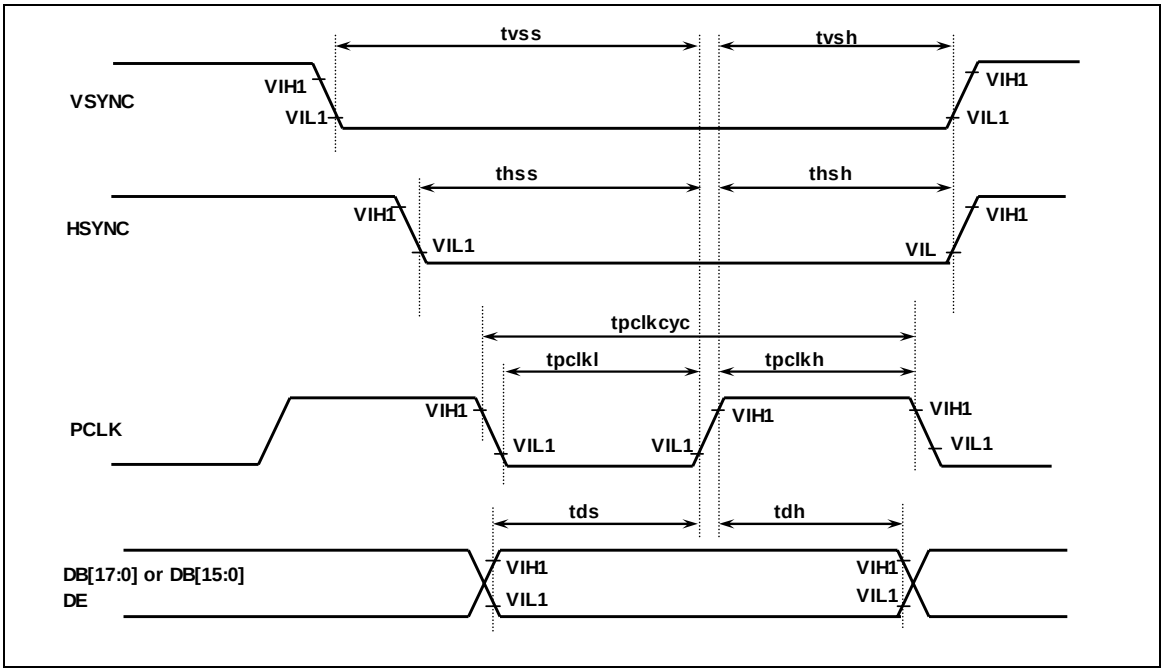


- **Figure B DBI Type C Timing**

DPI Timing Characteristics

Table 51 IOVCC1=1.65V ~ 3.30V

Item	Symbol		Unit	Test condition	Min.	Max.
VSYNC Setup Time	VSYNC	tvss	ns		30	-
VSYNC Hold Time		tvsh	ns		30	-
HSYNC Setup Time	HSYNC	thss	ns		30	-
HSYNC Hold Time		thsh	ns		30	-
Pixel Clock Cycle Time	PCLK	tpclkcyc	ns		60	-
Pixel Clock "Low" period		tpclkl	ns		30	-
Pixel Clock "High" period		tpclkh	ns		30	-
Data Setup Time	DB[17:0] or DB[15:0] DE	tds	ns		30	-
Data Hold Time		tdh	ns		30	-

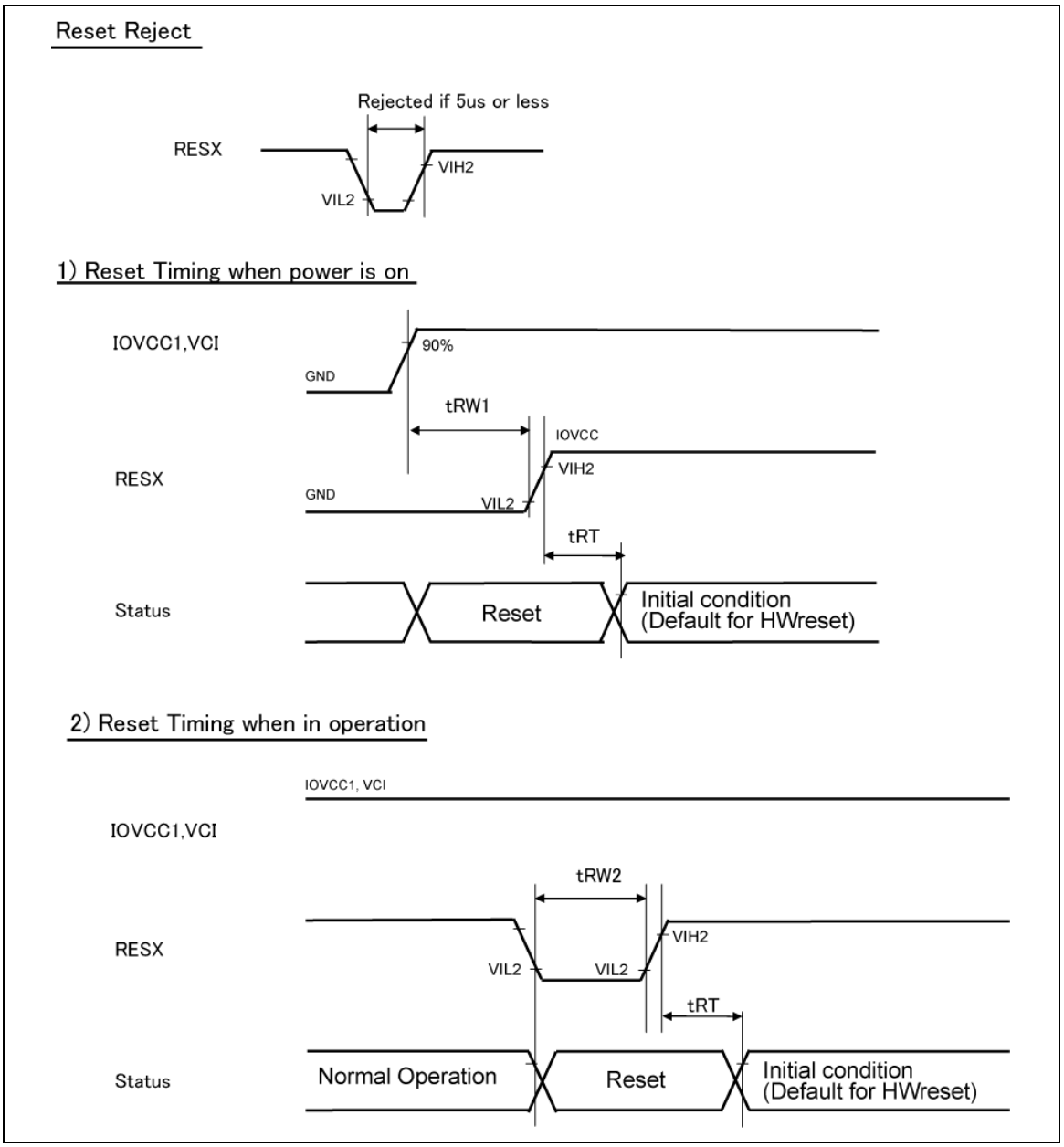


- **Figure C DPI Timing**

Reset Timing Characteristics

Table 52 (IOVCC1=1.65V ~ 3.10V, Ta=-40°C ~ +85°C)

Item	Symbol	Unit	Test Condition	Min.	Max.
Reset "Low" level width 1	tRW1	ms	Power On	1	–
Reset "Low" level width 2	tRW2	us	Operation	10	–
Reset time	tRT	ms		–	5

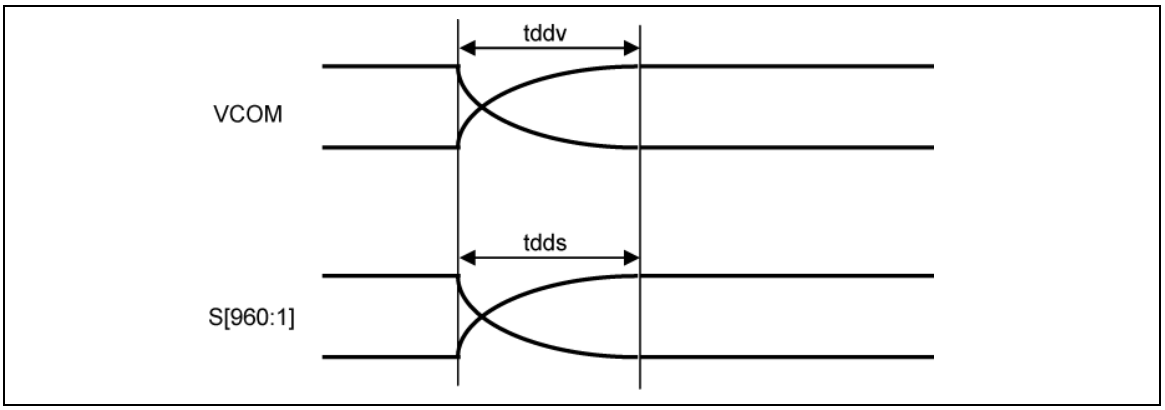


- **Figure E Reset Timing**

Liquid Crystal Driver Output Characteristics

Table 53

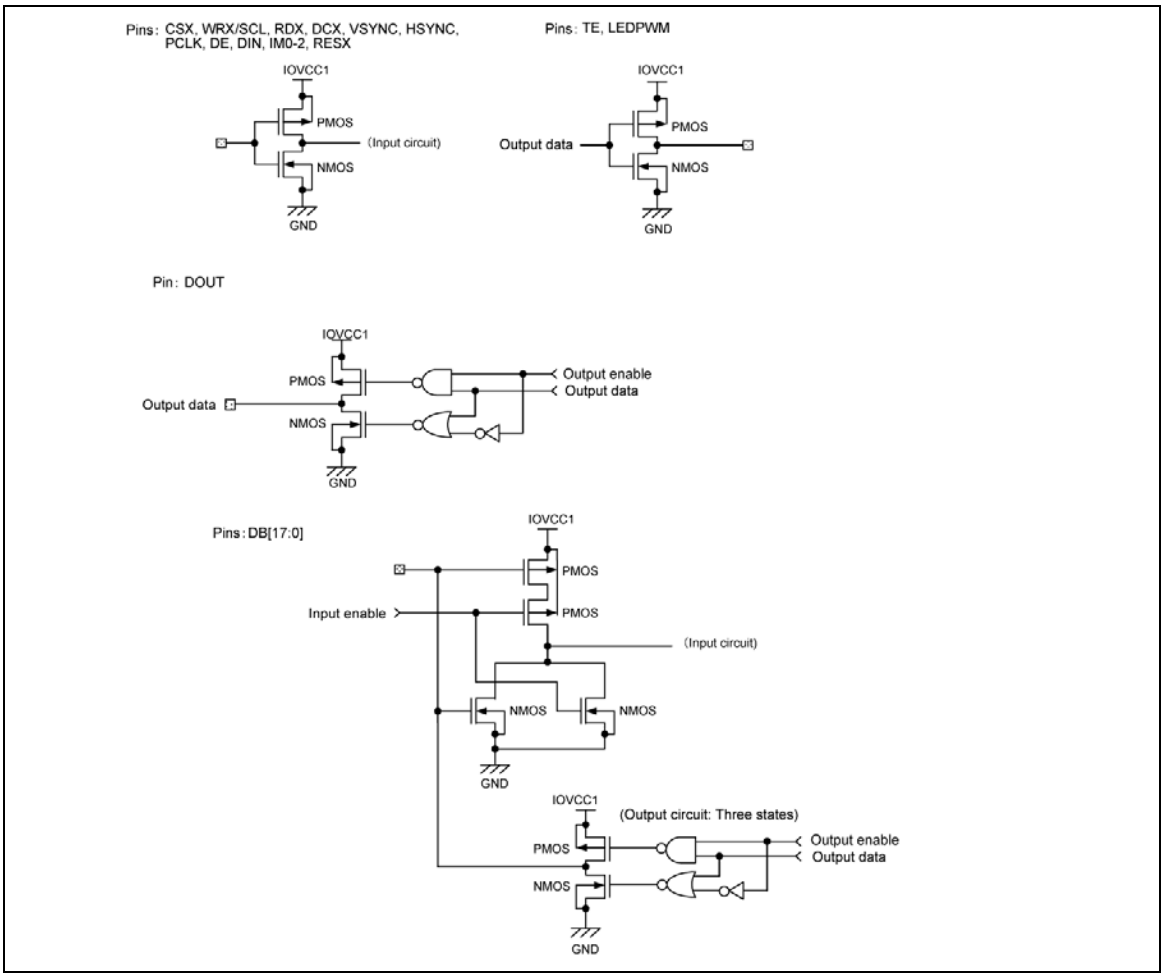
Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
VCOM output delay time	tddv	us	IOVCC1=1.80V, VCI=2.80V, Ta=25℃, REV=0, BC0=0, FP0=8'h5, BP0=8'h8, VC=3'h4, BT=3'h2, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h4, Time to reach ±35mV from VCOM polarity inversion timing, load resistance R = 100ohm, load capacitance C=20nF	-	25	-	9
Source driver output delay time	tdds	us	IOVCC=1.80V, VCC=VCI=2.80V, Ta=25℃, REV=0, BC0=0, FP0=8'h5, BP0=8'h8, VC=3'h4, BT=3'h2, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, DC30=3'h4, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0, (*: 0, 1, 2) Same change from same grayscale at all time-division source output pins. Time to reach ±35mV between source V0 and V63, Load resistance R =10kohm, load capacitance C=15pF	-	25	-	10



- **Figure F Liquid Crystal Driver Output Timing**

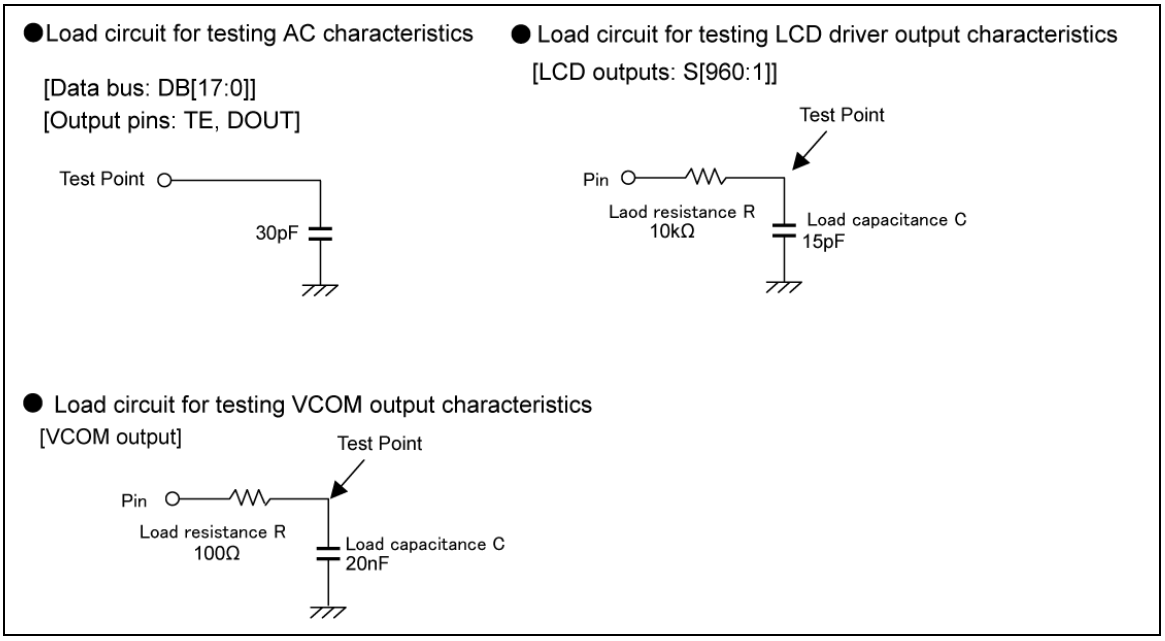
Notes on Electrical Characteristics

Notes: 1. DC/AC electrical characteristics of bare die and wafer are guaranteed at +85°C.
2. The following figures illustrate the configurations of input, I/O, and output pins.



- **Figure G**

3. TEST[2:1], VREFC, VDDTEST, TSC, and VPP1 shall be left open. IM[0:2] shall be fixed to IOVCC1 or ground (GND).
4. This excludes the current in the output drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because shoot-through current increases in the input circuit when the CMOS input is at a mid-level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.
6. Values are average current values.
7. The output voltage deviation is the difference in voltages between output pins that are placed side by side in the same display mode. It is a reference value.
8. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with the same display data.
9. VCOM output delay time depends on load on the liquid crystal panel. Therefore, frame frequency and one line cycle need to be specified, checking image quality on the panel to be used.
10. LCD driver output delay time depends on load on the liquid crystal panel. Therefore, frame frequency and one line cycle need to be specified, checking image quality on the panel to be used.



- **Figure H Test Circuits**

Revision Record

Rev.	Date	Page No	Contents of Modification
0.00	April 19, 2010		First issue
0.01	April 21, 2010	76	NVAD deletion
		176	NVAD[0] deletion
			CALB deletion
1.00	May 14, 2010	All	Preliminary Specification → Specification
1.10	July 01, 2010	15	Power Supply Circuit Pins; Signal; C21P, C21M → C12P, C12M
		56	Clock frequency 5.65MHz → 10.71MHz
		65	04h; read_DDB_start; Number of Parameter; 1 → 5
		66	A8h read_DDB_continue added.
		79	read_DDB_start; 04h; 5th parameter; Hex; 04h → FFh
		85	get_pixel_format; Description; “x = Don’t care.” added.
		105	write_memory_start; “parameter” → “pixel data”
		107	read_memory_start; “parameter” → “pixel data”
		131	read_DDB_continue; “Dummy Parameter” row added.
		145	Back Light Control (2); 1st parameter; DB1:0 → LEDON
		155	Description; “Step-up clock frequency in non-lit display area” column deleted. PTDC description added.
		169	VCOM Setting; Hex; xx → xxh
		176	NVM Access control; 2nd parameter; DB5; 0 → CALB, Description “CALB” added.
		182	Power/Display On/Off Sequence Examples; exit_sleep_mode; “Internal NVM data load / Automatic” deleted.
		210	Figure; G432 → Gmax
		211	Figure; G432 → Gmax
		237	DPI timing; tpclkcyc; Min; 100 → 60
		224	“32 bits are for Supplier ID (read by read_DDB_start)” added. “exit_sleep_mode_sequence” deleted.
1.20	April 26, 2011	176	Description of CALB added.
		226	"1" → "0", "0" → "1" (description)
1.30	May 10, 2011	164	Interface Setting (C6h) ; 1st parameter; DB1 :0 → EPL

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