**Course Title:** **Digital Logic**
**Course Number:** **ENGR-AD 113**

**Course Description:** This module provides a rigorous introduction to topics in digital logic design mostly focusing on combinational circuits but also touching upon basic concepts in sequential circuits. Introductory topics include: classification of digital systems, number systems and binary arithmetic, error detection and correction, and switching algebra. Combinational design analysis and synthesis topics include: logic function optimization, arithmetic units such as adders and subtractors, and control units such as decoders and multiplexers. A brief overview of sequential circuits by introducing basic memory elements such as flip-flops, and state diagrams concludes the module.

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| **Course Hour/Week** | 2 lectures per week (75 mins each) + 145 min lab/recitation per week, Fall second half semester (7 weeks), 2 hr final exam is after 7th week |
| **Credits** | 2 credits |
| **Course Category:** | Engineering Common Course |
| **Prerequisite**: | None |
| **Instructor** | Professor Yi Fang<br>C1-156; Email: yfang@nyu.edu ;<br>Lab Instructor: Muhammad Sheikh (faraz.afzal@nyu.edu) |

**Intended Learning Outcomes:** The following learning outcomes are anticipated upon completion of this course. Students will be able to:

- Identify, formulate and solve circuit problems (assessed by quizzes, exams, and laboratory projects). [(e.1), (e.2), (e.3)]
- Analyze a given logic circuit to identify its functionality and quantify its area, performance, etc. costs by applying mathematical and engineering knowledge (assessed by quizzes, exams, and laboratory projects). [(a.3)]
- Transform a given design specification sheet into an optimized logic design that meets desired speed and cost constraints (assessed by quizzes and laboratory projects). [(c.3)]
- Demonstrate skill in using simple software (CAD) tools to design, simulate and verify a logic circuit (assessed by laboratory projects). [(k.1)]
- Judiciously apply well-known design principles such as hierarchical design and iterative design techniques to further reduce design costs (assessed by quizzes, exams, and laboratory projects). [(c.1)]

**Text Book:** Digital Design (Fifth Edition) by M. Morris Mano and Michael D. Ciletti (2006); Chapters covered: 1-6

**Software for Lab:** Logicworks 5 Interactive Software by Capilano Computing (*CD comes with the textbook and can be used to install the software on personal computers/laptops*); ISE Xilinx FPGA suite

**Teaching and Learning Methodologies:** Lecture is the primary mode of delivery. PowerPoint slides will be provided to the students prior to the lectures. Students will be provided with homework problems that will not be graded; Homework will be assigned at the end of each lecture session. Selected problems from these homework sets will be asked in announced quizzes. These quizzes will be graded quickly and provided back to the students to enable them to learn from their mistakes. Lab sessions will be used to perform a demo (earlier in the semester) for the students, or to describe the lab project. Some projects are meant to be completed within the lab session, and some are take-home and to be completed by the next lab session. Every lab project requires a lab report. Some projects require a demo in addition. Recitation sessions are dedicated for reinforcing course topics via solving representative problem sets and holding class discussions.

**Evaluation:** Students will be graded as follows.

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| Four announced quizzes each with a question or two selected from the homework problems | 20% |
| Three lab projects, described in a lab session, individually completed at home and due by next lab | 20% |
| Midterm exam (written exam, closed notes and book). | 25% |
| Final exam (comprehensive, written exam, closed notes and book). | 35% |
| Total | 100% |

**Related Laboratory Exercises:** Laboratory projects on logic design, analysis and simple simulations (with the *LogicWorks* tool) will be described in lab sessions, and will be completed by students during the lab periods only for the first lab project. The remaining two projects will be described in a lab session, and completed by the students as a take home assignment by the next lab session (within two weeks). Reports and design files must be submitted electronically for all projects through NewClasses, which will be the basis for evaluation.

**Schedule**: A typical schedule for course topics, homework, and exam dates is given in the table below. This schedule is subject to change depending on the dates of holidays, etc.

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|---|---|
| **Lecture 1:** Introduction to Digital Logic Design<br>• Digital computer systems overview<br>• Information representation<br>• Number systems and base conversions | **Lecture 8:** Logic Function Minimization – Part II<br>• (Prime) implicants/implicates<br>• Don't care bits<br>• Systematic optimization |
| **Lecture 2:** Coding Theory Fundamentals<br>• Code-words and distance concept<br>• Error detection and correction<br>• Parity, Gray, BCD and Hamming codes | **Midterm** |
| **Lecture 3:** Arithmetic Operations (Quiz)<br>• Single/multiple bit addition/subtraction<br>• One's and two's complement representations<br>• Binary multiplication<br>• BCD addition/subtraction | **Lecture 9:** Complex Gates (Quiz)<br>• NAND/NOR gates<br>• Universal gate concept<br>• XOR/XNOR gates<br>• More complex gates |
| **Lecture 4:** Intro to Combinational Logic – Part I<br>• Binary logic and gates<br>• Boolean algebra | **Lecture 10:** Combinational Logic Design<br>• Design procedure and example<br>• Technology mapping and verification<br>• Homework 4 Assigned |
| **Lecture 5:** Intro to Combinational Logic – Part II (Quiz)<br>• Boolean algebra – continued<br>• Canonical forms<br>• Minterms and maxterms | **Lecture 11:** Arithmetic Circuit Design – Part I (Quiz)<br>• Half/full adder<br>• Ripple carry adder design<br>• Carry look-ahead adder design |
| **Lecture 6:** Intro to Combinational Logic – Part III<br>• Sum of minterms & product of maxterms<br>• Complement of functions<br>• Conversions between representations | **Lecture 12:** Arithmetic Circuit Design – Part II<br>• Subtractor design<br>• Adder-subtractor design<br>• Design by contraction |
| **Lecture 7:** Logic Function Minimization – Part I (Quiz)<br>• Cost metrics<br>• Karnaugh-maps | **Lecture 13:** Advanced topics (Quiz)<br>• Commonly used combinational blocks: Decoders, encoders, multiplexers<br>• Introductory view of sequential circuits |
| | **Final** |

## Lab projects (subject to changes):

- **Introduction to LogicWorks**
- **Simple combinational logic design (Lab Project #1)**
- **Alarm clock design (Lab Project #2)**
- **Design of RC and CLA adders (Lab Project #3)**

## Relationship to Outcomes:

| | Shared Engineering Outcomes | | | | | Program Specific Outcomes | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | CE | CompE | EE | ME | GenE |
| Lectures | x | | | | x | | x | x | | x |
| Labs | x | | | | x | | x | x | | x |

| | ABET Criteria | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | a | b | c | d | e | f | g | h | i | j | k |
| Lectures | x | | x | | x | | | | | | x |
| Labs | x | | x | | x | | | | | | x |

**Shared Engineering Outcomes:**

1. Apply techniques in the practice of leadership, innovation, inventiveness and entrepreneurship;
2. Identify social, economic, ethical and other factors that shape engineering solutions and incorporate them in conjunction with engineering principles in problem solving and designing systems, components, or processes to meet desired needs within realistic constraints;
3. Recognize and respond respectfully to cultural concerns and differences when solving problems both physical and ethical;
4. Exhibit guidance and organizational effectiveness in multidisciplinary teams as a participant and a leader;
5. Demonstrate competence in writing and speaking effectively, and in communicating significant technical information in a clear and concise manner.

**Program Specific Outcomes:**

- CE: Civil Engineering graduates will be able to work professionally in four of the technical areas of the civil engineering discipline, namely, structural, geotechnical, transportation and environmental, and also be able to apply the principles of project management to their work.
- CompE: Computer Engineering graduates will be able to analyze and design complex computing and network devices and systems containing hardware and software components.
- EE: Electrical Engineering graduates will be able to analyze and design complex electrical, electronic, and communication devices and systems containing hardware and software components.
- ME: Mechanical Engineering graduates will be able to work professionally in at least thermal and mechanical systems areas.
- GenE: General Engineering graduates will be able to analyze and design devices and systems in an interdisciplinary engineering thematic area.

**ABET Outcomes:**

(a) an ability to apply knowledge of mathematics, science, and engineering

(b) an ability to design and conduct experiments, as well as to analyze and interpret data

(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

(d) an ability to function on multidisciplinary teams

(e) an ability to identify, formulate, and solve engineering problems

(f) an understanding of professional and ethical responsibility

(g) an ability to communicate effectively

(h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context

(i) a recognition of the need for, and an ability to engage in life-long learning

(j) A knowledge of contemporary issues

(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice