

**VISVESVARAYA TECHNOLOGICAL UNIVERSITY**  
**Belgaum, Karnataka**



**PROJECT REPORT**  
**On**  
**VEHICLE DETECTION AND MONITORING USING**  
**MAGNETIC FIELD SENSORS**

*Submitted in partial fulfillment of the requirements for the award of degree*

**BACHELOR OF ENGINEERING**  
**In**  
**ELECTRONICS AND COMMUNICATION ENGINEERING**  
**By**

Pradeep Kumar. N

1BG10EC058

Nikunj Tonthanahal

1BG10EC054

Nafeeya Samar

1BG10EC047

Noor Zahara

1BG10EC055

**Under the guidance of**

***Internal Guide:***

*Mrs. Anuradha V. Rao*

*Assistant Prof,*

*Dept. of ECE, BNMIT.*

***External Guide:***

*Mr. Ravi Kumar D*

*Deputy General Manager,*

*PAC Dept., BEL*



Department of Electronics & Communication Engineering

***B.N.M. Institute of Technology***

Banashankari II Stage, Bangalore – 560 070

June 2014

# *B.N.M. Institute of Technology*

Banashankari II Stage, Bangalore – 560 070  
Department of Electronics & Communication Engineering



## CERTIFICATE

Certified that the project work entitled "**“VEHICLE DETECTION AND MONITORING USING MAGNETIC FIELD SENSORS”**" was carried out by **Pradeep Kumar.N (1BG10EC058)**, **Nikunj Tonthanahal (1BG10EC054)**, **Nafeeya Samar (1BG10EC047)**, **Noor Zahara (1BG10EC055)**, bonafide students of VIII semester in partial fulfillment for the award of Bachelor of Engineering degree in Electronics and Communication branch of the Visvesvaraya Technological University, Belgaum during the year 2013-14. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the report deposited in the department library. The project report has been approved as it satisfies the academic requirement in respect of Project work prescribed for the said degree.

Mrs. Anuradha V. Rao  
Assistant Professor  
Dept. of ECE, BNMIT

Dr. S. B. Bhanu Prashanth  
Head of the Department  
Dept. of ECE, BNMIT

Dr. M. S. Suresh  
Principal  
BNMIT

Name of the Examiners

Signature with Date

1.

2.

## ABSTRACT

In times of rapidly expanding mega cities all around the world, traffic congestion and mobility are becoming a growing problem. Only too familiar are the pictures of crowded highways packed with cabs, bikes, and cars, where nothing is moving due to constant traffic jams. Hence making traffic flows more efficient will be of greater importance with each passing day. By controlling the traffic, both travel time and negative impact on the environment can be reduced. However, efficient control requires cost-efficient and accurate estimation of traffic parameters, such as the number of vehicles passing a certain point per unit time, the current speed of vehicles, and their types.

The most popular methods of acquiring traffic parameters that are currently used in India, i.e. video image processing and infrared sensors, suffer from several drawbacks such as dependence on clear environmental conditions and suitable ambient light requirements.

The objective of the project is to develop a traffic monitoring and classification system using low power, low cost magnetic sensors and induction loops that are free from the aforementioned drawbacks.

The magnetic materials in a vehicle change the ambient magnetic field when the vehicle passes over the magnetic field sensors. This change is used to detect the vehicles moving over the sensor. The amount of change in magnetic field depends on the volume of the magnetic materials in the vehicle. Since two wheelers have comparatively lesser volume of magnetic materials, they produce smaller changes in the magnetic field compared to four wheelers. This difference is used for classification of the vehicles. The data acquired from this system is used to increase the efficiency of the existing roadways and to enhance the capacity of transportation networks at locations where the traffic densities are large.

### **Keywords**

Traffic Monitoring, iSense core, Gateway and Vehicle detection modules, Induction loops, Wireless sensor networks, ZigBee communication, Colpitt's oscillator, Arduino 2560.

## **ACKNOWLEDGEMENT**

First of all, we thank the almighty for providing us the strength and courage to complete the project in spite of the innumerable hurdles we faced.

We take this opportunity to express our profound gratitude to **Dr. M. S. Suresh, Principal, Prof. T. J. Rama Murthy, Director, BNMIT** for their continuous effort in creating a competitive environment in our college and encouragement through this course. We are also indebted to **Dr. S. B. Bhanu Prashanth, HOD, Department of Electronics and Communication Engineering, BNMIT**, for his valuable guidance and support.

We wholeheartedly thank our project supervisor, **Prof. Anuradha V. Rao, Department of Electronics and Communication Engineering, BNM Institute of Technology**, for continuously encouraging us to put in our best efforts. Her suggestion to improve the project is priceless and the support lent during trying times is fully appreciated.

We express sincere gratitude to our external guide **Mr. Ravikumar D, Deputy General Manager, Project and Consultancy Department** and **Mr. Surendra Kumar, Mr. Sourav Sarkar, Senior Engineers, Project and Consultancy Department**, at **Bharat Electronics Limited, Bangalore** for assigning the project and spending their valuable time in guiding us.

We also thank all the teaching and non teaching staff of BNMIT for their inspiration and for guiding us through the right paths.

Last but not the least, this project would not have been complete without the support, guidance and coordination of our parents and friends.

### **Project Associates:**

Pradeep Kumar. N	1BG10EC058
Nikunj Tonthanahal	1BG10EC054
Nafeeya Samar	1BG10EC047
Noor Zahara	1BG10EC055

# TABLE OF CONTENTS

I. INTRODUCTION .....	1
1.1 Motivation.....	1
1.2 Overview.....	1
1.1.1 Induction loop vehicle detection system.....	2
1.1.2 Anisotropic Magneto-Resistive vehicle detection system .....	4
II. DESIGN .....	9
2.1 General description .....	9
2.2 Hardware requirements .....	9
2.2.1 Inductive loops.....	9
2.2.2 Colpitt's Oscillator.....	10
2.2.3 Comparator .....	11
2.2.4 Quad Op-Amp IC MC33274 .....	11
2.2.5 Microcontroller: Arduino 2560.....	12
2.2.5 Voltage regulators: LM7805 and RT9164A .....	14
2.2.5.1 LM7805.....	14
2.2.5.1 RT9164A.....	15
2.2.6 Anisotropic Magneto Resistive sensors: KMZ52 .....	16
2.2.7 Microcontroller with transceiver: Jennic JN5148-001 .....	17
2.2.7.1 Wireless Transceiver.....	18
2.2.7.2 RISC CPU, On chip memory and Peripherals (Microcontroller) .....	22
2.3 Software requirements .....	24
2.3.1 LTspice IV .....	24
2.3.1.1 Simulating circuits using LTspice IV .....	25
2.3.2 Arduino IDE.....	28
2.3.2.1 Using the Arduino integrated development environment (IDE) to program ..	28
2.3.3 Cygwin .....	30
2.3.3.1 Description.....	30
2.3.5 iShell .....	31
2.3.6 Eclipse Indigo .....	35
2.3.6.1 Description .....	35
2.3.7 Microsoft Visual Studio 12.0.....	38
2.5 Design of AMR sensor vehicle detection system .....	46
III. RESULTS .....	51
3.1 Induction loop vehicle detection system.....	51

3.2 AMR sensor vehicle detection system.....	53
IV. CONCLUSION.....	54
V. FUTURE ENHANCEMENTS .....	55
VI. REFERENCES .....	56

# INTRODUCTION

# I. INTRODUCTION

## 1.1 Motivation

Traffic congestion and associated effects such as air pollution pose major concerns to the public. Congestion has increased dramatically during the past 20 years in all the major Indian cities. Congestion is an outcome of twin factors, (a) growth in number of vehicles on road, (b) limitations to expansion of road space. While the road length in urban areas was only 7 per cent of the total road length in India, in 2002, the number of registered motor vehicles in the 23 largest cities alone was 30 per cent of the total registered motor vehicles in the country. Thus, urban congestion is a serious problem and has severely constrained mobility.

Traffic congestion may be alleviated by improving the efficiency of the current transportation system through the implementation of advanced technologies. Real-time traffic surveillance is one of the most important components of such an approach, and real-time travel information is useful for advanced travel advisory systems. Emergency management agencies such as police, fire stations, and ambulance dispatchers may also benefit from real-time traffic information in routing their vehicles through the transportation network to save lives. Roadway safety and efficiency will be significantly enhanced by employing remote sensing and communication technologies capable of providing low-cost, scalable, and distributed data acquisition of road conditions. Such Intelligent Transportation System (ITS) applications require distributed acquisition of different traffic metrics such as traffic speed, volume, and density which can be obtained using magnetic sensors and induction loops.

## 1.2 Overview

In times of rapidly expanding mega cities all around the world, traffic congestion and mobility are becoming a growing problem. Maximizing the efficiency and capacity of existing transportation networks is vital because of the continued increase in traffic volume and the limited construction of new highway facilities in urban, inter-city, and rural areas. Even when additional facilities are built to ease congestion and promote the use of multiple occupancy vehicles, the cost is often quite high. An alternative to expensive new highway construction is the implementation of strategies that promote more efficient utilization of current road, rail, air, and water transportation facilities. Efficient control requires cost-efficient and accurate

estimation of traffic parameters, such as the number of vehicles passing a certain point per unit time, the current speed of vehicles, and their types. The estimation can be based on data collected from magnetic sensors placed close to the road or induction loops buried into the road surface.

A vehicle is built up of several types of magnetic materials; soft magnetic materials with no residual magnetization and hard magnetic materials with high residual magnetization. All of these materials in the vehicle create a disturbance in the earth magnetic field when the vehicle passes a specific region. When a magnetic sensor system with high field sensitivity and resolution, or a simple induction loop in placed in this region, it is possible to detect this change and hence the presence of vehicle. A generic block diagram of such a simple vehicle detection and monitoring system is shown in Fig 1.1.

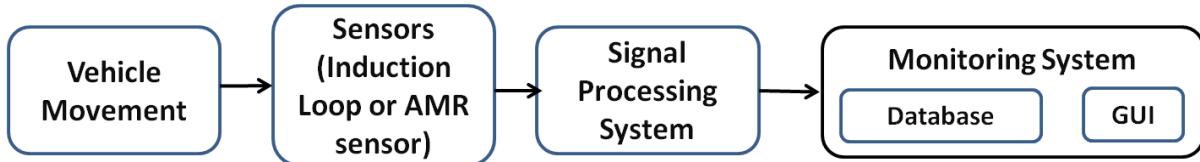


Fig 1.1 Block diagram of simple vehicle detection and monitoring system

The signal processing system processes the data from the sensors to eliminate any errors or false detections. Finally the traffic parameters acquired from the sensors are updated in a database and displayed using a GUI on the computer.

This project implements the induction loop as a means of acquiring vehicle count and classifying vehicles into two wheelers and four wheelers. The AMR sensors are used to acquire the count and speed of the vehicles.

### 1.1.1 Induction loop vehicle detection system

An induction loop is an insulated electric wire through which an alternating current is driven to set up an electromagnetic field which is disturbed when a vehicle passes over the loop. This disturbance is used to detect the presence of vehicles.

Since its introduction, the inductive-loop detector has become the most utilized sensor in a traffic management system. The principal components of an inductive-loop detector system include:

- One or more turns of insulated loop wire wound in a shallow slot sawed in the pavement.
- Lead-in cable from the loop to the controller cabinet.
- Electronics unit housed in a nearby controller cabinet.

Figure 1.2 displays a notional diagram of an inductive-loop detector.

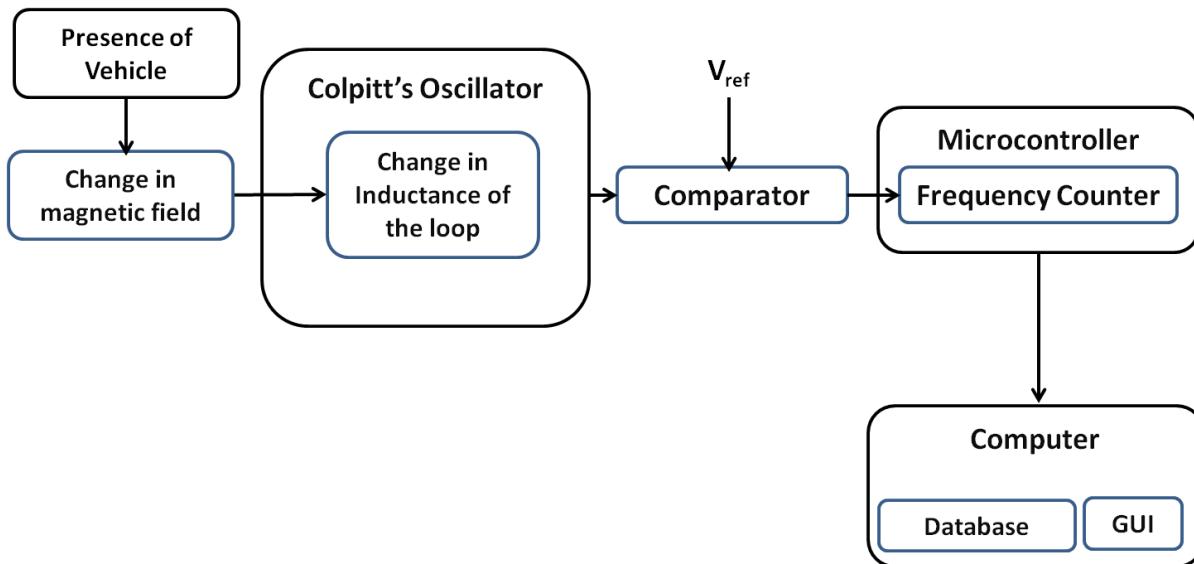


Fig 1.2 Block Diagram of Induction Loop Detector

The functioning of Inductive loop sensors is as follows. The inductive-loop is a part of the tank circuit of a Colpitt's oscillator in which the loop wire and lead-in cable are the inductive elements. The comparator acts as an A/D convertor and converts the analog output signal of the oscillator into a square wave. This is fed to a microcontroller which continuously measures the frequency of the square wave input. When a vehicle passes over the loop or is stopped within the loop, the vehicle induces eddy currents in the wire loops, which decrease their inductance. The decreased inductance results in an increase in the frequency of the oscillator output. This increase in frequency is used by the microcontroller to detect the presence of vehicles.

The amount of eddy currents induced in the loop and thus the change in frequency depends on the mass of the ferromagnetic material in the proximity of the loop. Since two wheelers and four wheelers have different amounts of ferromagnetic material in them, the corresponding

frequency change as they pass over the loop is also different. This difference is used by the microcontroller to classify the vehicles.

The traffic parameters i.e. the count and classification of vehicles is then sent by the microcontroller to a computer where they are displayed in the GUI and stored in a database. A flow chart for the functioning of the Induction loop detector system is shown in Fig 1.3.

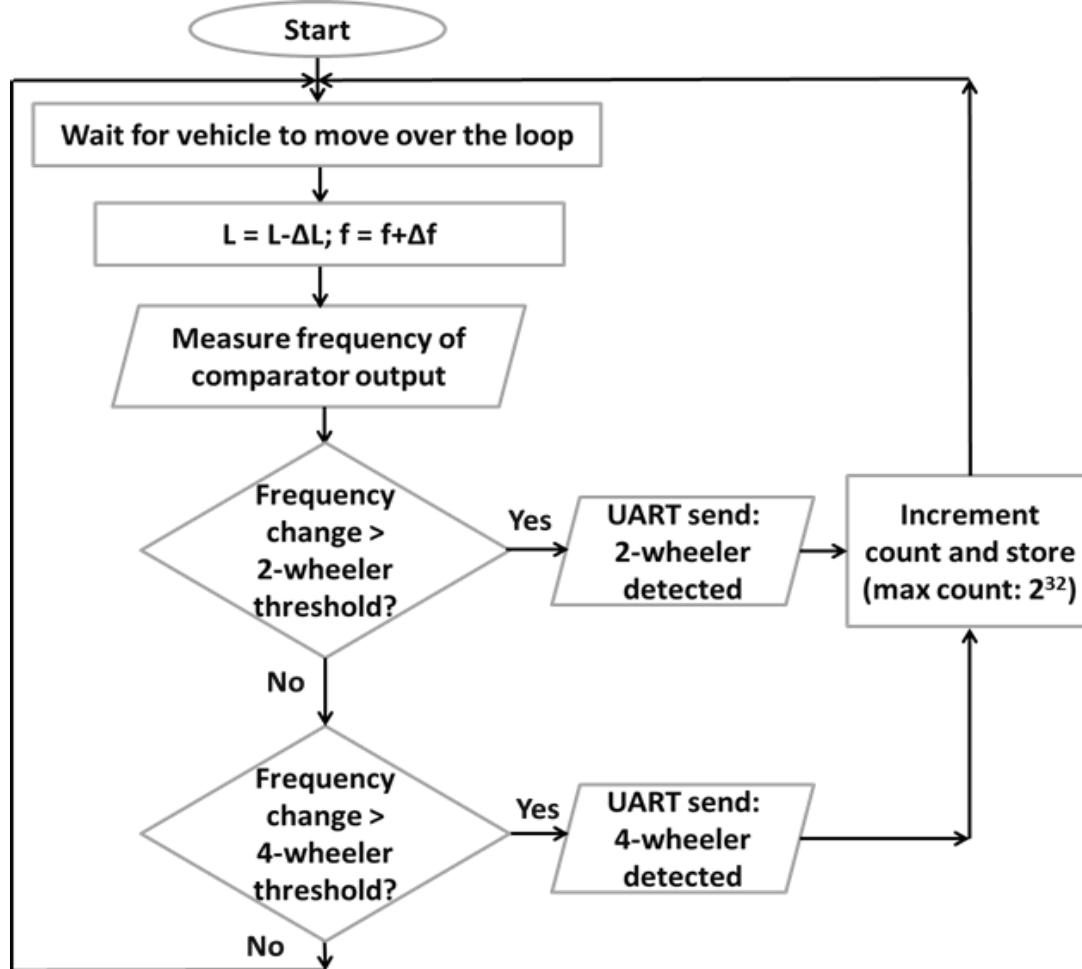


Fig 1.3 Flowchart for Induction Loop system

### 1.1.2 Anisotropic Magneto-Resistive vehicle detection system

An AMR sensor is a sensing device that utilizes the rate of change of magnetic resistance which is affected by the strength of the external magnetic field to detect the presence of vehicles.

Magnetic sensors were introduced as an alternative to the inductive-loop detector for specific applications. A magnetic sensor is designed to detect the presence or passage of a vehicle by

measuring the perturbation in the Earth's quiescent magnetic field caused by a ferrous metal object (e.g., a vehicle) when it enters the detection zone of the sensor.

Early magnetic sensors were utilized to determine if a vehicle had arrived at a "point" or small-area location. Modern AMR sensors are used for vehicle presence detection and counting. Unlike the inductive-loop detector, the magnetometer are usually used in places where cutting the deck pavement for loop installation is not permitted. Also, the magnetometer probe and its lead-in wire tend to survive in crumbly pavements longer than ordinary loops.

An iron or steel vehicle distorts the magnetic flux lines because ferrous materials are more permeable to magnetic flux than air. That is, the flux lines prefer to pass through the ferrous vehicle. As the vehicle moves along, it is always accompanied by a concentration of flux lines known as its "magnetic shadow" as illustrated in Fig 1.4. There is reduced flux to the sides of the vehicle and increased flux above and below it. An AMR sensor installed within the pavement detects the increased flux below the vehicle.

The block diagram of the AMR vehicle detection system is show in Fig 1.5. The system contains two slave modules that are buried along the length of the road with a distance of two meters between them. The slave modules consist of a two axis AMR sensor and a microcontroller interfaced with a ZigBee transceiver. The modules are used for speed calculation and communicate with a master module using ZigBee protocol. The master module consists of a microcontroller interfaced with a ZigBee transceiver and is connected to the computer through UART. The sensors on the slave modules detect the presence of vehicles and send a time stamp indicating the time at which the vehicle was detected to the master module. The difference in time indicated by the two time stamps is then used by the master module to calculate the speed using the following relation.

$$S = D/T \dots \dots \dots \quad (1.1)$$

where,

S is the speed,

D is the distance between the two AMR sensors i.e. 2m,

T is the difference between the times indicated by the two time stamps.

The traffic parameters i.e. the count and speed of the vehicles is then sent by the microcontroller to a computer where they are displayed in the GUI and stored in a database.

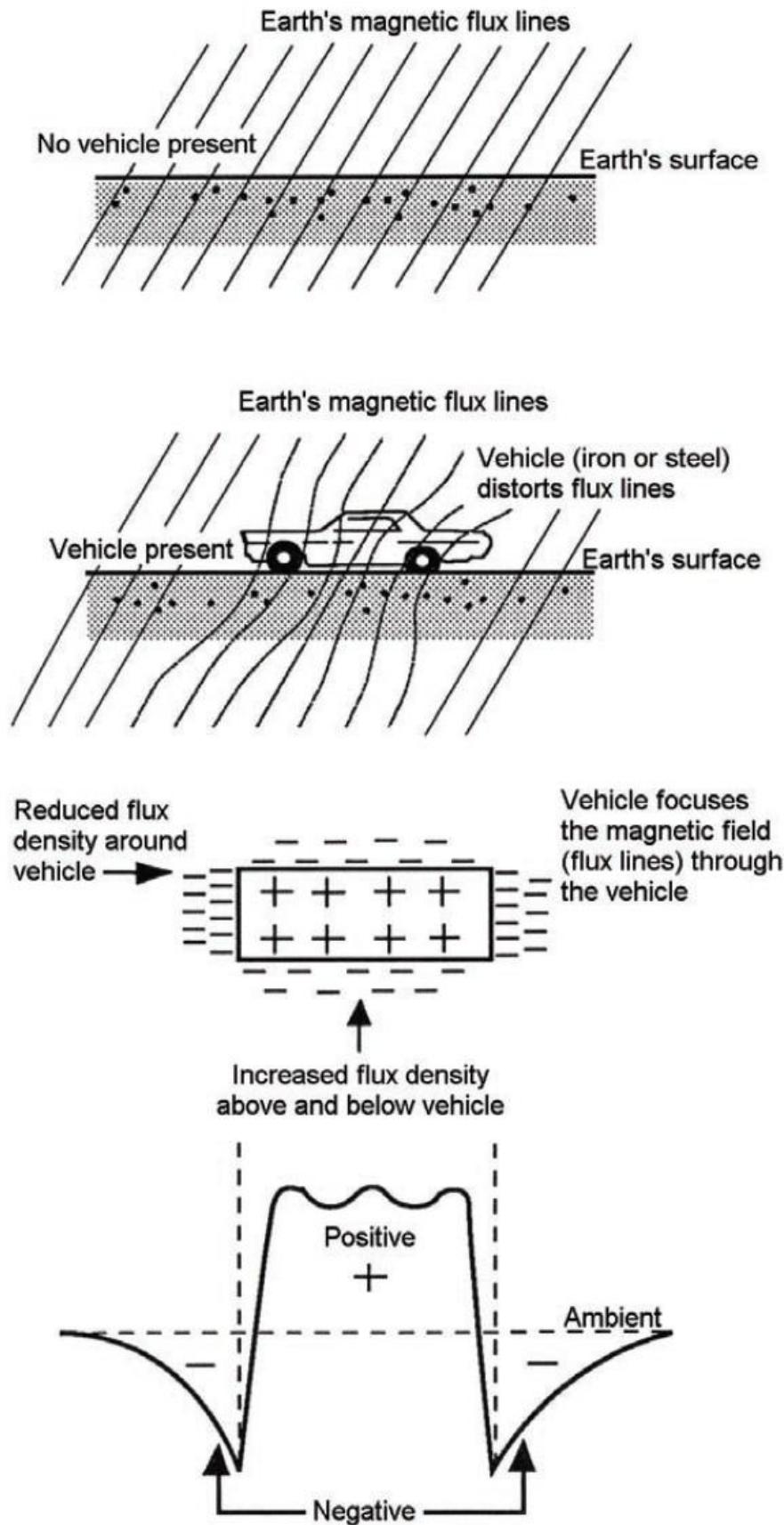


Fig 1.4 Distortion of Earth's quiescent magnetic field by a ferrous metal vehicle

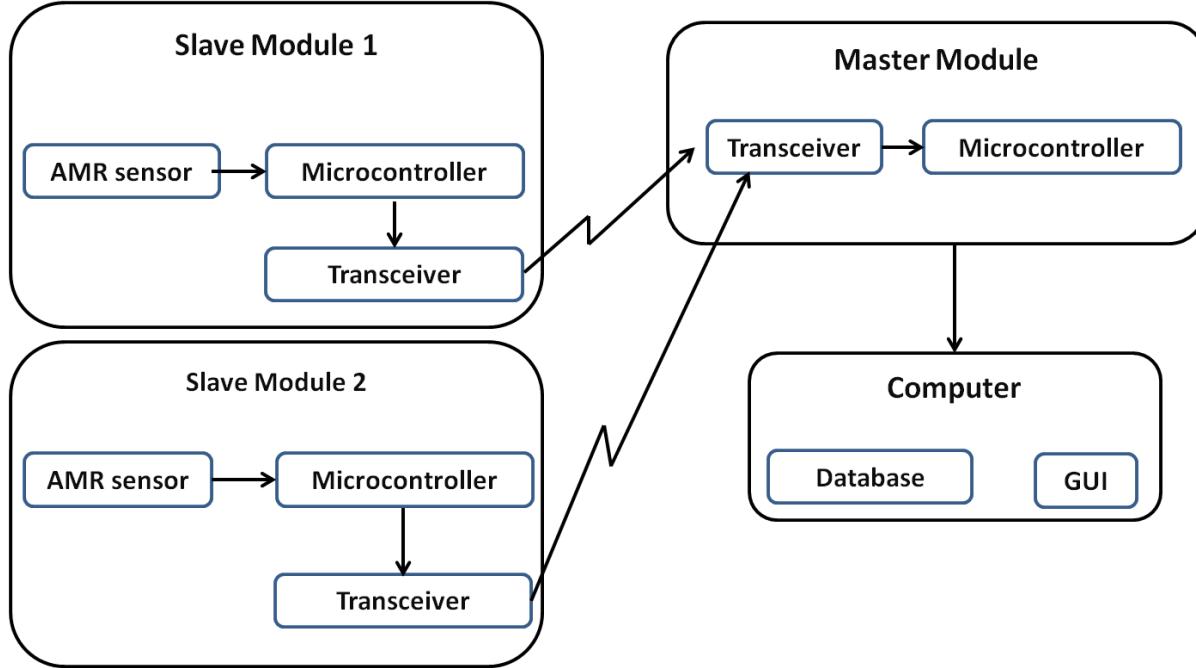


Fig 1.5 Block Diagram of AMR sensor Vehicle Detection System

A flow chart for the functioning of the slave and master modules is shown in Fig 1.6 and 1.7 respectively.

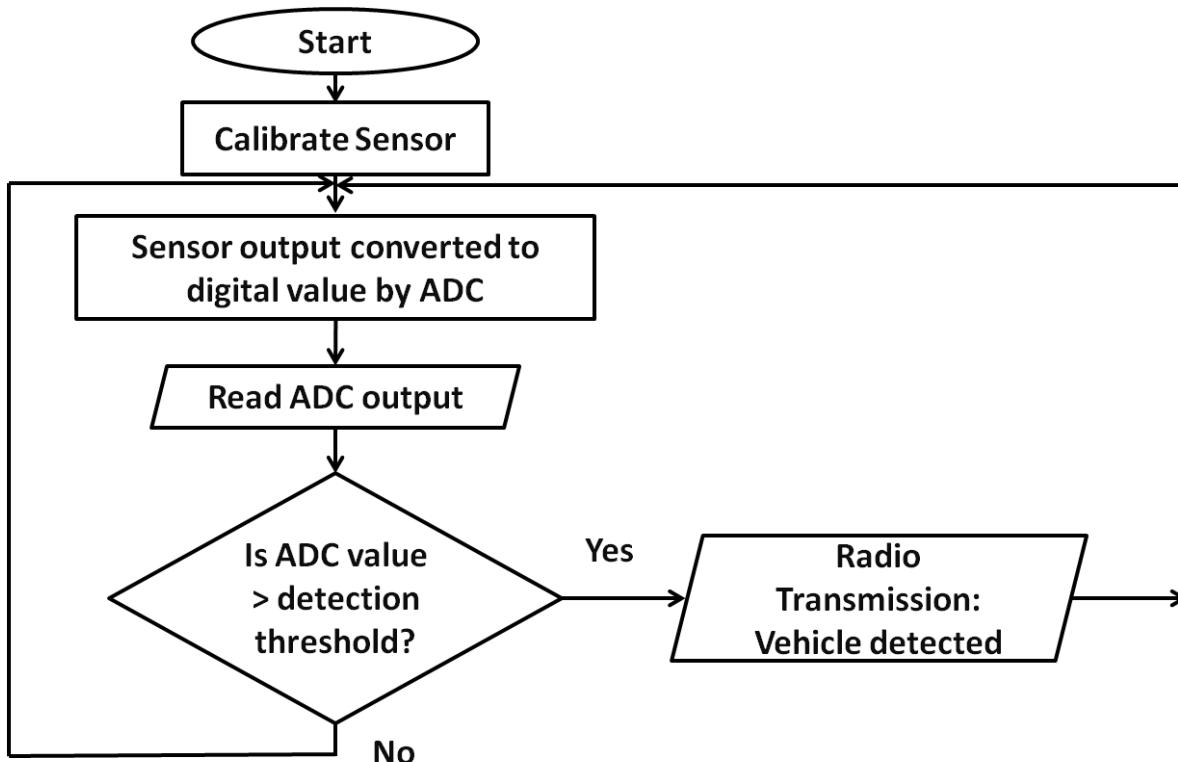


Fig 1.6 Flowchart for Slave Module

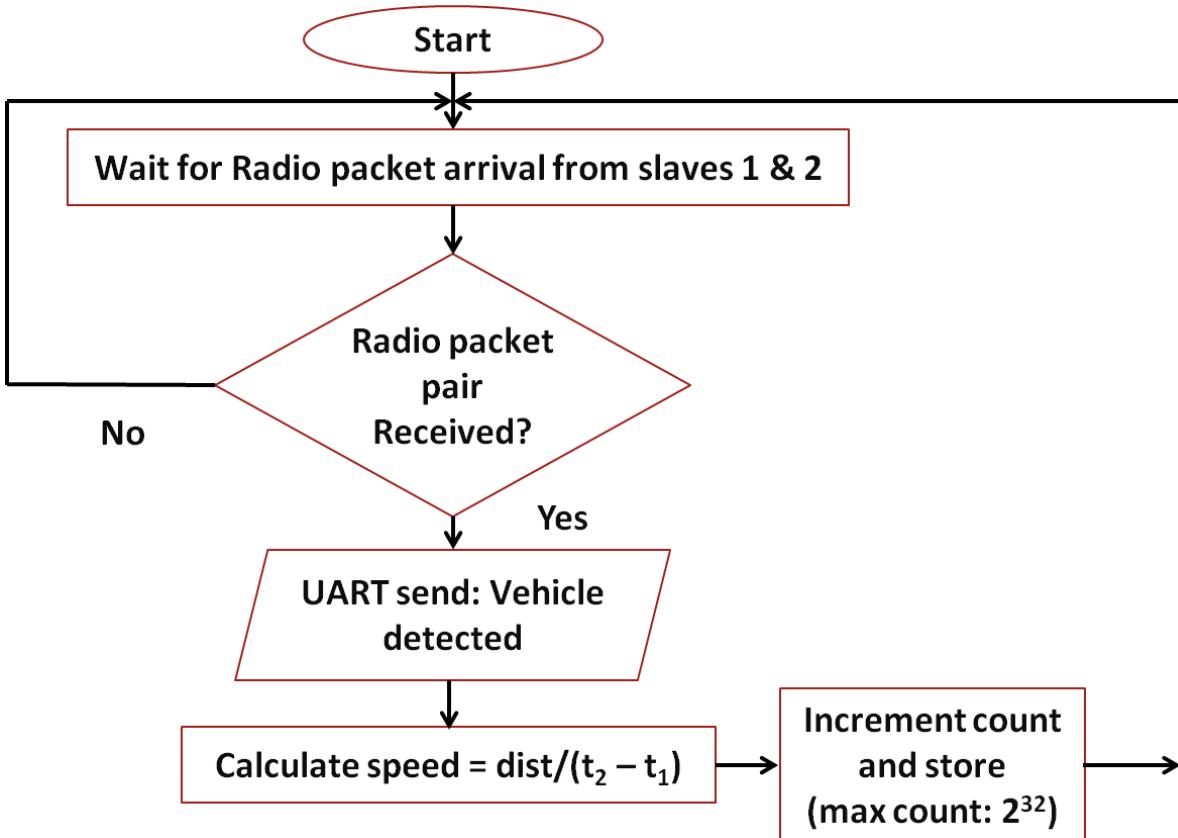


Fig 1.7 Flowchart for Master Module

# DESIGN

## II. DESIGN

### 2.1 General description

This project involves various hardware components such as iSense core, gateway and vehicle detection modules, Inductive loops, Colpitt's oscillator, Jennic and Arduino 2560 microcontrollers. The Eclipse IDE and Arduino software are used to program the Jennic microcontroller and Microsoft Visual Studio is used to develop the GUI. The project uses the concepts of embedded systems, measurements, sensors and wireless communication networks. This chapter highlights the details of each of the above topics.

### 2.2 Hardware requirements

- **Induction loop detection system**
  - i. Induction loop
  - ii. Colpitt's oscillator
  - iii. Comparator
  - iv. Quad Op-Amp IC MC33274
  - v. Microcontroller: Arduino 2560
  - vi. 9V battery
  - vii. Voltage regulators: LM7805 and RT9164A

#### 2.2.1 Inductive loops

Inductive-loop wire, lead-in wires, and lead-in cables typically use #12, #14, or #16 American Wire Gauge (AWG) wire. Here a #12 AWG wire is used. The loop in the roadway also contains an induced resistance (called the ground resistance) caused by transformer coupling between the loop and induced currents flowing in the roadway and sub grade materials.

A roadway inductive loop has a non-uniform flux field that produces an inductance value given by

$$L = \frac{\mu_r \mu_0 N^2 AF'}{l} \dots\dots\dots (2.1)$$

where,

$\mu_r$  = Relative permeability of material (1 for air)

$\mu_0 = 4\pi \times 10^{-7}$  henrys per meter.

$L$  = Inductance, henrys

$N$  = Number of turns

$I$  = Coil current, amperes.

$A$  = Cross sectional area of coil,  $m^2$

$F'$  = a factor to account for the non uniform flux in the roadway inductive loop

### 2.2.2 Colpitt's Oscillator

Oscillators are circuits that generate a continuous voltage output waveform at a required frequency with the values of the inductors, capacitors or resistors forming a frequency selective LC resonant tank circuit and feedback network. The frequency of the oscillatory voltage depends upon the value of the inductance and capacitance in the LC tank circuit. Then the frequency at which this will happen is given as:

$$X_L = 2\pi f L \dots\dots\dots (2.2)$$

$$X_C = \frac{1}{2\pi f C} \dots\dots\dots (2.3)$$

At resonance:  $X_L = X_C$

Equating 2.2 and 2.3,

$$\therefore 2\pi f L = \frac{1}{2\pi f C} \Rightarrow f^2 = \frac{1}{4\pi^2 L C}$$

Therefore the resonance frequency of an LC oscillator is

$$f = \frac{1}{2\pi \sqrt{LC}} \dots\dots\dots (2.4)$$

Where:

$L$  is the Inductance in Henry

$C$  is the Capacitance in Farad

$f_r$  is the Output Frequency in Hertz

Equation 2.4 shows that if either  $L$  or  $C$  is decreased, the frequency increases. This output frequency is commonly given the abbreviation of ( $f_r$ ) to identify it as the “resonant frequency”.

The Colpitt's oscillator of the induction loop detection system utilizes MC33274, a quad op-amp IC and oscillates at a resonant frequency of 50 KHz. The oscillator makes use of an inductive loop of  $100\mu\text{H}$  and effective capacitance of  $0.22\mu\text{F}$ . The output of the oscillator is fed

to a comparator which produces square waves of the same frequency as the oscillations, ready to be fed to the microcontroller.

### **2.2.3 Comparator**

The comparator is also implemented using the Quad op-amp IC MC33274 and operates with a reference voltage of 2.5V. It essentially acts as an A/D convertor and converts the input sine wave into a square wave at the output which is then fed to the microcontroller for frequency measurement.

### **2.2.4 Quad Op-Amp IC MC33274**

The MC33274 is quad operational amplifier that incorporates Bipolar inputs along with a patented Zip-R-Trim element for input offset voltage reduction. The MC33274 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual-doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no dead band crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The features of MC33274 are listed below.

- Input Offset Voltage Trimmed to  $100\mu\text{V}$  (Typical)
- Low Input Bias Current:  $300\text{nA}$
- Low Input Offset Current:  $3.0\text{nA}$
- High Input Resistance:  $16\text{ M}\Omega$
- Low Noise:  $18\text{ nV}/\sqrt{\text{Hz}}$  @  $1.0\text{ kHz}$
- High Gain Bandwidth Product:  $24\text{ MHz}$  @  $100\text{ kHz}$
- High Slew Rate:  $10\text{ V}/\mu\text{s}$
- Power Bandwidth:  $160\text{ kHz}$
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to  $500\text{ pF}$
- Large Output Voltage Swing:  $+14.1\text{ V}/-14.6\text{ V}$
- Low Total Harmonic Distortion:  $0.003\%$
- Power Supply Drain Current:  $2.15\text{ mA}$  per Amplifier

- Single or Split Supply Operation: +3.0 V to +36 V or  $\pm 1.5$  V to  $\pm 18$  V

The pin diagram of MC33274 is as shown in Fig 2.1

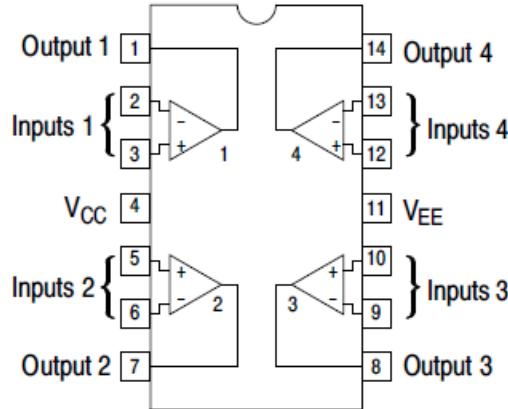


Fig 2.1 Pin diagram of MC33274 (top view)

### 2.2.5 Microcontroller: Arduino 2560

The Arduino board uses a High Performance, Low Power Atmel® AVR® 8-Bit Microcontroller. The ATmega 2560 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. Some of the peripheral features of the Arduino include two 8-bit Timer/Counters with separate Prescaler and Compare Mode.

The microcontroller board is suitable for wide temperature ranges varying from -40°C to 85°C.

It also includes properties of Ultra-Low Power Consumption with two different modes of operation:

- Active Mode: 1MHz, 1.8V: 500 $\mu$ A
- Power-down Mode: 0.1 $\mu$ A at 1.8V

It also has High Endurance Non-volatile Memory Segments

- 256KBytes of In-System Self-Programmable Flash
- 4Kbytes EEPROM
- 8Kbytes Internal SRAM
- Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
- Data retention: 20 years at 85°C/ 100 years at 25°C

This microcontroller is programmed to calculate the frequency of the signal fed at one of its I/O pins. The deviation of frequency from the central frequency of the oscillator determines that a vehicle is present in the inductive loop. This helps in vehicle detection.

The block diagram of ATmega 2560 is shown in Fig 2.2.

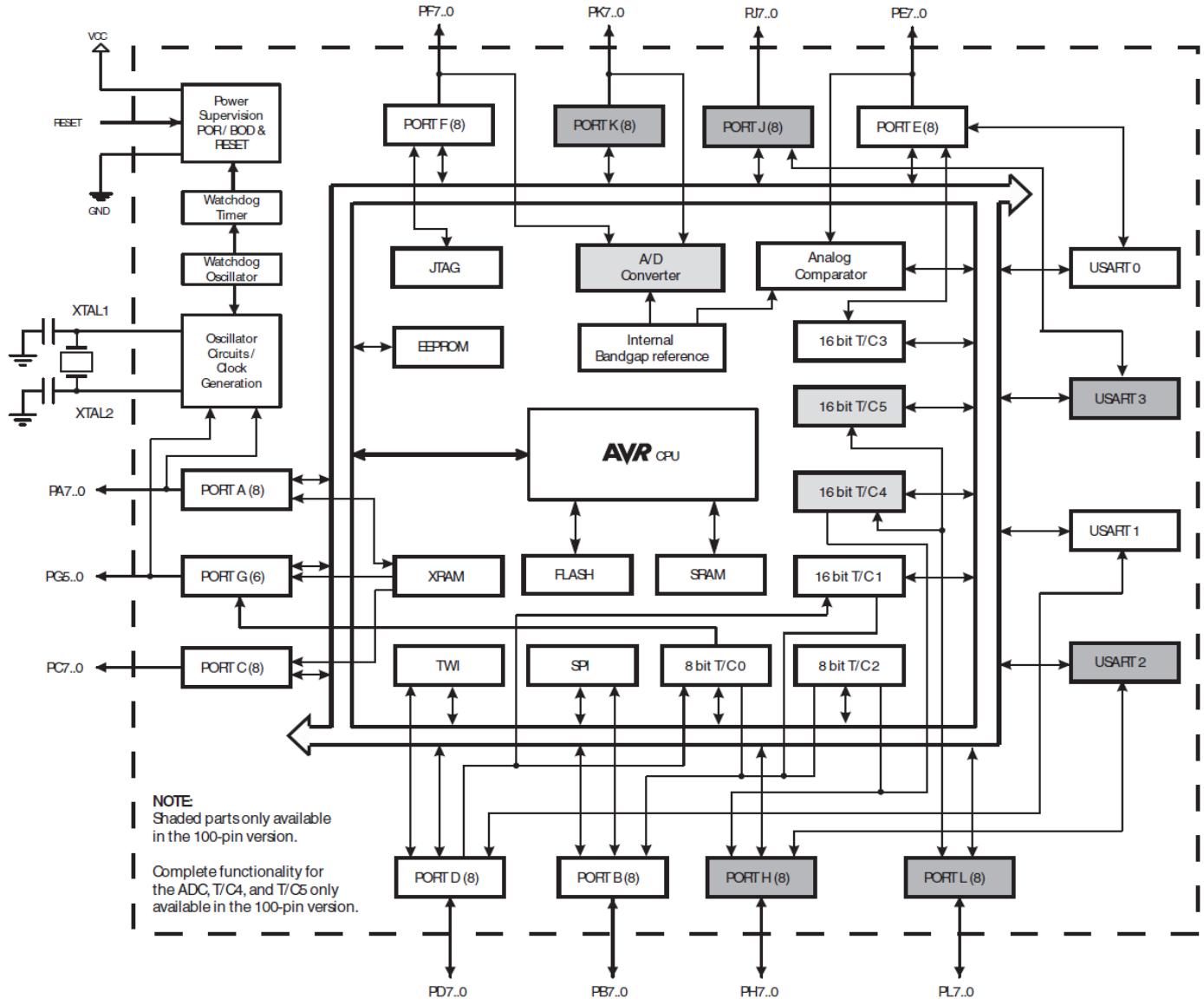


Fig 2.2 Block diagram of ATmega 2560

## 2.2.5 Voltage regulators: LM7805 and RT9164A

### 2.2.5.1 LM7805

The LM7805 is a three-terminal positive 5V regulator. This regulator can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. It employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, it can deliver over 1A output current. Although designed primarily as a fixed voltage regulator, it can be used with external components to obtain adjustable voltage and currents.

Fig 2.3 shows the pin configuration of LM7805.

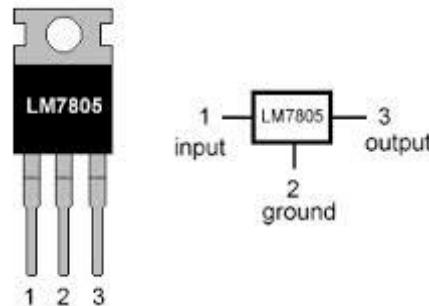


Fig 2.3 Pin configuration of LM7805

Here LM7805 is used to obtain a fixed 5V supply that is connected to the  $V_{cc}$  pin of op-amp MC33274.

The block diagram of LM7805 is shown in Fig 2.4

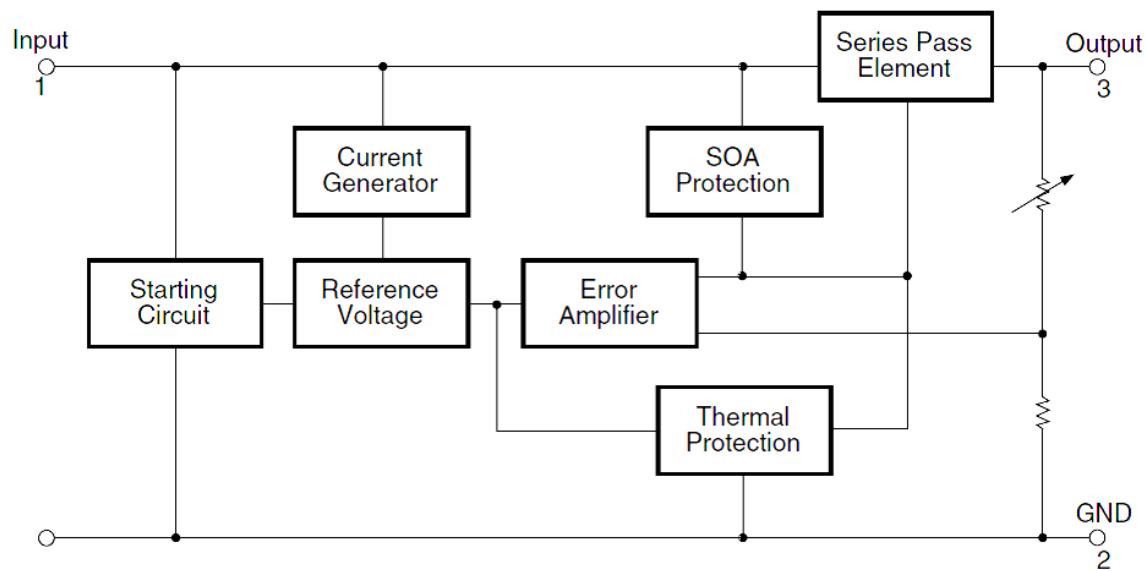


Fig 2.4 Block diagram of LM7805

### 2.2.5.1 RT9164A

The RT9164A is a high performance positive voltage regulators designed for applications requiring low dropout performance at fully rated current. Additionally, the RT9164A provides excellent regulation over variations in line and load. Outstanding features include low dropout performance at rated current, fast transient response, internal current-limiting and thermal-shutdown protection of the output device.

The pin configuration of RT9164A is shown in Fig 2.5

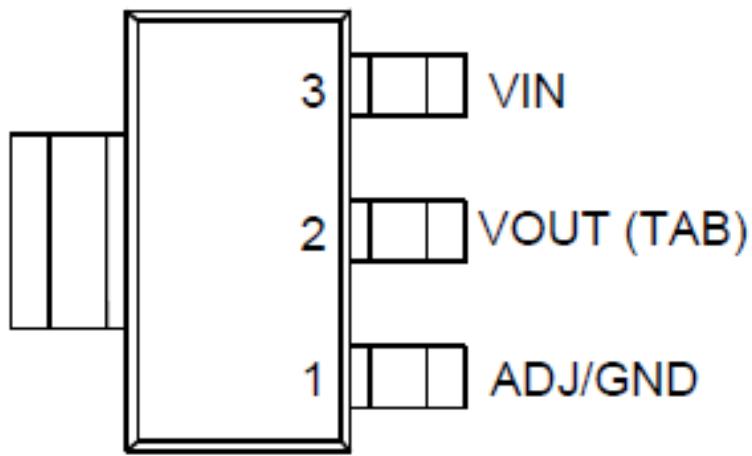


Fig 2.5 Pin configuration of RT9164A

#### Features of RT9164A:

- i. Low Dropout Performance, 1.4V Max
- ii. Full Current Rating Over Line and Temperature
- iii. Fast Transient Response
- iv.  $\pm 2\%$  Output Voltage Accuracy
- v. 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, and 3.5V Fixed
- vi. Adjustable Output Voltage

The functional block diagram of RT9164A is as shown in Fig 2.6

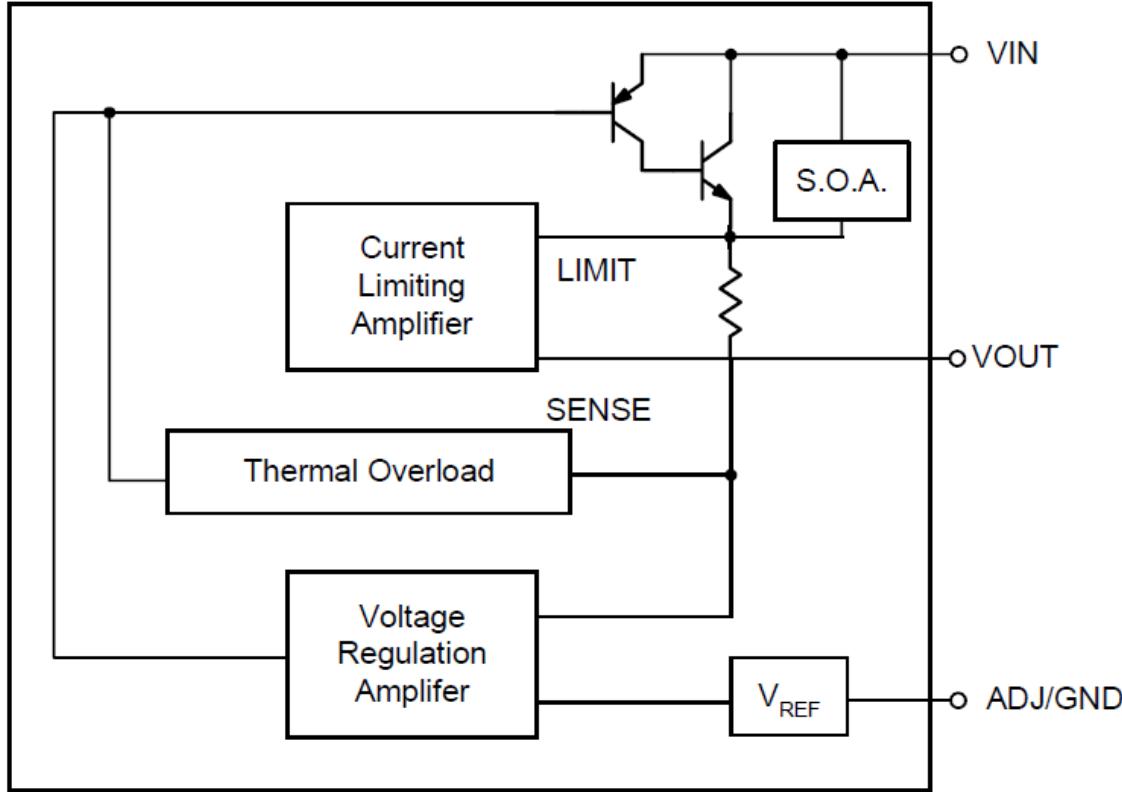


Fig 2.6 Functional block diagram of RT9164A

- **AMR sensor vehicle detection system**
  - i. Anisotropic Magneto Resistive sensors
  - ii. Microcontroller with transceiver: Jennic JN5148-001
  - iii. 1.5V batteries

### 2.2.6 Anisotropic Magneto Resistive sensors: KMZ52

The KMZ52 is an extremely sensitive magnetic field sensor, employing the magneto-resistive effect of thin-film Permalloy. The sensor contains two magneto-resistive Wheatstone bridges physically offset from one another by 90° and integrated compensation and set/reset coils. The integrated compensation coils allow magnetic field measurement with current feedback loops to generate outputs that are independent of drift in sensitivity. The orientation of sensitivity may be set or changed (flipped) by means of the integrated set/reset coils. A short current pulse should be applied to the compensation coils to recover (set) the sensor after exposure to strong disturbing magnetic fields. A negative current pulse will reset the sensor to

reversed sensitivity. By use of periodically alternated flipping pulses and a lock-in amplifier, the output is made independent of sensor and amplifier offset.

The features of KMZ52 are listed below.

- High sensitivity
- Integrated compensation coil
- Integrated set/reset coil.

The simplified circuit diagram of KMZ52 is as shown in Fig 2.7

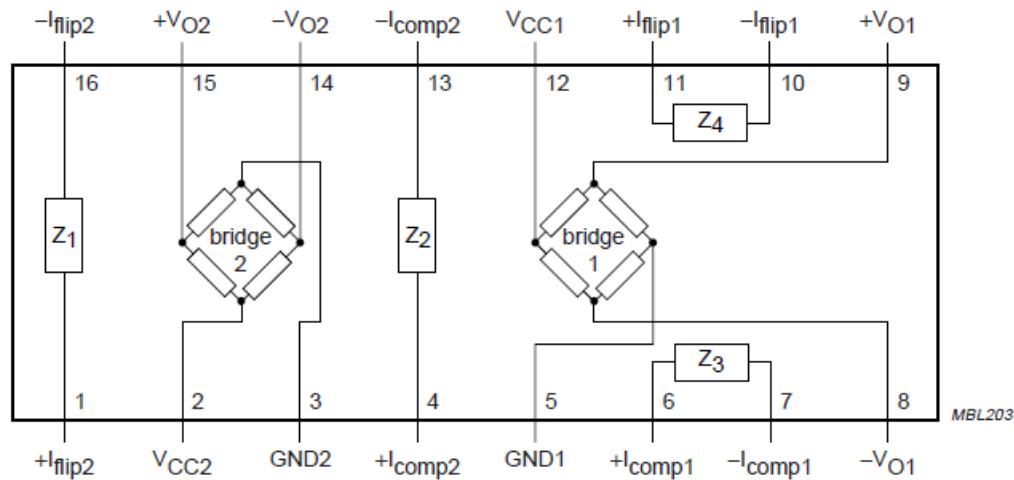


Fig 2.7 Simplified circuit diagram of KMZ52

### 2.2.7 Microcontroller with transceiver: Jennic JN5148-001

The JN5148-001 is an IEEE802.15.4 wireless microcontroller that provides a fully integrated solution for applications using the IEEE802.15.4 standard in the 2.4 - 2.5GHz ISM frequency band [1], including JenNet and ZigBee PRO. It includes all of the functionality required to meet the IEEE802.15.4, JenNet and ZigBee PRO specifications and has additional processor capability to run a wide range of applications including, but not limited to Smart Energy, Automatic Meter Reading, Remote Control, Home and Building Automation, Toys and Gaming.

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the

wireless network in addition to the product functionality and user interfaces. To minimise this complexity, NXP provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN5148. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

A simple block diagram of JN5148-001 is as shown in Fig 2.8

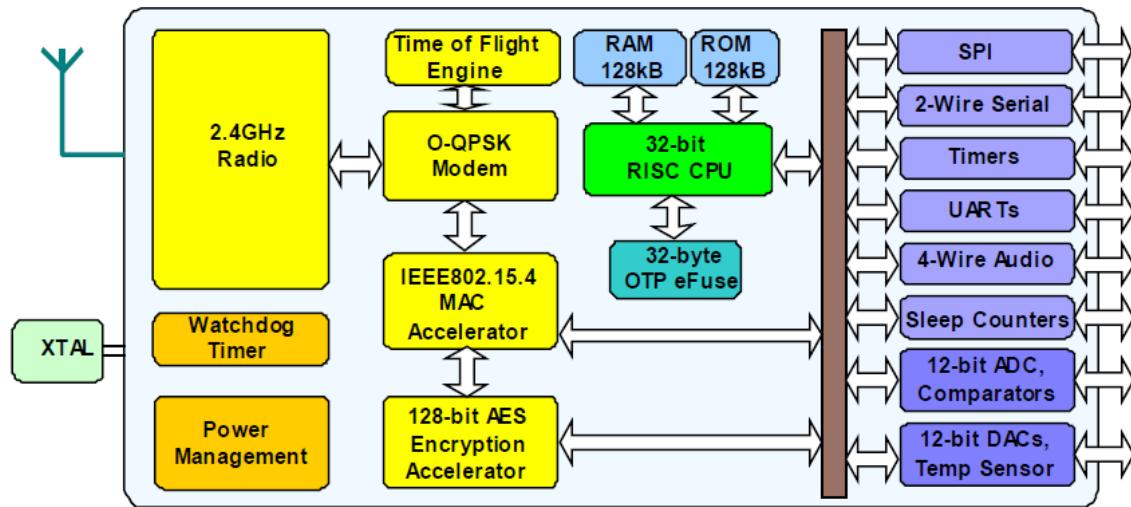


Fig 2.8 Block diagram of JN5148-001

The device includes a Wireless Transceiver, RISC CPU, on chip memory and an extensive range of peripherals.

### 2.2.7.1 Wireless Transceiver

The Wireless Transceiver comprises of

- 2.45GHz radio
- A modem
- A baseband controller

In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realized very easily.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 Media Access Control (MAC) under the control of a protocol stack. Applications

incorporating IEEE802.15.4 functionality can be rapidly developed by combining user-developed application software with a protocol stack library.

**Features: Transceiver**

- 2.4GHz IEEE802.15.4 compliant
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- 500 & 667kbps data rate modes
- Integrated sleep oscillator for low power
- On chip power regulation for 2.0V to 3.6V battery operation
- Deep sleep current 100nA
- Sleep current with active sleep timer 1.25µA
- Rx current 17.5mA
- Tx current 15.0mA
- Receiver sensitivity -95dBm
- Transmit power 2.5dBm

**Radio**

Fig 2.9 shows the single ended radio architecture.

The radio comprises a low-IF receive path and a direct modulation transmit path, which converge at the TX/RX switch. The switch connects to the external single ended matching network, which consists of two inductors and a capacitor, this arrangement creates a  $50\Omega$  port and removes the need for a balun. A  $50\Omega$  single ended antenna can be connected directly to this port.

The 32MHz crystal oscillator feeds a divider, which provides the frequency synthesizer with a reference frequency. The synthesizer contains programmable feedback dividers, phase detector, charge pump and internal Voltage Controlled Oscillator (VCO). The VCO has no external components, and includes calibration circuitry to compensate for differences in internal component values due to process and temperature variations. The VCO is controlled by a Phase Locked Loop (PLL) that has an internal loop filter. A programmable charge pump is also used to tune the loop characteristic.

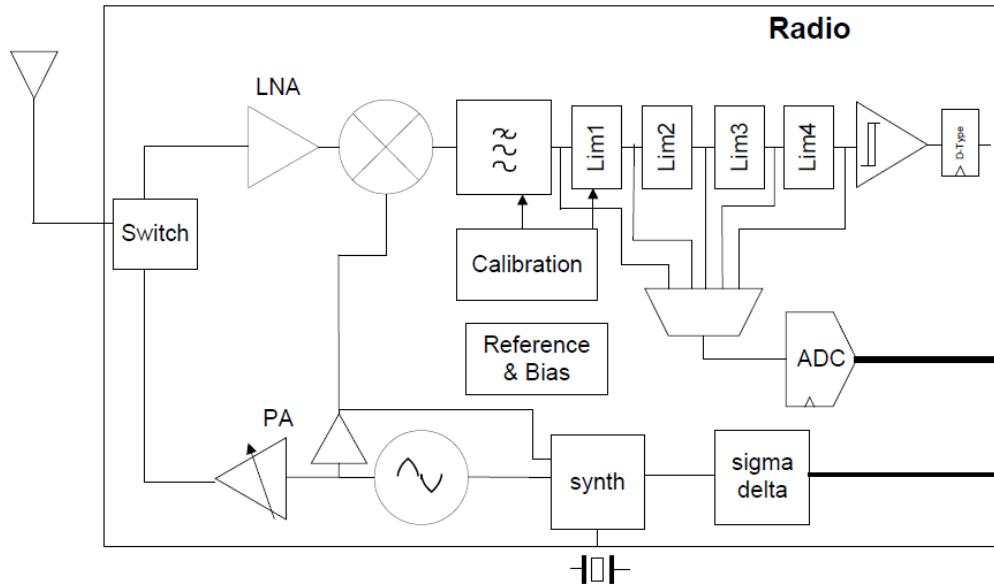


Fig 2.9 Radio Architecture

The receiver chain starts with the low noise amplifier / mixer combination whose outputs are passed to a lowpass filter, which provides the channel definition. The signal is then passed to a series of amplifier blocks forming a limiting strip. The signal is converted to a digital signal before being passed to the Modem. The gain control for the RX path is derived in the automatic gain control (AGC) block within the Modem, which samples the signal level at various points down the RX chain. To improve the performance and reduce current consumption, automatic calibration is applied to various blocks in the RX path.

In the transmit direction, the digital stream from the Modem is passed to a digital sigma-delta modulator which controls the feedback dividers in the synthesizer, (dual point modulation). The VCO frequency now tracks the applied modulation. The 2.4 GHz signal from the VCO is then passed to the RF Power Amplifier (PA), whose power control can be selected from one of three settings. The output of the PA drives the antenna via the RX/TX switch.

### Modem

The modem performs all the necessary modulation and spreading functions required for digital transmission and reception of data at 250kbps in the 2450MHz radio frequency band in compliance with the IEEE802.15.4 standard. It also provides high data rate modes at 500 and 667kbps. The architecture of the modem is as shown in Fig 2.10

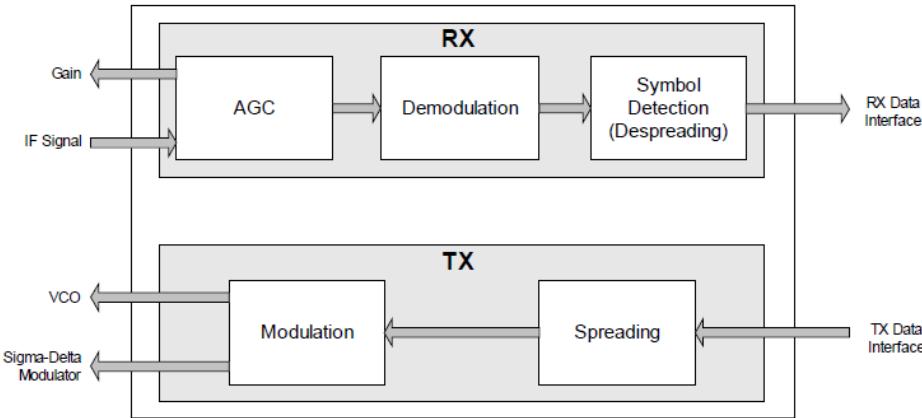


Fig 2.10 Modem Architecture

### Baseband Controller

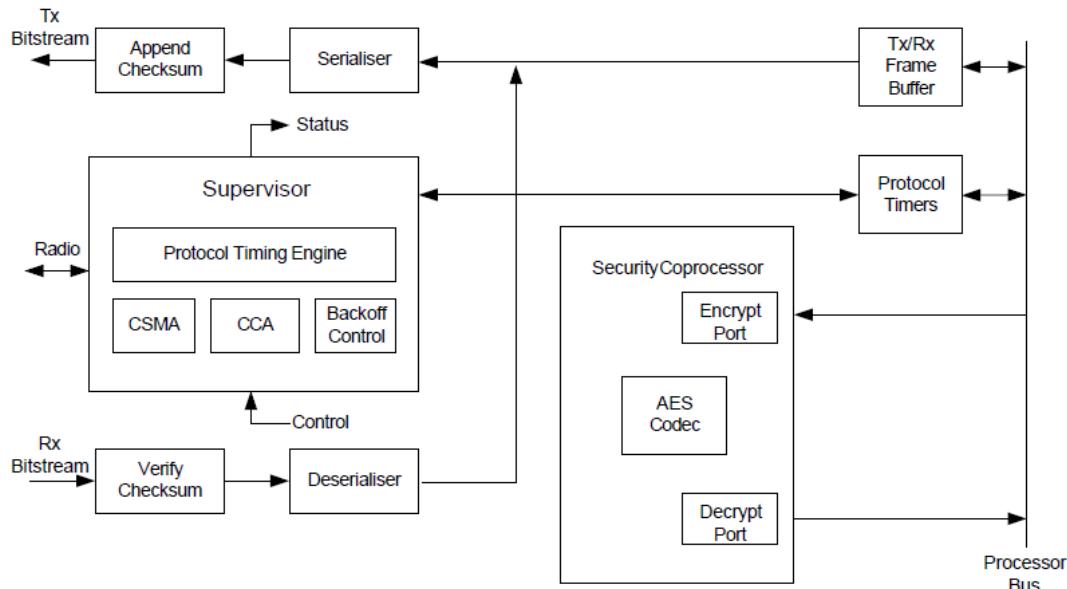


Fig 2.11 Baseband Controller

The baseband processor provides all time-critical functions of the IEEE802.15.4 MAC layer. Dedicated hardware guarantees air interface timing is precise. The MAC layer hardware/software partitioning, enables software to implement the sequencing of events required by the protocol and to schedule timed events with millisecond resolution, and the hardware to implement specific events with microsecond timing resolution. The protocol software layer performs the higher-layer aspects of the protocol, sending management and data messages between endpoint and coordinator nodes, using the services provided by the baseband processor. Fig 2.11 shows the block diagram of the baseband controller.

### 2.2.7.2 RISC CPU, On chip memory and Peripherals (Microcontroller)

A 32-bit RISC CPU allows software to be run on chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN5148 has a unified memory architecture, code memory, data memory, peripheral devices and I/O ports are organized within the same linear address space. The device contains 128kbytes of ROM, 128kbytes of RAM and a 32-byte One Time Programmable (OTP) eFuse memory.

#### Features: Microcontroller

- Low power 32-bit RISC CPU, 4 to 32MHz clock speed
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- 128kB ROM and 128kB RAM for bootloaded program code & data
- 4-input 12-bit ADC, 2 12-bit DACs, 2 comparators
- 3 application timer/counters,
- 2 UARTs
- SPI port with 5 selects
- 2-wire serial interface
- Watchdog timer
- Low power pulse counters
- Up to 21 DIO

The detailed block diagram of JN5148 is as shown in Fig 2.12

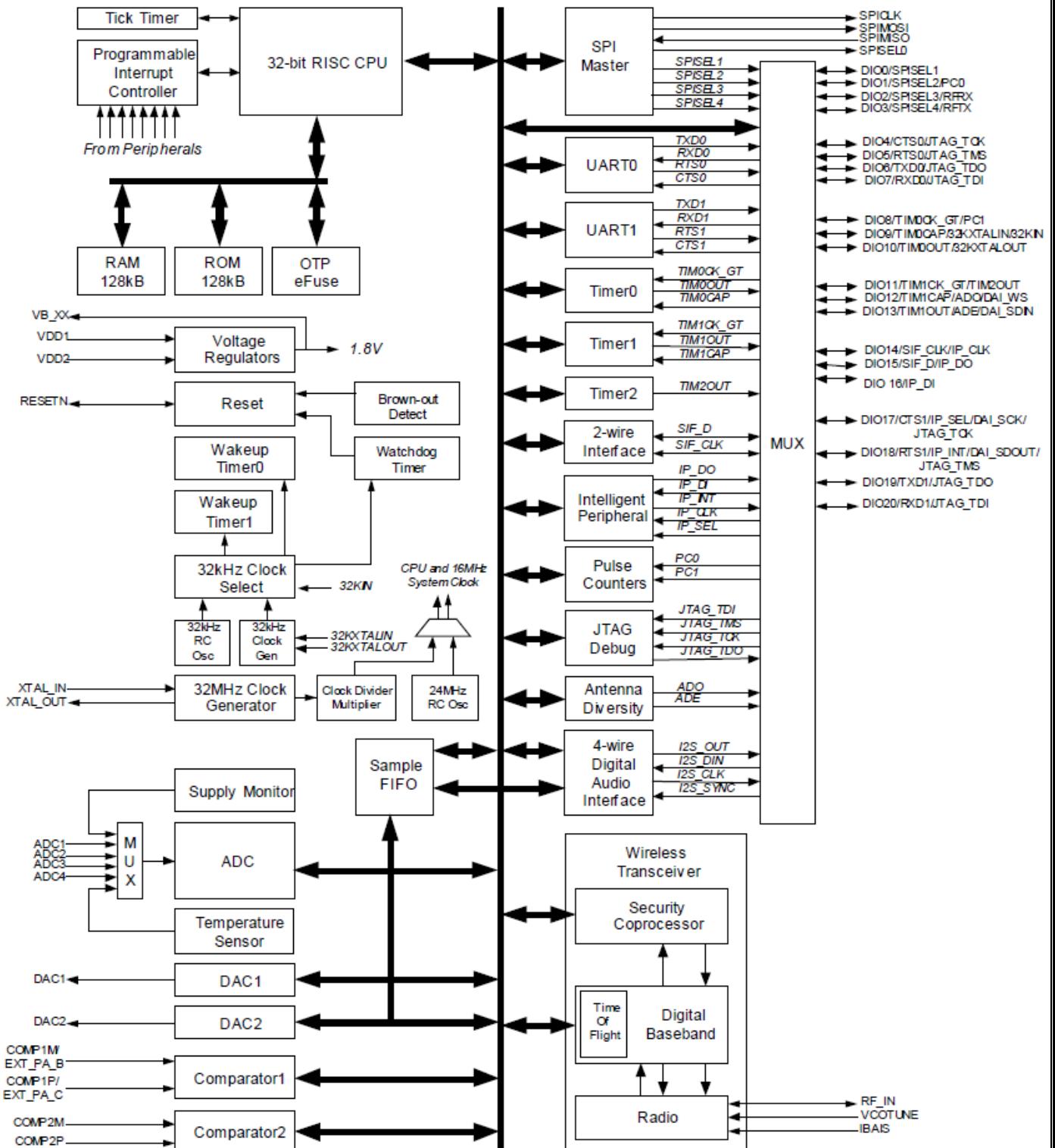


Fig 2.12 JN5148 Block Diagram

## 2.3 Software requirements

- i. LTspice IV
- ii. Arduino IDE
- iii. Cygwin
- iv. iSense API
- v. iShell
- vi. Eclipse Indigo (C++)
- vii. Microsoft visual studio 12.0

### 2.3.1 LTspice IV

LTspice IV is freeware computer software implementing a SPICE simulator of electronic circuits, produced by semiconductor manufacturer Linear Technology (LTC). LTspice was originally called SwitcherCAD and is sometimes still called by that name. The software is maintained by Mike Engelhardt. The application is written for Microsoft Windows but, since 2003,[5] it will run under the WINE Windows simulator under Linux. Since 2013 there is also a native OS X version available. From version IV LTspice requires at least a Pentium 4 processor and Windows 2000 or later.

LTspice provides a schematic capture and waveform viewer with enhancements and models to speed the simulation of switching regulators. Supplied with LTspice IV are macro models for 80% of LTC's switching regulators and operational amplifiers, transistors, MOSFETs, and passive components.

It is node-unlimited and 3rd party models can be imported. Circuit simulations based on transient, AC, noise and DC analysis can be plotted as well as Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated. It is a popular simulation software in fields including radio frequency electronics, power electronics, digital electronics, and other disciplines. LTspice IV does not generate printed circuit board (PCB) layouts, but netlists can be imported into layout programs.

The great advantage of LTspice over other Spice-based tools available is that it is free and its capabilities are unrestricted. This means that the size of the circuits and the hierarchy levels are limited only by the resources of the computer. Also, a circuit described by its Spice deck can be simulated without worrying about the number of nodes present in the circuit.

In LTspice it is easy to import sub-circuits like an Op-Amp macro model and other circuits not included in the default LTspice library.

### 2.3.1.1 Simulating circuits using LTspice IV

#### ➤ Opening a new circuit file

- On opening LTspice IV the home screen appears as shown in Fig 2.13

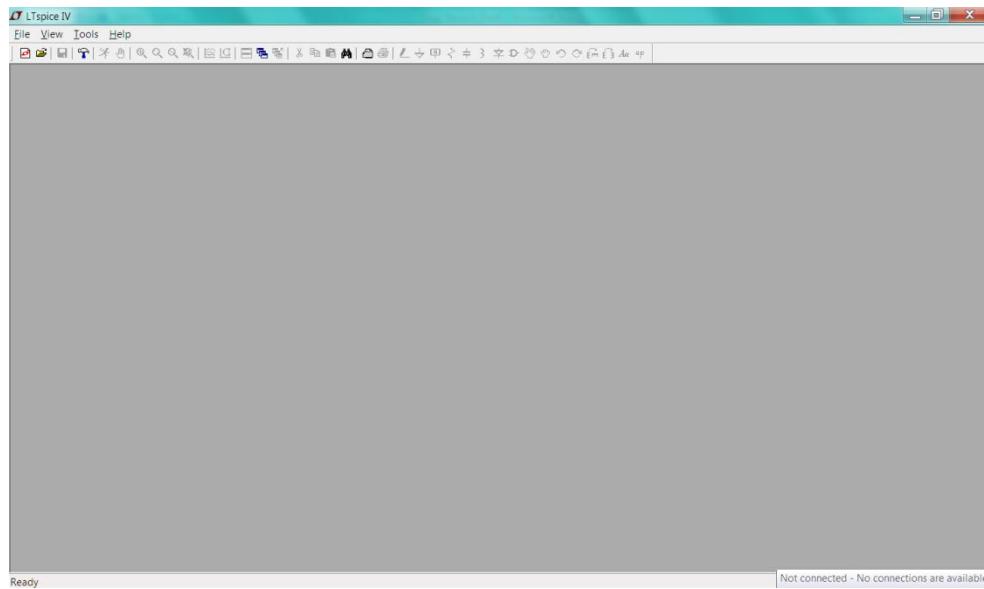


Fig 2.13 Home screen of LTspice IV

- A new circuit file can be created from the file menu, or by clicking the "New Schematic" icon.  
Now a draft screen as shown in Fig 2.14 appears

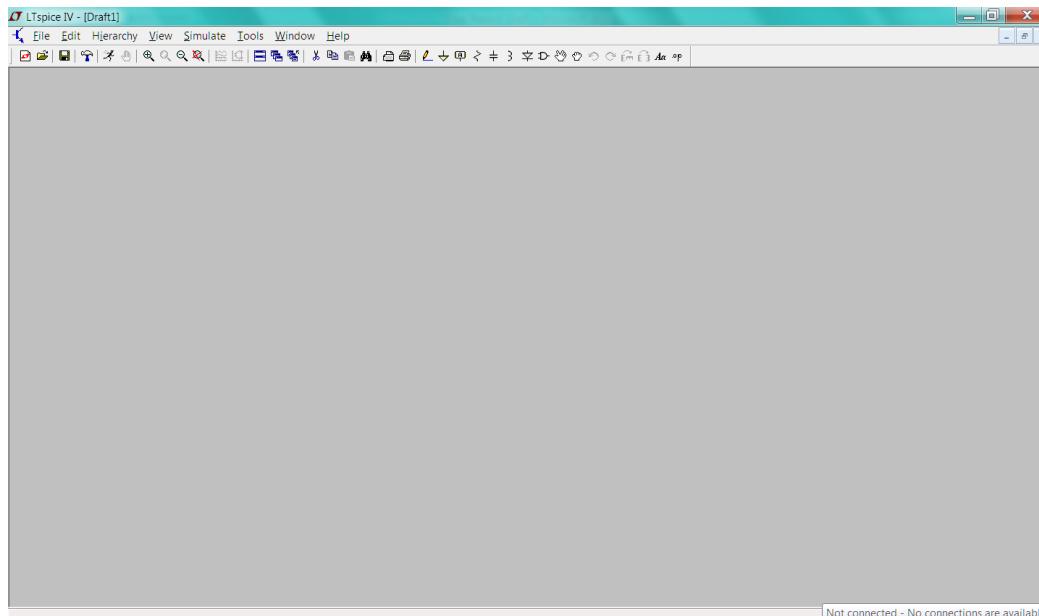


Fig 2.14 Blank draft screen on LTspice IV

➤ **Drawing the circuit:**

- Adding a GND: This is very important. No circuit simulation can be carried out if the circuit does not have a ground. A ground can be placed using one of the following methods.
  - pressing the 'g' key
  - using the ground icon
  - selecting 'ground' from the 'Edit' menu
- Getting the other components: The other components can be added by,
  - clicking on the icon for a specific component
  - clicking on the 'component' button
  - pressing "F2"
  - selecting "Component..." from the "Edit" menu

Once the component dialog box as shown in Fig 2.15 is open, any part that is needed in the circuit can be selected.

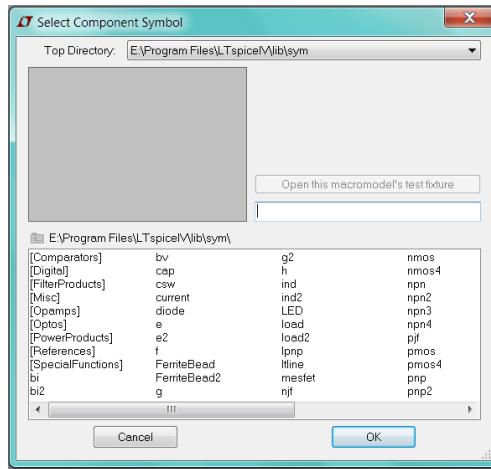


Fig 2.15 Component dialog box in LTspice IV

- **Connecting the Circuit:** All the components can now be connected using one of the following methods.
- clicking the "Draw Wire" button from the tool bar
  - pressing F3"
  - Selecting "Draw Wire" from the "Edit" menu.

## ➤ Simulation

The following checks must be carried out before simulating the circuit.

- Circuit is properly drawn and saved.
  - There must be no floating parts on the circuit (i.e. unattached devices).
  - All parts have the correct values.
  - There are no extra wires.
  - A ground is present in the circuit.
- 
- Choosing a simulation: On choosing “Edit simulation Cmd” from the Simulate menu (Fig 2.16), the Edit Simulation Command window appears as shown in Fig 2.17

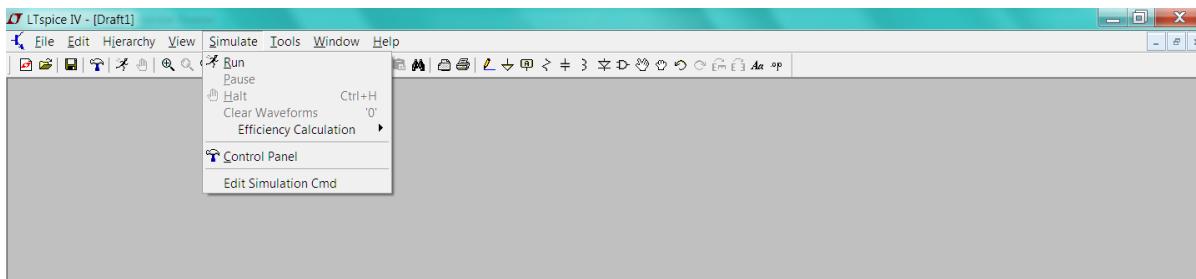


Fig 2.16 Choosing “Edit simulation Cmd” from the Simulate menu

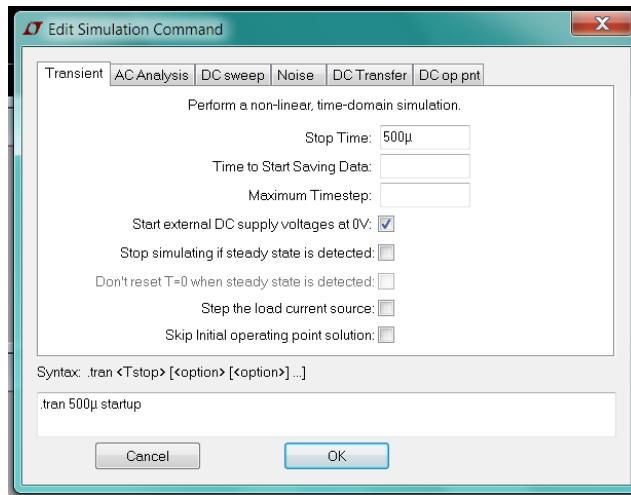


Fig 2.17 Edit simulation command window

The simulation can be run by enabling the type of analysis required and clicking the Simulate button on the tool bar or using the "Simulate/Run" command.

### 2.3.2 Arduino IDE

The Arduino integrated development environment (IDE) is a cross-platform application written in Java, and is derived from the IDE for the Processing programming language and the Wiring projects. It is designed to introduce programming to artists and other newcomers unfamiliar with software development. It includes a code editor with features such as syntax highlighting, brace matching, and automatic indentation, and is also capable of compiling and uploading programs to the board with a single click. A program or code written for Arduino is called a "sketch".

Arduino programs are written in C or C++. The Arduino IDE comes with a software library called "Wiring" from the original Wiring project, which makes many common input/output operations much easier. Users only need define two functions to make a runnable cyclic executive program:

`setup()`: a function run once at the start of a program that can initialize settings

`loop()`: a function called repeatedly until the board powers off.

#### 2.3.2.1 Using the Arduino integrated development environment (IDE) to program ATmega 2560

- The Arduino Mega will automatically draw power from either the USB connection to the computer or an external power supply.
- When powered up, the green power LED (labelled PWR) glows.
- On launching the Arduino IDE the following screen appears (Fig 2.18)

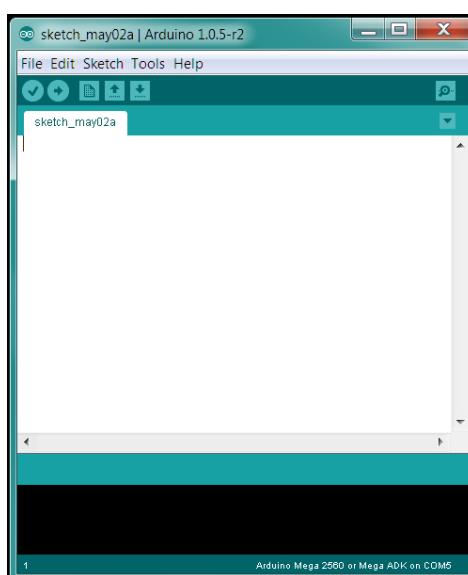
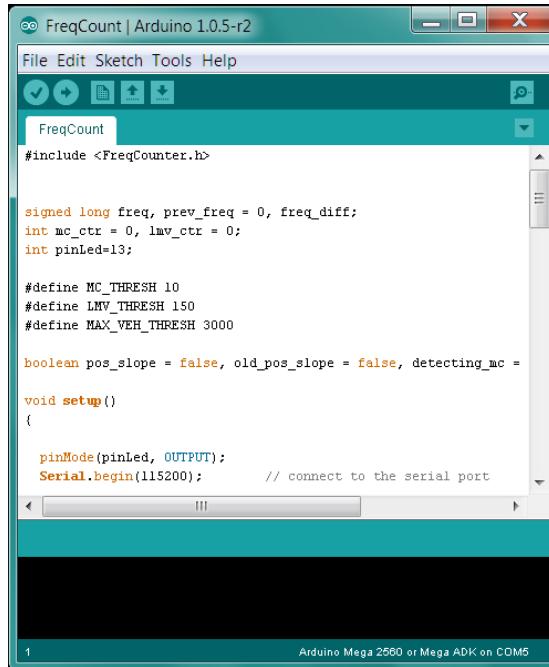


Fig 2.18 Arduino IDE

- A new sketch can now be opened by clicking “New” or an existing sketch can be opened by selecting “Open” from the “File” menu.

Fig 2.19 shows an opened sketch.



The screenshot shows the Arduino IDE interface with the title bar "FreqCount | Arduino 1.0.5-r2". The menu bar includes File, Edit, Sketch, Tools, and Help. The main window displays the code for a sketch named "FreqCount". The code includes #include <FreqCounter.h>, defines MC\_THRESH, LMV\_THRESH, and MAX\_VEH\_THRESH, initializes variables freq, prev\_freq, mc\_ctr, lmv\_ctr, and pinLed, sets up pins, and begins serial communication at 115200. The status bar at the bottom indicates "Arduino Mega 2560 or Mega ADK on COM5".

```

#include <FreqCounter.h>

signed long freq, prev_freq = 0, freq_diff;
int mc_ctr = 0, lmv_ctr = 0;
int pinLed=13;

#define MC_THRESH 10
#define LMV_THRESH 150
#define MAX_VEH_THRESH 3000

boolean pos_slope = false, old_pos_slope = false, detecting_mc =
void setup()
{
    pinMode(pinLed, OUTPUT);
    Serial.begin(115200); // connect to the serial port
}

```

Fig 2.19 A sketch on the Arduino IDE

- Next the correct board is selected from “Board menu” under Tools as shown in Fig 2.20

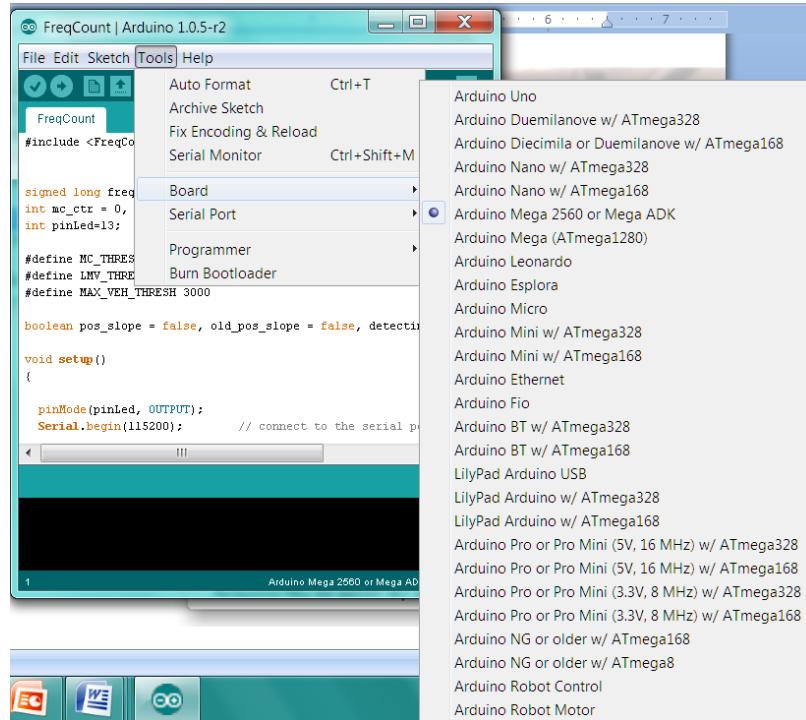


Fig 2.20 Selecting the correct board

- The correct serial port is now selected from the “Serial Port menu” under “Tools” menu.
- The program is then uploaded by clicking the "Upload" button in the environment.

The RX and TX LEDs on the board flash indicating that the program is being flashed on the microcontroller. If the upload is successful, the message "Done uploading." appears in the status bar.

### 2.3.3 Cygwin

Cygwin is a Unix-like environment and command-line interface for Microsoft Windows. Cygwin provides native integration of Windows-based applications, data, and other system resources with applications, software tools, and data of the Unix-like environment. Thus it is possible to launch Windows applications from the Cygwin environment, as well as to use Cygwin tools and applications within the Windows operating context.

Cygwin consists of two parts: a dynamic-link library (DLL) as an API compatibility layer providing a substantial part of the POSIX API functionality, and an extensive collection of software tools and applications that provide a Unix-like look and feel.

Cygwin was originally developed by Cygnus Solutions, which was later acquired by Red Hat. It is free and open source software, released under the GNU General Public License version 3. Today it is maintained by employees of Red Hat, NetApp and many other volunteers.

#### 2.3.3.1 Description

Cygwin consists of a library that implements the POSIX system call API in terms of Win32 system calls, a GNU development tool chain (including GCC and GDB) to allow software development, and a large number of application programs equivalent to those on Unix systems. Programmers have ported many Unix, GNU, BSD and Linux programs and packages to Cygwin, including the X Window System, K Desktop Environment 3, GNOME,[3] Apache, and TeX. Cygwin permits installing inetd, syslogd, sshd, Apache, and other daemons as standard Windows services, allowing Microsoft Windows systems to emulate Unix and Linux servers.

Cygwin programs are installed by running Cygwin's "setup" program, which downloads the necessary program and feature package files from repositories on the Internet. Setup can install, update, and remove programs and their source code packages. A complete installation will take

in excess of 17 GB of hard disk space, but usable configurations may require as little as 1 or 2 GB.

### 2.3.5 iShell

The iShell programming, operating and analysis tool is the personal computer counterpart of the iSense operating and networking firmware. Besides a broad variety of functions for operating iSense wireless sensor networks that is already included, iShell can easily be extended through adding user Plugins. iShell offers its functionality to the user in a number of different views that group activities on separate tabulator windows.

First of all iShell can be used for both wired and wireless programming of the iSense devices. Besides, the serial monitor view provides a text window for displaying messages transmitted from a connected device via a serial or USB connection. Other views for example

- send messages to the network via an attached sensor node,
- plot graphs of measured data captured in the network e.g. by the vehicle detection sensor or the accelerometer
- provide data export to Microsoft Excel
- display camera pictures captured by wireless sensors

#### ➤ Steps to program the core and vehicle detection modules using iShell:

- The first step is to connect the iSense device to the PC. It must at least consist of an iSense Core Module and an iSense Gateway Module connected to the PC via a USB cable.
- On opening iShell the following window appears (Fig 2.21)
- The port to which the device is connected to is selected by clicking the “Serial” option from the “Preferences” menu and selecting the proper COM port from the drop down list as shown in Fig 2.22
- If the connection was successful, the logging pane at the bottom of the iShell window displays “New connection to Jennic device on COMX” as shown in Fig 2.23
- While the “Serial Monitor” plugin and the “Flash Loader” plugin are always active and cannot be closed, all other Plugins can be opened and closed on the “Plugins” tab. Plugins such as “Curve-Illustrator”, “Over the air programming” can be activated in this tab as shown in Fig 2.24

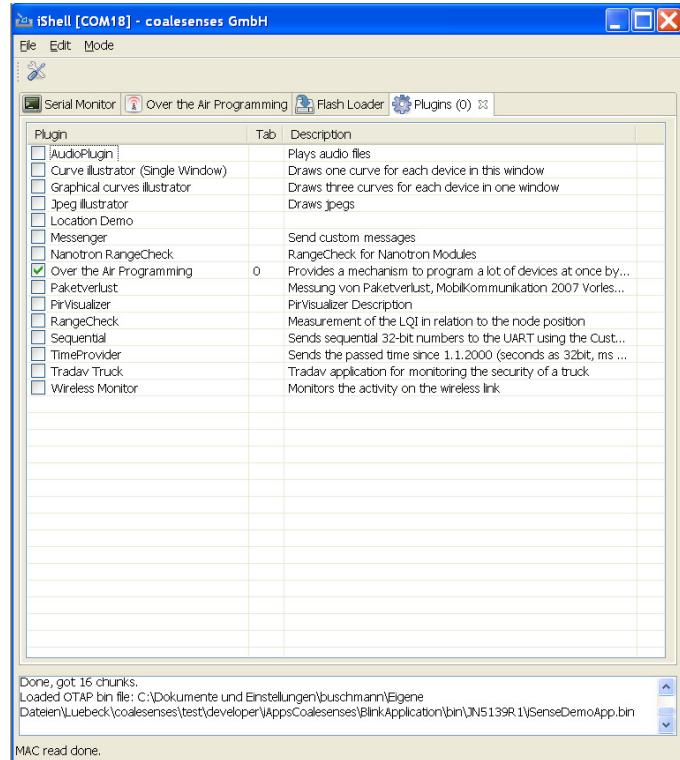


Fig 2.21 iShell

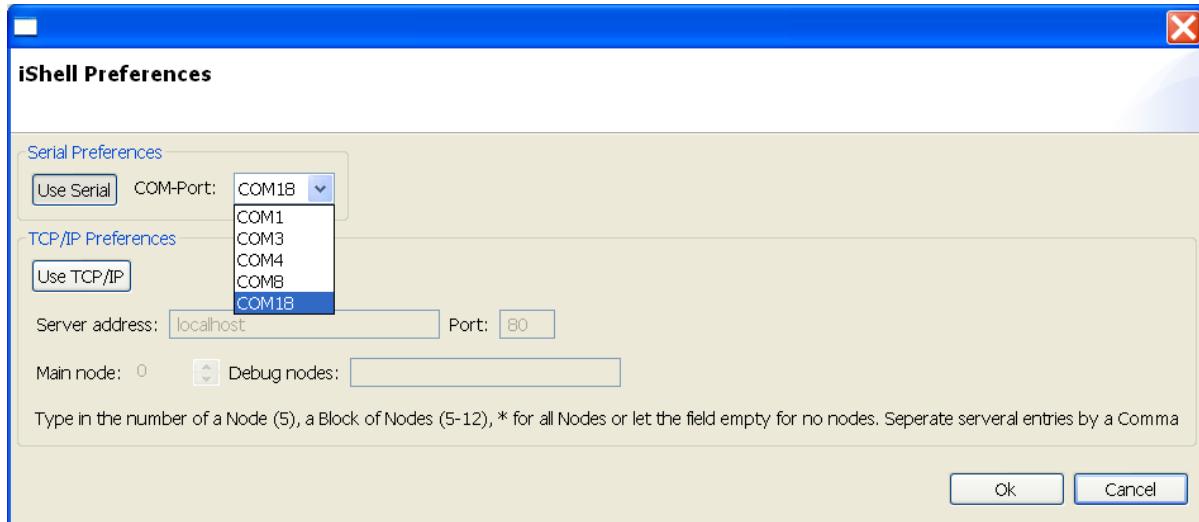


Fig 2.22 Selecting the proper port from the Preferences menu.

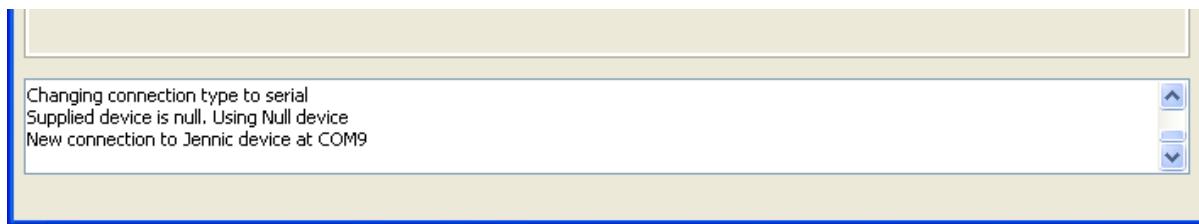


Fig 2.23 Notification indicating a successful connection

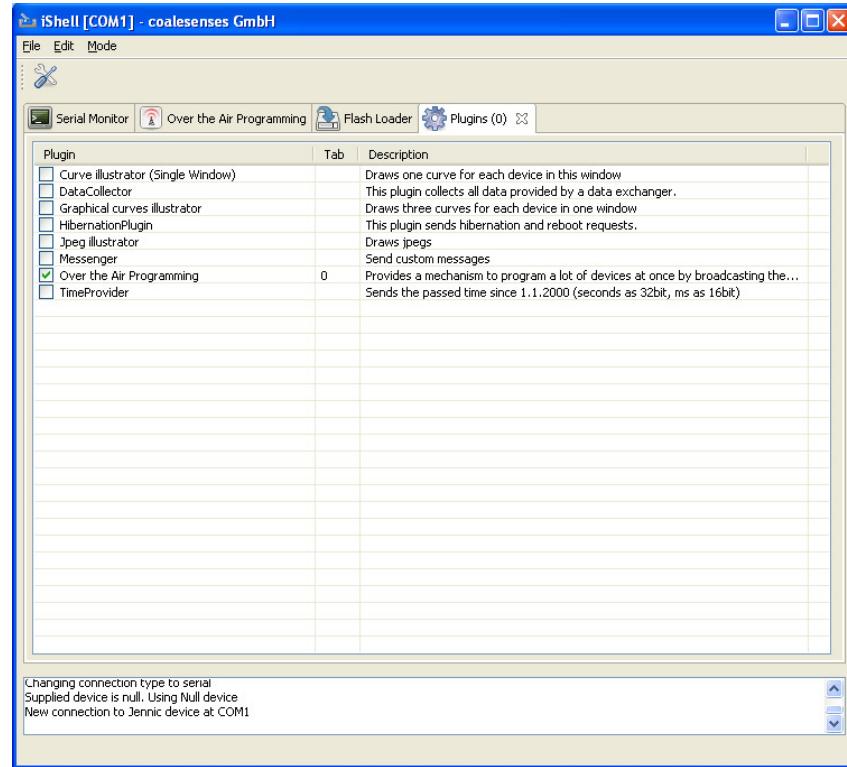


Fig 2.24 Activating Plugins from the “Plugins Tab”

- The “Flash Loader” plugin shown in Fig 2.25 provides functionality for flashing (i.e. programming) the connected device, analyzing the symbols in the program and reading and writing the device’s MAC address.

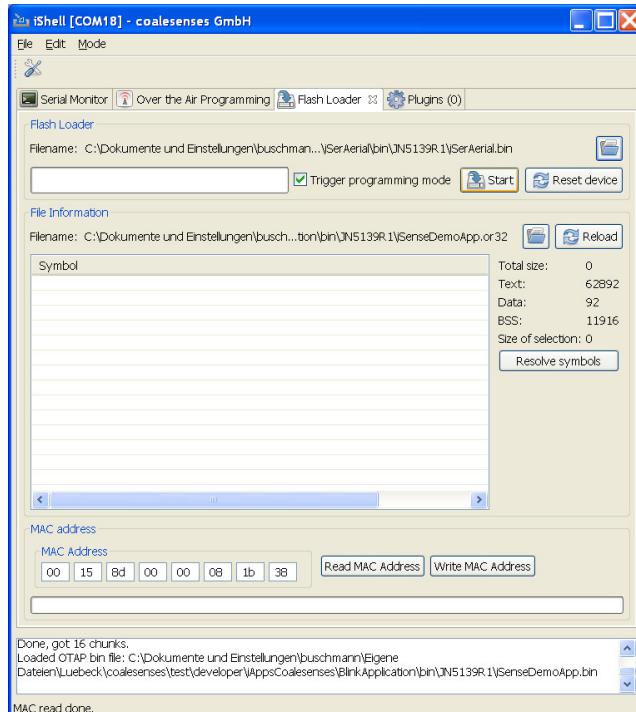


Fig 2.25 Flash Loader Plugin

- To flash a device, the \*.bin file to be flashed is selected by clicking on the file select button in the “Flash Loader” section. It is necessary to ensure that the target chip version of the program and the chip version of the connected device match.
- The binary program is then flashed to the iSense device connected to the PC by choosing “Trigger programming mode”, clicking on “Start”, and waiting for program download to complete. The flash progress displays the progress of the flash in the status line of the iShell window.
- In the “MAC Address” section, the address for the connected devices can be read or written. However, both actions involve restarting the device.
- The “Serial monitor” plugin shown in Fig 2.26 provides two modes, which can be set in the “Mode” menu.
- The plain text mode displays all contents of text messages. Unknown characters are displayed as small boxes.
- Operating the serial monitor in the packet mode means that only debug- and fatal-messages are displayed in grey and with red background respectively.

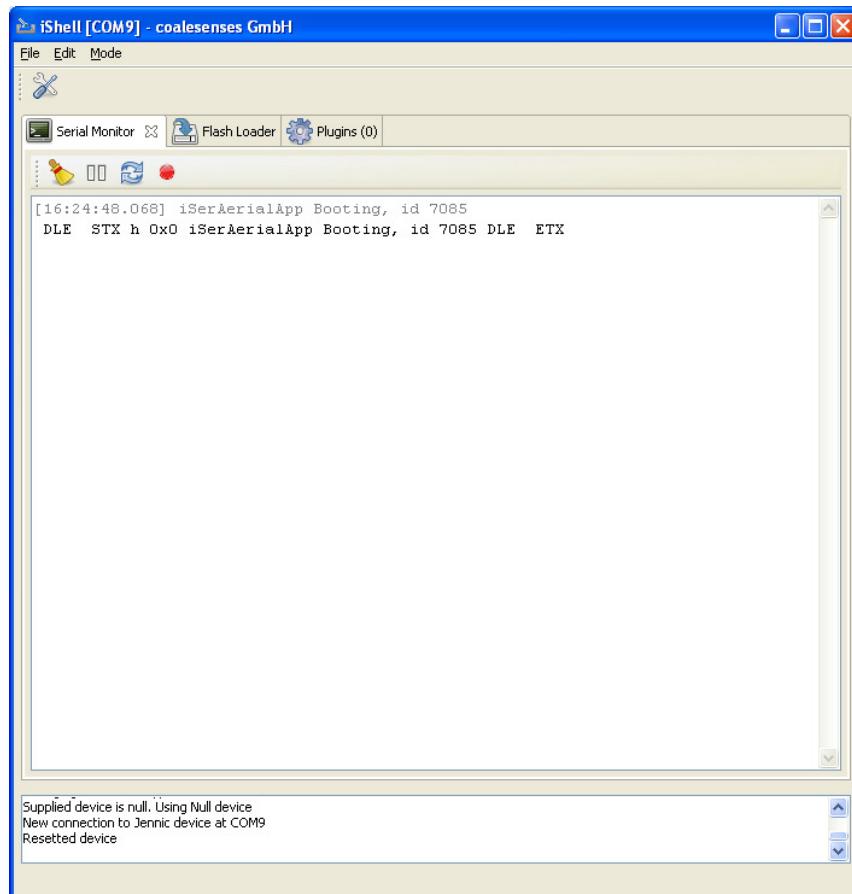


Fig 2.26 Serial monitor Plugin

- Four buttons permit managing the serial monitor as well as the iSense sensor node attached to iShell.
- The leftmost button clears the window, the second pauses or restarts the output of messages to the text area, the third button resets the connected device, which means to restart the application on the device. The rightmost starts/stops the recording of incoming messages to a file. On click, a file selection dialog opens. After a file name is specified, messages are recorded to that file. The messages are recorded regardless of whether the text area output is paused or not. Clicking the button again stops the recording of messages.

### **2.3.6 Eclipse Indigo**

Eclipse is an integrated development environment (IDE). It contains a base workspace and an extensible plug-in system for customizing the environment.

#### **2.3.6.1 Description**

Written mostly in Java, Eclipse can be used to develop applications. By means of various plug-ins, Eclipse may also be used to develop applications in other programming languages: Ada, ABAP, C, C++, COBOL, Fortran, Haskell, JavaScript, Lasso, Natural, Perl, PHP, Python, R, Ruby (including Ruby on Rails framework), Scala, Clojure, Groovy, Scheme, and Erlang. It can also be used to develop packages for the software Mathematica. Development environments include the Eclipse Java development tools (JDT) for Java and Scala, Eclipse CDT for C/C++ and Eclipse PDT for PHP, among others.

The initial codebase originated from IBM VisualAge. The Eclipse software development kit (SDK), which includes the Java development tools, is meant for Java developers. Users can extend its abilities by installing plug-ins written for the Eclipse Platform, such as development toolkits for other programming languages, and can write and contribute their own plug-in modules.

Released under the terms of the Eclipse Public License, Eclipse SDK is free and open source software (although it is incompatible with the GNU General Public License).

➤ **Steps to compile a C++ program on Eclipse Indigo**

- The first step is to Install Eclipse.
- The perspective can be changed to C++ by selecting “Window” > “Open Perspective” > “Other...” from the menu bar, and choosing “C/C++ (default)”.
- Next the applications are imported into Eclipse by selecting “File” > “Import” > “General” > “Existing Projects into Workspace” as shown in Fig 2.27

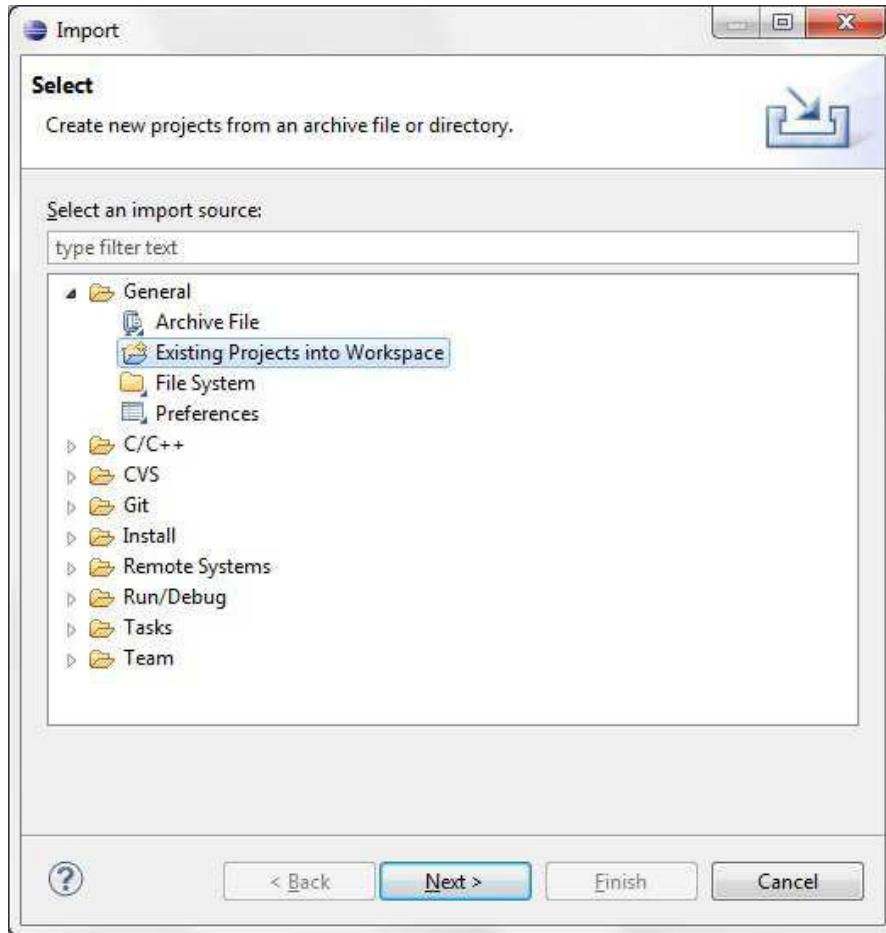


Fig 2.27 Importing projects

- Next the folder of the application to be imported is selected. It must be ensured that the check box corresponding to “Copy to workspace” is NOT ticked (Refer Fig 2.28)

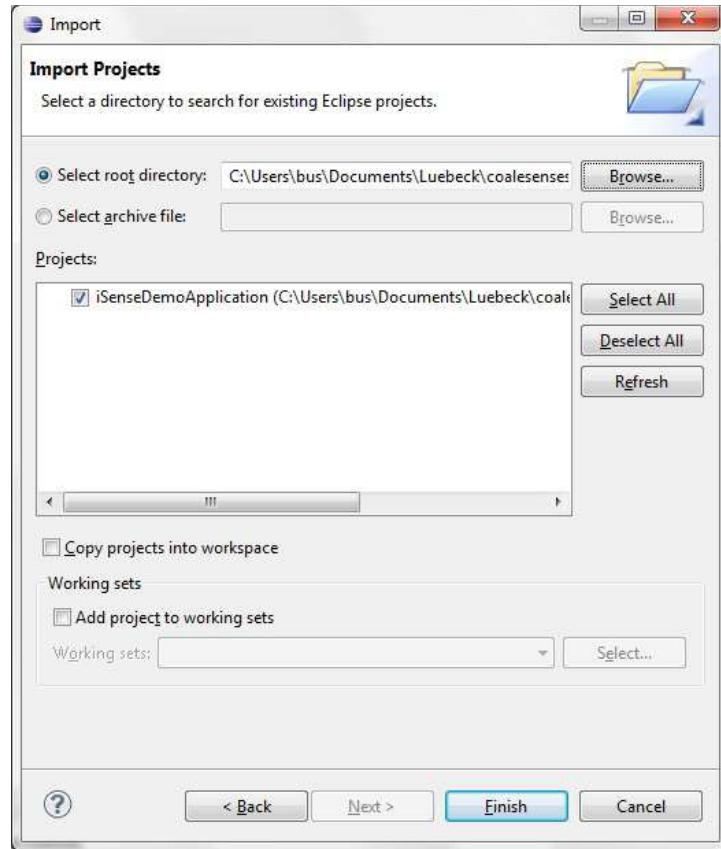


Fig 2.28 Importing existing projects into workspace

- On clicking “Finish”, the selected project is imported into the workspace. “Projects:” list, this commonly indicates that a project with the same name has already been imported into Eclipse before (no two projects with the same name can be imported into Eclipse at the same time).
- The program can be built by clicking on (JN5148) in the “Make Targets” pane on the right as shown in Fig 2.29

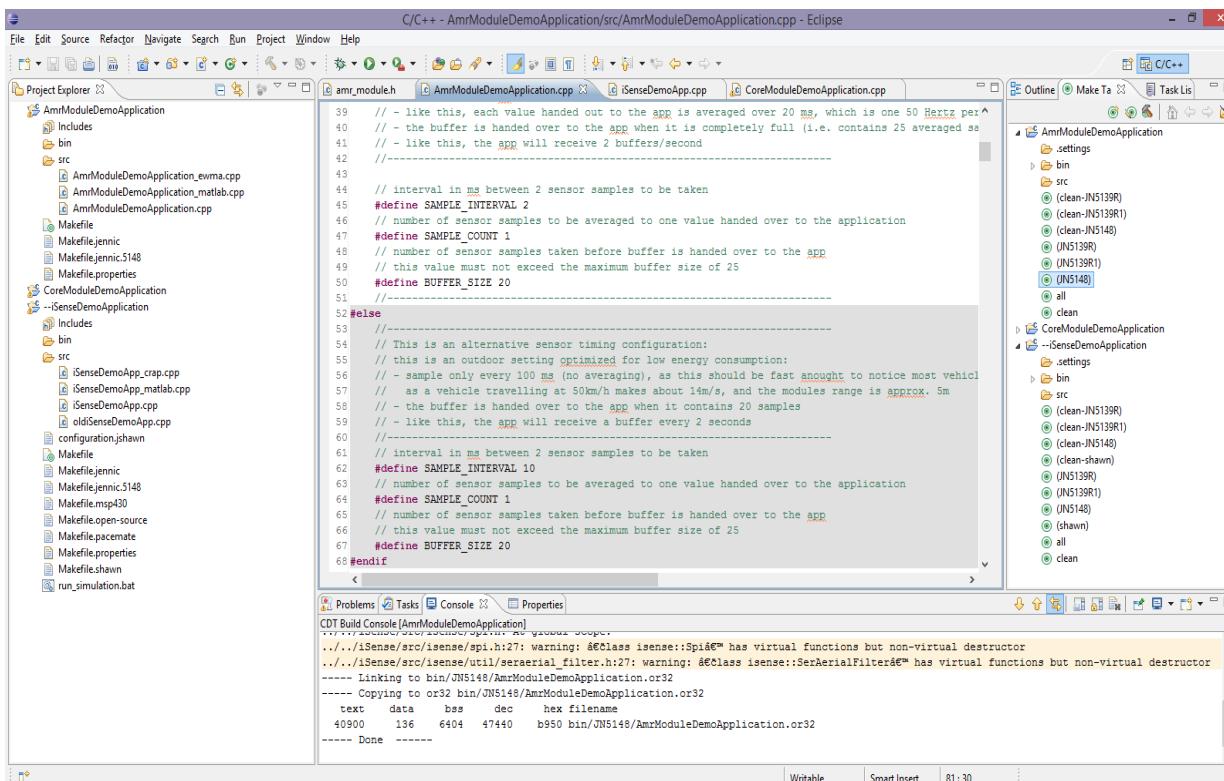


Fig 2.29 Building the program.

### **2.3.7 Microsoft Visual Studio 12.0**

Microsoft Visual Studio is an integrated development environment (IDE) from Microsoft. It is used to develop computer programs for Microsoft Windows superfamily of operating systems, as well as web sites, web applications and web services. Visual Studio uses Microsoft software development platforms such as Windows API, Windows Forms, Windows Presentation Foundation, Windows Store and Microsoft Silverlight. It can produce both native code and managed code.

Visual Studio supports different programming languages and allows the code editor and debugger to support (to varying degrees) nearly any programming language, provided a language-specific service exists. Built-in languages include C, C++ and C++/CLI (via Visual C++), VB.NET (via Visual Basic .NET), C# (via Visual C#), and F# (as of Visual Studio 2010). Support for other languages such as M, Python, and Ruby among others is available via language services installed separately. It also supports XML/XSLT, HTML/XHTML, JavaScript and CSS. Individual language-specific versions of Visual Studio also exist which provide more limited language services to the user: Microsoft Visual Basic, Visual J#, Visual C#, and Visual C++.

- **Developing a GUI on Visual Studio 2013:**
- On opening Visual Studio the following window appears (Fig 2.30 )

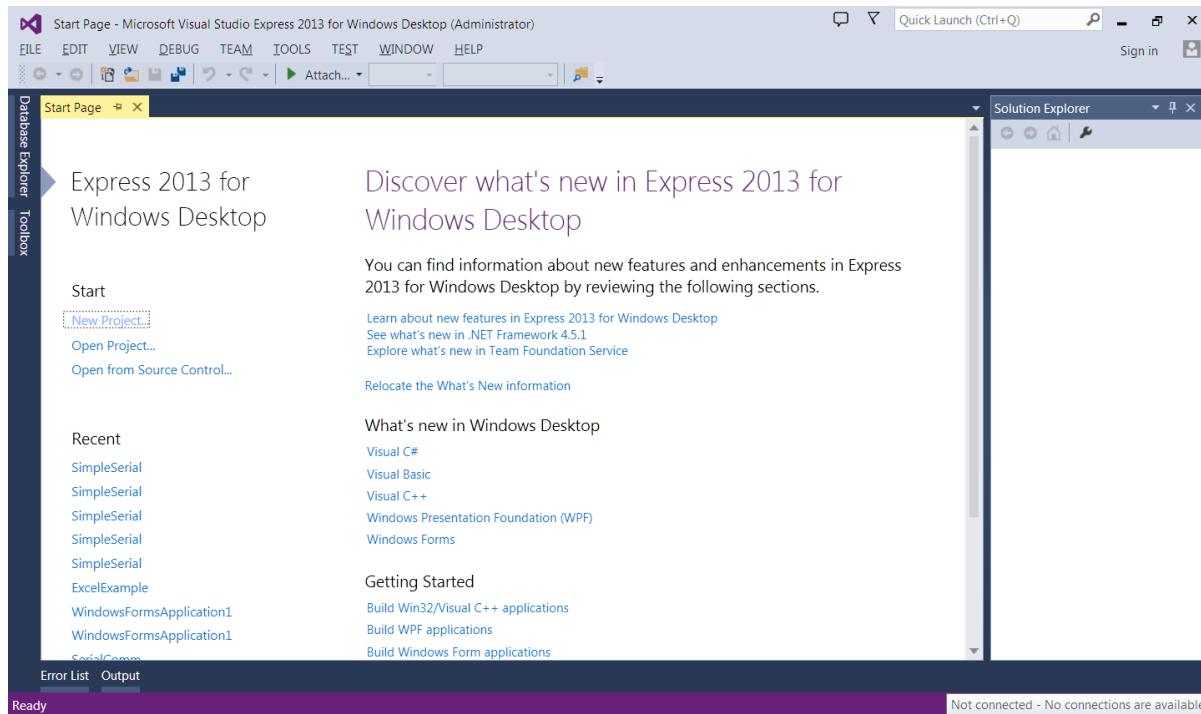


Fig 2.30 Microsoft Visual Studio 2013

- A new C# project is started by choosing “New Project” under the “Start” menu and choosing Visual C# Windows Forms Application as shown in Fig 2.31

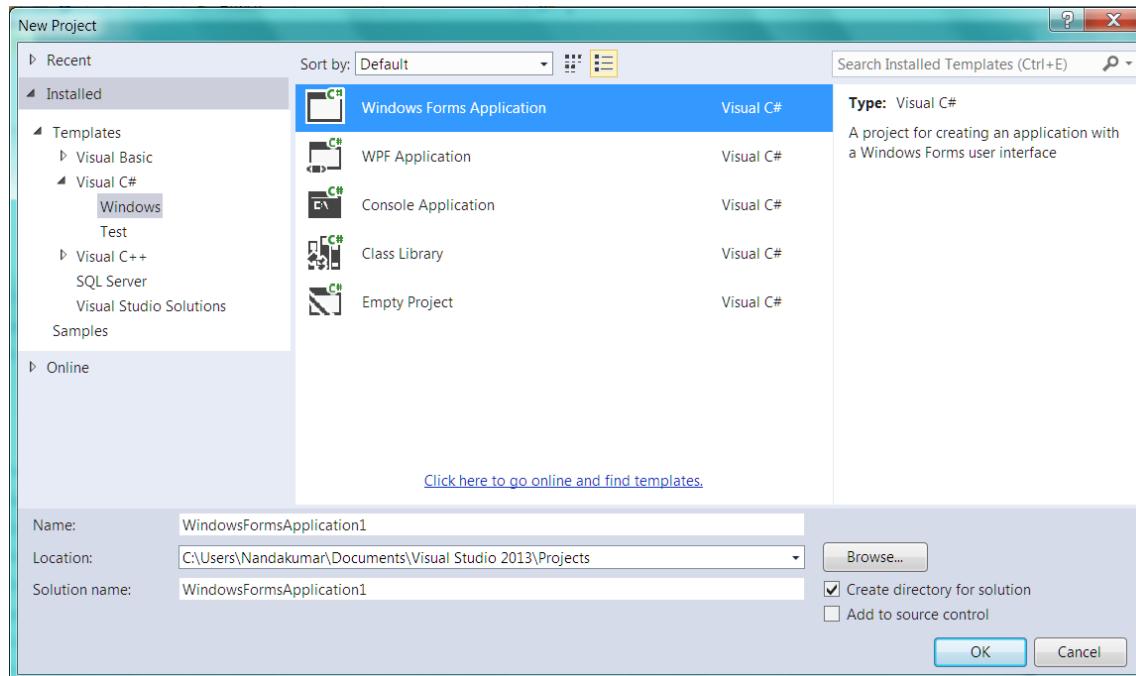


Fig 2.31 Creating a new C# project

- On completing the aforementioned steps, the following window appears (Fig 2.32).

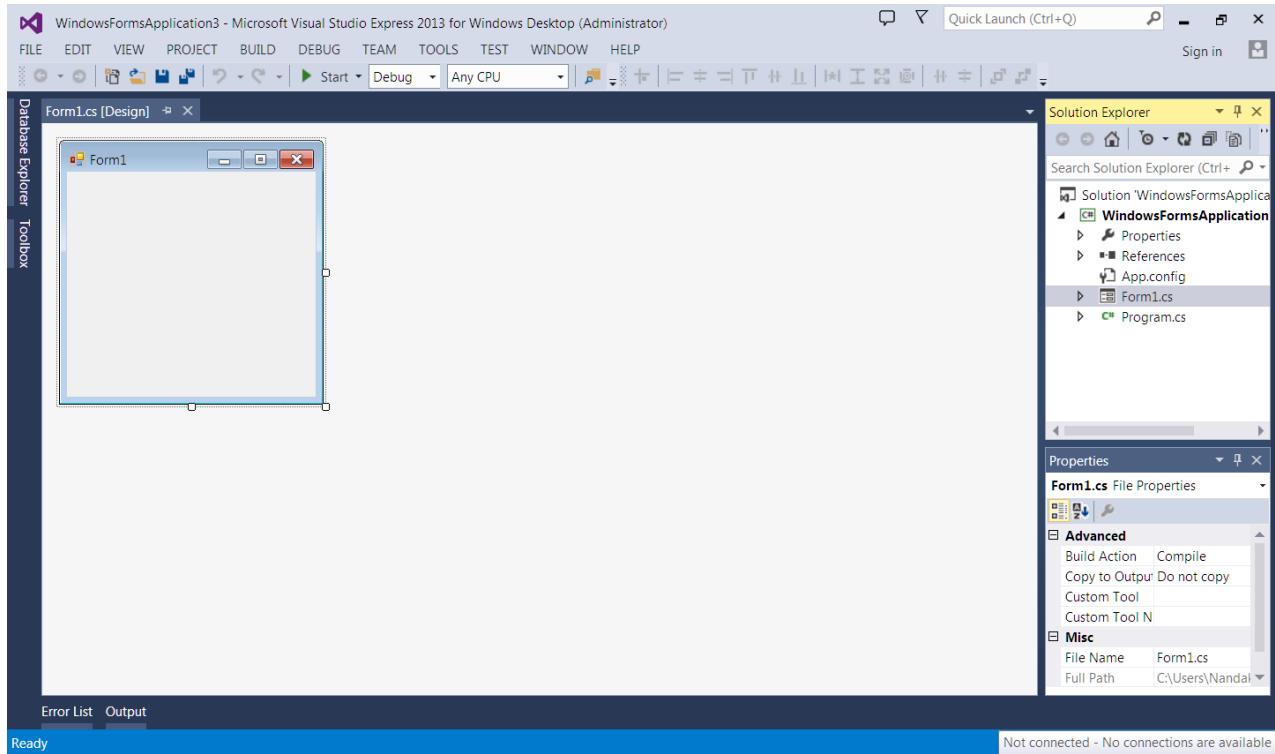


Fig 2.32 New Windows Form

- The GUI can now be designed using components from the Toolbox.
- Double clicking the GUI window opens the source code (Form1.cs)
- The code can be edited as per requirements.
- Finally the code is built and run by pressing F5.

## 2.4 Design of Induction loop detector using Colpitt's oscillator

An oscillator has a small signal feedback amplifier with an open-loop gain equal to or slightly greater than one for oscillations to start but to continue oscillations the average loop gain must return to unity. In addition to these reactive components, an amplifying device such as an Operational Amplifier or Bipolar Transistor is required. Unlike an amplifier there is no external AC input required to cause the Oscillator to work as the DC supply energy is converted by the oscillator into AC energy at the required frequency.

$$A = V_{out}/V_{in}$$

A= open loop voltage gain (i.e. without feedback)

Now let a fraction  $\beta$  of the output voltage  $V_{out}$  be supplied back to the input.

$$V_{in} = V_{in} + V_f = V_{in} + \beta V_{out} \dots\dots\dots (2.5)$$

$$V_{in} = V_{in} - V_f = V_{in} + \beta V_{out} \dots\dots\dots (2.6)$$

Equation 2.5 is for positive feedback while equation 2.6 is for negative feedback

Where  $V_s$  is the signal voltage and  $V_f$  is the feedback voltage.

That is:

$$V_{in} = V_s \pm \beta V_{out}$$

Considering negative feedback

$$A V_s - \beta V_{out} = V_{out}$$

$$AV_s = V_{out}(1 + A\beta)$$

The term  $A\beta$  is called the feedback factor whereas  $\beta$  is known as the feedback ratio and  $1 + A\beta$  is known as loop gain.

$$\frac{V_{out}}{V_s} = \frac{A}{1+A\beta} = A_f \dots\dots\dots (2.7)$$

where  $A_f$  = the closed loop gain

Equation 2.7 is normally refer to as the closed loop voltage gain for negative feedback and for positive feedback it is given by,

$$A_f = \frac{A}{1-A\beta}$$

LC Oscillators are circuits that generate a continuous voltage output waveform at a required frequency with the values of the inductors, capacitors or resistors forming a frequency selective LC resonant tank circuit and feedback network. This feedback network is an attenuation network which has a gain of less than one ( $\beta < 1$ ) and starts oscillations when  $A\beta > 1$  which returns to unity ( $A\beta = 1$ ) once oscillations commence. The LC oscillator's frequency is controlled using a tuned or resonant inductive/capacitive (L, C) circuit with the resulting output frequency being known as the Oscillation Frequency. By making the oscillators feedback a reactive network the phase angle of the feedback will vary as a function of frequency and this is called Phase-shift.

The frequency of the oscillator voltage depends upon the value of the inductance and capacitance in the LC tank circuit. We now know that for resonance to occur in the tank circuit, there must be a frequency point where the value of  $X_C$ , the capacitive reactance is the same as the value of  $X_L$ , the inductive reactance ( $X_L, X_C$ ) and which will therefore cancel out each other out leaving Only the D.C resistance in the circuit to oppose the flow of current. If we now place the

curve for inductive reactance of the inductor on top of the curve for capacitive reactance of the capacitor so that both curves are on the same frequency axes, the point of intersection will give us the resonance frequency point, ( $f_r$  or  $\omega_r$ ).

An induction loop detector provides a low cost method for detection of vehicles. The system consists of a loop of wire (typically 4 or 5 turns) buried approximately 20 mm below the road surface. The ends of the loop are returned to the vehicle detector usually housed some distance away in the controller cabinet. The output of the oscillator is converted into a square wave using a comparator and fed to the input capture pin of the microcontroller. The circuit diagram of the oscillator along with the comparator is shown in Fig 2.33

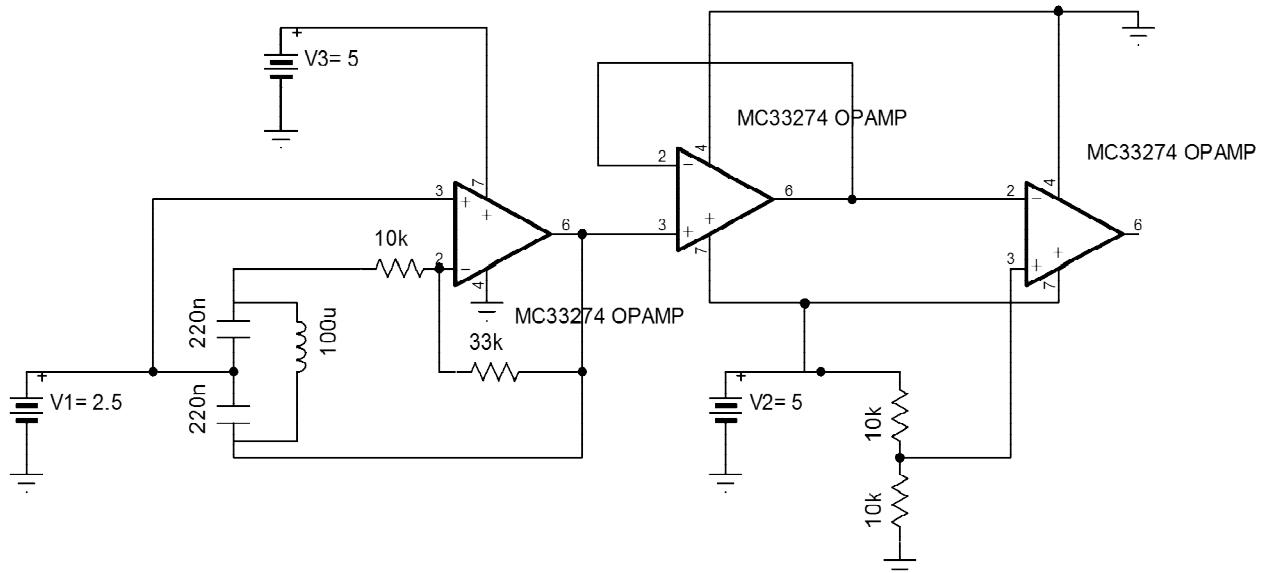


Fig 2.33 Circuit diagram of Colpitt's oscillator and comparator

The typical output waveforms of the oscillator and the comparator are shown in Fig 2.34

When the system is turned on, a high frequency counter sourced by a crystal oscillator is started on the microcontroller. Whenever a rising edge occurs on the input capture pin, the counter value is recorded. The difference in consecutive captured counter values can be used to determine the time period and frequency of the input signal.

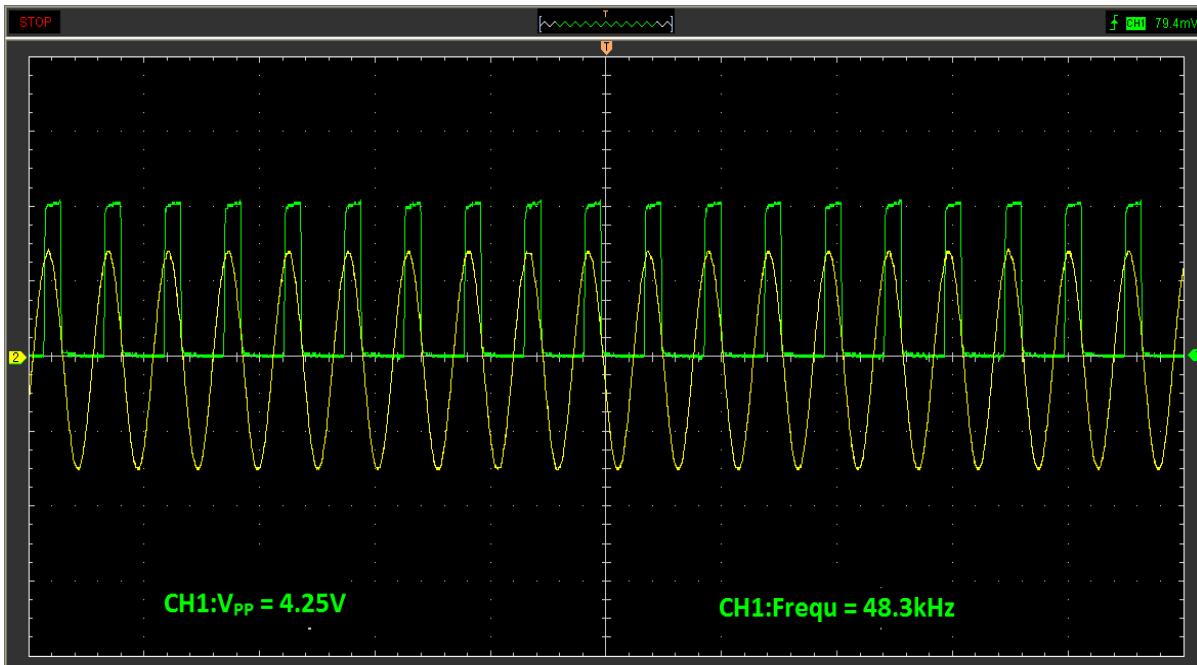


Fig 2.34 Output waveforms of the oscillator (in yellow) and the comparator (in green)

A decrease in the inductance of the loop occurs when a vehicle is positioned over it. This decrease causes a corresponding increase in the output frequency of the LC oscillator. This increase is sensed by the microcontroller that outputs a signal to the computer to indicate the presence of a vehicle. The amount of change in the inductance and hence the frequency is used to classify the vehicles as two wheelers and four wheelers.

The following data (Table 2.1) was used to arrive at the no. of turns of the induction loop.

Dimensions	No. of turns	Center frequency	Frequency drift
1.5ft x 1.5ft	10	48.3 kHz	500 Hz
6ft x 6ft	2	80 kHz (Unstable)	Unreliable
6ft x 6ft	3	51 kHz	300 Hz
6ft x 6ft	4	41 kHz	1000 Hz
6ft x 6ft	5	32.5 kHz	750 Hz

Table 2.1 Data used to arrive at the no. of turns of the induction loop

The dimension of 6ft x 6ft was chosen since the average width of a passenger car and the average length of a two wheeler is 6ft. This is important since maximum frequency drift is observed when the dimension of the metallic object is comparable to the dimension of the induction loop.

A snapshot of the induction loop and the detector components are shown in Fig 2.35 and Fig 2.36 respectively. Fig 2.37 shows the entire induction loop system.



Fig 2.35 Snapshot of the Induction Loop

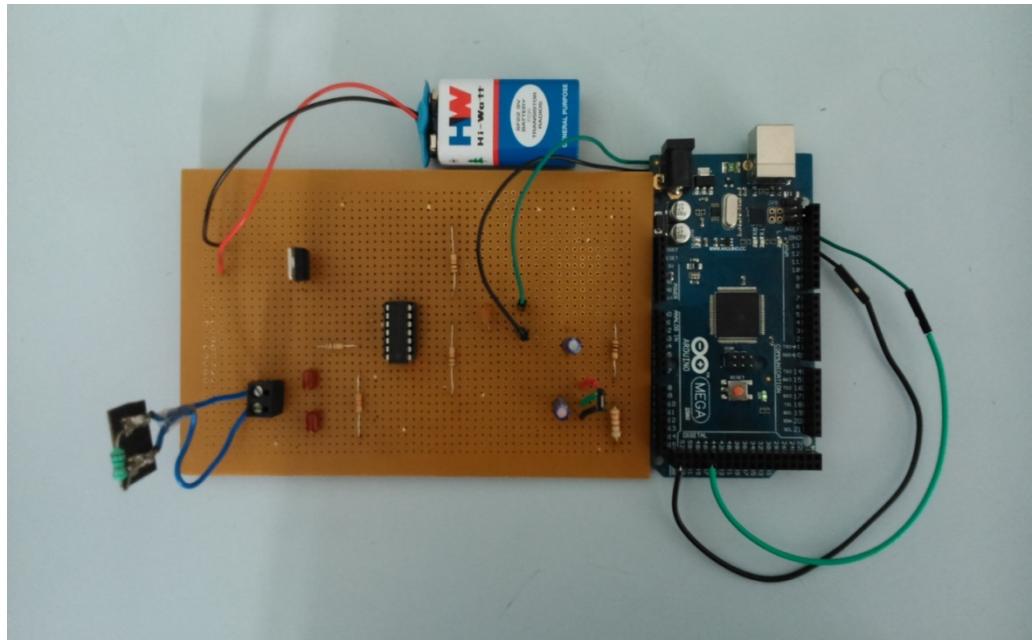


Fig 2.36 Snapshot of Induction Loop detector components

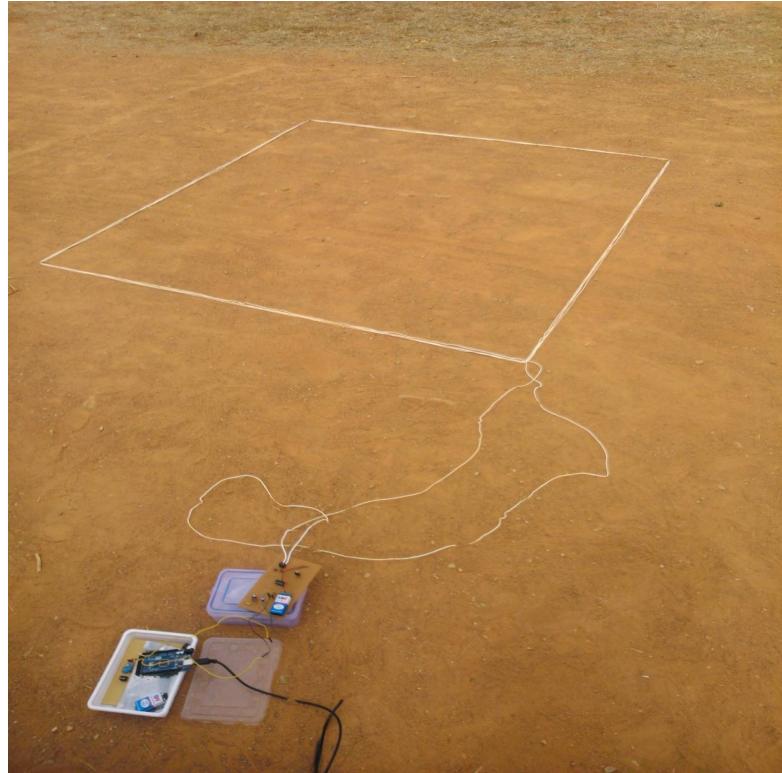


Fig 2.37 Snapshot of the induction loop system

A snapshot of the GUI used to display the traffic parameters acquired by the induction loop is shown in Fig 2.38



Fig 2.38 GUI for displaying traffic parameters acquired by the induction loop system

Table 2.2 shows the format of the database that stores the data about the count and class of vehicles acquired by the Induction Loop system.

Date	Two wheeler Count	Four Wheeler count	Total count
30/04/2014	9	9	18
01/05/2014	5	6	11
02/05/2014	3	2	5

Table 2.2 Database format for induction loop detector system

## 2.5 Design of AMR sensor vehicle detection system

The AMR sensor vehicle detection system consists of a core module and a vehicle detection module containing magnetic sensors. The iSense Core Module is based on a Jennic JN5148 wireless microcontroller, a chip that combines the controller and the wireless communication transceiver in a single housing. The controller provides 32 bit RISC computation, runs at a software-scalable frequency from 4 to 32 MHz and comprises 128kbytes of memory that are shared by program code and data. The radio part complies with the IEEE 802.15.4 standard. It achieves a data rate of 250kBit/s, provides hardware AES encryption and is ZigBee-ready.

A snapshot of the iSense Core Module is shown in Fig 2.39



Fig 2.39 iSense Core Module

The iSense Vehicle Detection Module (VDM10) is intended for detection of dynamic magnetic fields. The VDM10 is based on the two-axis anisotropic magneto-resistive (AMR) sensor Phillips KMZ52. The module also provides a de-gaussing circuitry and static magnetic field offset compensation. All three are controlled via I<sup>2</sup>C commands.

A snapshot of the vehicle detection module is shown in Fig 2.40

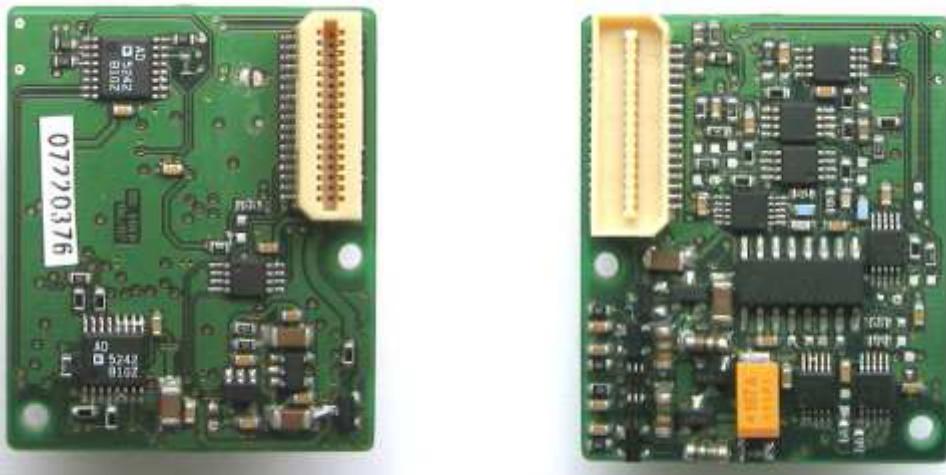


Fig 2.40 Snapshot of the Vehicle detection module

The typical output waveform of an AMR sensor when a vehicle passes over it is as shown in Fig 2.41

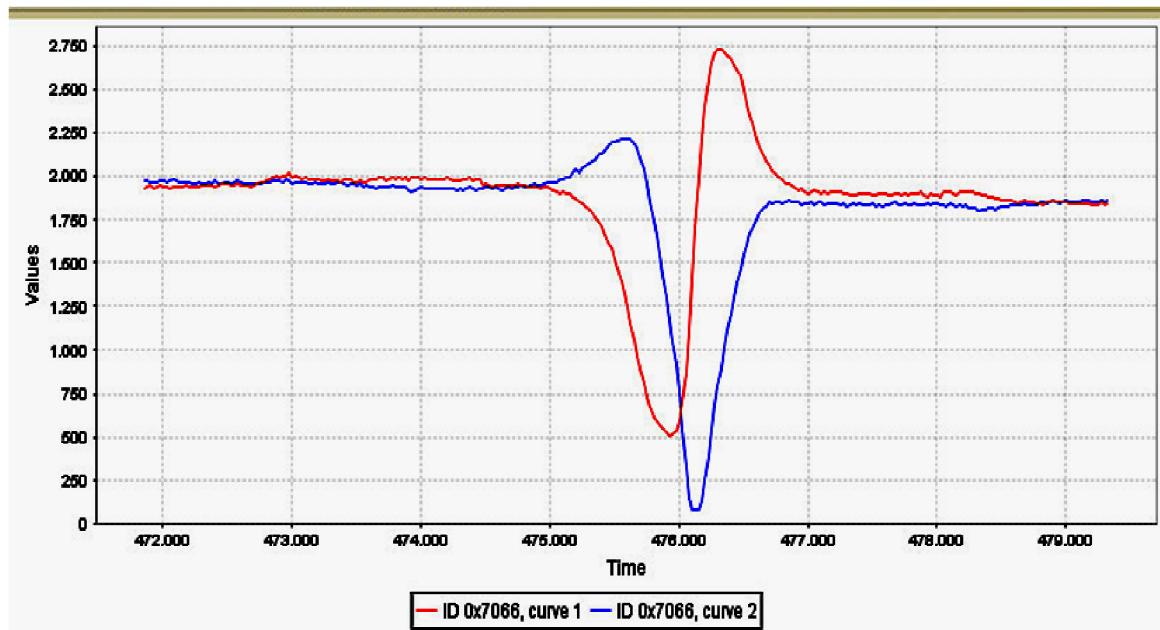


Fig 2.41 Typical output waveform of the AMR sensor. The two curves represent the output of the sensor in the two axes.

An AMR sensor vehicle detection system provides a low power solution for detection of vehicles. The system consists of two sensor modules which act as slaves and a core module which acts as a master. The slave modules communicate wirelessly with the master module via the ZigBee protocol. The master module is connected to a computer using a serial cable and communicates with it via UART. The computer is used to store the database and display it using a GUI.

The sensors on the slave modules detect the change in the ambient magnetic field. Initially they are calibrated to account for the magnetic field of the ambient environment and the default magnetic field generated by the earth. When a ferromagnetic material (commonly found in vehicles) passes over the sensor it disturbs the magnetic field around it. This change in magnetic field is detected by the sensor. It is observed that the output of the sensor peaks when a vehicle passes over it. These peaks are used to detect the presence of vehicles.

An EWMA (Exponentially weighted moving average) filter is used to eliminate the noise in the sensor output and obtain a smooth waveform. An algorithm running on the slave module that monitors the slope of the waveform when the sensor outputs cross a threshold is used to detect that a vehicle has passed over it. The absence of the slope detection algorithm can cause multiple detections for the same vehicle since the waveform stays over the threshold for several sampling instants. When a vehicle is detected, a time stamp indicating the time at which the vehicle crossed over the sensor is sent to the master module.

The slave modules are buried along the length of the road with a distance of two meters between them. Thus the time stamps sent by the two slave modules differ by a small value  $\Delta t$  as the vehicle passes over the two sensors one after the other. This difference is used to find the speed of the vehicle using the formula

$$S = D/\Delta t$$

Where

S is the speed,

D is the distance between the two sensors

$\Delta t$  is the time difference.

The sensor modules contain an internal clock which is used to keep track of time for which the slave modules are on. The internal clock is started at the moment the sensor modules are turned on. Since both the sensor modules cannot be turned on simultaneously, an initial time difference exists between the clocks of the two sensor modules. This time difference adds to  $\Delta t$  leading to an error

in the speed calculation. To eliminate this, the initial time difference is subtracted from  $\Delta t$ . This is achieved using a synchronization algorithm running on the master and slave modules.

When a vehicle is detected, the time difference  $\Delta t$  is calculated by the master module and sent to the PC via UART where the speed is computed and the count and speed are stored in the database.

A snapshot of the experimental setup used to calculate speed in case of AMR vehicle detection system is shown in Fig 2.42

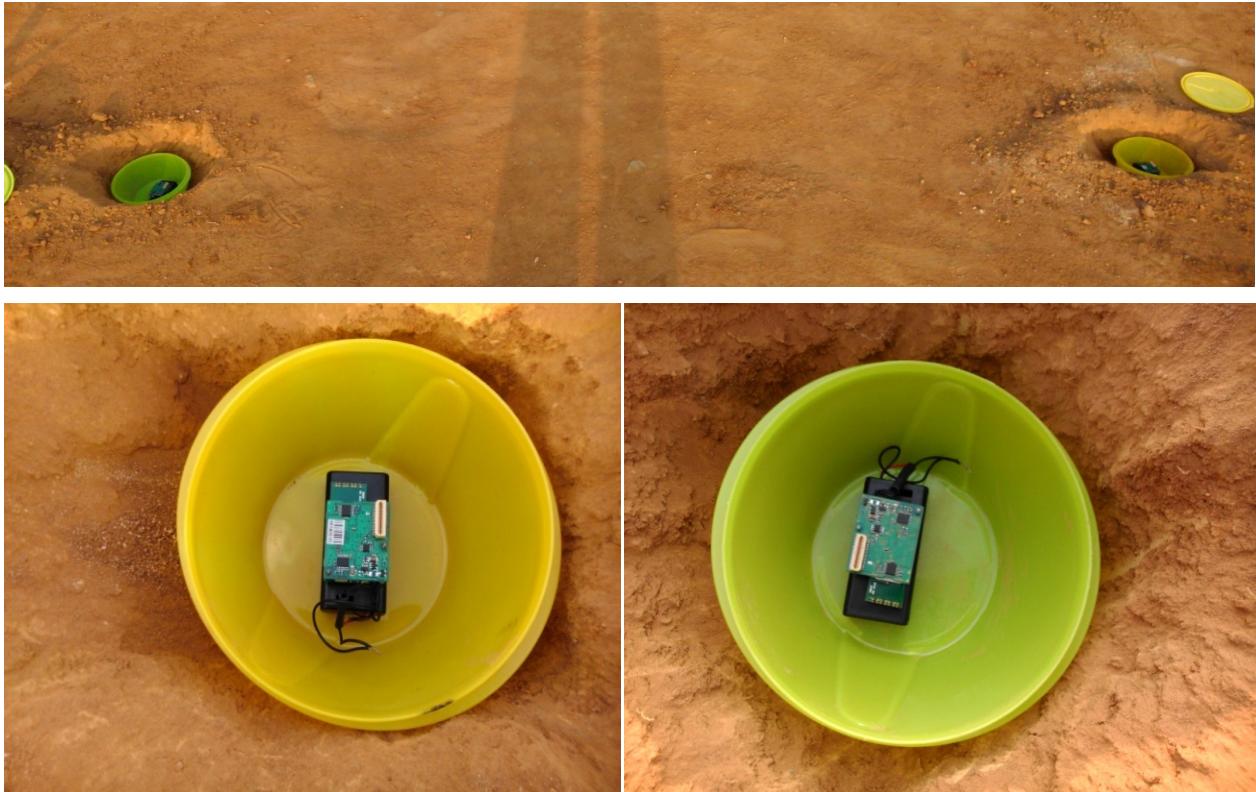


Fig 2.42 Experimental setup used to calculate speed in case of AMR vehicle detection system

Fig 2.43 shows a snapshot of the GUI used to display the traffic parameters acquired by the AMR vehicle detection system.



Fig 2.43 GUI to display the traffic parameters acquired by the AMR vehicle detection system

Table 2.3 shows the format of the database that stores the data about the count and speed of vehicles acquired by the AMR vehicle detection system.

Date	Vehicle count	Average speed (kmph)
03/05/2014	8	22.92
04/05/2014	8	24.20

Table 2.3 Database format for AMR sensor vehicle detection system

# RESULTS

### III. RESULTS

#### 3.1 Induction loop vehicle detection system

##### ➤ Frequency drifts

The induction loop system was tested to determine the frequency drifts for two wheelers and four wheelers at different speeds. Ten trials were carried out at each speed ranging from 10 to 40 for each type of vehicle. The results obtained are tabulated below (Table 3.1 and Table 3.2).

- Two wheelers

Speed (kmph)	Frequency drift (Hz)	Avg. frequency drift
10	55	55.3
	38	
	52	
	56	
	52	
	64	
	50	
	64	
	72	
	50	
20	50	48.2
	60	
	54	
	52	
	42	
	30	
	54	
	36	
	36	
	68	
30	48	39.4
	32	
	46	
	50	
	24	
	42	
	50	
	54	
	22	
	26	
40	24	34
	44	
	16	
	36	
	50	
	36	
	28	
	26	
	45	
	35	

Table 3.1 Frequency drift values for different speeds in case of two wheelers

- Four wheelers

Speed (kmph)	Frequency drift (Hz)	Avg. frequency drift
10	1100	1010.8
	896	
	880	
	962	
	872	
	1106	
	1136	
	990	
	1068	
	1098	
20	958	1006.2
	1262	
	764	
	806	
	1406	
	900	
	856	
	1010	
	960	
	1140	
30	1200	1000.2
	924	
	986	
	1212	
	688	
	952	
	982	
	872	
	940	
	1246	
40	916	937.8
	746	
	1056	
	1014	
	936	
	960	
	1020	
	899	
	943	
	888	

Table 3.2 Frequency drift values for different speeds in case of four wheelers

Thus the frequency drift is found to decrease with speed in case of both two wheelers and four wheelers. This is due to the fact that the vehicle stays within the loop for a shorter duration of time as the speed increases. Thus the eddy currents induced in the loop are lower resulting in a smaller decrease in inductance and hence a smaller increase in frequency.

➤ Accuracy of count

No. of trials = 50

No. of times a vehicle went undetected or detected more than once = 4

**Accuracy = 92%**

➤ Accuracy of classification

No. of trials = 50

No. of times a two wheeler was detected as a four wheeler or vice versa = 5

**Accuracy = 90%**

### 3.2 AMR sensor vehicle detection system

➤ Accuracy of detected speed

The AMR sensor vehicle detection system was tested to determine the accuracy of the detected speed for two wheelers and four wheelers at different speeds. Eight trials were carried out for each type of vehicle. The results obtained are tabulated below (Table 3.3).

Type of vehicle	Actual speed (kmph)	Detected speed (kmph)	Error (in %)
Two wheelers	10	8.98	10.2
	10	7.64	23.6
	20	18.00	10.0
	20	21.56	7.8
	30	26.54	11.5
	30	28.87	3.8
	40	35.64	10.9
	40	36.11	9.7
Four wheelers	10	10.58	5.8
	10	12.00	20
	20	18.23	8.8
	20	20.57	2.8
	30	27.91	7.0
	30	30.35	1.2
	40	37.22	6.9
	40	36.78	8.1

Table 3.3 Accuracy of the detected speed for two wheelers and four wheelers at different speeds

The actual error values may be lower than the mentioned values since the actual speed was observed on analog speedometers.

➤ Accuracy of count

No. of trials = 25

No. of times a vehicle went undetected or detected more than once = 1

**Accuracy = 96%**

# CONCLUSION

## IV. CONCLUSION

- One of the advantages of Induction loop detector system over AMR sensor vehicle detection system is that the initial installation costs are much lower. They can also detect stopped vehicles.
- However, significant and reliable change in magnetic field occurs only when the vehicle is completely inside the loop, as against the AMR sensors which are more sensitive to the presence of magnetic materials.
- Magnetic sensors are more economical compared to inductive loops as they are easy to reinstall and maintenance costs are low.
- Magnetic sensors are smaller in size compared to inductive loops which require a minimum area of around 36 sq. ft.
- Magnetic sensors have proven to be more immune to noise and stable compared to frequency drifts occurring in the induction loop system due to environmental changes.
- Devices embedded in asphalt often get damaged as a result of pressure exerted on the ground by heavy vehicles passing. Small sensors have therefore an advantage over those like large inductive loops, as their re-installation is associated with lower costs.
- The sensing and measurement architecture of magnetic sensors uses a minimal level of energy and uses state-of-the-art low-power sensing, amplification, and communication technologies.
- Thus magnetic sensor systems are more efficient and reliable than induction loops.

# **FUTURE ENHANCEMENTS**

## V. FUTURE ENHANCEMENTS

### ➤ **Induction Loop vehicle detection system**

- Two loops can be used to determine the speed of the vehicles.
- Methods for solving the problem of detection of vehicles moving parallel to each other can be implemented.

### ➤ **AMR vehicle detection system**

- Sensors with higher sampling rate can be used to classify vehicles based on their magnetic signature.

Auxiliary sensors such as video processing systems and infrared sensors can be used in conjunction with the induction loop and AMR sensor systems to eliminate false counts and increase the accuracy of the traffic parameters acquired.

# REFERENCES

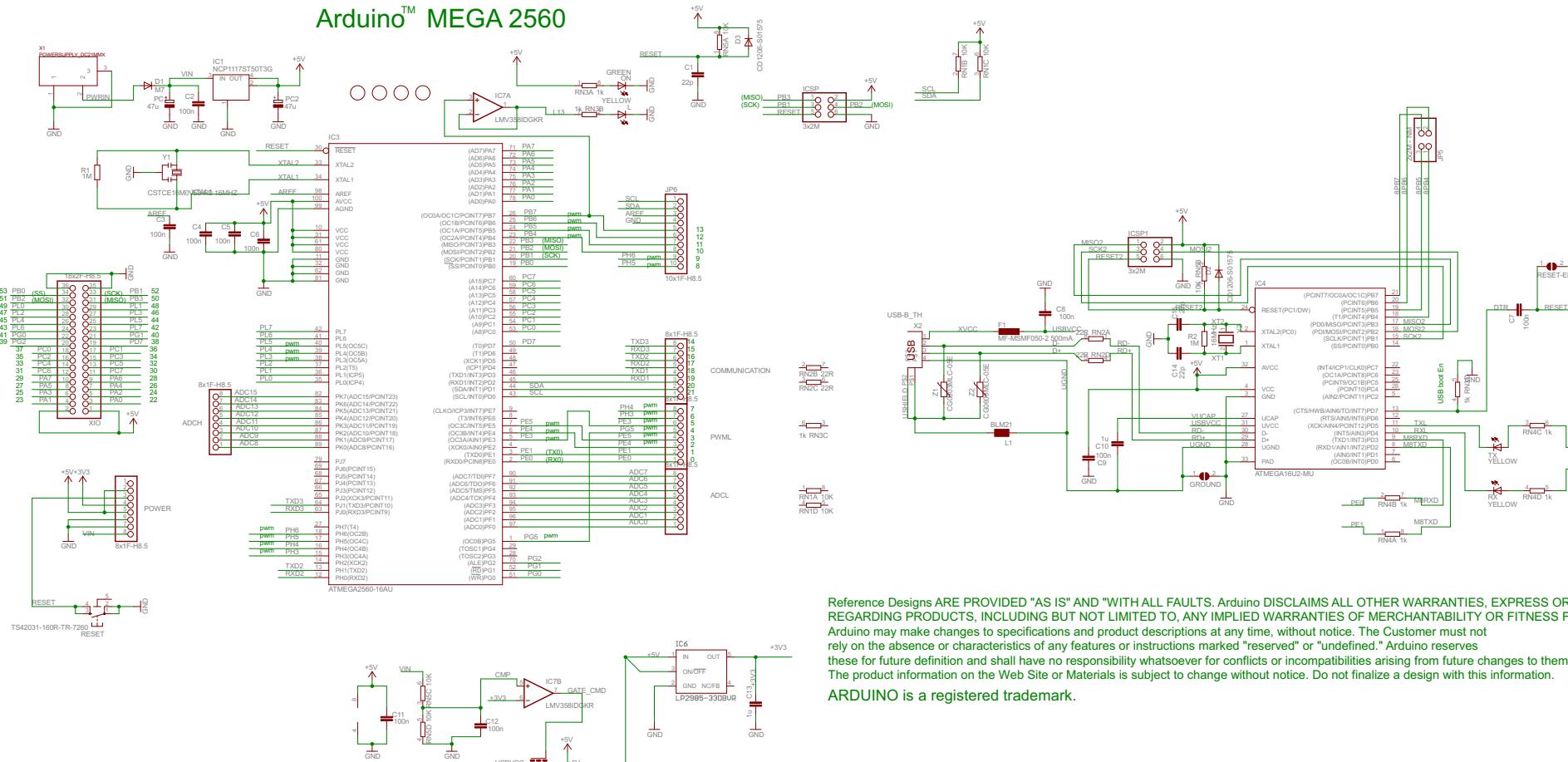
## VI. REFERENCES

- [1] Ravneet Bajwa, Ram Rajagopal, Pravin Varaiya and Robert Kavaler. In-Pavement Wireless Sensor Network for Vehicle Classification.
- [2] Sing Yiu Cheung, Sinem Coleri Ergen and Pravin Varaiya. Traffic Surveillance with Wireless Magnetic Sensors.
- [3] Farshad Ahdi, Mehdi Kalantari Khandani, Masoud Hamed, Ali Haghani. Traffic data collection and anonymous vehicle detection using wireless sensor networks.
- [4] Traffic Detector Handbook: Third Edition—Volume I. Publication No. FHWA-HRT-06-108.
- [5] D. Cebon. Handbook of Vehicle-Road Interaction. Swets and Zeitlinger Publishers, 1999.
- [6] Sun C. (2004). An investigation in the use of inductive loop signatures for vehicle classification. California PATH Research Report UCB-ITS-PRR-2002-4.
- [7] Zhang, X., Y. Wang, N.L. Nihan (2004). Monitoring a freeway network in real-time using single-loop detectors: System design and implementation, 83rd TRB Annual Meeting, Washington, D.C.
- [8] Ding, J (2003). Vehicle detection by sensor network nodes. MS thesis, Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA.
- [9] Oh, S., S.G. Ritchie, C (2002). Oh. Real time traffic measurement from single loop inductive signatures, 81st TRB Annual Meeting, Washington, D.C.
- [11] G.S.M. Galandanci & K.O. Ewansiha. Design and simulation of a 20 khz to 50 khz variable frequency oscillator (vfo). [www.arpapress.com/](http://www.arpapress.com/) Volumes/ Vol16Issue1/ IJRRAS\_16\_1\_04.pdf
- [12] Gordon, R.L., R.A. Reiss, H. Haenel, E.R. Case, R.L. French, A. Mohaddes, and R. Wolcott; Traffic Control Systems Handbook, FHWA-SA-95-032, Federal Highway Administration, U.S. Department of Transportation, Washington, D.C., Feb. 1996
- [13] Seri Oh, Stephen G. Ritchie, and Cheol Oh. Real Time Traffic Measurement From Single Loop Inductive Signatures, presented for 81st Annual Meeting of the Transportation Research board, Washington D.C., January 2002.
- [14] Chao Chen, Jaimyoung Kwon, John Rice, Alexander Skabardonis and Pravin Varaiya. Detecting Errors and Imputing Missing Data for Single Loop Surveillance Systems, Presented in the 82nd Transportation Research Board Annual Meeting, Washington D.C., January 2003.

- [15] Luz Elena Y. Mimbela and Lawrence A. Klein. A Summary of Vehicle Detection and Surveillance Technologies used in Intelligent Transportation Systems, the Vehicle Detector Clearinghouse, New Mexico State University, Fall 2000.
- [16] Sun, C., S.G. Ritchie, and K. Tsai. Algorithm Development for Derivation of Section-Related Measures of Traffic System Performance using Inductive Loop Detectors. In Transportation Research Record 1643, TRB, National Research Council, Washington, D.C., 1998, pp. 171-180.
- [17] Marcin Bugdol, Zuzanna Segiet, Michal Krecichwost, Paweł KASPEREK, Vehicle Detection System Using Magnetic Sensors, Transport Problems 2014 Volume 9 Issue 1
- [18] Ripka, P. Magnetic Sensors and Magnetometers. Norwood: Artech House. 2001.
- [19] Texas Transportation Institute. Alternative Vehicle Detection Technologies for Traffic Signal Systems: Technical Report. Austin. 2008.
- [20] Tumański, S. Thin Film Magnetoresistive Sensors. London: IOP Publ. 2001.

# **APPENDIX**

## Arduino™ MEGA 2560



Reference Designs ARE PROVIDED "AS IS" AND "WITH ALL FAULTS. Arduino DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING PRODUCTS, INCLUDING BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE

Arduino may make changes to specifications and product descriptions at any time, without notice. The Customer must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Arduino reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The product information on the Web Site or Materials is subject to change without notice. Do not finalize a design with this information.

**ARDUINO** is a registered trademark.

## Features

- High Performance, Low Power Atmel® AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 135 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 × 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16MHz
  - On-Chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 64K/128K/256KBytes of In-System Self-Programmable Flash
  - 4Kbytes EEPROM
  - 8Kbytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/ 100 years at 25°C
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
    - Endurance: Up to 64Kbytes Optional External Memory Space
- Atmel® QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix® acquisition
  - Up to 64 sense channels
- JTAG (IEEE std. 1149.1 compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - Four 16-bit Timer/Counter with Separate Prescaler, Compare- and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four 8-bit PWM Channels
  - Six/Twelve PWM Channels with Programmable Resolution from 2 to 16 Bits (ATmega1281/2561, ATmega640/1280/2560)
  - Output Compare Modulator
  - 8/16-channel, 10-bit ADC (ATmega1281/2561, ATmega640/1280/2560)
  - Two/Four Programmable Serial USART (ATmega1281/2561, ATmega640/1280/2560)
  - Master/Slave SPI Serial Interface
  - Byte Oriented 2-wire Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 54/86 Programmable I/O Lines (ATmega1281/2561, ATmega640/1280/2560)
  - 64-pad QFN/MLF, 64-lead TQFP (ATmega1281/2561)
  - 100-lead TQFP, 100-ball CBGA (ATmega640/1280/2560)
  - RoHS/Fully Green
- Temperature Range:
  - -40°C to 85°C Industrial
- Ultra-Low Power Consumption
  - Active Mode: 1MHz, 1.8V: 500µA
  - Power-down Mode: 0.1µA at 1.8V
- Speed Grade:
  - ATmega640V/ATmega1280V/ATmega1281V:
    - 0 - 4MHz @ 1.8V - 5.5V, 0 - 8MHz @ 2.7V - 5.5V
  - ATmega2560V/ATmega2561V:
    - 0 - 2MHz @ 1.8V - 5.5V, 0 - 8MHz @ 2.7V - 5.5V
  - ATmega640/ATmega1280/ATmega1281:
    - 0 - 8MHz @ 2.7V - 5.5V, 0 - 16MHz @ 4.5V - 5.5V
  - ATmega2560/ATmega2561:
    - 0 - 16MHz @ 4.5V - 5.5V



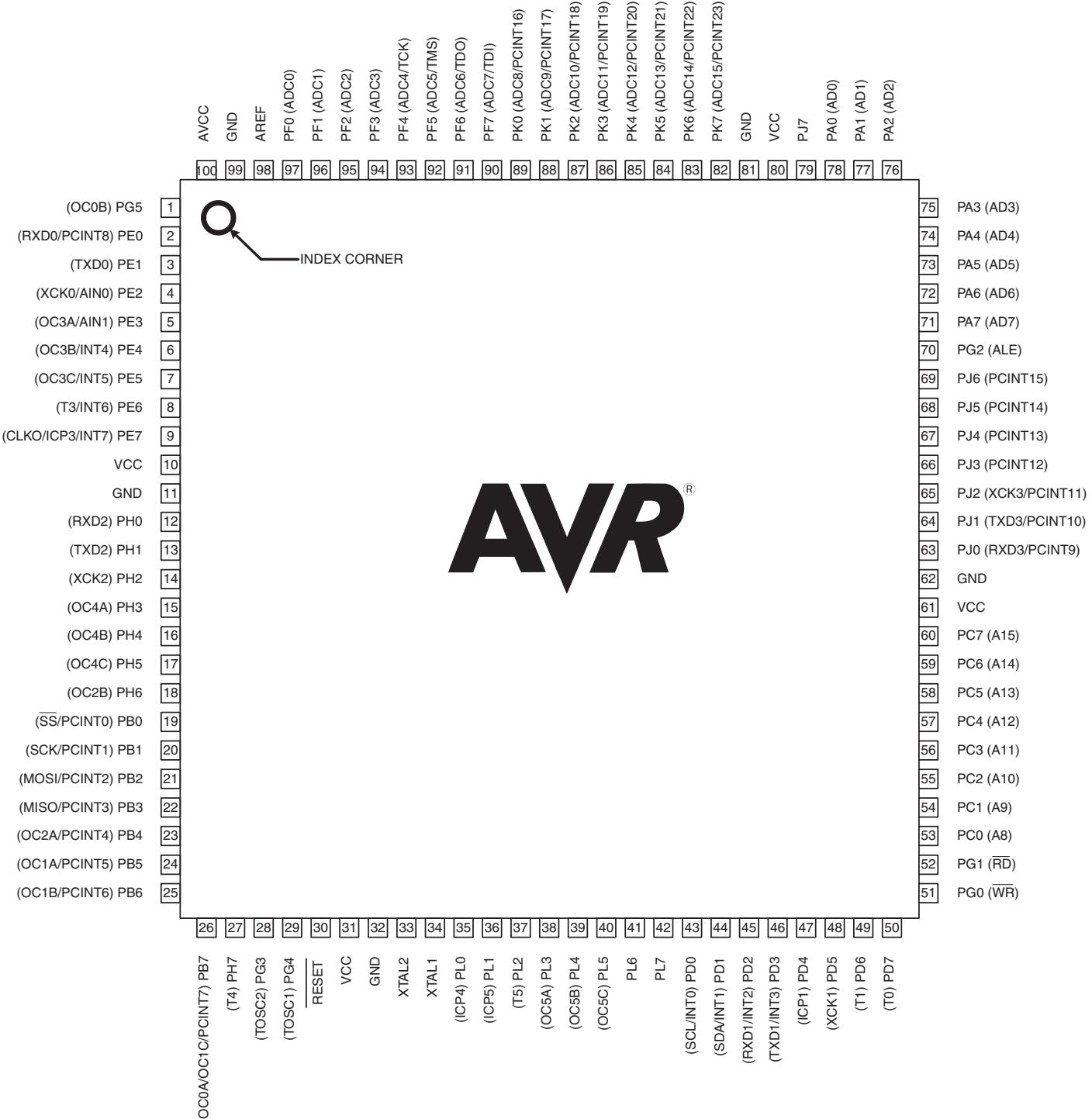
## 8-bit Atmel Microcontroller with 64K/128K/256K Bytes In-System Programmable Flash

**ATmega640/V  
ATmega1280/V  
ATmega1281/V  
ATmega2560/V  
ATmega2561/V**



## 1. Pin Configurations

**Figure 1-1.** TQFP-pinout ATmega640/1280/2560



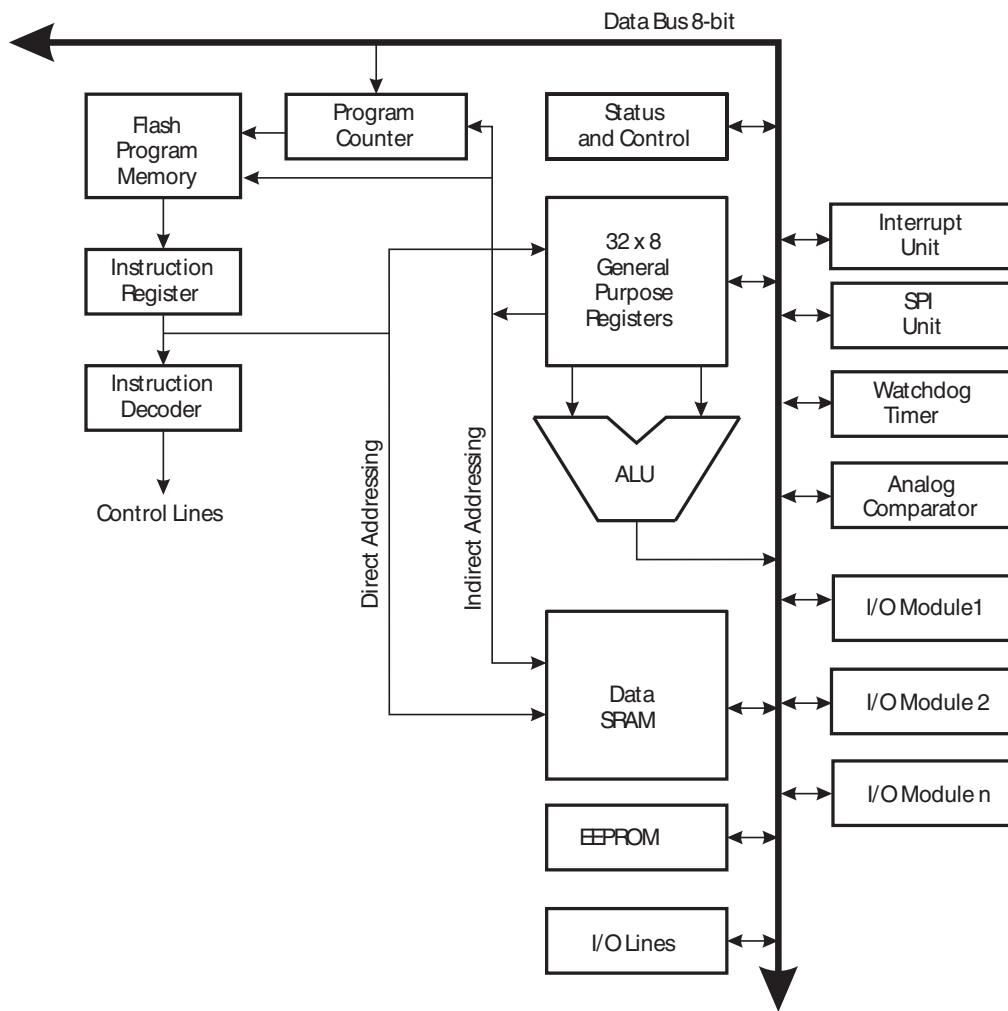
## 7. AVR CPU Core

### 7.1 Introduction

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

### 7.2 Architectural Overview

Figure 7-1. Block Diagram of the AVR Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

The fast-access Register File contains  $32 \times 8$ -bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16-bit or 32-bit instruction.

Program Flash memory space is divided in two sections, the Boot Program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the Reset routine (before subroutines or interrupts are executed). The Stack Pointer (SP) is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional Global Interrupt Enable bit in the Status Register. All interrupts have a separate Interrupt Vector in the Interrupt Vector table. The interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register File, 0x20 - 0x5F. In addition, the ATmega640/1280/1281/2560/2561 has Extended I/O space from 0x60 - 0x1FF in SRAM where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

## 7.3 ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See the “[Instruction Set Summary](#)” on page 416 for a detailed description.

## 16. 8-bit Timer/Counter0 with PWM

### 16.1 Features

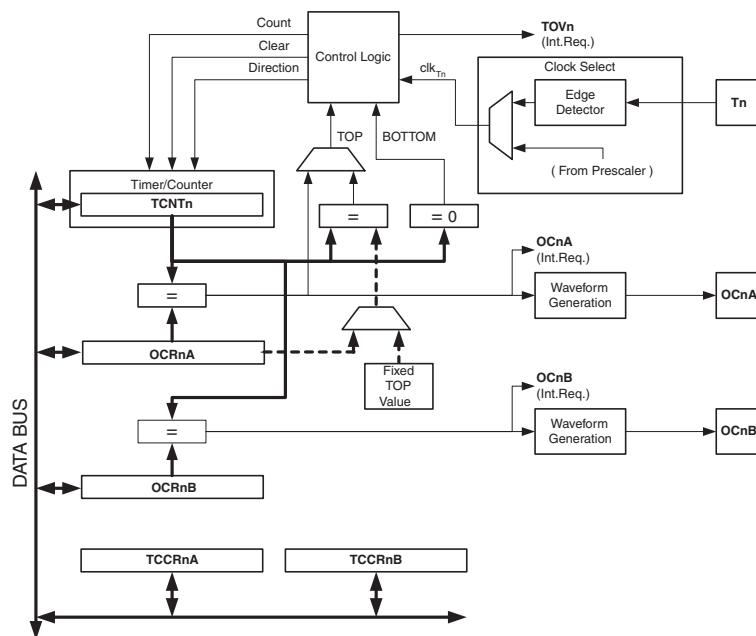
- Two Independent Output Compare Units
- Double Buffered Output Compare Registers
- Clear Timer on Compare Match (Auto Reload)
- Glitch Free, Phase Correct Pulse Width Modulator (PWM)
- Variable PWM Period
- Frequency Generator
- Three Independent Interrupt Sources (TOV0, OCF0A, and OCF0B)

### 16.2 Overview

Timer/Counter0 is a general purpose 8-bit Timer/Counter module, with two independent Output Compare Units, and with PWM support. It allows accurate program execution timing (event management) and wave generation.

A simplified block diagram of the 8-bit Timer/Counter is shown in [Figure 16-1](#). For the actual placement of I/O pins, refer to “[TQFP-pinout ATmega640/1280/2560](#)” on page 2. CPU accessible I/O Registers, including I/O bits and I/O pins, are shown in bold. The device-specific I/O Register and bit locations are listed in the “[Register Description](#)” on page 129.

**Figure 16-1.** 8-bit Timer/Counter Block Diagram



#### 16.2.1 Registers

The Timer/Counter (TCNT0) and Output Compare Registers (OCR0A and OCR0B) are 8-bit registers. Interrupt request (abbreviated to Int.Req. in the figure) signals are all visible in the Timer Interrupt Flag Register (TIFR0). All interrupts are individually masked with the Timer Interrupt Mask Register (TIMSK0). TIFR0 and TIMSK0 are not shown in the figure.

The Timer/Counter can be clocked internally, via the prescaler, or by an external clock source on the T0 pin. The Clock Select logic block controls which clock source and edge the Timer/Counter

## 18. Timer/Counter 0, 1, 3, 4, and 5 Prescaler

Timer/Counter 0, 1, 3, 4, and 5 share the same prescaler module, but the Timer/Counters can have different prescaler settings. The description below applies to all Timer/Counters.  $T_n$  is used as a general name,  $n = 0, 1, 3, 4$ , or 5.

### 18.1 Internal Clock Source

The Timer/Counter can be clocked directly by the system clock (by setting the CSn2:0 = 1). This provides the fastest operation, with a maximum Timer/Counter clock frequency equal to system clock frequency ( $f_{CLK\_I/O}$ ). Alternatively, one of four taps from the prescaler can be used as a clock source. The prescaled clock has a frequency of either  $f_{CLK\_I/O}/8$ ,  $f_{CLK\_I/O}/64$ ,  $f_{CLK\_I/O}/256$ , or  $f_{CLK\_I/O}/1024$ .

### 18.2 Prescaler Reset

The prescaler is free running, that is, operates independently of the Clock Select logic of the Timer/Counter, and it is shared by the Timer/Counter  $T_n$ . Since the prescaler is not affected by the Timer/Counter's clock select, the state of the prescaler will have implications for situations where a prescaled clock is used. One example of prescaling artifacts occurs when the timer is enabled and clocked by the prescaler (6 > CSn2:0 > 1). The number of system clock cycles from when the timer is enabled to the first count occurs can be from 1 to  $N+1$  system clock cycles, where  $N$  equals the prescaler divisor (8, 64, 256, or 1024).

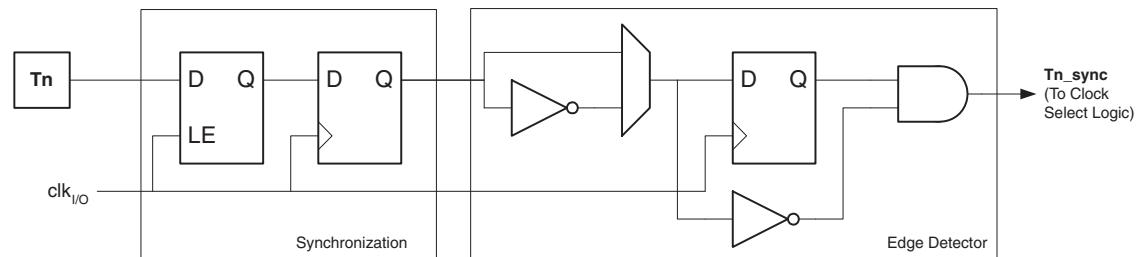
It is possible to use the prescaler reset for synchronizing the Timer/Counter to program execution. However, care must be taken if the other Timer/Counter that shares the same prescaler also uses prescaling. A prescaler reset will affect the prescaler period for all Timer/Counters it is connected to.

### 18.3 External Clock Source

An external clock source applied to the  $T_n$  pin can be used as Timer/Counter clock ( $clk_{T_n}$ ). The  $T_n$  pin is sampled once every system clock cycle by the pin synchronization logic. The synchronized (sampled) signal is then passed through the edge detector. [Figure 18-1](#) shows a functional equivalent block diagram of the  $T_n$  synchronization and edge detector logic. The registers are clocked at the positive edge of the internal system clock ( $clk_{I/O}$ ). The latch is transparent in the high period of the internal system clock.

The edge detector generates one  $clk_{T_n}$  pulse for each positive (CSn2:0 = 7) or negative (CSn2:0 = 6) edge it detects.

**Figure 18-1.**  $T_n/T_0$  Pin Sampling



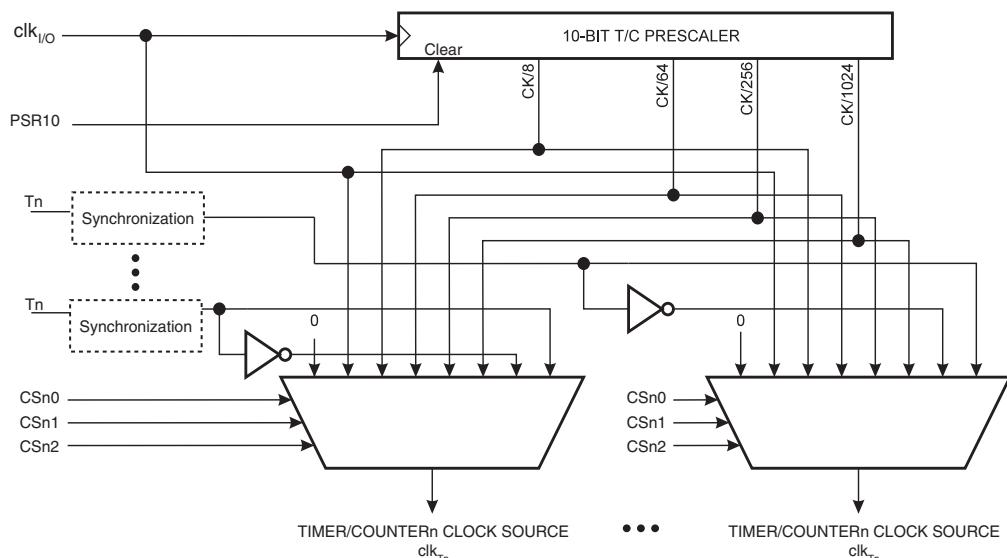
The synchronization and edge detector logic introduces a delay of 2.5 to 3.5 system clock cycles from an edge has been applied to the Tn pin to the counter is updated.

Enabling and disabling of the clock input must be done when Tn has been stable for at least one system clock cycle, otherwise it is a risk that a false Timer/Counter clock pulse is generated.

Each half period of the external clock applied must be longer than one system clock cycle to ensure correct sampling. The external clock must be guaranteed to have less than half the system clock frequency ( $f_{ExtClk} < f_{clk\_I/O}/2$ ) given a 50/50% duty cycle. Since the edge detector uses sampling, the maximum frequency of an external clock it can detect is half the sampling frequency (Nyquist sampling theorem). However, due to variation of the system clock frequency and duty cycle caused by Oscillator source (crystal, resonator, and capacitors) tolerances, it is recommended that maximum frequency of an external clock source is less than  $f_{clk\_I/O}/2.5$ .

An external clock source can not be prescaled.

**Figure 18-2.** Prescaler for synchronous Timer/Counters



## 18.4 Register Description

### 18.4.1 GTCCR – General Timer/Counter Control Register

Bit	7	6	5	4	3	2	1	0	
0x23 (0x43)	TSM	-	-	-	-	-	PSRASY	PSRSYNC	GTCCR
Read/Write	R/W	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – TSM: Timer/Counter Synchronization Mode**

Writing the TSM bit to one activates the Timer/Counter Synchronization mode. In this mode, the value that is written to the PSRASY and PSRSYNC bits is kept, hence keeping the corresponding prescaler reset signals asserted. This ensures that the corresponding Timer/Counters are halted and can be configured to the same value without the risk of one of them advancing during configuration. When the TSM bit is written to zero, the PSRASY and PSRSYNC bits are cleared by hardware, and the Timer/Counters start counting simultaneously.

## 20. 8-bit Timer/Counter2 with PWM and Asynchronous Operation

Timer/Counter2 is a general purpose, single channel, 8-bit Timer/Counter module. The main features are:

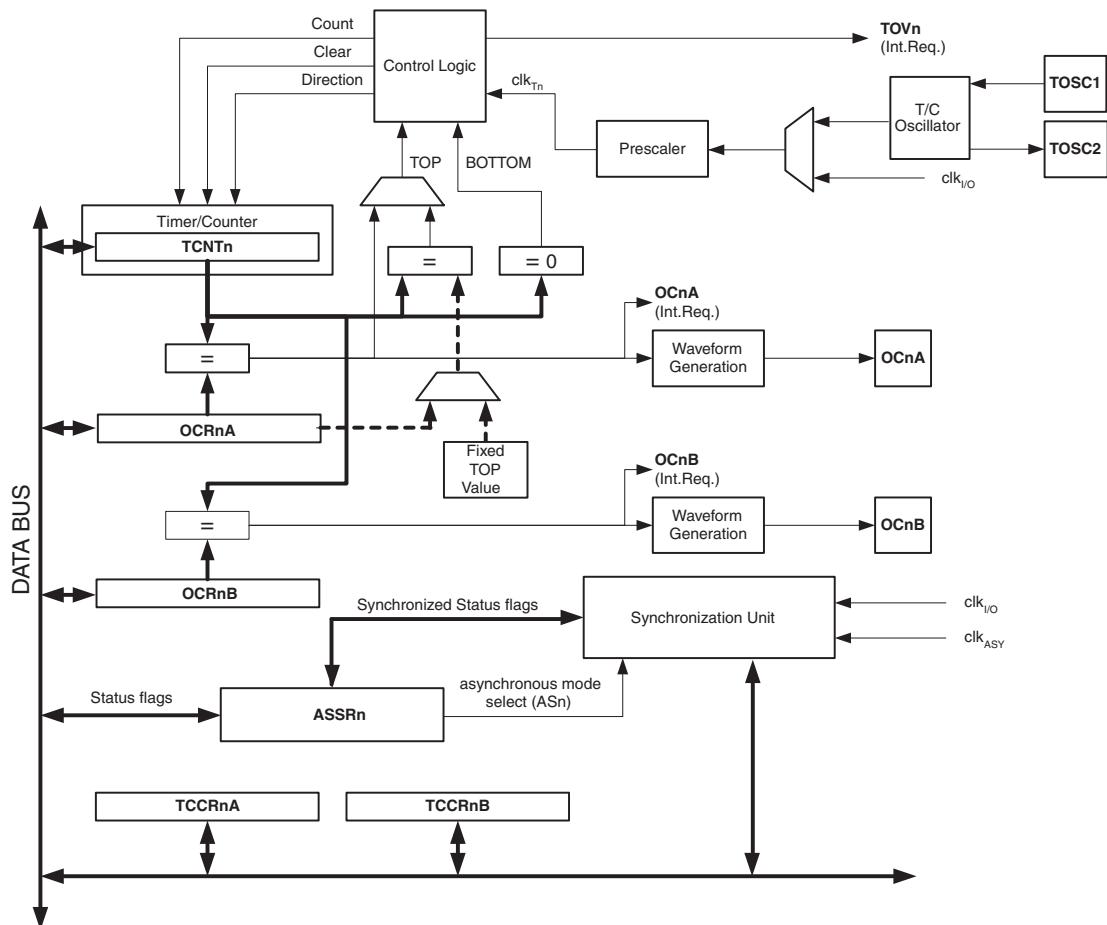
- Single Channel Counter
- Clear Timer on Compare Match (Auto Reload)
- Glitch-free, Phase Correct Pulse Width Modulator (PWM)
- Frequency Generator
- 10-bit Clock Prescaler
- Overflow and Compare Match Interrupt Sources (TOV2, OCF2A and OCF2B)
- Allows Clocking from External 32kHz Watch Crystal Independent of the I/O Clock

### 20.1 Overview

A simplified block diagram of the 8-bit Timer/Counter is shown in [Figure 17-12](#). For the actual placement of I/O pins, see “[Pin Configurations](#)” on page 2. CPU accessible I/O Registers, including I/O bits and I/O pins, are shown in bold. The device-specific I/O Register and bit locations are listed in the “[Register Description](#)” on page 187.

The Power Reduction Timer/Counter2 bit, PRTIM2, in “[PRR0 – Power Reduction Register 0](#)” on page 56 must be written to zero to enable Timer/Counter2 module.

**Figure 20-1.** 8-bit Timer/Counter Block Diagram

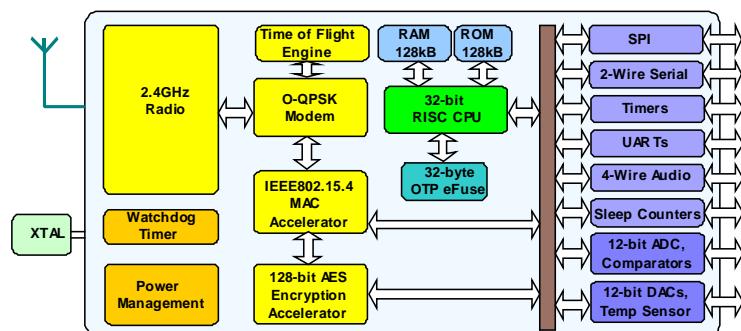


### Overview

The JN5148-001 is an ultra low power, high performance wireless microcontroller targeted at JenNet and ZigBee PRO networking applications. The device features an enhanced 32-bit RISC processor offering high coding efficiency through variable width instructions, a multi-stage instruction pipeline and low power operation with programmable clock speeds. It also includes a 2.4GHz IEEE802.15.4 compliant transceiver, 128kB of ROM, 128kB of RAM, and a rich mix of analogue and digital peripherals. The large memory footprint allows the device to run both a network stack (e.g. ZigBee PRO) and an embedded application or in a co-processor mode. The operating current is below 18mA, allowing operation direct from a coin cell.

Enhanced peripherals include low power pulse counters running in sleep mode designed for pulse counting in AMR applications and a unique Time of Flight ranging engine, allowing accurate location services to be implemented on wireless sensor networks. It also includes a 4-wire I<sup>2</sup>S audio interface, to interface directly to mainstream audio CODECs, as well as conventional MCU peripherals.

### Block Diagram



Benefits
<ul style="list-style-type: none"> <li>Single chip integrates transceiver and microcontroller for wireless sensor networks</li> <li>Large memory footprint to run ZigBee PRO or JenNet together with an application</li> <li>Very low current solution for long battery life</li> <li>Highly featured 32-bit RISC CPU for high performance and low power</li> <li>System BOM is low in component count and cost</li> <li>Extensive user peripherals</li> </ul>

Applications
<ul style="list-style-type: none"> <li>Robust and secure low power wireless applications</li> <li>ZigBee PRO and JenNet networks</li> <li>Smart metering (e.g. AMR)</li> <li>Home and commercial building automation</li> <li>Location Aware services – e.g. Asset Tracking</li> <li>Industrial systems</li> <li>Telemetry</li> <li>Remote Control</li> <li>Toys and gaming peripherals</li> </ul>

### Features: Transceiver

- 2.4GHz IEEE802.15.4 compliant
- Time of Flight ranging engine
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- 500 & 667kbps data rate modes
- Integrated sleep oscillator for low power
- On chip power regulation for 2.0V to 3.6V battery operation
- Deep sleep current 100nA
- Sleep current with active sleep timer 1.25µA
- <\$0.50 external component cost
- Rx current 17.5mA
- Tx current 15.0mA
- Receiver sensitivity -95dBm
- Transmit power 2.5dBm

### Features: Microcontroller

- Low power 32-bit RISC CPU, 4 to 32MHz clock speed
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- 128kB ROM and 128kB RAM for bootloaded program code & data
- JTAG debug interface
- 4-input 12-bit ADC, 2 12-bit DACs, 2 comparators
- 3 application timer/counters, 2 UARTs
- SPI port with 5 selects
- 2-wire serial interface
- 4-wire digital audio interface
- Watchdog timer
- Low power pulse counters
- Up to 21 DIO

**Industrial temp (-40°C to +85°C)**

**8x8mm 56-lead Punched QFN**

**Lead-free and RoHS compliant**

# 1 Introduction

The JN5148-001 is an IEEE802.15.4 wireless microcontroller that provides a fully integrated solution for applications using the IEEE802.15.4 standard in the 2.4 - 2.5GHz ISM frequency band [1], including JenNet and ZigBee PRO. It includes all of the functionality required to meet the IEEE802.15.4, JenNet and ZigBee PRO specifications and has additional processor capability to run a wide range of applications including, but not limited to Smart Energy, Automatic Meter Reading, Remote Control, Home and Building Automation, Toys and Gaming.

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimise this complexity, NXP provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN5148. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, the register details of the JN5148 are not provided in the datasheet.

The device includes a Wireless Transceiver, RISC CPU, on chip memory and an extensive range of peripherals.

Hereafter, the JN5148-001 will be referred to as JN5148.

## 1.1 Wireless Transceiver

The Wireless Transceiver comprises a 2.45GHz radio, a modem, a baseband controller and a security coprocessor. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realised very easily. Appendix B.4, describes a complete reference design including Printed Circuit Board (PCB) design and Bill Of Materials (BOM).

The security coprocessor provides hardware-based 128-bit AES-CCM\* modes as specified by the IEEE802.15.4 2006 standard. Specifically this includes encryption and authentication covered by the MIC –32/ -64/ -128, ENC and ENC-MIC –32/ -64/ -128 modes of operation.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 Medium Access Control (MAC) under the control of a protocol stack. Applications incorporating IEEE802.15.4 functionality can be rapidly developed by combining user-developed application software with a protocol stack library.

## 1.2 RISC CPU and Memory

A 32-bit RISC CPU allows software to be run on chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN5148 has a unified memory architecture, code memory, data memory, peripheral devices and I/O ports are organised within the same linear address space. The device contains 128kbytes of ROM, 128kbytes of RAM and a 32-byte One Time Programmable (OTP) eFuse memory.

---

## 1.3 Peripherals

The following peripherals are available on chip:

- Master SPI port with five select outputs
- Two UARTs with support for hardware or software flow control
- Three programmable Timer/Counters – all three support Pulse Width Modulation (PWM) capability, two have capture/compare facility
- Two programmable Sleep Timers and a Tick Timer
- Two-wire serial interface (compatible with SMBus and I<sup>2</sup>C) supporting master and slave operation
- Four-wire digital audio interface (compatible with I<sup>2</sup>S)
- Slave SPI port for Intelligent peripheral mode (shared with digital I/O)
- Twenty-one digital I/O lines (multiplexed with peripherals such as timers and UARTs)
- Four channel, 12-bit, Analogue to Digital converter
- Two 12-bit Digital to Analogue converters
- Two programmable analogue comparators
- Internal temperature sensor and battery monitor
- Time Of Flight ranging engine
- Two low power pulse counters
- Random number generator
- Watchdog Timer and Voltage Brown-out
- Sample FIFO for digital audio interface or ADC/DAC
- JTAG hardware debug port

User applications access the peripherals using the Integrated Peripherals API. This allows applications to use a tested and easily understood view of the peripherals allowing rapid system development.

## 1.4 Block Diagram

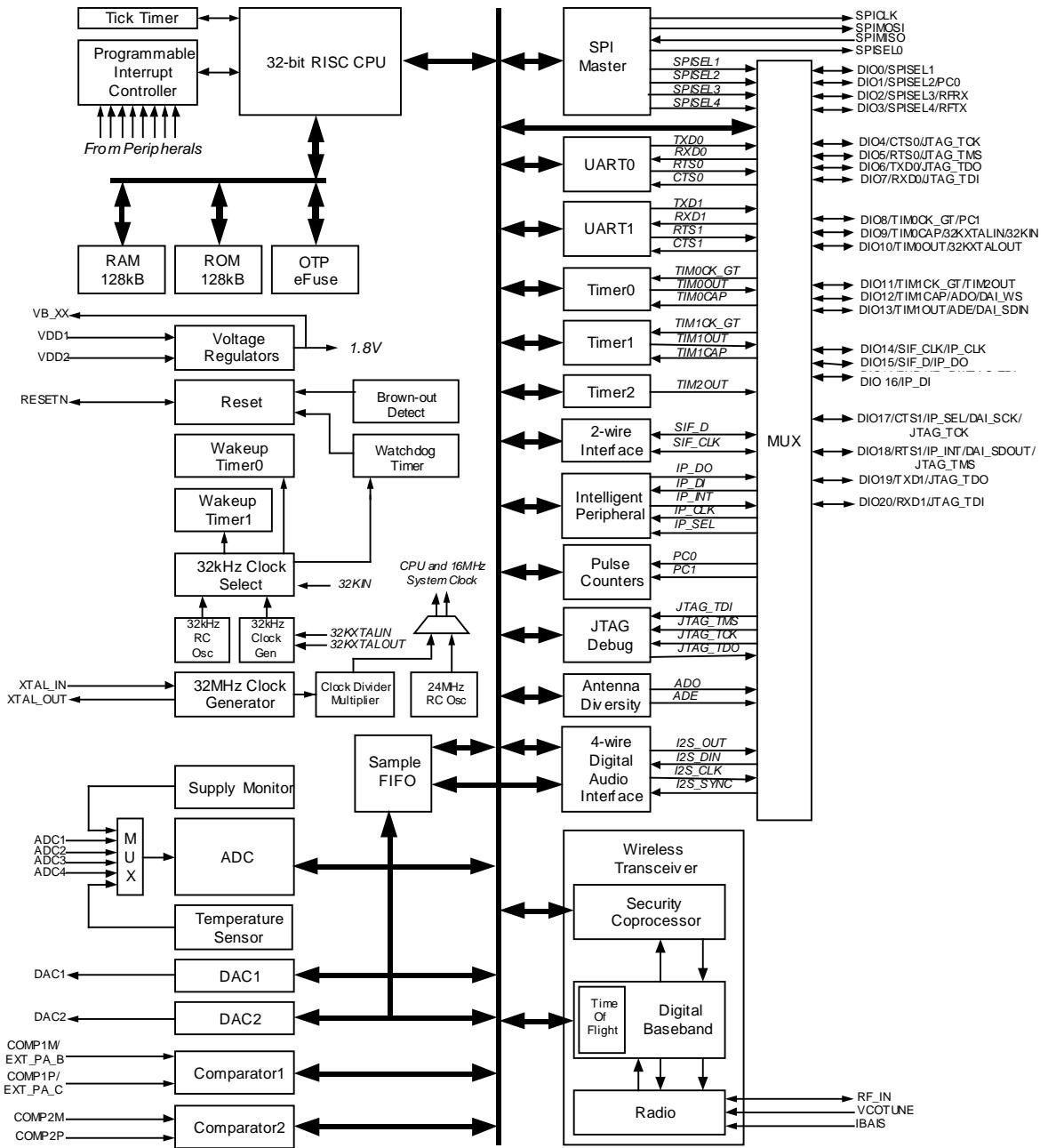


Figure 1: JN5148 Block Diagram

## 2 Pin Configurations

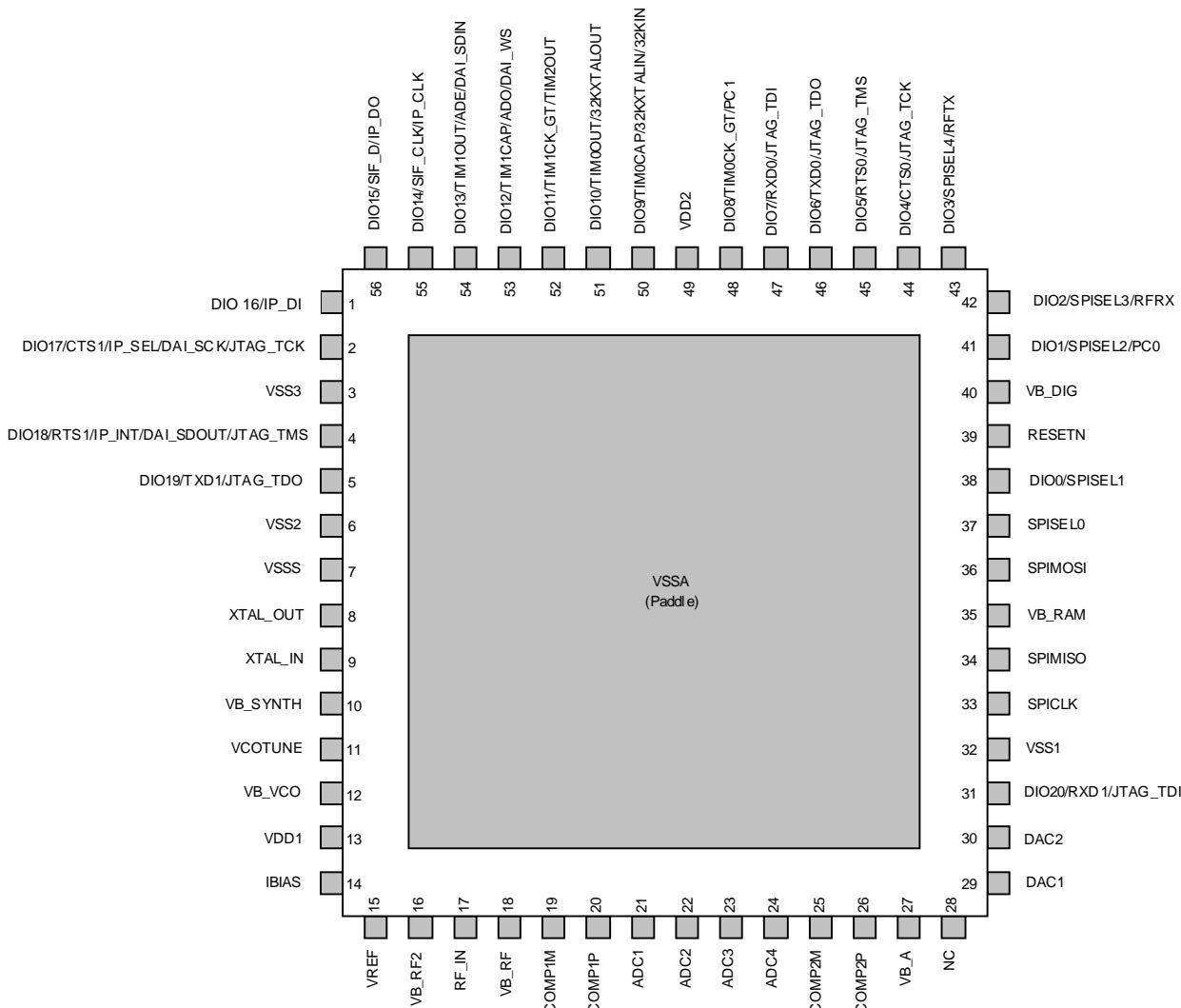


Figure 2: 56-pin QFN Configuration (top view)



**Note:** Please refer to Appendix B.4 JN5148 Module Reference Design for important applications information regarding the connection of the PADDLE to the PCB.

## 2.1 Pin Assignment

Pin No	Power supplies			Signal Type	Description	
10, 12, 16, 18, 27, 35, 40	VB_SYNTH, VB_VCO, VB_RF2, VB_RF, VB_A, VB_RAM, VB_DIG			1.8V	Regulated supply voltage	
13, 49	VDD1, VDD2			3.3V	Supplies: VDD1 for analogue, VDD2 for digital	
32, 6, 3, 7, Paddle	VSS1, VSS2, VSS3, VSSS, VSSA			0V	Grounds (see appendix A.2 for paddle details)	
28	NC				No connect	
	<b>General</b>					
39	RESETN			CMOS	Reset input	
8, 9	XTAL_OUT, XTAL_IN			1.8V	System crystal oscillator	
	<b>Radio</b>					
11	VCOTUNE			1.8V	VCO tuning RC network	
14	IBIAS			1.8V	Bias current control	
17	RF_IN			1.8V	RF antenna	
	<b>Analogue Peripheral I/O</b>					
21, 22, 23, 24	ADC1, ADC2, ADC3, ADC4			3.3V	ADC inputs	
15	VREF			1.8V	Analogue peripheral reference voltage	
29, 30	DAC1, DAC2			3.3V	DAC outputs	
19, 20	COMP1M/EXT_PA_B, COMP1P/EXT_PA_C			3.3V	Comparator 1 inputs and external PA control	
25, 26	COMP2M, COMP2P			3.3V	Comparator 2 inputs	
	<b>Digital Peripheral I/O</b>					
	Primary	Alternate Functions				
33	SPICLK			CMOS	SPI Clock Output	
36	SPIMOSI			CMOS	SPI Master Out Slave In Output	
34	SPIMISO			CMOS	SPI Master In Slave Out Input	
37	SPISEL0			CMOS	SPI Slave Select Output 0	
38	DIO0	SPISEL1		CMOS	DIO0 or SPI Slave Select Output 1	
41	DIO1	SPISEL2	PC0	CMOS	DIO1, SPI Slave Select Output 2 or Pulse Counter0 Input	
42	DIO2	SPISEL3	RFRX	CMOS	DIO2, SPI Slave Select Output 3 or Radio Receive Control Output	
43	DIO3	SPISEL4	RFTX	CMOS	DIO3, SPI Slave Select Output 4 or Radio Transmit Control Output	
44	DIO4	CTS0	JTAG_TCK	CMOS	DIO4, UART 0 Clear To Send Input or JTAG CLK	
45	DIO5	RTS0	JTAG_TMS	CMOS	DIO5, UART 0 Request To Send Output or JTAG Mode Select	
46	DIO6	TXD0	JTAG_TDO	CMOS	DIO6, UART 0 Transmit Data Output or JTAG Data Output	
47	DIO7	RXD0	JTAG_TDI	CMOS	DIO7, UART 0 Receive Data Input or JTAG Data Input	
48	DIO8	TIM0CK_GT	PC1	CMOS	DIO8, Timer0 Clock/Gate Input or Pulse Counter1 Input	
50	DIO9	TIM0CAP	32KXTALIN	32KIN	CMOS	DIO9, Timer0 Capture Input, 32K External Crystal Input or 32K Clock Input

Pin No	Digital Peripheral I/O					Signal Type	Description
	Primary	Alternate Functions					
51	DIO10	TIM0OUT	32KXTALOUT			CMOS	DIO10, Timer0 PWM Output or 32K External Crystal Output
52	DIO11	TIM1CK_GT	TIM2OUT			CMOS	DIO11, Timer1 Clock/Gate Input or Timer2 PWM Output
53	DIO12	TIM1CAP	ADO	DAI_WS		CMOS	DIO12, Timer1 Capture Input, Antenna Diversity or Digital Audio Word Select
54	DIO13	TIM1OUT	ADE	DAI_SDIN		CMOS	DIO13, Timer1 PWM Output, Antenna Diversity or Digital Audio Data Input
55	DIO14	SIF_CLK	IP_CLK			CMOS	DIO14, Serial Interface Clock or Intelligent Peripheral Clock Input
56	DIO15	SIF_D	IP_DO			CMOS	DIO15, Serial Interface Data or Intelligent Peripheral Data Out
1	DIO16	IP_DI				CMOS	DIO16 or Intelligent Peripheral Data In
2	DIO17	CTS1	IP_SEL	DAI_SCK	JTAG_TCK	CMOS	DIO17, UART 1 Clear To Send Input, Intelligent Peripheral Device Select Input or Digital Audio Clock or JTAG CLK
4	DIO18	RTS1	IP_INT	DAI_SDOUT	JTAG_TMS	CMOS	DIO18, UART 1 Request To Send Output, Intelligent Peripheral Interrupt Output or Digital Audio Data Output or JTAG Mode Select
5	DIO19	TXD1			JTAG_TDO	CMOS	DIO19 or UART 1 Transmit Data Output or JTAG Data Out
31	DIO 20	RXD1			JTAG_TDI	CMOS	DIO 20, UART 1 Receive Data Input or JTAG data In



The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5148 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

## 3 CPU

The CPU of the JN5148 is a 32-bit load and store RISC processor. It has been architected for three key requirements:

- Low power consumption for battery powered applications
- High performance to implement a wireless protocol at the same time as complex applications
- Efficient coding of high-level languages such as C provided with the NXP Software Developer's Kit

It features a linear 32-bit logical address space with unified memory architecture, accessing both code and data in the same address space. Registers for peripheral units, such as the timers, UARTs and the baseband processor are also mapped into this space.

The CPU has access to a block of 15 32-bit General-Purpose (GP) registers together with a small number of special purpose registers which are used to store processor state and control interrupt handling. The contents of any GP register can be loaded from or stored to memory, while arithmetic and logical operations, shift and rotate operations, and signed and unsigned comparisons can be performed either between two registers and stored in a third, or between registers and a constant carried in the instruction. Operations between general or special-purpose registers execute in one cycle while those that access memory require a further cycle to allow the memory to respond.

The instruction set manipulates 8, 16 and 32-bit data; this means that programs can use objects of these sizes very efficiently. Manipulation of 32-bit quantities is particularly useful for protocols and high-end applications allowing algorithms to be implemented in fewer instructions than on smaller word-size processors, and to execute in fewer clock cycles. In addition, the CPU supports hardware Multiply that can be used to efficiently implement algorithms needed by Digital Signal Processing applications.

The instruction set is designed for the efficient implementation of high-level languages such as C. Access to fields in complex data structures is very efficient due to the provision of several addressing modes, together with the ability to be able to use any of the GP registers to contain the address of objects. Subroutine parameter passing is also made more efficient by using GP registers rather than pushing objects onto the stack. The recommended programming method for the JN5148 is by using C, which is supported by a software developer kit comprising a C compiler, linker and debugger.

The CPU architecture also contains features that make the processor suitable for embedded, real-time applications. In some applications, it may be necessary to use a real-time operating system to allow multiple tasks to run on the processor. To provide protection for device-wide resources being altered by one task and affecting another, the processor can run in either supervisor or user mode, the former allowing access to all processor registers, while the latter only allows the GP registers to be manipulated. Supervisor mode is entered on reset or interrupt; tasks starting up would normally run in user mode in a RTOS environment.

Embedded applications require efficient handling of external hardware events. When using JenOS, prioritised interrupts are supported, with 15 priority levels, and can be configured as required by the application.

To improve power consumption a number of power-saving modes are implemented in the JN5148, described more fully in section 21 - Power Management and Sleep Modes. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on an interrupt it will wake up to service the request. Additionally, it is possible under software control, to set the speed of the CPU to 4, 8, 16 or 32MHz. This feature can be used to trade-off processing power against current consumption.

## 4 Memory Organisation

This section describes the different memories found within the JN5148. The device contains ROM, RAM, OTP eFuse memory, the wireless transceiver and peripherals all within the same linear address space.

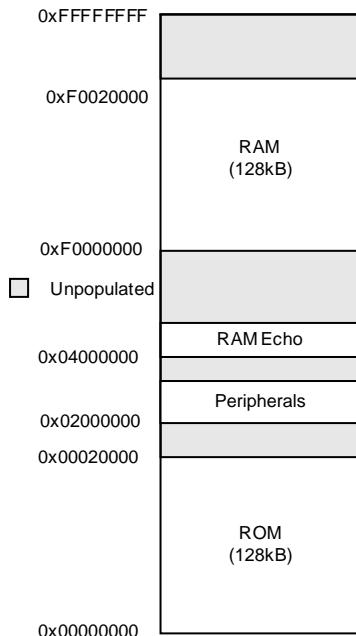


Figure 5: JN5148 Memory Map

### 4.1 ROM

The ROM is 128k bytes in size, and can be accessed by the processor in a single CPU clock cycle. The ROM contents include bootloader to allow external Flash memory contents to be booted into RAM at runtime, a default interrupt vector table, an interrupt manager, IEEE802.15.4 MAC and APIs for interfacing on-chip peripherals. The operation of the boot loader is described in detail in Application Note [7]. The interrupt manager routes interrupt calls to the application's soft interrupt vector table contained within RAM. Section 7 contains further information regarding the handling of interrupts. ROM contents are shown in Figure 6.

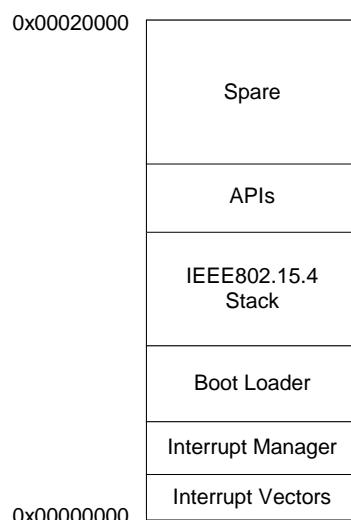


Figure 6: Typical ROM contents

## 4.2 RAM

The JN5148 contains 128kBytes of high speed RAM. It can be used for both code and data storage and is accessed by the CPU in a single clock cycle. At reset, a boot loader controls the loading of segments of code and data from an external memory connected to the SPI port, into RAM. Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are un-powered. Typical RAM contents are shown in Figure 7.

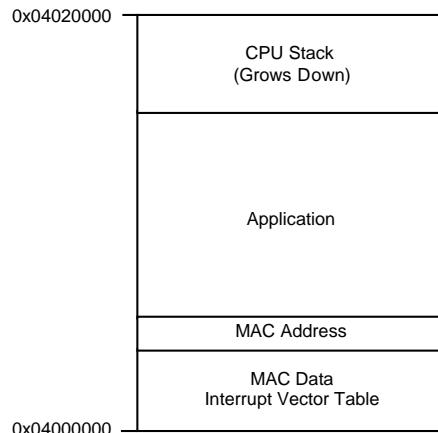


Figure 7: Typical RAM Contents

## 4.3 OTP eFuse Memory

The JN5148 contains a total of 32bytes of eFuse memory; this is a One Time Programmable (OTP) memory that can be used to support on chip 64-bit MAC ID and a 128-bit AES security key. A limited number of bits are available for customer use for storage of configuration information; configuration of these is made through use of software APIs.

For further information on how to program and use the eFuse memory, please contact technical support via the on-line tech-support system.

Alternatively, NXP can provide an eFuse programming service for customers that wish to use the eFuse but do not wish to undertake this for themselves. For further details of this service, please contact your local NXP sales office.

## 4.4 External Memory

An external memory with an SPI interface may be used to provide storage for program code and data for the device when external power is removed. The memory is connected to the SPI interface using select line SPISEL0; this select line is dedicated to the external memory interface and is not available for use with other external devices. See Figure 8 for connection details.

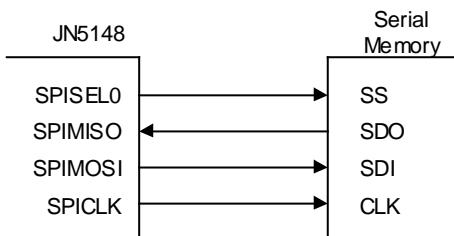


Figure 8: Connecting External Serial Memory

At reset, the contents of this memory are copied into RAM by the software boot loader. The Flash memory devices that are supported as standard through the JN5148 bootloader are given in Table 1. NXP recommends that where possible one of these devices should be selected.

Manufacturer	Device Number
SST (Silicon Storage Technology)	25VF010A (1Mbit device)
Numonyx	M25P10-A (1Mbit device), M25P40 (4Mbit device)

**Table 1: Supported Flash Memories**

Applications wishing to use an alternate Flash memory device should refer to application note [2] JN-AN-1038 Programming Flash devices not supported by the JN51xx ROM-based bootloader. This application note provides guidance on developing an interface to an alternate device.

#### 4.4.1 External Memory Encryption

The contents of the external serial memory may be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in eFuse.

When bootloading program code from external serial memory, the JN5148 automatically accesses the encryption key to execute the decryption process. User program code does not need to handle any of the decryption process; it is transparent.

With encryption enabled, the time taken to boot code from external flash is increased.

### 4.5 Peripherals

All peripherals have their registers mapped into the memory space. Access to these registers requires 3 clock cycles. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see the JN51xx Integrated Peripherals API User Guide (JN-UG-3066)[5].

### 4.6 Unused Memory Addresses

Any attempt to access an unpopulated memory area will result in a bus error exception (interrupt) being generated.

# 8 Wireless Transceiver

The wireless transceiver comprises a 2.45GHz radio, modem, a baseband processor, a security coprocessor and PHY controller. These blocks, with protocol software provided as a library, implement an IEEE802.15.4 standards-based wireless transceiver that transmits and receives data over the air in the unlicensed 2.4GHz band.

## 8.1 Radio

Figure 14 shows the single ended radio architecture.

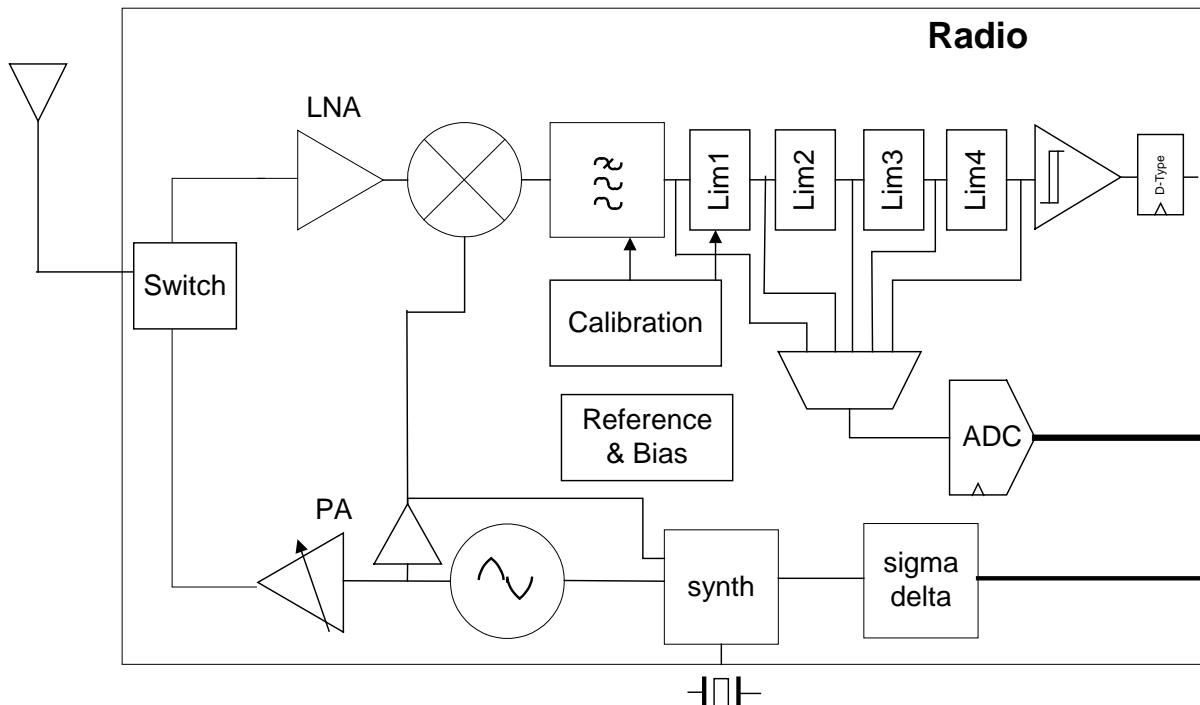


Figure 14: Radio Architecture

The radio comprises a low-IF receive path and a direct modulation transmit path, which converge at the TX/RX switch. The switch connects to the external single ended matching network, which consists of two inductors and a capacitor, this arrangement creates a 50Ω port and removes the need for a balun. A 50Ω single ended antenna can be connected directly to this port.

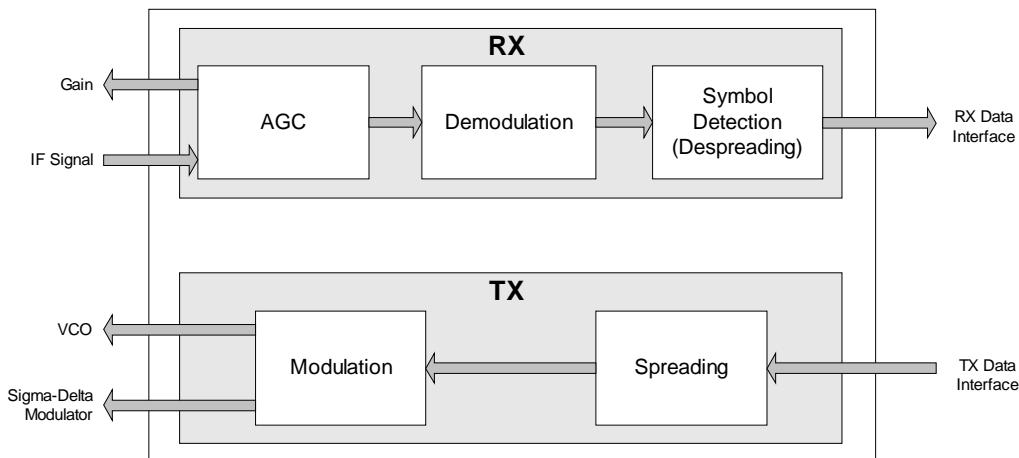
The 32MHz crystal oscillator feeds a divider, which provides the frequency synthesiser with a reference frequency. The synthesiser contains programmable feedback dividers, phase detector, charge pump and internal Voltage Controlled Oscillator (VCO). The VCO has no external components, and includes calibration circuitry to compensate for differences in internal component values due to process and temperature variations. The VCO is controlled by a Phase Locked Loop (PLL) that has an internal loop filter. A programmable charge pump is also used to tune the loop characteristic.

The receiver chain starts with the low noise amplifier / mixer combination whose outputs are passed to a lowpass filter, which provides the channel definition. The signal is then passed to a series of amplifier blocks forming a limiting strip. The signal is converted to a digital signal before being passed to the Modem. The gain control for the RX path is derived in the automatic gain control (AGC) block within the Modem, which samples the signal level at various points down the RX chain. To improve the performance and reduce current consumption, automatic calibration is applied to various blocks in the RX path.

In the transmit direction, the digital stream from the Modem is passed to a digital sigma-delta modulator which controls the feedback dividers in the synthesiser, (dual point modulation). The VCO frequency now tracks the applied modulation. The 2.4 GHz signal from the VCO is then passed to the RF Power Amplifier (PA), whose power control can be selected from one of three settings. The output of the PA drives the antenna via the RX/TX switch.

## 8.2 Modem

The modem performs all the necessary modulation and spreading functions required for digital transmission and reception of data at 250kbps in the 2450MHz radio frequency band in compliance with the IEEE802.15.4 standard. It also provides a high data rate modes at 500 and 667kbps.



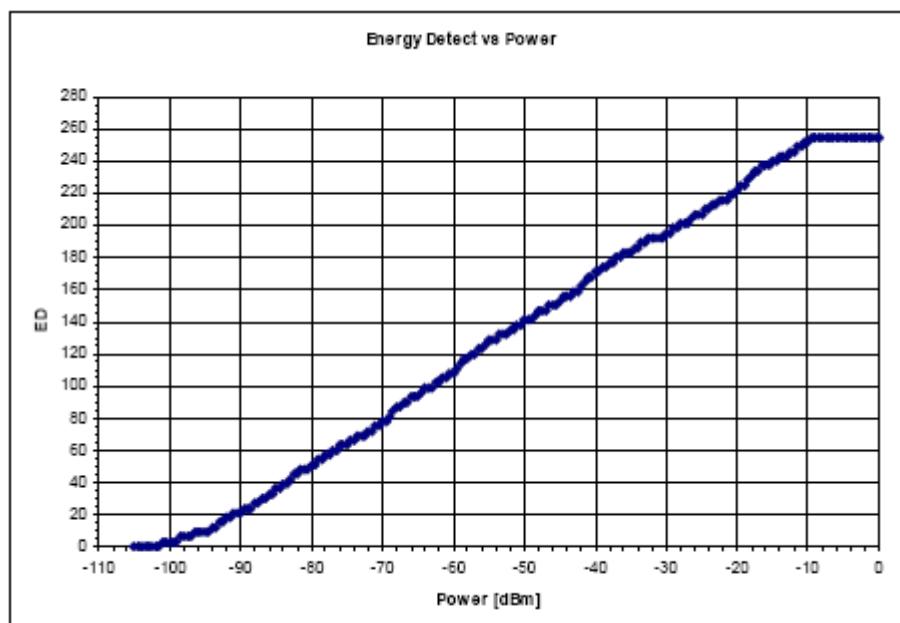
**Figure 18 Modem Architecture**

Features provided to support network channel selection algorithms include Energy Detection (ED), Link Quality Indication (LQI) and fully programmable Clear Channel Assessment (CCA).

The Modem provides a digital Receive Signal Strength Indication (RSSI) that facilitates the implementation of the IEEE 802.15.4 ED function and LQI function.

The ED and LQI are both related to receiver power in the same way, as shown in Fig19. LQI is associated with a received packet, whereas ED is an indication of signal power on air at a particular moment.

The CCA capability of the Modem supports all modes of operation defined in the IEEE 802.15.4 standard, namely Energy above ED threshold, Carrier Sense and Carrier Sense and/or energy above ED threshold.



**Figure 19 Energy Detect Value vs Receive Power Level**

## 8.3 Baseband Processor

The baseband processor provides all time-critical functions of the IEEE802.15.4 MAC layer. Dedicated hardware guarantees air interface timing is precise. The MAC layer hardware/software partitioning, enables software to implement the sequencing of events required by the protocol and to schedule timed events with millisecond resolution, and the hardware to implement specific events with microsecond timing resolution. The protocol software layer performs the higher-layer aspects of the protocol, sending management and data messages between endpoint and coordinator nodes, using the services provided by the baseband processor.

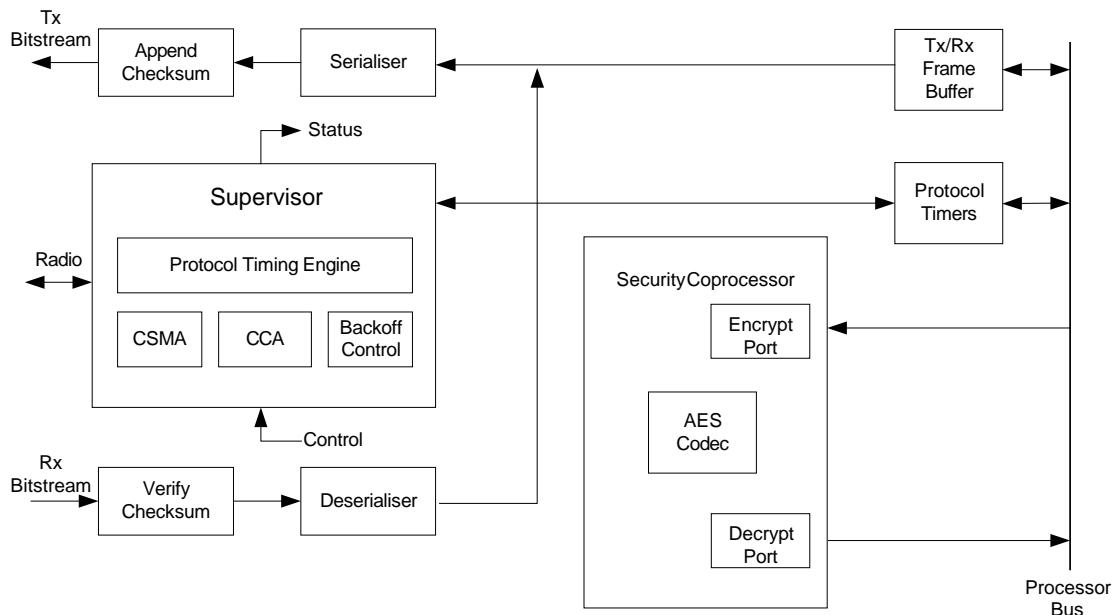


Figure 20: Baseband Processor

### 8.3.1 Transmit

A transmission is performed by software writing the data to be transferred into the Tx/Rx Frame Buffer, together with parameters such as the destination address and the number of retries allowed, and programming one of the protocol timers to indicate the time at which the frame is to be sent. This time will be determined by the software tracking the higher-layer aspects of the protocol such as superframe timing and slot boundaries. Once the packet is prepared and protocol timer set, the supervisor block controls the transmission. When the scheduled time arrives, the supervisor controls the sequencing of the radio and modem to perform the type of transmission required. It can perform all the algorithms required by IEEE802.15.4 such as CSMA/CA, GTS without processor intervention including retries and random backoffs.

When the transmission begins, the header of the frame is constructed from the parameters programmed by the software and sent with the frame data through the serialiser to the Modem. At the same time, the radio is prepared for transmission. During the passage of the bitstream to the modem, it passes through a CRC checksum generator that calculates the checksum on-the-fly, and appends it to the end of the frame.

If using slotted access, it is possible for a transmission to overrun the time in its allocated slot; the Baseband Processor handles this situation autonomously and notifies the protocol software via interrupt, rather than requiring it to handle the overrun explicitly.

### 8.3.2 Reception

During reception, the radio is set to receive on a particular channel. On receipt of data from the modem, the frame is directed into the Tx/Rx Frame Buffer where both header and frame data can be read by the protocol software. An interrupt may be provided on receipt of the frame header. As the frame data is being received from the modem it is passed through a checksum generator; at the end of the reception the checksum result is compared with the checksum at the end of the message to ensure that the data has been received correctly. An interrupt may be

provided to indicate successful packet reception. During reception, the modem determines the Link Quality, which is made available at the end of the reception as part of the requirements of IEEE802.15.4.

### 8.3.3 Auto Acknowledge

Part of the protocol allows for transmitted frames to be acknowledged by the destination sending an acknowledge packet within a very short window after the transmitted frame has been received. The JN5148 baseband processor can automatically construct and send the acknowledgement packet without processor intervention and hence avoid the protocol software being involved in time-critical processing within the acknowledge sequence. The JN5148 baseband processor can also request an acknowledge for packets being transmitted and handle the reception of acknowledged packets without processor intervention.

### 8.3.4 Beacon Generation

In beaconing networks, the baseband processor can automatically generate and send beacon frames; the repetition rate of the beacons is programmed by the CPU, and the baseband then constructs the beacon contents from data delivered by the CPU. The baseband processor schedules the beacons and transmits them without CPU intervention.

### 8.3.5 Security

The transmission and reception of secured frames using the Advanced Encryption Standard (AES) algorithm is handled by the security coprocessor and the stack software. The application software must provide the appropriate encrypt/decrypt keys for the transmission or reception. On transmission, the key can be programmed at the same time as the rest of the frame data and setup information.

## 8.4 Security Coprocessor

The security coprocessor is available to the application software to perform encryption/decryption operations. A hardware implementation of the encryption engine significantly speeds up the processing of the encrypted packets over a pure software implementation. The AES library for the JN5148 provides operations that utilise the encryption engine in the device and allow the contents of memory buffers to be transformed. Information such as the type of security operation to be performed and the encrypt/decrypt key to be used must also be provided.

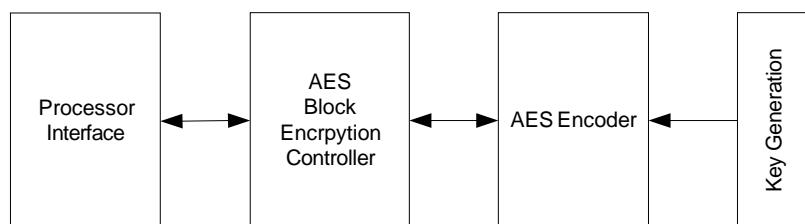


Figure 21: Security Coprocessor Architecture

## 8.5 Location Awareness

The JN5148 provides the ability for an application to obtain the Time Of Flight (TOF) between two network nodes. The TOF information is an alternative metric to that of the existing Energy Detect value (RSSI) that has been typically used for calculating the relative inter-nodal separation, for subsequent use in a location awareness system.

For short ranges RSSI will typically give a better accuracy than TOF, however for distances above 5 to 10 meters TOF will offer significant improvements in accuracy compared to RSSI. In general, the RSSI error scales with distance, such that if the distance doubles then the error doubles.

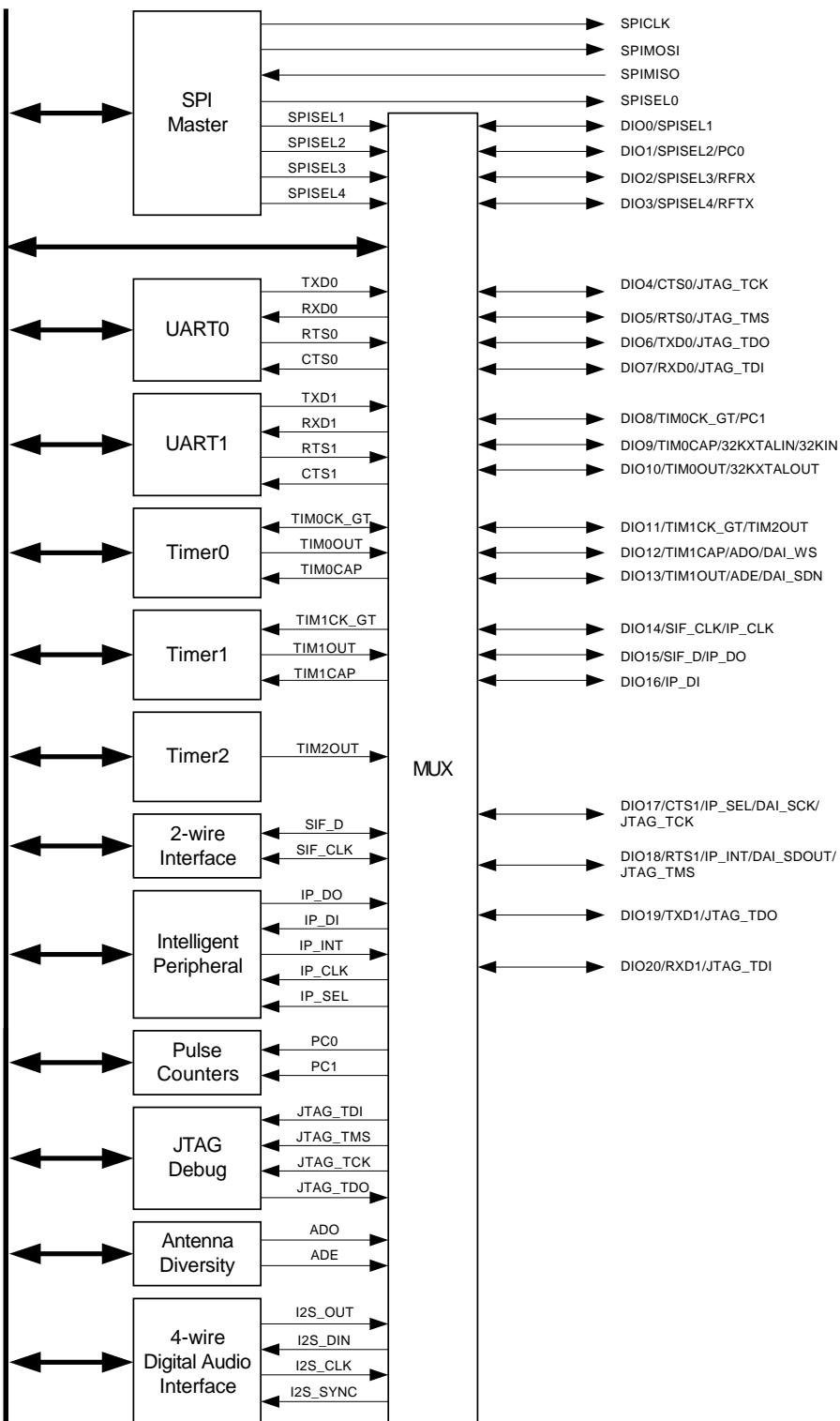


Figure 22 DIO Block Diagram

### 22.3.16 Radio Transceiver

This JN5148 meets all the requirements of the IEEE802.15.4 standard over 2.0 - 3.6V and offers the following improved RF characteristics. All RF characteristics are measured single ended.

This part also meets the following regulatory body approvals, when used with NXP's Module Reference Designs. Compliant with FCC part 15, rules, IC Canada, ETSI ETS 300-328 and Japan ARIB STD-T66



**The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5148 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.**

Parameter	Min	Typical	Max	Notes
<b>RF Port Characteristics</b>				
Type				Single Ended
Impedance <sup>1</sup>		50ohm		2.4-2.5GHz
Frequency range	2.400 GHz		2.485GHz	
ESD levels (pin 17)		TDB		

1) With external matching inductors and assuming PCB layout as in Appendix B.4.

## Radio Parameters: 2.0-3.6V, +25°C

Parameter	Min	Typical	Max	Unit	Notes
<b>Receiver Characteristics</b>					
Receive sensitivity	-92	-95		dBm	Nominal for 1% PER, as per 802.15.4 section 6.5.3.3
Maximum input signal		+5		dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection (-1/+1 ch) [CW Interferer]		19/34 [27/49]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Alternate channel rejection (-2 / +2 ch) [CW Interferer]		40/45 [54/54]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		48		dBc	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		52		dBc	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 8dB lower. (Note1)
Spurious emissions (RX)		-61	<-70 -58	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		40		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm. Available through Hardware API
<b>Transmitter Characteristics</b>					
Transmit power	+0.5	+2.5		dBm	
Output power control range		-35		dB	In three 12dB steps (Note3)
Spurious emissions (TX)		-40	<-70 <-70	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to 12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz
EVM [Offset]		10 [2.0]	15	%	At maximum output power
Transmit Power Spectral Density		-38	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, section 6.5.3.1



# LM78XX / LM78XXA

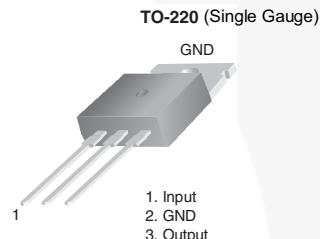
## 3-Terminal 1 A Positive Voltage Regulator

### Features

- Output Current up to 1 A
- Output Voltages: 5, 6, 8, 9, 10, 12, 15, 18, 24 V
- Thermal Overload Protection
- Short-Circuit Protection
- Output Transistor Safe Operating Area Protection

### Description

The LM78XX series of three-terminal positive regulators is available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down, and safe operating area protection. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed-voltage regulators, these devices can be used with external components for adjustable voltages and currents.



### Ordering Information<sup>(1)</sup>

Product Number	Output Voltage Tolerance	Package	Operating Temperature	Packing Method
LM7805CT	$\pm 4\%$	TO-220 (Single Gauge)	-40°C to +125°C	Rail
LM7806CT				
LM7808CT				
LM7809CT				
LM7810CT				
LM7812CT				
LM7815CT				
LM7818CT				
LM7824CT	$\pm 2\%$		0°C to +125°C	
LM7805ACT				
LM7809ACT				
LM7810ACT				
LM7812ACT				
LM7815ACT				

#### Note:

1. Above output voltage tolerance is available at 25°C.

## Block Diagram

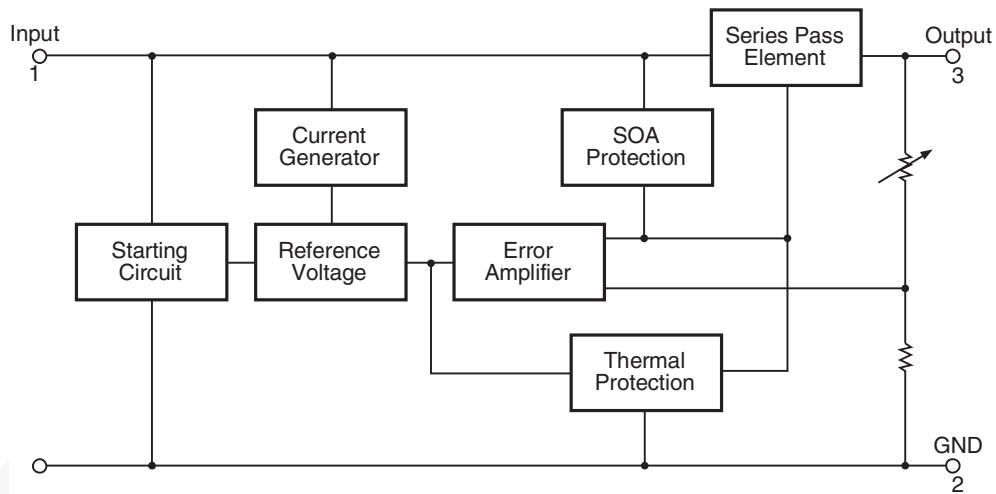


Figure 1. Block Diagram

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_I$	Input Voltage	$V_O = 5 \text{ V to } 18 \text{ V}$	V
		$V_O = 24 \text{ V}$	
$R_{\theta JC}$	Thermal Resistance, Junction-Case (TO-220)	5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-Air (TO-220)	65	$^\circ\text{C/W}$
$T_{OPR}$	Operating Temperature Range	LM78xx: -40 to +125	$^\circ\text{C}$
		LM78xxA: 0 to +125	
$T_{STG}$	Storage Temperature Range	-65 to +150	$^\circ\text{C}$

## Electrical Characteristics (LM7805)

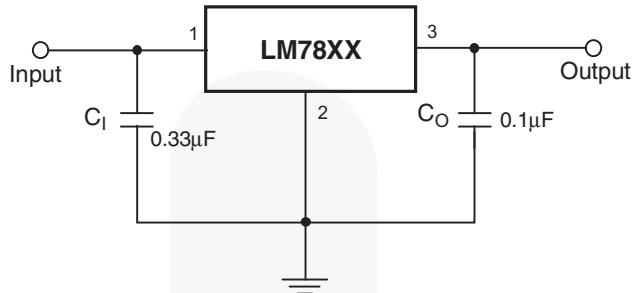
Refer to the test circuit,  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ ,  $I_O = 500 \text{ mA}$ ,  $V_I = 10 \text{ V}$ ,  $C_I = 0.1 \mu\text{F}$ , unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_O$	Output Voltage	$T_J = +25^{\circ}\text{C}$		4.80	5.00	5.20	V
		$I_O = 5 \text{ mA to } 1 \text{ A}$ , $P_O \leq 15 \text{ W}$ , $V_I = 7 \text{ V to } 20 \text{ V}$		4.75	5.00	5.25	
Regline	Line Regulation <sup>(2)</sup>	$T_J = +25^{\circ}\text{C}$	$V_I = 7 \text{ V to } 25 \text{ V}$		4.0	100.0	mV
			$V_I = 8 \text{ V to } 12 \text{ V}$		1.6	50.0	
Regload	Load Regulation <sup>(2)</sup>	$T_J = +25^{\circ}\text{C}$	$I_O = 5 \text{ mA to } 1.5 \text{ A}$		9.0	100.0	mV
			$I_O = 250 \text{ mA to } 750 \text{ mA}$		4.0	50.0	
$I_Q$	Quiescent Current	$T_J = +25^{\circ}\text{C}$			5.0	8.0	mA
$\Delta I_Q$	Quiescent Current Change	$I_O = 5 \text{ mA to } 1 \text{ A}$			0.03	0.50	mA
		$V_I = 7 \text{ V to } 25 \text{ V}$			0.30	1.30	
$\Delta V_O/\Delta T$	Output Voltage Drift <sup>(3)</sup>	$I_O = 5 \text{ mA}$			-0.8		mV/°C
$V_N$	Output Noise Voltage	$f = 10 \text{ Hz to } 100 \text{ kHz}$ , $T_A = +25^{\circ}\text{C}$			42.0		µV/ $V_O$
RR	Ripple Rejection <sup>(3)</sup>	$f = 120 \text{ Hz}$ , $V_I = 8 \text{ V to } 18 \text{ V}$		62.0	73.0		dB
$V_{DROP}$	Dropout Voltage	$T_J = +25^{\circ}\text{C}$ , $I_O = 1 \text{ A}$			2.0		V
$R_O$	Output Resistance <sup>(3)</sup>	$f = 1 \text{ kHz}$			15.0		mΩ
$I_{SC}$	Short-Circuit Current	$T_J = +25^{\circ}\text{C}$ , $V_I = 35 \text{ V}$			230		mA
$I_{PK}$	Peak Current <sup>(3)</sup>	$T_J = +25^{\circ}\text{C}$			2.2		A

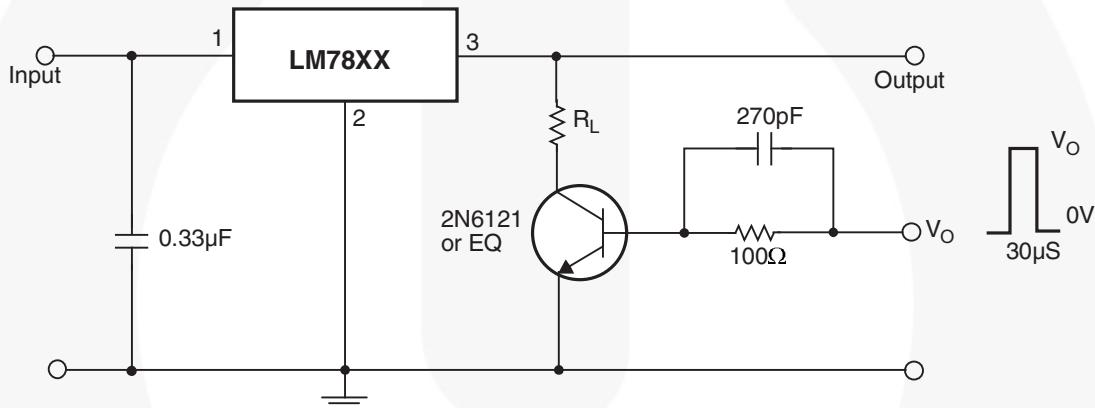
### Notes:

2. Load and line regulation are specified at constant junction temperature. Changes in  $V_O$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.
3. These parameters, although guaranteed, are not 100% tested in production.

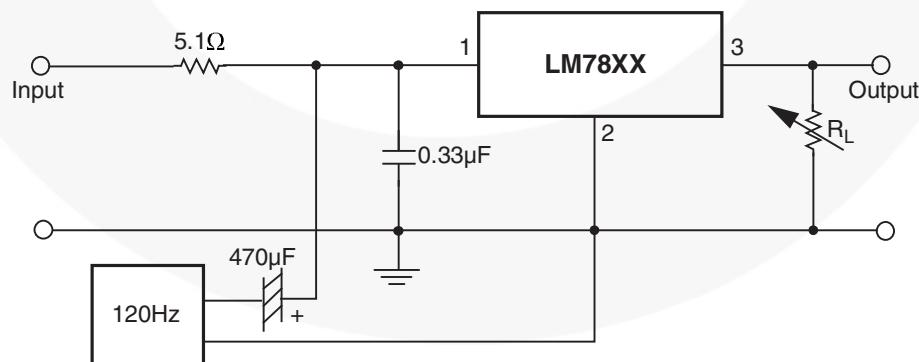
## Typical Applications



**Figure 6. DC Parameters**

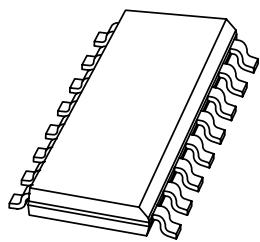


**Figure 7. Load Regulation**



**Figure 8. Ripple Rejection**

# DATA SHEET



## **KMZ52** Magnetic Field Sensor

Product specification

2000 Jun 09

# Magnetic Field Sensor

**KMZ52**

## FEATURES

- High sensitivity
- Integrated compensation coil
- Integrated set/reset coil.

## APPLICATIONS

- Navigation
- Current and earth magnetic field measurement
- Traffic detection.

## DESCRIPTION

The KMZ52 is an extremely sensitive magnetic field sensor, employing the magnetoresistive effect of thin-film permalloy. The sensor contains two magnetoresistive Wheatstone bridges physically offset from one another by 90° and integrated compensation and set/reset coils. The integrated compensation coils allow magnetic field measurement with current feedback loops to generate outputs that are independent of drift in sensitivity. The orientation of sensitivity may be set or changed (flipped) by means of the integrated set/reset coils. A short current pulse should be applied to the compensation coils to recover (set) the sensor after exposure to strong disturbing magnetic fields. A negative current pulse will reset the sensor to reversed sensitivity. By use of periodically alternated flipping pulses and a lock-in amplifier, the output is made independent of sensor and amplifier offset.

## PINNING

SYMBOL	PIN	DESCRIPTION
+I <sub>flip2</sub>	1	flip coil
V <sub>CC2</sub>	2	bridge supply voltage
GND2	3	ground
+I <sub>comp2</sub>	4	compensation coil
GND1	5	ground
+I <sub>comp1</sub>	6	compensation coil
-I <sub>comp1</sub>	7	compensation coil
-V <sub>O1</sub>	8	bridge output voltage
+V <sub>O1</sub>	9	bridge output voltage
-I <sub>flip1</sub>	10	flip coil
+I <sub>flip1</sub>	11	flip coil
V <sub>CC1</sub>	12	bridge supply voltage
-I <sub>comp2</sub>	13	compensation coil
-V <sub>O2</sub>	14	bridge output voltage
+V <sub>O2</sub>	15	bridge output voltage
-I <sub>flip2</sub>	16	flip coil

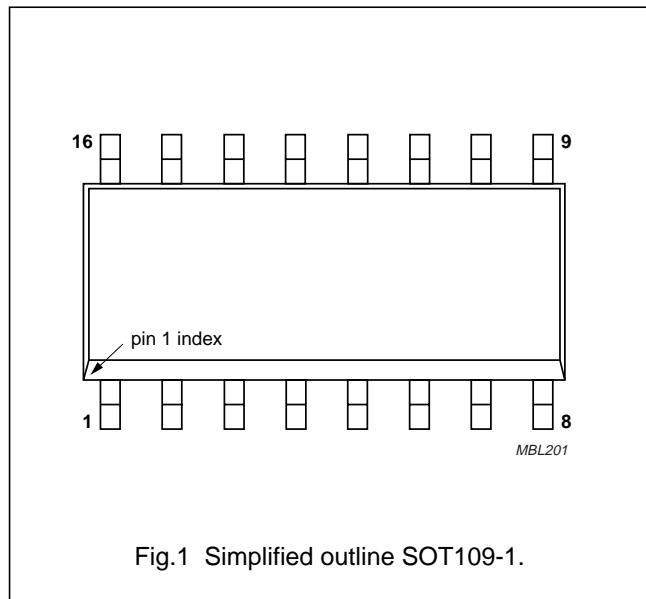


Fig.1 Simplified outline SOT109-1.

# Magnetic Field Sensor

KMZ52

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	bridge supply voltage	–	5	8	V
S	sensitivity (uncompensated)	12	16	–	$\frac{mV/V}{kA/m}$
$V_{offset}$	offset voltage per supply voltage	–1.5	0	+1.5	mV/V
$R_{bridge}$	bridge resistance	1	2	3	k $\Omega$
$R_{comp}$	compensation coil resistance	100	170	300	$\Omega$
$A_{comp}$	field factor of compensation coil; note 1	19	22	25	$\frac{A/m}{mA}$
$R_{flip}$	resistance of set/reset coil	1	2	3	$\Omega$
$I_{flip}$	recommended flipping current for stable operation; note 2	±800	±1000	±1200	mA
$t_{flip}$	flip pulse duration; note 2	1	3	100	$\mu s$

### Notes

1. The compensation coil generates a field  $H_{comp} = A_{comp} \times I_{comp}$  in addition to the external field  $H_{ext}$ . Sensor output will become zero if  $H_{ext} = H_{comp}$ .
2. Average power consumption of the flipping coil, defined by current, pulse duration and pulse repetition rate may not exceed the specified limit, see Chapter "Limiting values".

## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{CC}$	bridge supply voltage	–	8	V
$P_{tot}$	total power dissipation	–	130	mW
$T_{stg}$	storage temperature	–65	+150	°C
$T_{amb}$	maximum operating temperature	–40	–125	°C
$I_{comp}$	maximum compensation current	–	15	mA
$I_{flip (max)}$	maximum flipping current	–	1500	mA
$P_{flip (max)}$	maximum flipping power dissipation	–	50	mW
$V_{isol}$	voltage between isolated systems: flip coil and Wheatstone bridge; compensation coil and Wheatsone bridge; flip coil and compensation coil	–	60	V

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th j-a}$	terminal resistance from junction to ambient	105	K/W

## Magnetic Field Sensor

KMZ52

## CHARACTERISTICS

 $T_{\text{bridge}} = 25^\circ\text{C}$ ;  $V_{\text{CC}1} = V_{\text{CC}2} = 5 \text{ V}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{CC}}$	bridge supply voltage	note 1	–	5	8	V
H	field strength operating range in sensor plane		–0.2	–	+0.2	kA/m
S	sensitivity	open circuit	12	16	–	$\frac{\text{mV/V}}{\text{kA/m}}$
TCS	temperature coefficient of sensitivity	$T_s = -25 \text{ to } +125^\circ\text{C}$	–	0.31	–	%/K
$k_{\text{SX}}$	sensitivity synchronism	note 2	92	100	108	%
$\text{TCV}_O$	temperature coefficient of output voltage	$V_{\text{CC}} = 5 \text{ V}; T_{\text{bridge}} = -25 \text{ to } +125^\circ\text{C}$	–	–0.4	–	%/K
$R_{\text{bridge}}$	bridge resistance	note 3	1	2	3	kΩ
$\text{TCR}_{\text{bridge}}$	temperature coefficient of bridge resistance	$T_{\text{bridge}} = -25 \text{ to } +125^\circ\text{C};$ note 4	–	0.3	–	%/K
$V_{\text{offset}}$	offset voltage per supply voltage		–1.5	0	+1.5	mV/V
$\text{TCV}_{\text{offset}}$	temperature coefficient of offset voltage	$T_{\text{bridge}} = -25 \text{ to } +125^\circ\text{C};$ note 5	–3	0	+3	$\frac{\mu\text{V/V}}{\text{K}}$
FH	hysteresis of output voltage		–	–	2	%FS
$R_{\text{comp}}$	resistance of compensation coil	note 6	100	170	300	Ω
$A_{\text{comp}}$	field factor of compensation coil		19	22	25	$\frac{\text{A/m}}{\text{mA}}$
$R_{\text{flip}}$	resistance of set/reset coil	note 7	1	2	3	Ω
$\text{TCR}_{\text{flip}}$	temperature coefficient of resistance of set/reset coil	$T_{\text{flip}} = -25 \text{ to } +125^\circ\text{C}$	–	0.39	–	%/K
$I_{\text{flip}}$	recommended flipping current for stable operation		±800	±1000	±1200	mA
$t_{\text{flip}}$	flip pulse duration		1	3	100	μs
$R_{\text{isol}}$	isolating resistance	note 8	1	–	–	MΩ
$V_{\text{isol}}$	voltage between isolated systems	note 8	–	–	50	V
$R_{\text{isol\_dice}}$	isolating resistance between dice	die 1 to die 2	1	–	–	MΩ
f	operating frequency		0	–	1	MHz
α	angle die-to-die	note 9	88	90	92	deg
β	angle dice-to-package	note 9	–5	0	+5	deg

## Notes

- Due to the ratiometric output, the same supply voltage ( $V_{\text{CC}}$ ) must be applied to both dice in one KMZ52 device.
- $k_{\text{SX}} = 100 \times \frac{A_{\text{comp}1} \times S_1}{A_{\text{comp}2} \times S_2} \%$
- Bridge resistance die 1: between pins 5 and 12; bridge resistance die 2: between pins 2 and 3.
- $$\text{TCR}_{\text{bridge}} = 100 \frac{R_{\text{bridge}(T_2)} - R_{\text{bridge}(T_1)}}{R_{\text{bridge}(T_1)}(T_2 - T_1)} \quad \text{Where } T_1 = -25^\circ\text{C}; T_2 = 125^\circ\text{C}.$$

## Magnetic Field Sensor

KMZ52

---

5.  $TCV_{\text{offset}} = \frac{V_{\text{offset}(T_2)} - V_{\text{offset}(T_1)}}{(T_2 - T_1)}$  Where  $T_1 = -25^{\circ}\text{C}$ ;  $T_2 = 125^{\circ}\text{C}$ .
6. Resistance of compensation coil die 1: between pins 6 and 7;  
resistance of compensation coil die 2: between pins 4 to 13.
7. Resistance of set/reset coil die 1: between pins 10 and 11;  
resistance of set/reset coil die 2: between pins 1 to 16.
8. Isolating resistance die 1: pins 7 and 8, 7 and 10 and 8 to 10;  
isolating resistance die 2: pins 1 to 2, 1 to 4 and 2 to 4.
9. Angle die-to-die: die 2 is turned by  $90 \pm 2$  degrees in anticlockwise direction with respect to die 1;  
angle dice-to-package: both dice in their fixed die-to-die position are tilted towards the package edges by  
 $0 \pm 5$  degrees.

# Magnetic Field Sensor

KMZ52

## APPLICATION INFORMATION

If the angle  $\alpha$  between external magnetic field  $H$  and the long axis of the package is zero,  $H$  is parallel to the most sensitive direction of die 2 and perpendicular to the sensitive direction of die 1. A magnetic field turning clockwise (see Fig.2) thus yields an output proportional to  $\cos \alpha$  ( $V_{out2}$ ) and an output proportional to  $\sin \alpha$  ( $V_{out1}$ ).

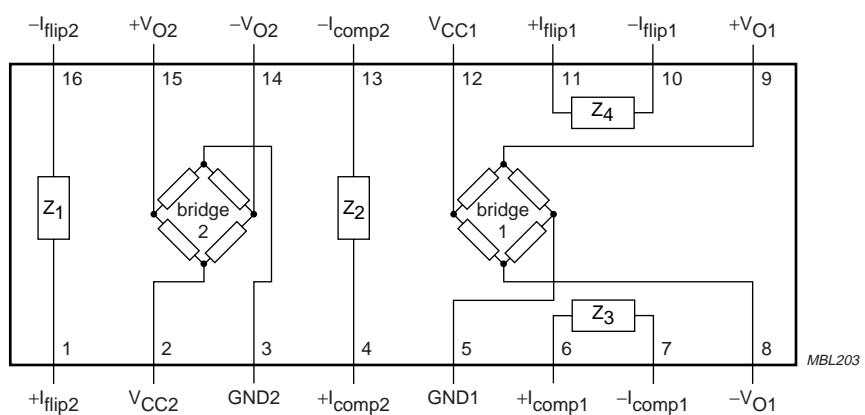
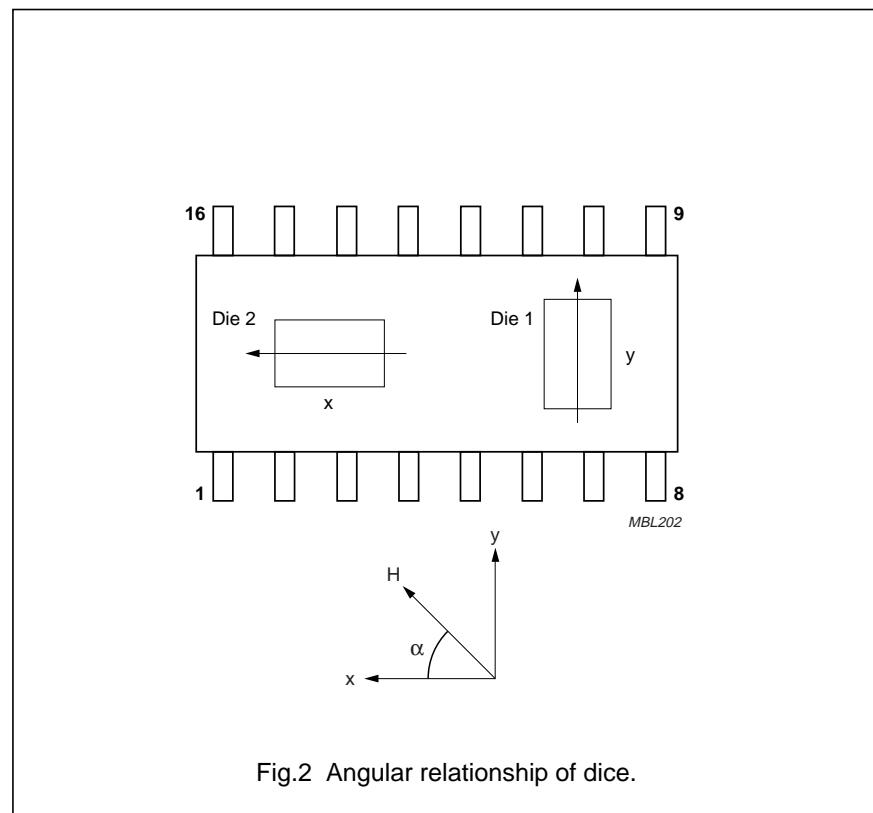


Fig.3 Simplified circuit diagram.

# MC33272A, MC33274A, NCV33272A, NCV33274A

## Single Supply, High Slew Rate, Low Input Offset Voltage Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip-R-Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual-doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

### Features

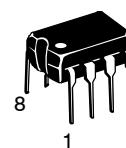
- Input Offset Voltage Trimmed to 100  $\mu$ V (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 M $\Omega$
- Low Noise: 18 nV/ $\sqrt{\text{Hz}}$  @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/ $\mu$ s
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ -14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or  $\pm 1.5$  V to  $\pm 18$  V
- ESD Diodes Provide Added Protection to the Inputs
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- Pb-Free Packages are Available



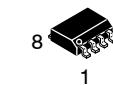
ON Semiconductor®

<http://onsemi.com>

### DUAL



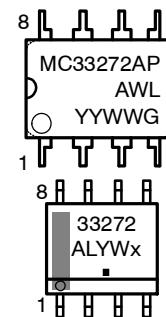
PDIP-8  
P SUFFIX  
CASE 626



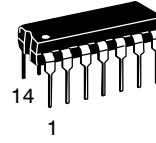
SOIC-8  
D SUFFIX  
CASE 751

x = A for MC33272AD/DR2  
= N for NCV33272ADR2

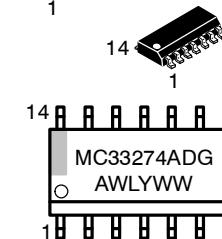
### MARKING DIAGRAMS



### QUAD



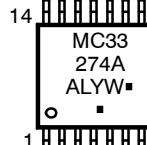
PDIP-14  
P SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DTB SUFFIX  
CASE 948G



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

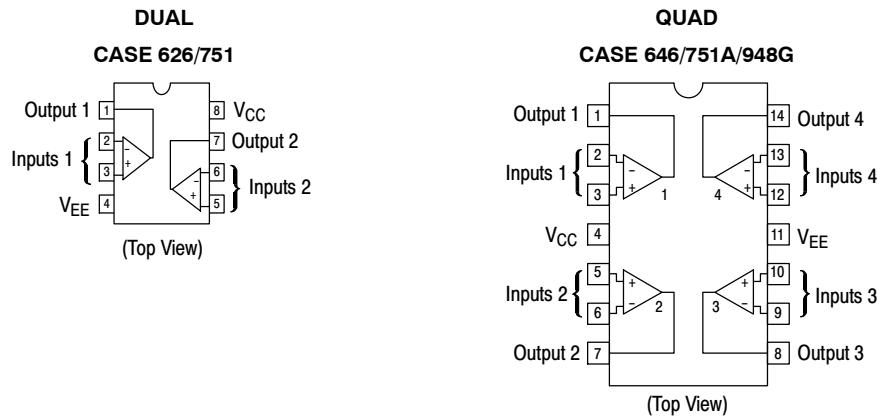
(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

# MC33272A, MC33274A, NCV33272A, NCV33274A

## PIN CONNECTIONS



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub> to V <sub>EE</sub>	+36	V
Input Differential Voltage Range	V <sub>IDR</sub>	Note 1	V
Input Voltage Range	V <sub>IR</sub>	Note 1	V
Output Short Circuit Duration (Note 2)	t <sub>SC</sub>	Indefinite	sec
Maximum Junction Temperature	T <sub>J</sub>	+150	°C
Storage Temperature	T <sub>stg</sub>	-60 to +150	°C
ESD Protection at Any Pin – Human Body Model – Machine Model	V <sub>esd</sub>	2000 200	V
Maximum Power Dissipation	P <sub>D</sub>	Note 2	mW
Operating Temperature Range MC33272A, MC33274A NCV33272A, NCV33274A	T <sub>A</sub>	-40 to +85 -40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both input voltages should not exceed V<sub>CC</sub> or V<sub>EE</sub>.
2. Power dissipation must be considered to ensure maximum junction temperature (T<sub>J</sub>) is not exceeded (see Figure 2).

# MC33272A, MC33274A, NCV33272A, NCV33274A

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15$  V,  $V_{EE} = -15$  V,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

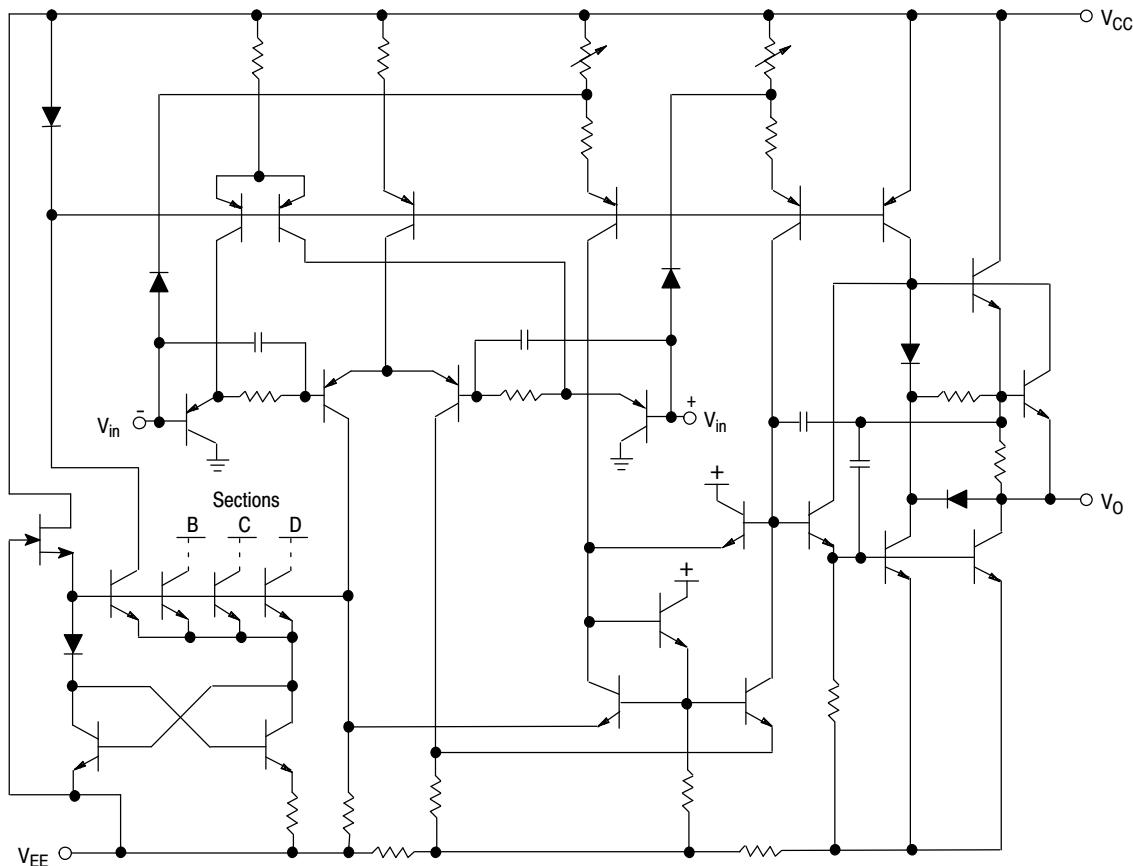
Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ( $R_S = 10 \Omega$ , $V_{CM} = 0$ V, $V_O = 0$ V) $(V_{CC} = +15$ V, $V_{EE} = -15$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$ $T_A = -40^\circ$ to $+125^\circ\text{C}$ (NCV33272A) $T_A = -40^\circ$ to $+125^\circ\text{C}$ (NCV33274A) $(V_{CC} = 5.0$ V, $V_{EE} = 0$ V) $T_A = +25^\circ\text{C}$	3	$ V_{IO} $	—	0.1	1.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10 \Omega$ , $V_{CM} = 0$ V, $V_O = 0$ V, $T_A = -40^\circ$ to $+125^\circ\text{C}$	3	$\Delta V_{IO}/\Delta T$	—	2.0	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ( $V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$	4, 5	$I_{IB}$	—	300	650	nA
—	—	—	—	—	800	—
Input Offset Current ( $V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$	—	$ I_{IO} $	—	3.0	65	nA
—	—	—	—	—	80	—
Common Mode Input Voltage Range ( $\Delta V_{IO} = 5.0$ mV, $V_O = 0$ V) $T_A = +25^\circ\text{C}$	6	$V_{ICR}$	$V_{EE}$ to $(V_{CC} - 1.8)$			V
Large Signal Voltage Gain ( $V_O = 0$ V to 10 V, $R_L = 2.0 \text{ k}\Omega$ ) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$	7	$A_{VOL}$	90 86	100 —	— —	dB
Output Voltage Swing ( $V_{ID} = \pm 1.0$ V) $(V_{CC} = +15$ V, $V_{EE} = -15$ V) $R_L = 2.0 \text{ k}\Omega$ $R_L = 2.0 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$ $(V_{CC} = 5.0$ V, $V_{EE} = 0$ V) $R_L = 2.0 \text{ k}\Omega$ $R_L = 2.0 \text{ k}\Omega$	8, 9, 12 10, 11	$V_{O+}$ $V_{O-}$ $V_{O+}$ $V_{O-}$ $V_{OL}$ $V_{OH}$	13.4 — 13.4 — — 3.7	13.9 —13.9 14 —14.7 — —	— —13.5 — —14.1 0.2 5.0	V
Common Mode Rejection ( $V_{in} = +13.2$ V to $-15$ V)	13	CMR	80	100	—	dB
Power Supply Rejection $V_{CC}/V_{EE} = +15$ V/ $-15$ V, $+5.0$ V/ $-15$ V, $+15$ V/ $-5.0$ V	14, 15	PSR	80	105	—	dB
Output Short Circuit Current ( $V_{ID} = 1.0$ V, Output to Ground) Source Sink	16	$I_{SC}$	+25 -25	+37 -37	— —	mA
Power Supply Current Per Amplifier ( $V_O = 0$ V) $(V_{CC} = +15$ V, $V_{EE} = -15$ V) $T_A = +25^\circ\text{C}$ $T_A = T_{low}$ to $T_{high}$ $(V_{CC} = 5.0$ V, $V_{EE} = 0$ V) $T_A = +25^\circ\text{C}$	17	$I_{CC}$	—	2.15	2.75 3.0	mA
—	—	—	—	—	2.75	—

3. MC33272A, MC33274A     $T_{low} = -40^\circ\text{C}$      $T_{high} = +85^\circ\text{C}$   
 NCV33272A, NCV33274A     $T_{low} = -40^\circ\text{C}$      $T_{high} = +125^\circ\text{C}$

# MC33272A, MC33274A, NCV33272A, NCV33274A

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +15$  V,  $V_{EE} = -15$  V,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate ( $V_{in} = -10$ V to $+10$ V, $R_L = 2.0$ k $\Omega$ , $C_L = 100$ pF, $A_V = +1.0$ V)	18, 33	SR	8.0	10	—	V/ $\mu$ s
Gain Bandwidth Product ( $f = 100$ kHz)	19	GBW	17	24	—	MHz
AC Voltage Gain ( $R_L = 2.0$ k $\Omega$ , $V_O = 0$ V, $f = 20$ kHz)	20, 21, 22	$A_{vO}$	—	65	—	dB
Unity Gain Bandwidth (Open Loop)		BW	—	5.5	—	MHz
Gain Margin ( $R_L = 2.0$ k $\Omega$ , $C_L = 0$ pF)	23, 24, 26	$A_m$	—	12	—	dB
Phase Margin ( $R_L = 2.0$ k $\Omega$ , $C_L = 0$ pF)	23, 25, 26	$\phi_m$	—	55	—	Deg
Channel Separation ( $f = 20$ Hz to $20$ kHz)	27	CS	—	-120	—	dB
Power Bandwidth ( $V_O = 20$ V <sub>pp</sub> , $R_L = 2.0$ k $\Omega$ , THD $\leq 1.0\%$ )		BWP	—	160	—	kHz
Total Harmonic Distortion ( $R_L = 2.0$ k $\Omega$ , $f = 20$ Hz to $20$ kHz, $V_O = 3.0$ V <sub>rms</sub> , $A_V = +1.0$ )	28	THD	—	0.003	—	%
Open Loop Output Impedance ( $V_O = 0$ V, $f = 6.0$ MHz)	29	$ Z_{O_l} $	—	35	—	$\Omega$
Differential Input Resistance ( $V_{CM} = 0$ V)		$R_{in}$	—	16	—	M $\Omega$
Differential Input Capacitance ( $V_{CM} = 0$ V)		$C_{in}$	—	3.0	—	pF
Equivalent Input Noise Voltage ( $R_S = 100$ $\Omega$ , $f = 1.0$ kHz)	30	$e_n$	—	18	—	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current ( $f = 1.0$ kHz)	31	$i_n$	—	0.5	—	pA/ $\sqrt{\text{Hz}}$



**Figure 1. Equivalent Circuit Schematic**  
(Each Amplifier)

# 1A Fixed and Adjustable Low Dropout Positive Voltage Regulators

## General Description

The RT9164A series of high performance positive voltage regulators is designed for applications requiring low dropout performance at fully rated current. Additionally, the RT9164A series provides excellent regulation over variations in line and load. Outstanding features include low dropout performance at rated current, fast transient response, internal current-limiting, and thermal-shutdown protection of the output device. The RT9164A series of three terminal regulators offers fixed and adjustable voltage options available in space-saving SOT-223, TO-252, and TO-263 packages.

## Ordering Information

RT9164A-□□□□

Package Type
G : SOT-223
L: TO-252
LR : TO-252 (R-Type)
M : TO-263
Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)
Output Voltage
Default : Adjustable
15 : 1.5V
18 : 1.8V
25 : 2.5V
28 : 2.85V
30 : 3.0V
33 : 3.3V
35 : 3.5V

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

## Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

## Features

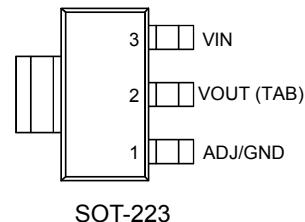
- **Low Dropout Performance, 1.4V Max**
- **Full Current Rating Over Line and Temperature**
- **Fast Transient Response**
- **$\pm 2\%$  Output Voltage Accuracy**
- **1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, and 3.5V Fixed Adjustable Output Voltage**
- **SOT-223, TO-252, and TO-263 Packages**
- **RoHS Compliant and 100% Lead (Pb)-Free**

## Applications

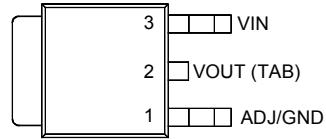
- Active SCSI Termination
- Low Voltage Microcontrollers
- Switching Power Supply Post-Regulator

## Pin Configurations

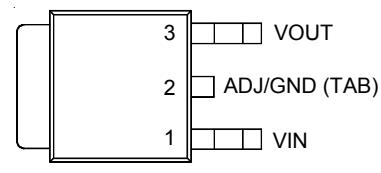
(TOP VIEW)



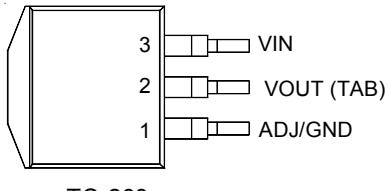
SOT-223



TO-252

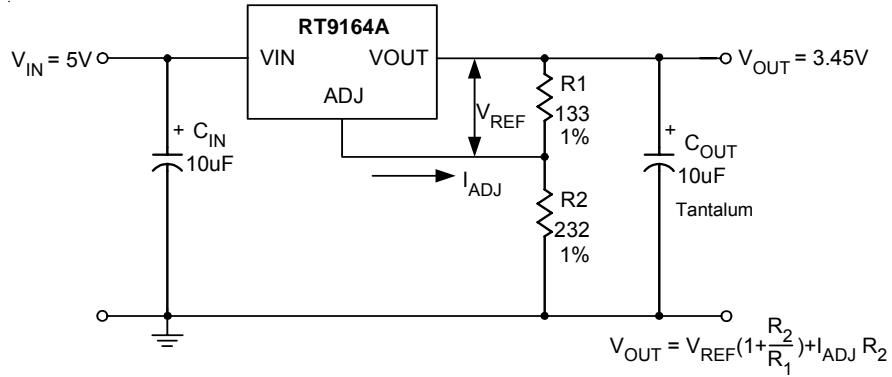


TO-252 (R-Type)



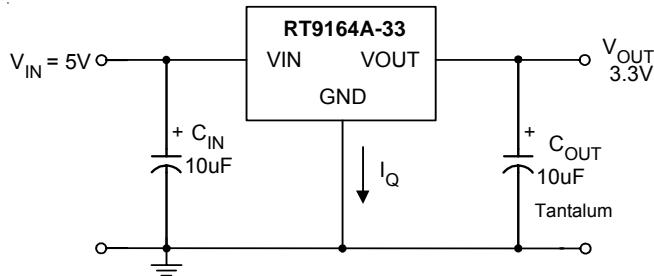
TO-263

## Typical Application Circuit



- (1)  $C_{IN}$  needed if device is far from filter capacitors.
- (2)  $C_{OUT}$  required for stability.

Figure 1. Adjustable Voltage Regulator



- (1)  $C_{IN}$  needed if device is far from filter capacitors.
- (2)  $C_{OUT}$  required for stability.

Figure 2. Fixed Voltage Regulator

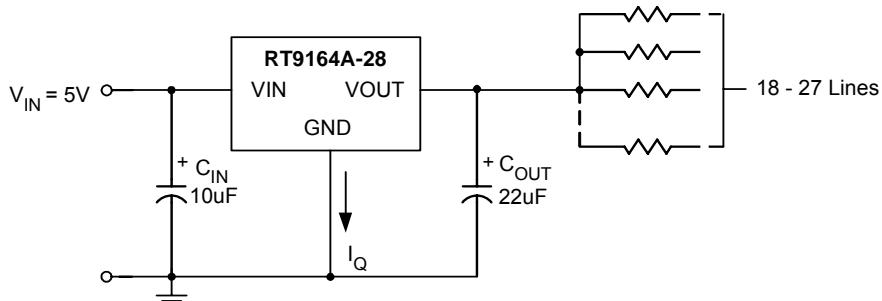
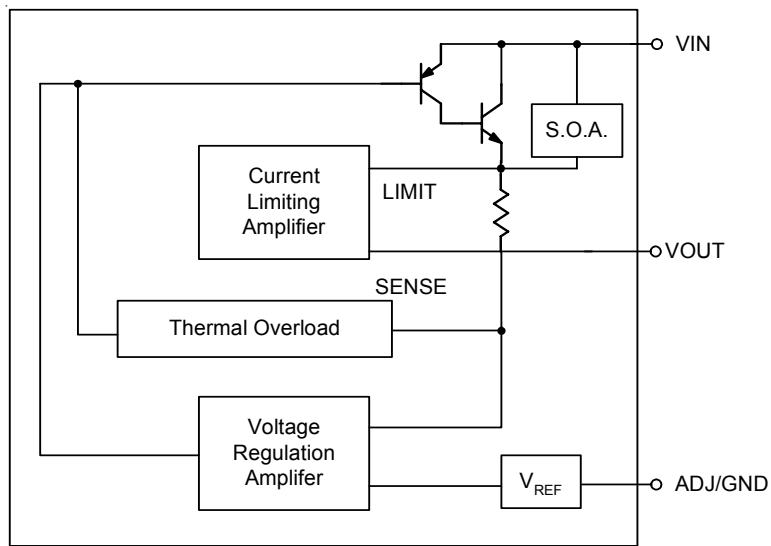


Figure 3. Active SCSI Bus Terminator

## Function Block Diagram



## Functional Pin Description

Pin Name	Pin Function
ADJ/GND	Adjust Output or Ground.
VOUT	Output Voltage.
VIN	Power Input.

**Absolute Maximum Ratings** (Note 1)

• Supply Input Voltage	-----	15V
• Power Dissipation, $P_D$ @ $T_A = 25^\circ C$	-----	
SOT-223	-----	0.740W
TO-252	-----	1.471W
TO-263	-----	2.222W°C
• Package Thermal Resistance (Note 2)	-----	
SOT-223, $\theta_{JA}$	-----	135°C/W
SOT-223, $\theta_{JC}$	-----	19°C/W
TO-252, $\theta_{JA}$	-----	68°C/W
TO-252, $\theta_{JC}$	-----	7.5°C/W
TO-263, $\theta_{JA}$	-----	45°C/W
TO-263, $\theta_{JC}$	-----	7.8°C/W
• Lead Temperature (Soldering, 10 sec.)	-----	260°C
• Junction Temperature	-----	150°C
• Storage Temperature Range	-----	-65°C to 150°C
• ESD Susceptibility (Note 3)	-----	
HBM (Human Body Mode)	-----	8 kV
MM (Machine Mode)	-----	750V

**Recommended Operating Conditions** (Note 4)

• Supply Input Voltage	-----	3V to 14V
• Junction Temperature Range	-----	-40°C to 125°C

**Electrical Characteristics**

(TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage (Note 5)	V <sub>REF</sub>	I <sub>OUT</sub> = 10mA, (V <sub>IN</sub> - V <sub>OUT</sub> ) = 2V, T <sub>A</sub> = 25°C	1.243	1.256	1.281	V
		10mA < I <sub>OUT</sub> < 1.0A, 1.5V < V <sub>IN</sub> - V <sub>OUT</sub> < 10V	1.231	1.256	1.294	V
Output Voltage (Note 5)	V <sub>OUT</sub>	I <sub>OUT</sub> = 10mA, V <sub>IN</sub> = 3.3V, T <sub>J</sub> = 25°C	1.485	1.5	1.53	V
		10mA < I <sub>OUT</sub> < 1.0A, 3.3V < V <sub>IN</sub> < 10V	1.470	1.5	1.55	
		I <sub>OUT</sub> = 10mA, V <sub>IN</sub> = 3.3V, T <sub>J</sub> = 25°C	1.797	1.815	1.85	
		10mA < I <sub>OUT</sub> < 1.0A, 3.3V < V <sub>IN</sub> < 10V	1.779	1.815	1.87	
		I <sub>OUT</sub> = 10mA, V <sub>IN</sub> = 4.0V, T <sub>J</sub> = 25°C	2.475	2.500	2.550	
		10mA < I <sub>OUT</sub> < 1.0A, 4.0V < V <sub>IN</sub> < 10V	2.450	2.500	2.575	
		I <sub>OUT</sub> = 10mA, V <sub>IN</sub> = 4.25V, T <sub>J</sub> = 25°C	2.822	2.850	2.910	
		10mA < I <sub>OUT</sub> < 1.0A, 4.25V < V <sub>IN</sub> < 10V	2.793	2.850	2.936	
		I <sub>OUT</sub> = 10mA, V <sub>IN</sub> = 4.5V, T <sub>J</sub> = 25°C	2.970	3.000	3.060	
		10mA < I <sub>OUT</sub> < 1.0A, 4.5V < V <sub>IN</sub> < 10V	2.940	3.000	3.090	

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit	
Output Voltage (Note 5)	RT9164A -33	V <sub>OUT</sub>	I <sub>OUT</sub> = 10mA, V <sub>IN</sub> = 4.75V, T <sub>J</sub> = 25°C	3.267	3.300	3.365	V	
			10mA < I <sub>OUT</sub> < 1.0A, 4.75V < V <sub>IN</sub> < 10V	3.234	3.300	3.400		
	RT9164A -35		I <sub>OUT</sub> = 10mA, V <sub>IN</sub> = 5V, T <sub>J</sub> = 25°C	3.465	3.500	3.570		
			10mA < I <sub>OUT</sub> < 1.0A, 5.0V < V <sub>IN</sub> < 10V	3.430	3.500	3.605		
Line Regulation (Note 5)	RT9164A	ΔV <sub>LINE</sub>	I <sub>OUT</sub> = 10mA, 1.5V ≤ V <sub>IN</sub> - V <sub>OUT</sub> ≤ 10V	--	0.1	0.3	%	
	RT9164A -15		I <sub>OUT</sub> = 10mA, 3.3V ≤ V <sub>IN</sub> ≤ 15V	--	1	6	mV	
	RT9164A -18		I <sub>OUT</sub> = 10mA, 3.3V ≤ V <sub>IN</sub> ≤ 15V	--	1	6		
	RT9164A -25		I <sub>OUT</sub> = 10mA, 4.0V ≤ V <sub>IN</sub> ≤ 15V	--	1	6		
	RT9164A -28		I <sub>OUT</sub> = 10mA, 4.25V ≤ V <sub>IN</sub> ≤ 15V	--	1	6		
	RT9164A -30		I <sub>OUT</sub> = 10mA, 4.5V ≤ V <sub>IN</sub> ≤ 15V	--	1	6		
	RT9164A -33		I <sub>OUT</sub> = 10mA, 4.75V ≤ V <sub>IN</sub> ≤ 15V	--	1	6		
	RT9164A -35		I <sub>OUT</sub> = 10mA, 5.0V ≤ V <sub>IN</sub> ≤ 15V	--	1	6		
Load Regulation (Note 5)	RT9164A	ΔV <sub>LOAD</sub>	(V <sub>IN</sub> - V <sub>OUT</sub> ) = 3V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	0.2	0.4	%	
	RT9164A -15		V <sub>IN</sub> = 3.3V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	1	10	mV	
	RT9164A -18		V <sub>IN</sub> = 3.3V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	1	10		
	RT9164A -25		V <sub>IN</sub> = 4.0V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	1	10		
	RT9164A -28		V <sub>IN</sub> = 4.25V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	1	10		
	RT9164A -30		V <sub>IN</sub> = 4.5V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	1	12		
	RT9164A -33		V <sub>IN</sub> = 4.75V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	1	12		
	RT9164A -35		V <sub>IN</sub> = 5.0V, 10mA ≤ I <sub>OUT</sub> ≤ 1.0A	--	1	15		
Dropout Voltage (Note 6)		V <sub>DROP</sub>	I <sub>OUT</sub> = 500mA	--	1.15	1.25	V	
			I <sub>OUT</sub> = 1.0A	--	1.3	1.4		
Current Limit		I <sub>LIM</sub>	V <sub>IN</sub> = 5V	1.0	1.8	-	A	
Minimum Load Current	RT9164A		(V <sub>IN</sub> - V <sub>OUT</sub> ) = 2V	--	5	10	mA	
Quiescent Current	RT9164A -XX	I <sub>Q</sub>	V <sub>IN</sub> = 5V	--	5	10		
Ripple Rejection		PSRR	f <sub>RIPPLE</sub> = 120Hz, (V <sub>IN</sub> - V <sub>OUT</sub> ) = 2V, V <sub>RIPPLE</sub> = 1V <sub>P-P</sub>	--	72	-	dB	
Adjust Pin Current		I <sub>ADJ</sub>		--	65	120	μA	
Adjust Pin Current Change		ΔI <sub>ADJ</sub>	10mA ≤ I <sub>OUT</sub> ≤ 1.0A, V <sub>IN</sub> = 5V	--	0.2	5	μA	