Data Sheet: JN5148-001

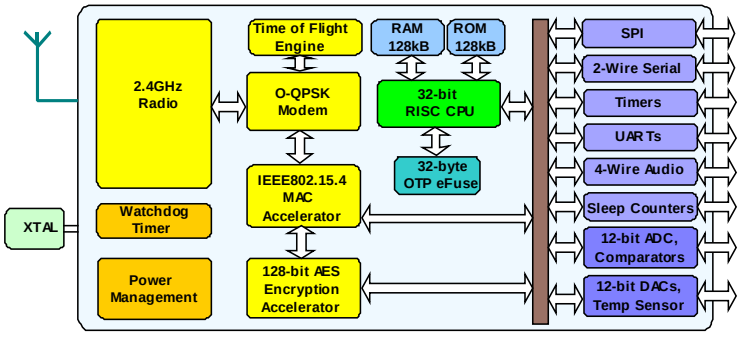
IEEE802.15.4 Wireless Microcontroller

Overview

The JN5148-001 is an ultra low power, high performance wireless microcontroller targeted at JenNet and ZigBee PRO networking applications. The device features an enhanced 32-bit RISC processor offering high coding efficiency through variable width instructions, a multi-stage instruction pipeline and low power operation with programmable clock speeds. It also includes a 2.4GHz IEEE802.15.4 compliant transceiver, 128kB of ROM, 128kB of RAM, and a rich mix of analogue and digital peripherals. The large memory footprint allows the device to run both a network stack (e.g. ZigBee PRO) and an embedded application or in a co-processor mode. The operating current is below 18mA, allowing operation direct from a coin cell.

Enhanced peripherals include low power pulse counters running in sleep mode designed for pulse counting in AMR applications and a unique Time of Flight ranging engine, allowing accurate location services to be implemented on wireless sensor networks. It also includes a 4-wire I^2S audio interface, to interface directly to mainstream audio CODECs, as well as conventional MCU peripherals.

Block Diagram



Benefits

- Single chip integrates transceiver and microcontroller for wireless sensor networks
- Large memory footprint to run ZigBee PRO or JenNet together with an application
- Very low current solution for long battery life
- Highly featured 32-bit RISC CPU for high performance and low power
- System BOM is low in component count and cost
- Extensive user peripherals

Applications

- Robust and secure low power wireless applications
- ZigBee PRO and JenNet networks
- Smart metering (e.g. AMR)
- Home and commercial building automation
- Location Aware services – e.g. Asset Tracking
- Industrial systems
- Telemetry
- Remote Control
- Toys and gaming peripherals

Features: Transceiver

- 2.4GHz IEEE802.15.4 compliant
- Time of Flight ranging engine
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- 500 & 667kbps data rate modes
- Integrated sleep oscillator for low power
- On chip power regulation for 2.0V to 3.6V battery operation
- Deep sleep current 100nA
- Sleep current with active sleep timer 1.25µA
- <$0.50 external component cost
- Rx current 17.5mA
- Tx current 15.0mA
- Receiver sensitivity -95dBm
- Transmit power 2.5dBm

Features: Microcontroller

- Low power 32-bit RISC CPU, 4 to 32MHz clock speed
- Variable instruction width for high coding efficiency
- Multi-stage instruction pipeline
- 128kB ROM and 128kB RAM for bootloaded program code & data
- JTAG debug interface
- 4-input 12-bit ADC, 2 12-bit DACs, 2 comparators
- 3 application timer/counters,
- 2 UARTs
- SPI port with 5 selects
- 2-wire serial interface
- 4-wire digital audio interface
- Watchdog timer
- Low power pulse counters
- Up to 21 DIO

Industrial temp (-40°C to +85°C)

8x8mm 56-lead Punched QFN

Lead-free and RoHS compliant

1 Introduction

The JN5148-001 is an IEEE802.15.4 wireless microcontroller that provides a fully integrated solution for applications using the IEEE802.15.4 standard in the 2.4 - 2.5GHz ISM frequency band [1], including JenNet and ZigBee PRO. It includes all of the functionality required to meet the IEEE802.15.4, JenNet and ZigBee PRO specifications and has additional processor capability to run a wide range of applications including, but not limited to Smart Energy, Automatic Meter Reading, Remote Control, Home and Building Automation, Toys and Gaming.

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimise this complexity, NXP provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN5148. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, the register details of the JN5148 are not provided in the datasheet.

The device includes a Wireless Transceiver, RISC CPU, on chip memory and an extensive range of peripherals.

Hereafter, the JN5148-001 will be referred to as JN5148.

1.1 Wireless Transceiver

The Wireless Transceiver comprises a 2.45GHz radio, a modem, a baseband controller and a security coprocessor. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realised very easily. Appendix B.4, describes a complete reference design including Printed Circuit Board (PCB) design and Bill Of Materials (BOM).

The security coprocessor provides hardware-based 128-bit AES-CCM* modes as specified by the IEEE802.15.4 2006 standard. Specifically this includes encryption and authentication covered by the MIC –32/ -64/ -128, ENC and ENC-MIC –32/ -64/ -128 modes of operation.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 Medium Access Control (MAC) under the control of a protocol stack. Applications incorporating IEEE802.15.4 functionality can be rapidly developed by combining user-developed application software with a protocol stack library.

1.2 RISC CPU and Memory

A 32-bit RISC CPU allows software to be run on chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN5148 has a unified memory architecture, code memory, data memory, peripheral devices and I/O ports are organised within the same linear address space. The device contains 128kbytes of ROM, 128kbytes of RAM and a 32-byte One Time Programmable (OTP) eFuse memory.

1.3 Peripherals

The following peripherals are available on chip:

- Master SPI port with five select outputs
- Two UARTs with support for hardware or software flow control
- Three programmable Timer/Counters – all three support Pulse Width Modulation (PWM) capability, two have capture/compare facility
- Two programmable Sleep Timers and a Tick Timer
- Two-wire serial interface (compatible with SMbus and I^2C) supporting master and slave operation
- Four-wire digital audio interface (compatible with I²S)
- Slave SPI port for Intelligent peripheral mode (shared with digital I/O)
- Twenty-one digital I/O lines (multiplexed with peripherals such as timers and UARTs)
- Four channel, 12-bit, Analogue to Digital converter
- Two 12-bit Digital to Analogue converters
- Two programmable analogue comparators
- Internal temperature sensor and battery monitor
- Time Of Flight ranging engine
- Two low power pulse counters
- Random number generator
- Watchdog Timer and Voltage Brown-out
- Sample FIFO for digital audio interface or ADC/DAC
- JTAG hardware debug port

User applications access the peripherals using the Integrated Peripherals API. This allows applications to use a tested and easily understood view of the peripherals allowing rapid system development.

1.4 Block Diagram

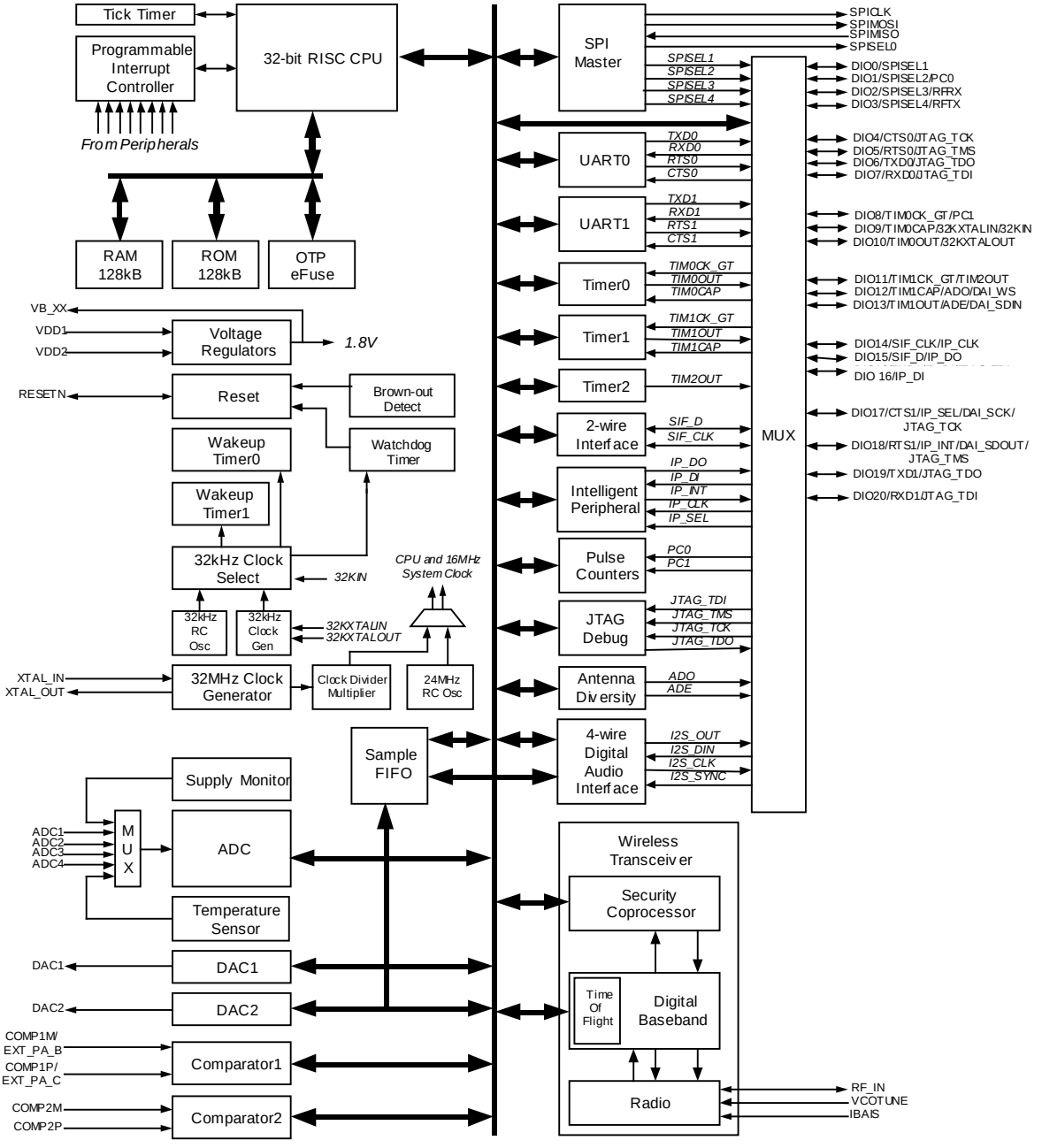


Figure 1: JN5148 Block Diagram

2 Pin Configurations

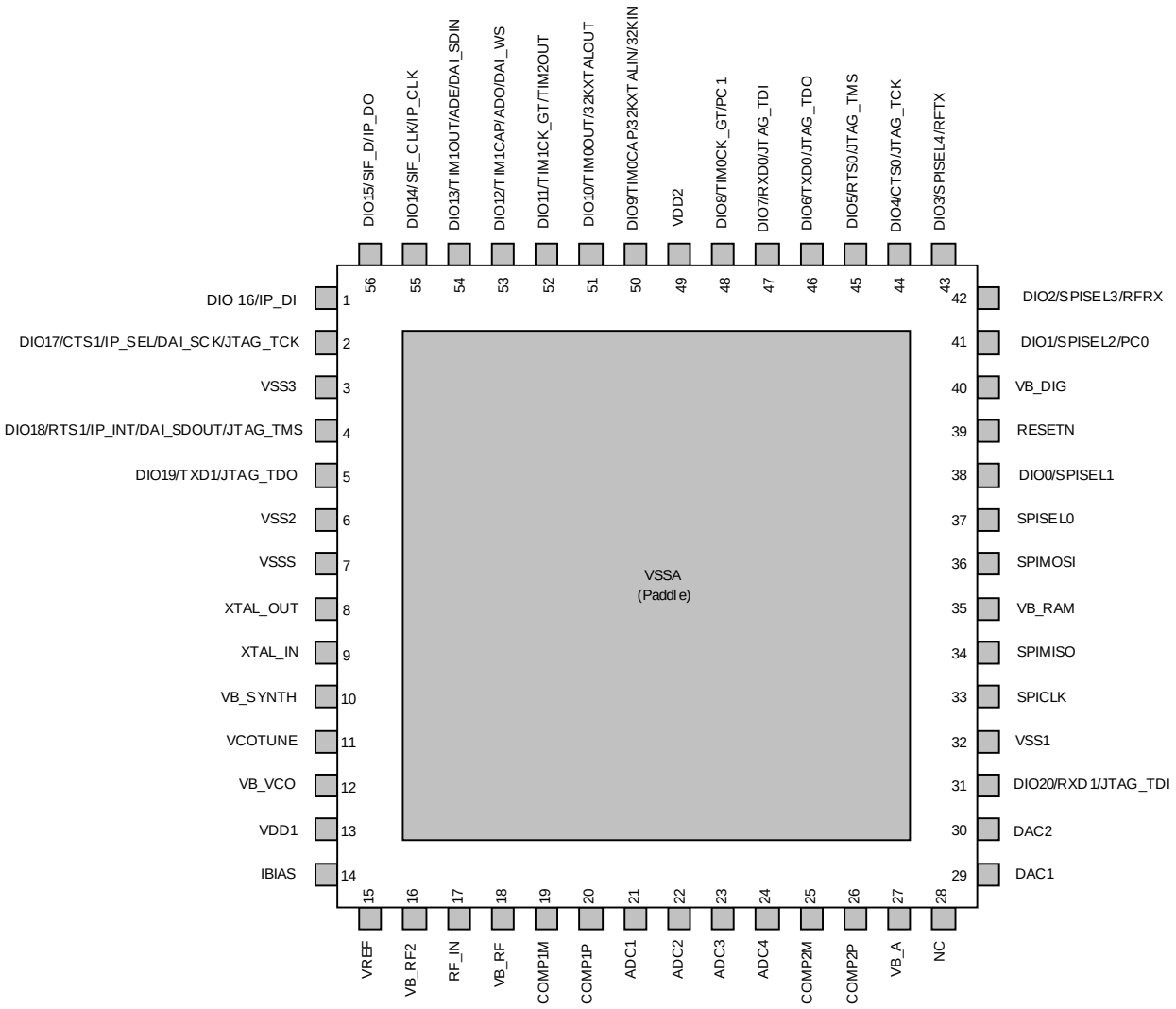


Figure 2: 56-pin QFN Configuration (top view)

Note: Please refer to Appendix B.4 JN5148 Module Reference Design for important applications information regarding the connection of the PADDLE to the PCB.

2.1 Pin Assignment

Pin No	Power supplies				Signal Type	Description
10, 12, 16, 18, 27, 35, 40	VB_SYNTH, VB_VCO, VB_RF2, VB_RF, VB_A, VB_RAM, VB_DIG				1.8V	Regulated supply voltage
13, 49	VDD1, VDD2				3.3V	Supplies: VDD1 for analogue, VDD2 for digital
32, 6, 3, 7, Paddle	VSS1, VSS2, VSS3, VSSS, VSSA				0V	Grounds (see appendix A.2 for paddle details)
28	NC					No connect
	General					
39	RESETN				CMOS	Reset input
8, 9	XTAL_OUT, XTAL_IN				1.8V	System crystal oscillator
	Radio					
11	VCOTUNE				1.8V	VCO tuning RC network
14	IBIAS				1.8V	Bias current control
17	RF_IN				1.8V	RF antenna
	Analogue Peripheral I/O					
21, 22, 23, 24	ADC1, ADC2, ADC3, ADC4				3.3V	ADC inputs
15	VREF				1.8V	Analogue peripheral reference voltage
29, 30	DAC1, DAC2				3.3V	DAC outputs
19, 20	COMP1M/EXT_PA_B, COMP1P/EXT_PA_C				3.3V	Comparator 1 inputs and external PA control
25, 26	COMP2M, COMP2P				3.3V	Comparator 2 inputs
	Digital Peripheral I/O					
	Primary	**Alternate Functions**				
33	SPICLK				CMOS	SPI Clock Output
36	SPIMOSI				CMOS	SPI Master Out Slave In Output
34	SPIMISO				CMOS	SPI Master In Slave Out Input
37	SPISEL0				CMOS	SPI Slave Select Output 0
38	DIO0	SPISEL1			CMOS	DIO0 or SPI Slave Select Output 1
41	DIO1	SPISEL2	PC0		CMOS	DIO1, SPI Slave Select Output 2 or Pulse Counter0 Input
42	DIO2	SPISEL3	RFRX		CMOS	DIO2, SPI Slave Select Output 3 or Radio Receive Control Output
43	DIO3	SPISEL4	RFTX		CMOS	DIO3, SPI Slave Select Output 4 or Radio Transmit Control Output
44	DIO4	CTS0	JTAG_TCK		CMOS	DIO4, UART 0 Clear To Send Input or JTAG CLK
45	DIO5	RTS0	JTAG_TMS		CMOS	DIO5, UART 0 Request To Send Output or JTAG Mode Select
46	DIO6	TXD0	JTAG_TDO		CMOS	DIO6, UART 0 Transmit Data Output or JTAG Data Output
47	DIO7	RXD0	JTAG_TDI		CMOS	DIO7, UART 0 Receive Data Input or JTAG Data Input
48	DIO8	TIM0CK_GT	PC1		CMOS	DIO8, Timer0 Clock/Gate Input or Pulse Counter1 Input
50	DIO9	TIM0CAP	32KXTALIN	32KIN	CMOS	DIO9, Timer0 Capture Input, 32K External Crystal Input or 32K Clock Input

Pin No	Digital Peripheral I/O					Signal Type	Description
	Primary	Alternate Functions					
51	DIO10	TIM0OUT	32KXTALOUT			CMOS	DIO10, Timer0 PWM Output or 32K External Crystal Output
52	DIO11	TIM1CK_GT	TIM2OUT			CMOS	DIO11, Timer1 Clock/Gate Input or Timer2 PWM Output
53	DIO12	TIM1CAP	ADO	DAI_WS		CMOS	DIO12, Timer1 Capture Input, Antenna Diversity or Digital Audio Word Select
54	DIO13	TIM1OUT	ADE	DAI_SDIN		CMOS	DIO13, Timer1 PWM Output, Antenna Diversity or Digital Audio Data Input
55	DIO14	SIF_CLK	IP_CLK			CMOS	DIO14, Serial Interface Clock or Intelligent Peripheral Clock Input
56	DIO15	SIF_D	IP_DO			CMOS	DIO15, Serial Interface Data or Intelligent Peripheral Data Out
1	DIO16	IP_DI				CMOS	DIO16 or Intelligent Peripheral Data In
2	DIO17	CTS1	IP_SEL	DAI_SCK	JTAG_TCK	CMOS	DIO17, UART 1 Clear To Send Input, Intelligent Peripheral Device Select Input or Digital Audio Clock or JTAG CLK
4	DIO18	RTS1	IP_INT	DAI_SDOUT	JTAG_TMS	CMOS	DIO18, UART 1 Request To Send Output, Intelligent Peripheral Interrupt Output or Digital Audio Data Output or JTAG Mode Select
5	DIO19	TXD1			JTAG_TDO	CMOS	DIO19 or UART 1 Transmit Data Output or JTAG Data Out
31	DIO 20	RXD1			JTAG_TDI	CMOS	DIO 20, UART 1 Receive Data Input or JTAG data In

The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5148 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

3 CPU

The CPU of the JN5148 is a 32-bit load and store RISC processor. It has been architected for three key requirements:

- Low power consumption for battery powered applications
- High performance to implement a wireless protocol at the same time as complex applications
- Efficient coding of high-level languages such as C provided with the NXP Software Developer's Kit

It features a linear 32-bit logical address space with unified memory architecture, accessing both code and data in the same address space. Registers for peripheral units, such as the timers, UARTs and the baseband processor are also mapped into this space.

The CPU has access to a block of 15 32-bit General-Purpose (GP) registers together with a small number of special purpose registers which are used to store processor state and control interrupt handling. The contents of any GP register can be loaded from or stored to memory, while arithmetic and logical operations, shift and rotate operations, and signed and unsigned comparisons can be performed either between two registers and stored in a third, or between registers and a constant carried in the instruction. Operations between general or special-purpose registers execute in one cycle while those that access memory require a further cycle to allow the memory to respond.

The instruction set manipulates 8, 16 and 32-bit data; this means that programs can use objects of these sizes very efficiently. Manipulation of 32-bit quantities is particularly useful for protocols and high-end applications allowing algorithms to be implemented in fewer instructions than on smaller word-size processors, and to execute in fewer clock cycles. In addition, the CPU supports hardware Multiply that can be used to efficiently implement algorithms needed by Digital Signal Processing applications.

The instruction set is designed for the efficient implementation of high-level languages such as C. Access to fields in complex data structures is very efficient due to the provision of several addressing modes, together with the ability to be able to use any of the GP registers to contain the address of objects. Subroutine parameter passing is also made more efficient by using GP registers rather than pushing objects onto the stack. The recommended programming method for the JN5148 is by using C, which is supported by a software developer kit comprising a C compiler, linker and debugger.

The CPU architecture also contains features that make the processor suitable for embedded, real-time applications. In some applications, it may be necessary to use a real-time operating system to allow multiple tasks to run on the processor. To provide protection for device-wide resources being altered by one task and affecting another, the processor can run in either supervisor or user mode, the former allowing access to all processor registers, while the latter only allows the GP registers to be manipulated. Supervisor mode is entered on reset or interrupt; tasks starting up would normally run in user mode in a RTOS environment.

Embedded applications require efficient handling of external hardware events. When using JenOS, prioritised interrupts are supported, with 15 priority levels, and can be configured as required by the application.

To improve power consumption a number of power-saving modes are implemented in the JN5148, described more fully in section 21 - Power Management and Sleep Modes. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on an interrupt it will wake up to service the request. Additionally, it is possible under software control, to set the speed of the CPU to 4, 8, 16 or 32MHz. This feature can be used to trade-off processing power against current consumption.

4 Memory Organisation

This section describes the different memories found within the JN5148. The device contains ROM, RAM, OTP eFuse memory, the wireless transceiver and peripherals all within the same linear address space.

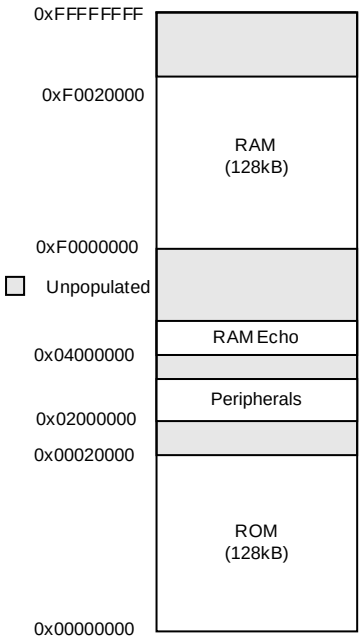


Figure 5: JN5148 Memory Map

4.1 ROM

The ROM is 128k bytes in size, and can be accessed by the processor in a single CPU clock cycle. The ROM contents include bootloader to allow external Flash memory contents to be bootloaded into RAM at runtime, a default interrupt vector table, an interrupt manager, IEEE802.15.4 MAC and APIs for interfacing on-chip peripherals. The operation of the boot loader is described in detail in Application Note [7]. The interrupt manager routes interrupt calls to the application's soft interrupt vector table contained within RAM. Section 7 contains further information regarding the handling of interrupts. ROM contents are shown in Figure 6.

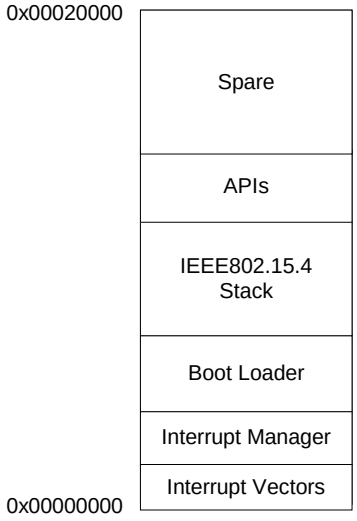


Figure 6: Typical ROM contents

4.2 RAM

The JN5148 contains 128kBytes of high speed RAM. It can be used for both code and data storage and is accessed by the CPU in a single clock cycle. At reset, a boot loader controls the loading of segments of code and data from an external memory connected to the SPI port, into RAM. Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are un-powered. Typical RAM contents are shown in Figure 7.

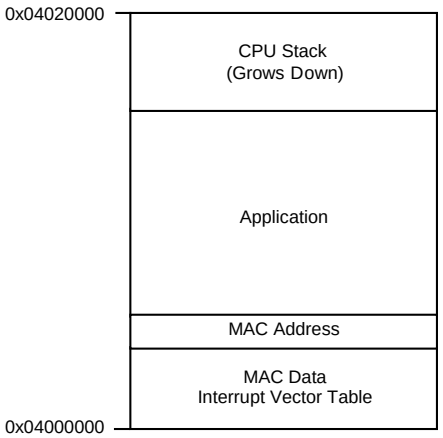


Figure 7: Typical RAM Contents

4.3 OTP eFuse Memory

The JN5148 contains a total of 32bytes of eFuse memory; this is a One Time Programmable (OTP) memory that can be used to support on chip 64-bit MAC ID and a 128-bit AES security key. A limited number of bits are available for customer use for storage of configuration information; configuration of these is made through use of software APIs.

For further information on how to program and use the eFuse memory, please contact technical support via the on-line tech-support system.

Alternatively, NXP can provide an eFuse programming service for customers that wish to use the eFuse but do not wish to undertake this for themselves. For further details of this service, please contact your local NXP sales office.

4.4 External Memory

An external memory with an SPI interface may be used to provide storage for program code and data for the device when external power is removed. The memory is connected to the SPI interface using select line SPISEL0; this select line is dedicated to the external memory interface and is not available for use with other external devices. See Figure 8 for connection details.

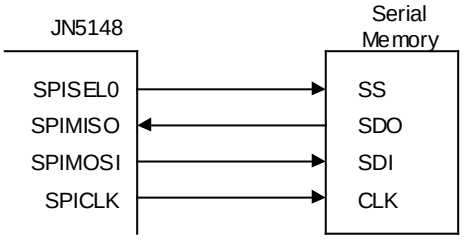


Figure 8: Connecting External Serial Memory

At reset, the contents of this memory are copied into RAM by the software boot loader. The Flash memory devices that are supported as standard through the JN5148 bootloader are given in Table 1. NXP recommends that where possible one of these devices should be selected.

Manufacturer	Device Number
SST (Silicon Storage Technology)	25VF010A (1Mbit device)
Numonyx	M25P10-A (1Mbit device), M25P40 (4Mbit device)

Table 1: Supported Flash Memories

Applications wishing to use an alternate Flash memory device should refer to application note [2] JN-AN-1038 Programming Flash devices not supported by the JN51xx ROM-based bootloader. This application note provides guidance on developing an interface to an alternate device.

4.4.1 External Memory Encryption

The contents of the external serial memory may be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in eFuse.

When bootloading program code from external serial memory, the JN5148 automatically accesses the encryption key to execute the decryption process. User program code does not need to handle any of the decryption process; it is transparent.

With encryption enabled, the time taken to boot code from external flash is increased.

4.5 Peripherals

All peripherals have their registers mapped into the memory space. Access to these registers requires 3 clock cycles. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see the JN51xx Integrated Peripherals API User Guide (JN-UG-3066)[5].

4.6 Unused Memory Addresses

Any attempt to access an unpopulated memory area will result in a bus error exception (interrupt) being generated.

8 Wireless Transceiver

The wireless transceiver comprises a 2.45GHz radio, modem, a baseband processor, a security coprocessor and PHY controller. These blocks, with protocol software provided as a library, implement an IEEE802.15.4 standards-based wireless transceiver that transmits and receives data over the air in the unlicensed 2.4GHz band.

8.1 Radio

Figure 14 shows the single ended radio architecture.

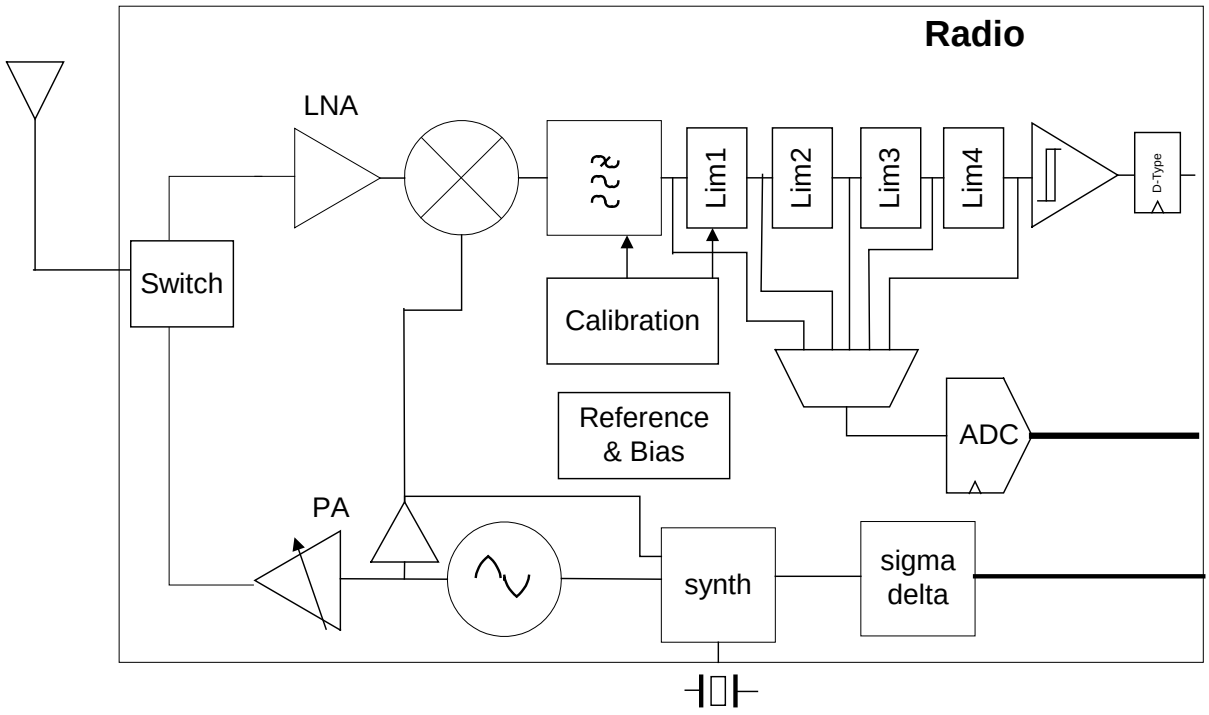


Figure 14: Radio Architecture

The radio comprises a low-IF receive path and a direct modulation transmit path, which converge at the TX/RX switch. The switch connects to the external single ended matching network, which consists of two inductors and a capacitor, this arrangement creates a 50Ω port and removes the need for a balun. A 50Ω single ended antenna can be connected directly to this port.

The 32MHz crystal oscillator feeds a divider, which provides the frequency synthesiser with a reference frequency. The synthesiser contains programmable feedback dividers, phase detector, charge pump and internal Voltage Controlled Oscillator (VCO). The VCO has no external components, and includes calibration circuitry to compensate for differences in internal component values due to process and temperature variations. The VCO is controlled by a Phase Locked Loop (PLL) that has an internal loop filter. A programmable charge pump is also used to tune the loop characteristic.

The receiver chain starts with the low noise amplifier / mixer combination whose outputs are passed to a lowpass filter, which provides the channel definition. The signal is then passed to a series of amplifier blocks forming a limiting strip. The signal is converted to a digital signal before being passed to the Modem. The gain control for the RX path is derived in the automatic gain control (AGC) block within the Modem, which samples the signal level at various points down the RX chain. To improve the performance and reduce current consumption, automatic calibration is applied to various blocks in the RX path.

In the transmit direction, the digital stream from the Modem is passed to a digital sigma-delta modulator which controls the feedback dividers in the synthesiser, (dual point modulation). The VCO frequency now tracks the applied modulation. The 2.4 GHz signal from the VCO is then passed to the RF Power Amplifier (PA), whose power control can be selected from one of three settings. The output of the PA drives the antenna via the RX/TX switch

8.2 Modem

The modem performs all the necessary modulation and spreading functions required for digital transmission and reception of data at 250kbps in the 2450MHz radio frequency band in compliance with the IEEE802.15.4 standard. It also provides a high data rate modes at 500 and 667kbps.

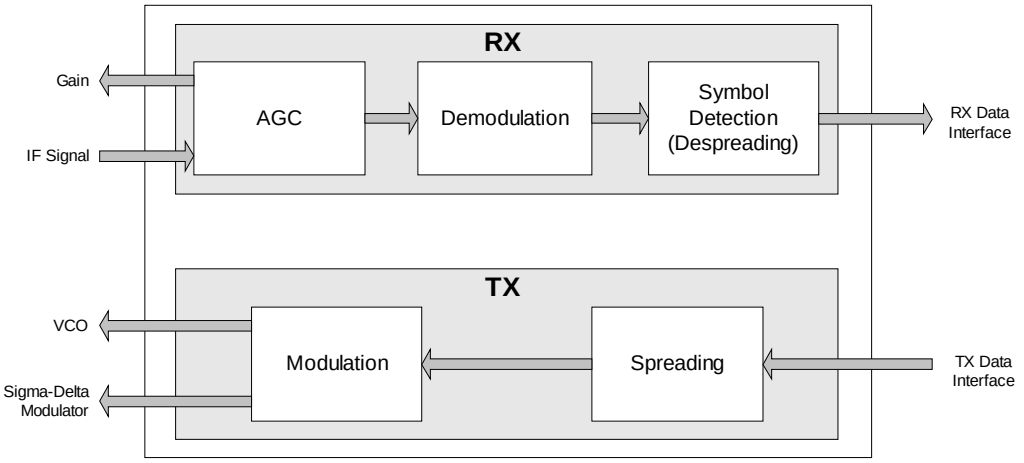


Figure 18 Modem Architecture

Features provided to support network channel selection algorithms include Energy Detection (ED), Link Quality Indication (LQI) and fully programmable Clear Channel Assessment (CCA).

The Modem provides a digital Receive Signal Strength Indication (RSSI) that facilitates the implementation of the IEEE 802.15.4 ED function and LQI function.

The ED and LQI are both related to receiver power in the same way, as shown in Fig19. LQI is associated with a received packet, whereas ED is an indication of signal power on air at a particular moment.

The CCA capability of the Modem supports all modes of operation defined in the IEEE 802.15.4 standard, namely Energy above ED threshold, Carrier Sense and Carrier Sense and/or energy above ED threshold.

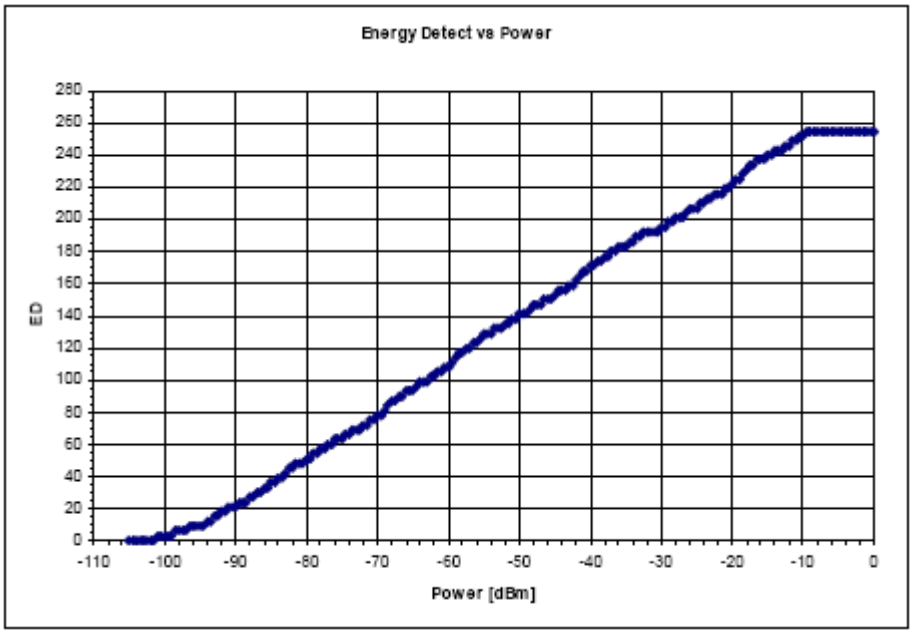


Figure 19 Energy Detect Value vs Receive Power Level

8.3 Baseband Processor

The baseband processor provides all time-critical functions of the IEEE802.15.4 MAC layer. Dedicated hardware guarantees air interface timing is precise. The MAC layer hardware/software partitioning, enables software to implement the sequencing of events required by the protocol and to schedule timed events with millisecond resolution, and the hardware to implement specific events with microsecond timing resolution. The protocol software layer performs the higher-layer aspects of the protocol, sending management and data messages between endpoint and coordinator nodes, using the services provided by the baseband processor.

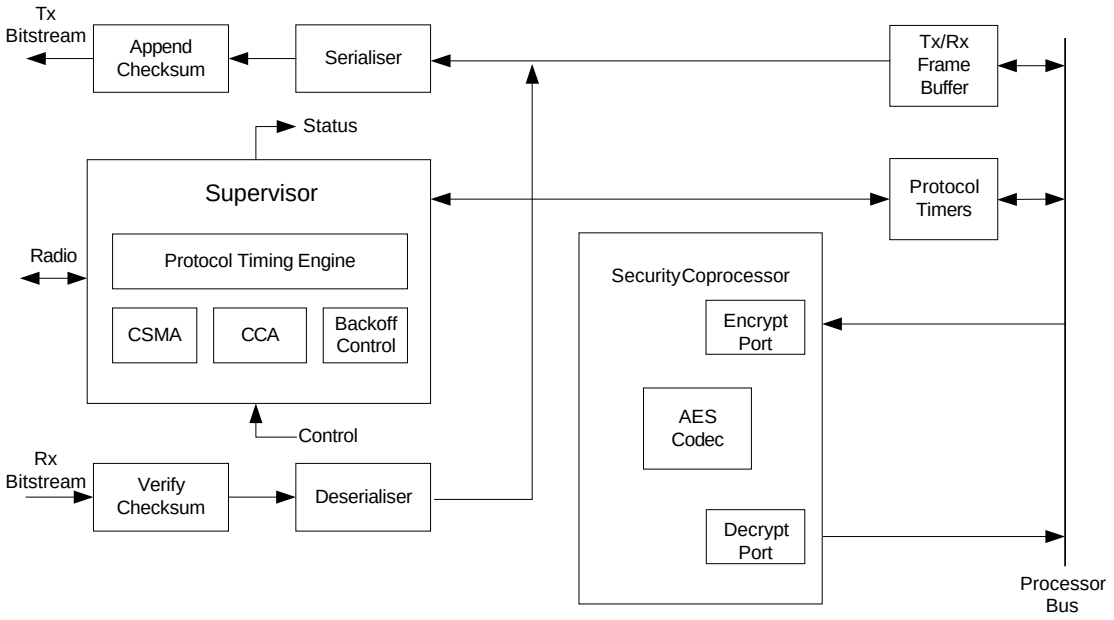


Figure 20: Baseband Processor

8.3.1 Transmit

A transmission is performed by software writing the data to be transferred into the Tx/Rx Frame Buffer, together with parameters such as the destination address and the number of retries allowed, and programming one of the protocol timers to indicate the time at which the frame is to be sent. This time will be determined by the software tracking the higher-layer aspects of the protocol such as superframe timing and slot boundaries. Once the packet is prepared and protocol timer set, the supervisor block controls the transmission. When the scheduled time arrives, the supervisor controls the sequencing of the radio and modem to perform the type of transmission required. It can perform all the algorithms required by IEEE802.15.4 such as CSMA/CA, GTS without processor intervention including retries and random backoffs.

When the transmission begins, the header of the frame is constructed from the parameters programmed by the software and sent with the frame data through the serialiser to the Modem. At the same time, the radio is prepared for transmission. During the passage of the bitstream to the modem, it passes through a CRC checksum generator that calculates the checksum on-the-fly, and appends it to the end of the frame.

If using slotted access, it is possible for a transmission to overrun the time in its allocated slot; the Baseband Processor handles this situation autonomously and notifies the protocol software via interrupt, rather than requiring it to handle the overrun explicitly.

8.3.2 Reception

During reception, the radio is set to receive on a particular channel. On receipt of data from the modem, the frame is directed into the Tx/Rx Frame Buffer where both header and frame data can be read by the protocol software. An interrupt may be provided on receipt of the frame header. As the frame data is being received from the modem it is passed through a checksum generator; at the end of the reception the checksum result is compared with the checksum at the end of the message to ensure that the data has been received correctly. An interrupt may be

provided to indicate successful packet reception. During reception, the modem determines the Link Quality, which is made available at the end of the reception as part of the requirements of IEEE802.15.4.

8.3.3 Auto Acknowledge

Part of the protocol allows for transmitted frames to be acknowledged by the destination sending an acknowledge packet within a very short window after the transmitted frame has been received. The JN5148 baseband processor can automatically construct and send the acknowledgement packet without processor intervention and hence avoid the protocol software being involved in time-critical processing within the acknowledge sequence. The JN5148 baseband processor can also request an acknowledge for packets being transmitted and handle the reception of acknowledged packets without processor intervention.

8.3.4 Beacon Generation

In beaconing networks, the baseband processor can automatically generate and send beacon frames; the repetition rate of the beacons is programmed by the CPU, and the baseband then constructs the beacon contents from data delivered by the CPU. The baseband processor schedules the beacons and transmits them without CPU intervention.

8.3.5 Security

The transmission and reception of secured frames using the Advanced Encryption Standard (AES) algorithm is handled by the security coprocessor and the stack software. The application software must provide the appropriate encrypt/decrypt keys for the transmission or reception. On transmission, the key can be programmed at the same time as the rest of the frame data and setup information.

8.4 Security Coprocessor

The security coprocessor is available to the application software to perform encryption/decryption operations. A hardware implementation of the encryption engine significantly speeds up the processing of the encrypted packets over a pure software implementation. The AES library for the JN5148 provides operations that utilise the encryption engine in the device and allow the contents of memory buffers to be transformed. Information such as the type of security operation to be performed and the encrypt/decrypt key to be used must also be provided.

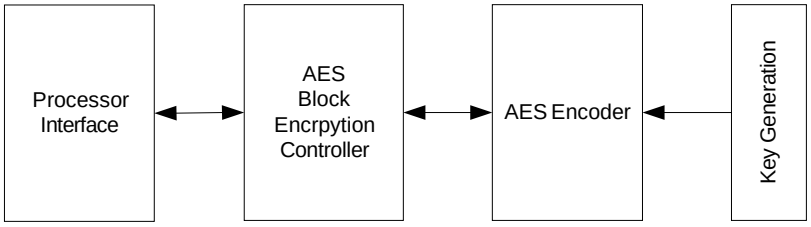


Figure 21: Security Coprocessor Architecture

8.5 Location Awareness

The JN5148 provides the ability for an application to obtain the Time Of Flight (TOF) between two network nodes. The TOF information is an alternative metric to that of the existing Energy Detect value (RSSI) that has been typically used for calculating the relative inter-nodal separation, for subsequent use in a location awareness system.

For short ranges RSSI will typically give a better accuracy than TOF, however for distances above 5 to 10 meters TOF will offer significant improvements in accuracy compared to RSSI. In general, the RSSI error scales with distance, such that if the distance doubles then the error doubles.

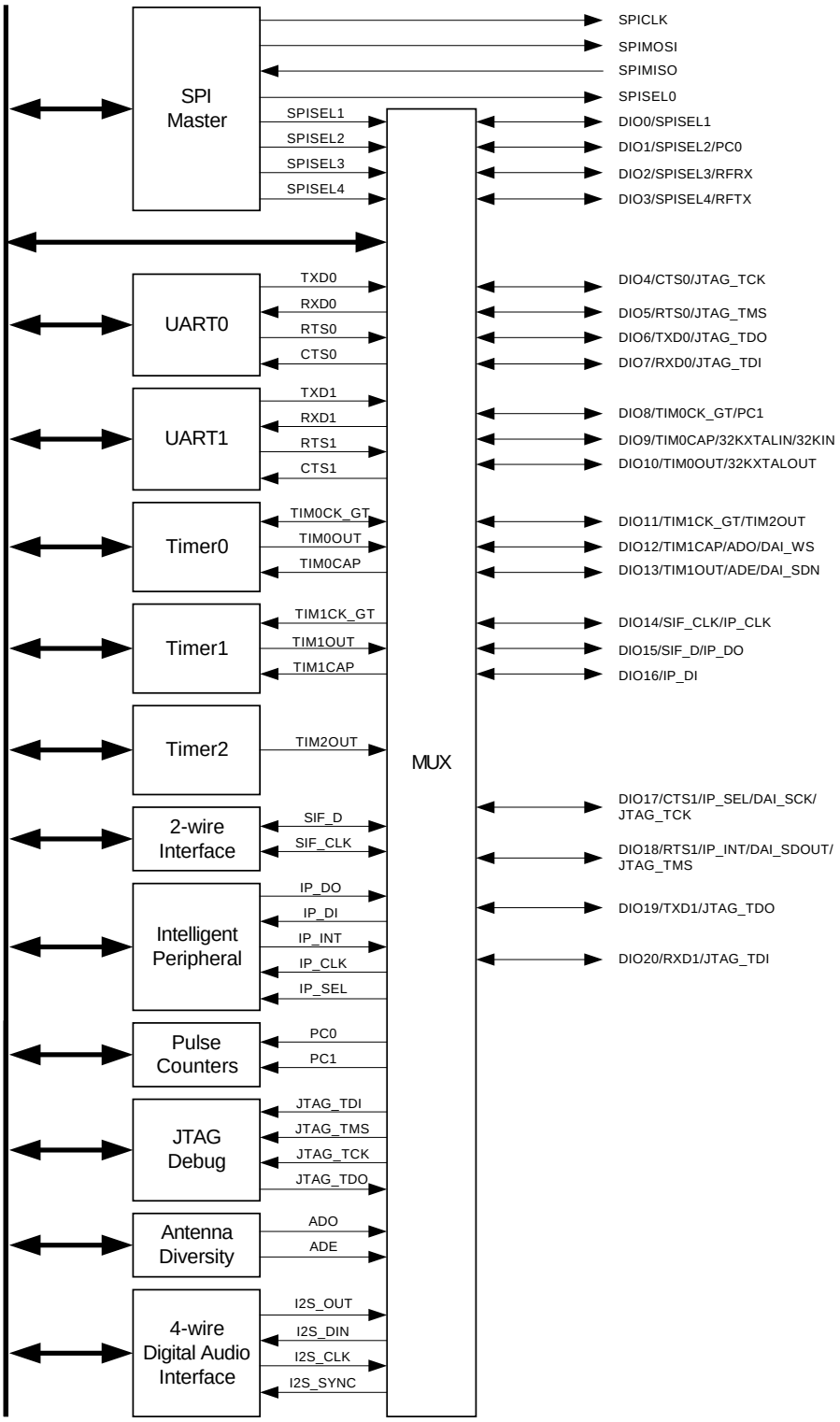


Figure 22 DIO Block Diagram

22.3.16 Radio Transceiver

This JN5148 meets all the requirements of the IEEE802.15.4 standard over 2.0 - 3.6V and offers the following improved RF characteristics. All RF characteristics are measured single ended.

This part also meets the following regulatory body approvals, when used with NXP's Module Reference Designs. Compliant with FCC part 15, rules, IC Canada, ETSI ETS 300-328 and Japan ARIB STD-T66

The PCB schematic and layout rules detailed in Appendix B.4 must be followed. Failure to do so will likely result in the JN5148 failing to meet the performance specification detailed herein and worst case may result in device not functioning in the end application.

Parameter	Min	Typical	Max	Notes
RF Port Characteristics				
Type				Single Ended
Impedance [1]		50ohm		2.4-2.5GHz
Frequency range	2.400 GHz		2.485GHz	
ESD levels (pin 17)		TDB		

1) With external matching inductors and assuming PCB layout as in Appendix B.4.

Radio Parameters: 2.0-3.6V, +25ºC

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity	-92	-95		dBm	Nominal for 1% PER, as per 802.15.4 section 6.5.3.3
Maximum input signal		+5		dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection (-1/+1 ch) [CW Interferer]		19/34 [27/49]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Alternate channel rejection (-2 / +2 ch) [CW Interferer]		40/45 [54/54]		dBc	For 1% PER, with wanted signal 3dB, above sensitivity. (Note1,2) (modulated interferer)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		48		dBc	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		52		dBc	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 8dB lower. (Note1)
Spurious emissions (RX)		 -61	 <-70 -58	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		40		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm. Available through Hardware API
Transmitter Characteristics					
Transmit power	+0.5	+2.5		dBm	
Output power control range		-35		dB	In three 12dB steps (Note3)
Spurious emissions (TX)		 -40	 <-70 <-70	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz
EVM [Offset]		10 [2.0]	15	%	At maximum output power
Transmit Power Spectral Density		-38	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, section 6.5.3.1