MC33272A, MC33274A, NCV33272A, NCV33274A

Single Supply, High Slew Rate, Low Input Offset Voltage Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip−R−Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual−doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

Features

- Input Offset Voltage Trimmed to 100 μV (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 MΩ
- Low Noise: 18 nV/$\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/μs
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ −14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or ±1.5 V to ±18 V
- ESD Diodes Provide Added Protection to the Inputs
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- Pb−Free Packages are Available

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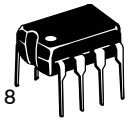
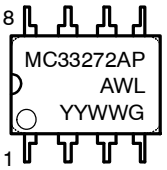
MARKING DIAGRAMS

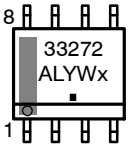
DUAL



PDIP−8
P SUFFIX
CASE 626

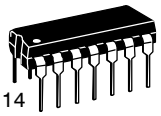


SOIC−8
D SUFFIX
CASE 751



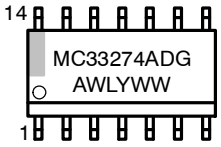
x = A for MC33272AD/DR2
= N for NCV33272ADR2

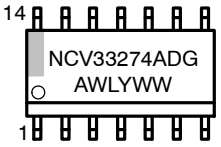
QUAD

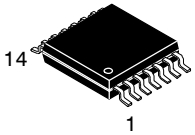


PDIP−14
P SUFFIX
CASE 646

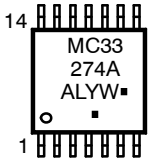
SOIC−14
D SUFFIX
CASE 751A

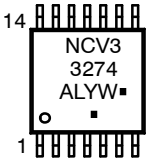






TSSOP−14
DTB SUFFIX
CASE 948G





A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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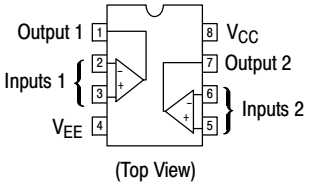
PIN CONNECTIONS

DUAL

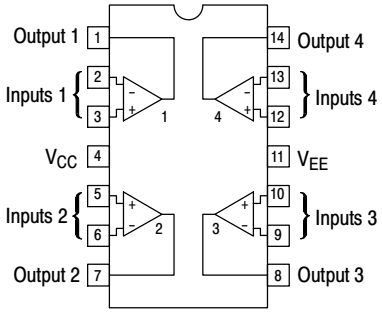
CASE 626/751



(Top View)

QUAD

CASE 646/751A/948G



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
ESD Protection at Any Pin – Human Body Model – Machine Model	V_{esd}	 2000 200	V
Maximum Power Dissipation	P_D	Note 2	mW
Operating Temperature Range MC33272A, MC33274A NCV33272A, NCV33274A	T_A	−40 to +85 −40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\|V_{IO}\|$				mV
(V_{CC} = +15 V, V_{EE} = −15 V)						
T_A = +25°C			–	0.1	1.0	
T_A = −40° to +85°C			–	–	1.8	
T_A = −40° to +125°C (NCV33272A)			–	–	2.5	
T_A = −40° to +125°C (NCV33274A)			–	–	3.5	
(V_{CC} = 5.0 V, V_{EE} = 0)						
T_A = +25°C			–	–	2.0	
Average Temperature Coefficient of Input Offset Voltage	3	$\Delta V_{IO}/\Delta T$				μV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = −40° to +125°C			–	2.0	–	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 5	I_{IB}				nA
T_A = +25°C			–	300	650	
T_A = T_{low} to T_{high}			–	–	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\|I_{IO}\|$				nA
T_A = +25°C			–	3.0	65	
T_A = T_{low} to T_{high}			–	–	80	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	6	V_{ICR}				V
T_A = +25°C			V_{EE} to (V_{CC} −1.8)			
Large Signal Voltage Gain (V_O = 0 V to 10 V, R_L = 2.0 kΩ)	7	A_{VOL}				dB
T_A = +25°C			90	100	–	
T_A = T_{low} to T_{high}			86	–	–	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 12					V
(V_{CC} = +15 V, V_{EE} = −15 V)						
R_L = 2.0 kΩ		V_O+	13.4	13.9	–	
R_L = 2.0 kΩ		V_O−	–	−13.9	−13.5	
R_L = 10 kΩ		V_O+	13.4	14	–	
R_L = 10 kΩ		V_O−	–	−14.7	−14.1	
(V_{CC} = 5.0 V, V_{EE} = 0 V)	10, 11					
R_L = 2.0 kΩ		V_{OL}	–	–	0.2	
R_L = 2.0 kΩ		V_{OH}	3.7	–	5.0	
Common Mode Rejection (V_{in} = +13.2 V to −15 V)	13	CMR	80	100	–	dB
Power Supply Rejection	14, 15	PSR				dB
V_{CC}/V_{EE} = +15 V/ −15 V, +5.0 V/ −15 V, +15 V/ −5.0 V			80	105	–	
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	16	I_{SC}				mA
Source			+25	+37	–	
Sink			−25	−37	–	
Power Supply Current Per Amplifier (V_O = 0 V)	17	I_{CC}				mA
(V_{CC} = +15 V, V_{EE} = −15 V)						
T_A = +25°C			–	2.15	2.75	
T_A = T_{low} to T_{high}			–	–	3.0	
(V_{CC} = 5.0 V, V_{EE} = 0 V)						
T_A = +25°C			–	–	2.75	

3. MC33272A, MC33274A T_{low} = −40°C T_{high} = +85°C
   NCV33272A, NCV33274A T_{low} = −40°C T_{high} = +125°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	18, 33	SR	8.0	10	–	V/μs
Gain Bandwidth Product (f = 100 kHz)	19	GBW	17	24	–	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	20, 21, 22	A_{VO}	–	65	–	dB
Unity Gain Bandwidth (Open Loop)		BW	–	5.5	–	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 24, 26	A_m	–	12	–	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 25, 26	ϕ_m	–	55	–	Deg
Channel Separation (f = 20 Hz to 20 kHz)	27	CS	–	−120	–	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	–	160	–	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	28	THD	–	0.003	–	%
Open Loop Output Impedance (V_O = 0 V, f = 6.0 MHz)	29	$\|Z_O\|$	–	35	–	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	–	16	–	MΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	–	3.0	–	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	30	e_n	–	18	–	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	31	i_n	–	0.5	–	$pA/\sqrt{Hz}$

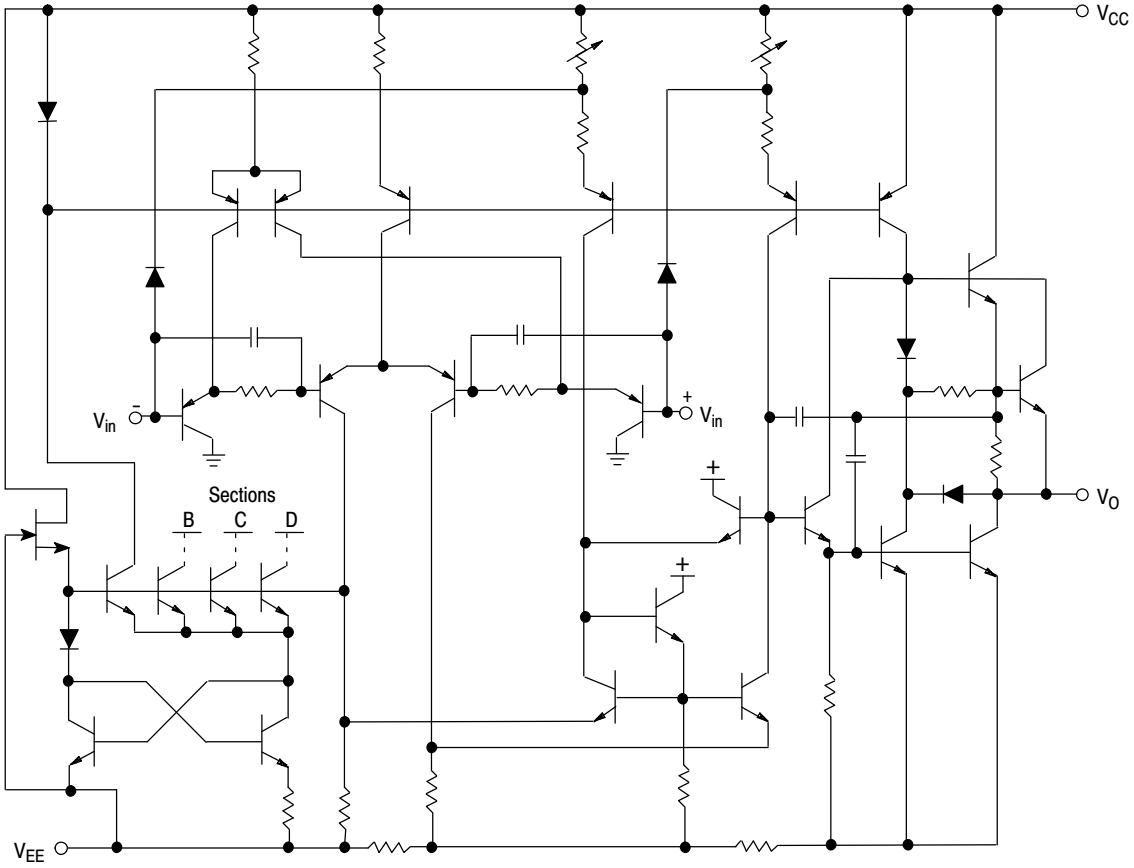


Figure 1. Equivalent Circuit Schematic
(Each Amplifier)