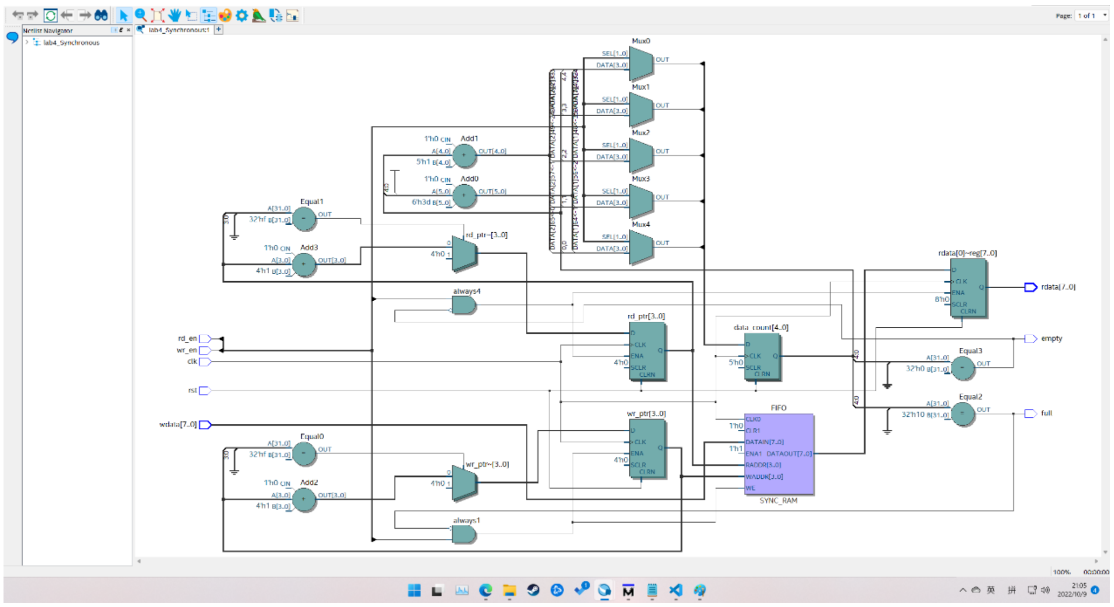
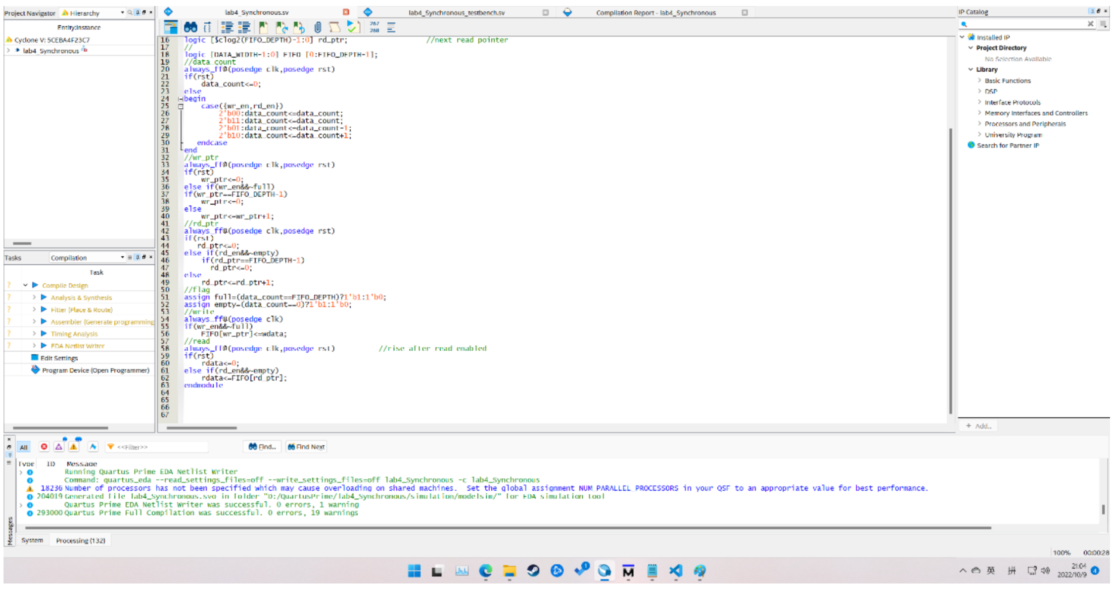
This lab uses 4 hours.

Synchronous code

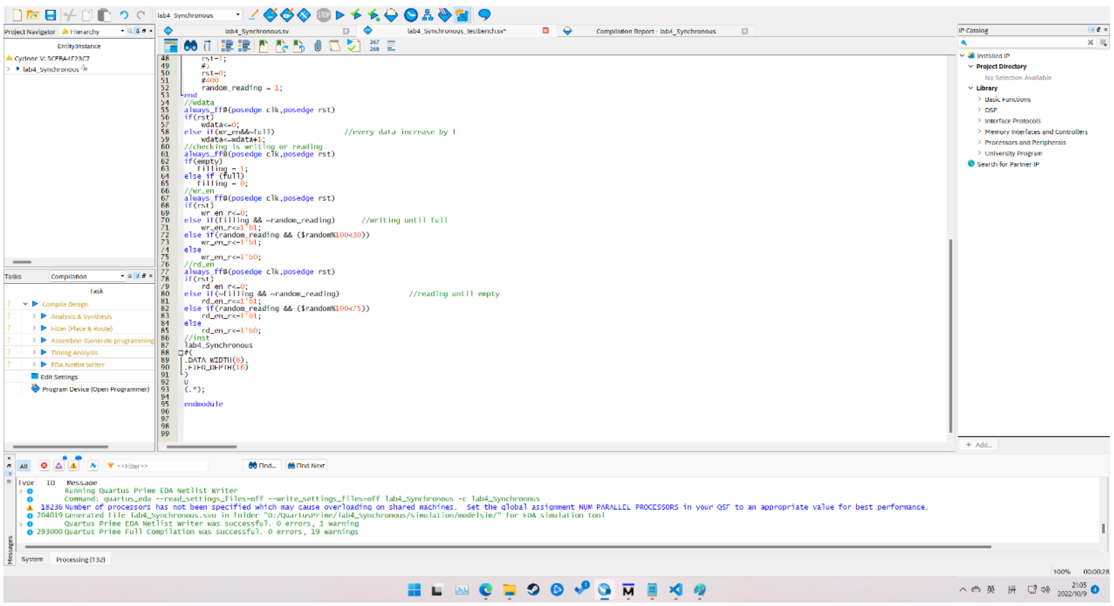




```
logic [$clog2(FIFO_DEPTH)-1:0] rd_ptr;                    //next read pointer
//
logic [DATA_WIDTH-1:0] FIFO [0:FIFO_DEPTH-1];
//data_count
always_ff@(posedge clk,posedge rst)
if(rst)
    data_count<=0;
else
begin
    case({wr_en,rd_en})
        2'b00:data_count<=data_count;
        2'b11:data_count<=data_count;
        2'b01:data_count<=data_count-1;
        2'b10:data_count<=data_count+1;
   endcase
end
//wr_ptr
always_ff@(posedge clk,posedge rst)
if(rst)
    wr_ptr<=0;
else if(wr_en&&~full)
if(wr_ptr==FIFO_DEPTH-1)
    wr_ptr<=0;
else
    wr_ptr<=wr_ptr+1;
//rd_ptr
always_ff@(posedge clk,posedge rst)
if(rst)
   rd_ptr<=0;
else if(rd_en&&~empty)
    if(rd_ptr==FIFO_DEPTH-1)
      rd_ptr<=0;
else
    rd_ptr<=rd_ptr+1;
//flag
assign full=(data_count==FIFO_DEPTH)?1'b1:1'b0;
assign empty=(data_count==0)?1'b1:1'b0;
//write
always_ff@(posedge clk)
if(wr_en&&~full)
    FIFO[wr_ptr]<=wdata;
//read
always_ff@(posedge clk,posedge rst)           //rise after read enabled
if(rst)
    rdata<=0;
else if(rd_en&&~empty)
    rdata<=FIFO[rd_ptr];
endmodule
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Synchronous -c lab4_Synchronous
      18236  Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
      204019 Generated file lab4_Synchronous.svo in folder "D:/QuartusPrime/lab4_Synchronous/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
      293000 Quartus Prime Full Compilation was successful. 0 errors, 19 warnings
```

Synchronous testbench



```
    rst=1;
    #5
    rst=0;
    #400
    random_reading = 1;
end
//wdata
always_ff@(posedge clk,posedge rst)
if(rst)
    wdata<=0;
else if(wr_en&&~full)                    //every data increase by 1
    wdata<=wdata+1;
//checking is writing or reading
always_ff@(posedge clk,posedge rst)
if(empty)
   filling = 1;
else if (full)
   filling = 0;
//wr_en
always_ff@(posedge clk,posedge rst)
if(rst)
    wr_en_r<=0;
else if(filling && ~random_reading)      //writing until full
    wr_en_r<=1'b1;
else if(random_reading && ($random%100<30))
    wr_en_r<=1'b1;
else
    wr_en_r<=1'b0;
//rd_en
always_ff@(posedge clk,posedge rst)
if(rst)
    rd_en_r<=0;
else if(~filling && ~random_reading)             //reading until empty
    rd_en_r<=1'b1;
else if(random_reading && ($random%100<75))
    rd_en_r<=1'b1;
else
    rd_en_r<=1'b0;
//inst
lab4_Synchronous
#(
.DATA_WIDTH(8),
.FIFO_DEPTH(16)
)
U
(.*);

endmodule
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Synchronous -c lab4_Synchronous
     18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
    204019 Generated file lab4_Synchronous.svo in folder "D:/QuartusPrime/lab4_Synchronous/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
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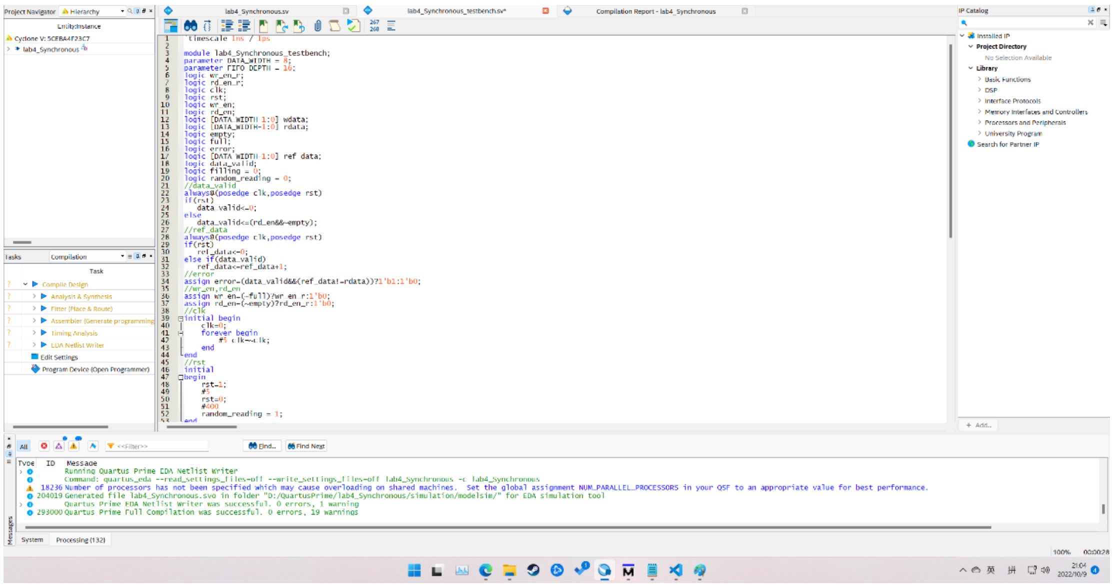
```

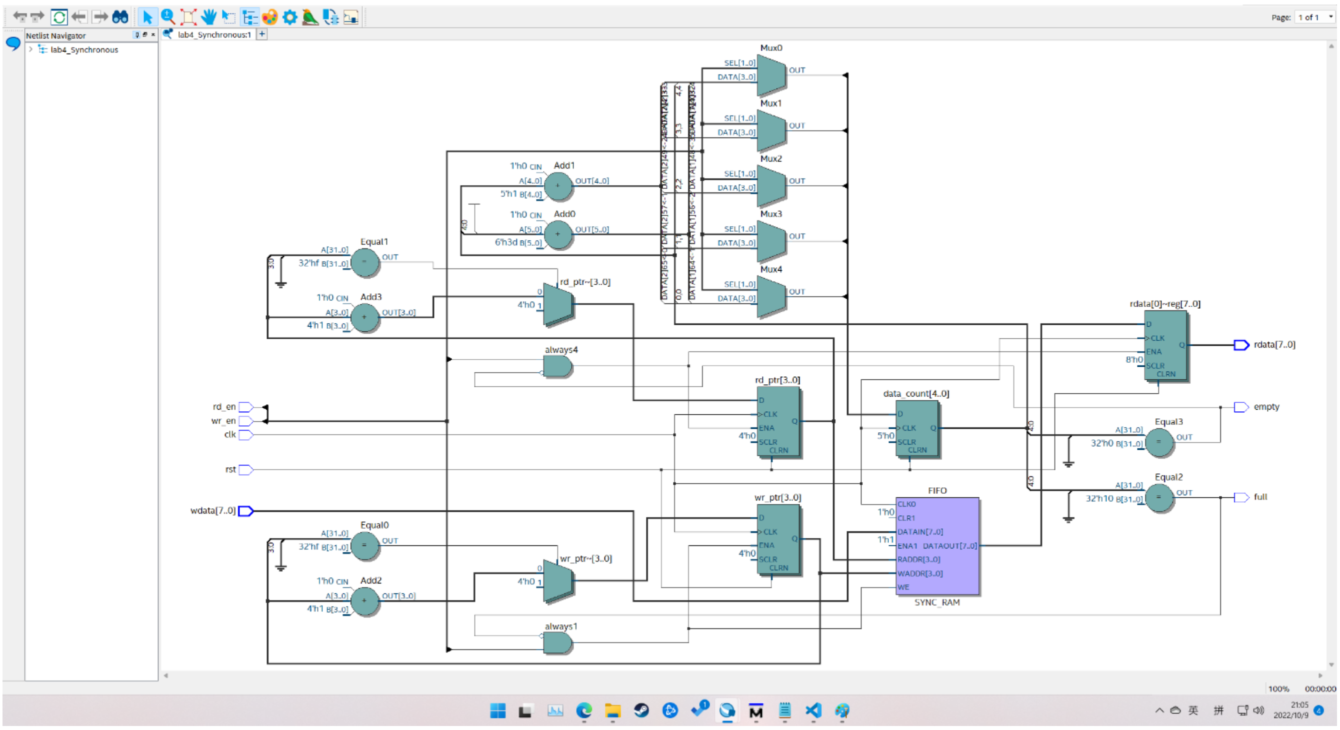


```
`timescale 1ns / 1ps

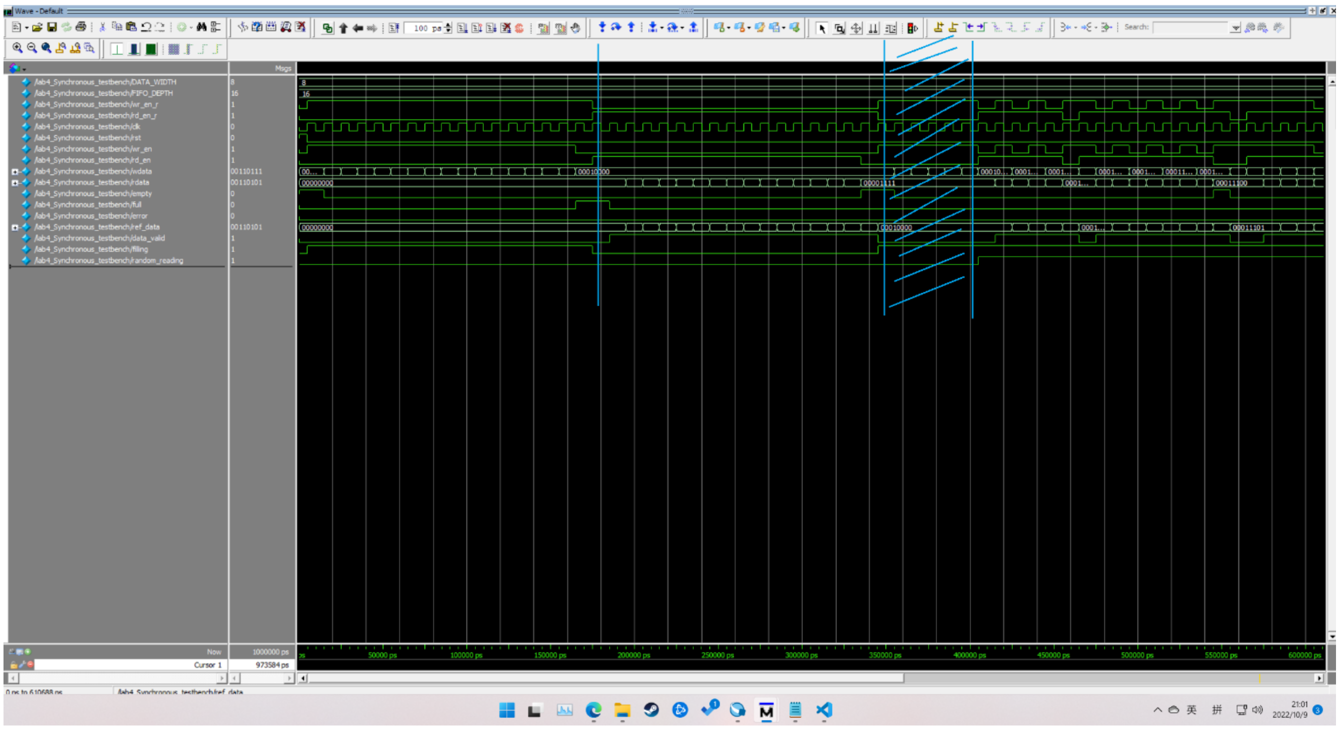
module lab4_Synchronous_testbench;
parameter DATA_WIDTH = 8;
parameter FIFO_DEPTH = 16;
logic wr_en_r;
logic rd_en_r;
logic clk;
logic rst;
logic wr_en;
logic rd_en;
logic [DATA_WIDTH-1:0] wdata;
logic [DATA_WIDTH-1:0] rdata;
logic empty;
logic full;
logic error;
logic [DATA_WIDTH-1:0] ref_data;
logic data_valid;
logic filling = 0;
logic random_reading = 0;
//data_valid
always@(posedge clk,posedge rst)
if(rst)
   data_valid<=0;
else
   data_valid<=(rd_en&&~empty);
//ref_data
always@(posedge clk,posedge rst)
if(rst)
   ref_data<=0;
else if(data_valid)
   ref_data<=ref_data+1;
//error
assign error=(data_valid&&(ref_data!=rdata))?1'b1:1'b0;
//wr_en,rd_en
assign wr_en=(~full)?wr_en_r:1'b0;
assign rd_en=(~empty)?rd_en_r:1'b0;
//clk
initial begin
    clk=0;
    forever begin
        #5 clk=~clk;
    end
end
//rst
initial
begin
    rst=1;
    #5
    rst=0;
    #400
    random_reading = 1;
end
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Synchronous -c lab4_Synchronous
     18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
    204019 Generated file lab4_Synchronous.svo in folder "D:/QuartusPrime/lab4_Synchronous/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
    293000 Quartus Prime Full Compilation was successful. 0 errors, 19 warnings
```

Synchronous RTL

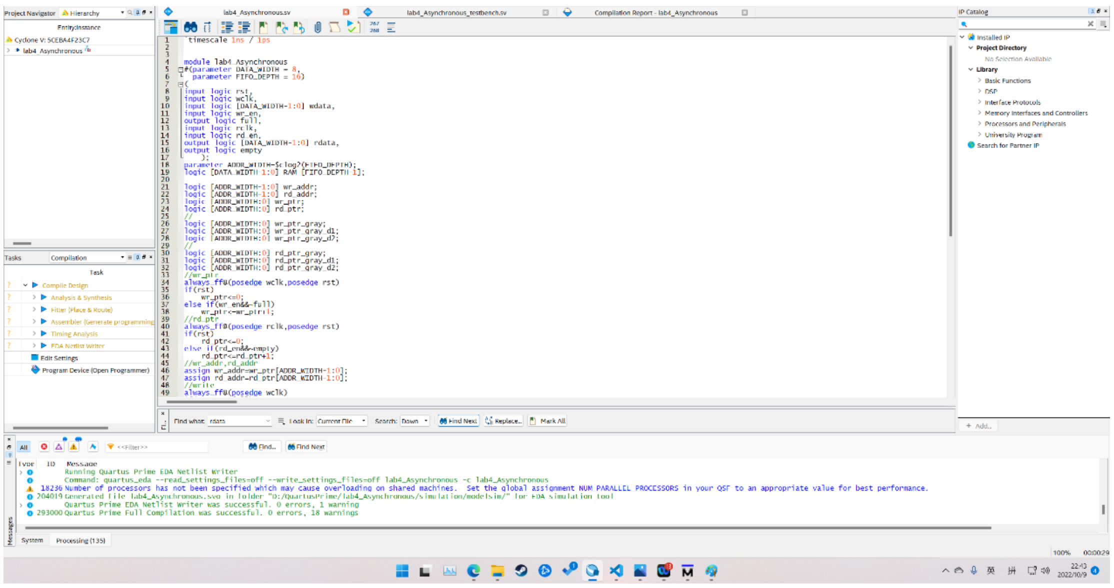


Synchronous waveform



The first section is let FIFO write from 0 to 16. At first, empty is high, after first data is written, it is low. When data is 16, the FIFO is full, so full is high. Then in the second section, FIFO reads data, from 0 to 16. Then empty is high again. In third section, the FIFO randomly reads and writes. So both read and write would trigger randomly. The waveform is as expected.

Asynchronous code

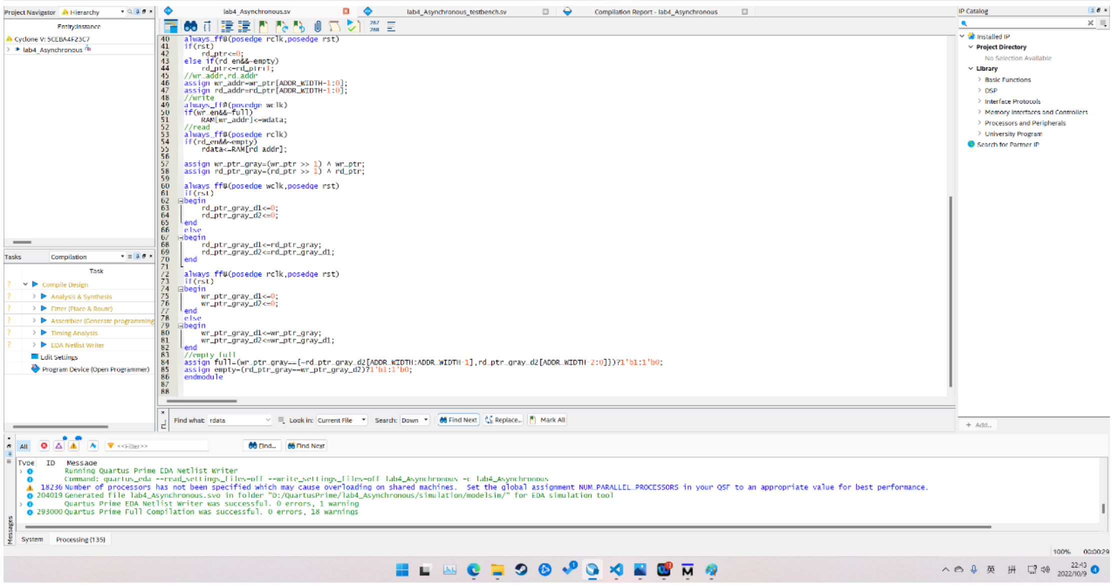


```
`timescale 1ns / 1ps


module lab4_Asynchronous
#(parameter DATA_WIDTH = 8,
  parameter FIFO_DEPTH = 16)
(
input logic rst,
input logic wclk,
input logic [DATA_WIDTH-1:0] wdata,
input logic wr_en,
output logic full,
input logic rclk,
input logic rd_en,
output logic [DATA_WIDTH-1:0] rdata,
output logic empty
    );
parameter ADDR_WIDTH=$clog2(FIFO_DEPTH);
logic [DATA_WIDTH-1:0] RAM [FIFO_DEPTH-1];

logic [ADDR_WIDTH-1:0] wr_addr;
logic [ADDR_WIDTH-1:0] rd_addr;
logic [ADDR_WIDTH:0] wr_ptr;
logic [ADDR_WIDTH:0] rd_ptr;
//
logic [ADDR_WIDTH:0] wr_ptr_gray;
logic [ADDR_WIDTH:0] wr_ptr_gray_d1;
logic [ADDR_WIDTH:0] wr_ptr_gray_d2;
//
logic [ADDR_WIDTH:0] rd_ptr_gray;
logic [ADDR_WIDTH:0] rd_ptr_gray_d1;
logic [ADDR_WIDTH:0] rd_ptr_gray_d2;
//wr_ptr
always_ff@(posedge wclk,posedge rst)
if(rst)
    wr_ptr<=0;
else if(wr_en&&~full)
    wr_ptr<=wr_ptr+1;
//rd_ptr
always_ff@(posedge rclk,posedge rst)
if(rst)
    rd_ptr<=0;
else if(rd_en&&~empty)
    rd_ptr<=rd_ptr+1;
//wr_addr,rd_addr
assign wr_addr=wr_ptr[ADDR_WIDTH-1:0];
assign rd_addr=rd_ptr[ADDR_WIDTH-1:0];
//write
always_ff@(posedge wclk)
```

```
Type  ID     Message
              Running Quartus Prime EDA Netlist Writer
              Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Asynchronous -c lab4_Asynchronous
      18236  Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
      204019 Generated file lab4_Asynchronous.svo in folder "D:/QuartusPrime/lab4_Asynchronous/simulation/modelsim/" for EDA simulation tool
              Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
      293000 Quartus Prime Full Compilation was successful. 0 errors, 18 warnings
```



```
always_ff@(posedge rclk,posedge rst)
if(rst)
    rd_ptr<=0;
else if(rd_en&&~empty)
    rd_ptr<=rd_ptr+1;
//wr_addr,rd_addr
assign wr_addr=wr_ptr[ADDR_WIDTH-1:0];
assign rd_addr=rd_ptr[ADDR_WIDTH-1:0];
//write
always_ff@(posedge wclk)
if(wr_en&&~full)
    RAM[wr_addr]<=wdata;
//read
always_ff@(posedge rclk)
if(rd_en&&~empty)
    rdata<=RAM[rd_addr];

assign wr_ptr_gray=(wr_ptr >> 1) ^ wr_ptr;
assign rd_ptr_gray=(rd_ptr >> 1) ^ rd_ptr;

always_ff@(posedge wclk,posedge rst)
if(rst)
begin
    rd_ptr_gray_d1<=0;
    rd_ptr_gray_d2<=0;
end
else
begin
    rd_ptr_gray_d1<=rd_ptr_gray;
    rd_ptr_gray_d2<=rd_ptr_gray_d1;
end

always_ff@(posedge rclk,posedge rst)
if(rst)
begin
    wr_ptr_gray_d1<=0;
    wr_ptr_gray_d2<=0;
end
else
begin
    wr_ptr_gray_d1<=wr_ptr_gray;
    wr_ptr_gray_d2<=wr_ptr_gray_d1;
end
//empty full
assign full=(wr_ptr_gray=={~rd_ptr_gray_d2[ADDR_WIDTH:ADDR_WIDTH-1],rd_ptr_gray_d2[ADDR_WIDTH-2:0]})?1'b1:1'b0;
assign empty=(rd_ptr_gray==wr_ptr_gray_d2)?1'b1:1'b0;
endmodule
```

```
Type  ID     Message
              Running Quartus Prime EDA Netlist Writer
              Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Asynchronous -c lab4_Asynchronous
      18236  Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
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              Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
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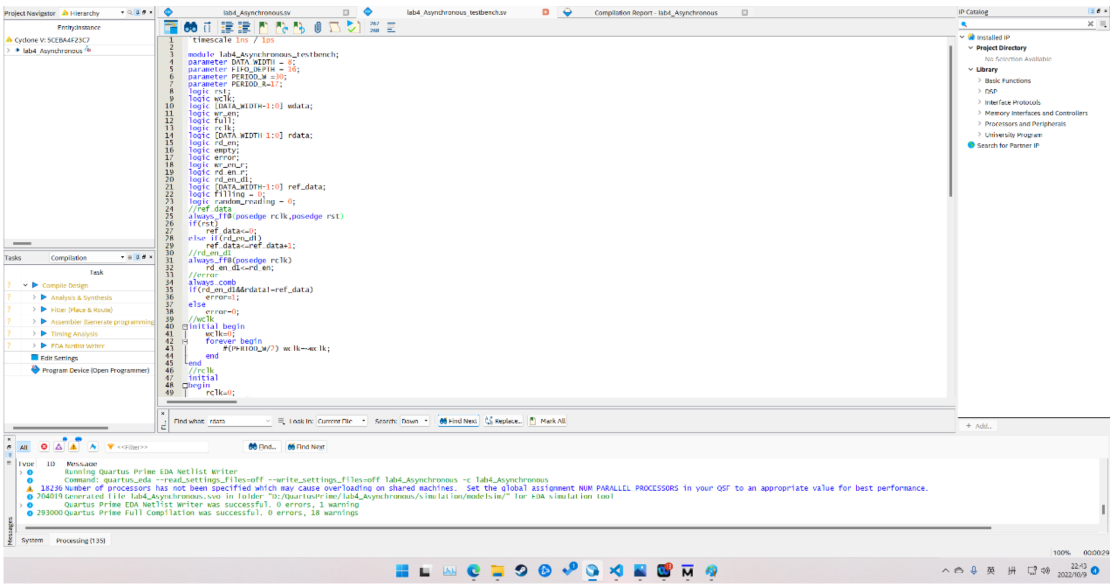
```

Asynchronous testbench



```
`timescale 1ns / 1ps

module lab4_Asynchronous_testbench;
parameter DATA_WIDTH = 8;
parameter FIFO_DEPTH = 16;
parameter PERIOD_W =30;
parameter PERIOD_R=17;
logic rst;
logic wclk;
logic [DATA_WIDTH-1:0] wdata;
logic wr_en;
logic full;
logic rclk;
logic [DATA_WIDTH-1:0] rdata;
logic rd_en;
logic empty;
logic error;
logic wr_en_r;
logic rd_en_r;
logic rd_en_d1;
logic [DATA_WIDTH-1:0] ref_data;
logic filling = 0;
logic random_reading = 0;
//ref_data
always_ff@(posedge rclk,posedge rst)
if(rst)
    ref_data<=0;
else if(rd_en_d1)
    ref_data<=ref_data+1;
//rd_en_d1
always_ff@(posedge rclk)
    rd_en_d1<=rd_en;
//error
always_comb
if(rd_en_d1&&rdata!=ref_data)
    error=1;
else
    error=0;
//wclk
initial begin
    wclk=0;
    forever begin
        #(PERIOD_W/2) wclk=~wclk;
    end
end
//rclk
initial
begin
    rclk=0;
```

```
Type  ID     Message
            Running Quartus Prime EDA Netlist Writer
            Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Asynchronous -c lab4_Asynchronous
      18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
      204019 Generated file lab4_Asynchronous.svo in folder "D:/QuartusPrime/lab4_Asynchronous/simulation/modelsim/" for EDA simulation tool
            Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
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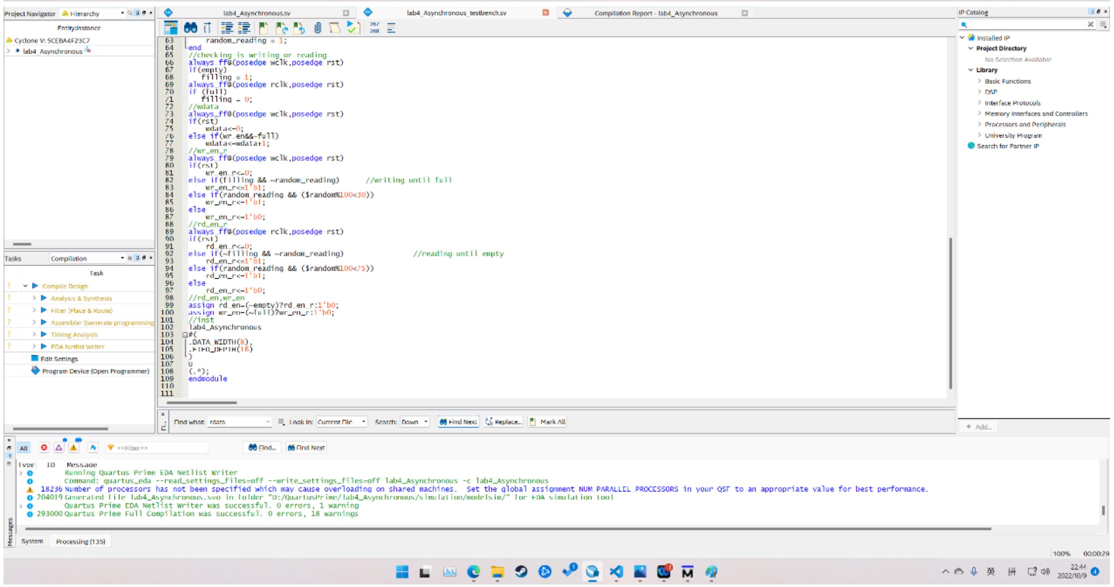
```



```
    random_reading = 1;
end
//checking is writing or reading
always_ff@(posedge wclk,posedge rst)
if(empty)
   filling = 1;
always_ff@(posedge rclk,posedge rst)
if (full)
   filling = 0;
//wdata
always_ff@(posedge wclk,posedge rst)
if(rst)
    wdata<=0;
else if(wr_en&&~full)
    wdata<=wdata+1;
//wr_en_r
always_ff@(posedge wclk,posedge rst)
if(rst)
    wr_en_r<=0;
else if(filling && ~random_reading)      //writing until full
    wr_en_r<=1'b1;
else if(random_reading && ($random%100<30))
    wr_en_r<=1'b1;
else
    wr_en_r<=1'b0;
//rd_en_r
always_ff@(posedge rclk,posedge rst)
if(rst)
    rd_en_r<=0;
else if(~filling && ~random_reading)              //reading until empty
    rd_en_r<=1'b1;
else if(random_reading && ($random%100<75))
    rd_en_r<=1'b1;
else
    rd_en_r<=1'b0;
//rd_en,wr_en
assign rd_en=(~empty)?rd_en_r:1'b0;
assign wr_en=(~full)?wr_en_r:1'b0;
//inst
lab4_Asynchronous
#(
.DATA_WIDTH(8),
.FIFO_DEPTH(16)
)
u
(.*);
endmodule
```

```
Type  ID     Message
            Running Quartus Prime EDA Netlist Writer
            Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Asynchronous -c lab4_Asynchronous
      18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
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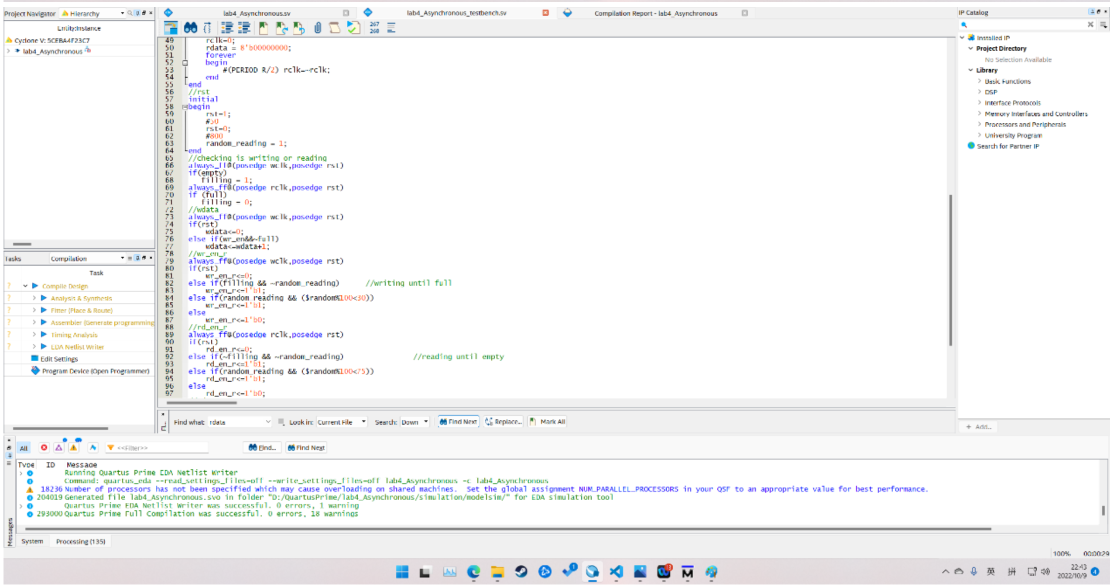

```
    rclk=0;
    rdata = 8'b00000000;
    forever
    begin
        #(PERIOD_R/2) rclk=~rclk;
    end
end
//rst
initial
begin
    rst=1;
    #50
    rst=0;
    #800
    random_reading = 1;
end
//checking is writing or reading
always_ff@(posedge wclk,posedge rst)
if(empty)
   filling = 1;
always_ff@(posedge rclk,posedge rst)
if (full)
   filling = 0;
//wdata
always_ff@(posedge wclk,posedge rst)
if(rst)
    wdata<=0;
else if(wr_en&&~full)
    wdata<=wdata+1;
//wr_en_r
always_ff@(posedge wclk,posedge rst)
if(rst)
    wr_en_r<=0;
else if(filling && ~random_reading)      //writing until full
    wr_en_r<=1'b1;
else if(random_reading && ($random%100<30))
    wr_en_r<=1'b1;
else
    wr_en_r<=1'b0;
//rd_en_r
always_ff@(posedge rclk,posedge rst)
if(rst)
    rd_en_r<=0;
else if(~filling && ~random_reading)              //reading until empty
    rd_en_r<=1'b1;
else if(random_reading && ($random%100<75))
    rd_en_r<=1'b1;
else
    rd_en_r<=1'b0;
```

```
Type  ID     Message
            Running Quartus Prime EDA Netlist Writer
            Command: quartus_eda --read_settings_files=off --write_settings_files=off lab4_Asynchronous -c lab4_Asynchronous
      18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
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            Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
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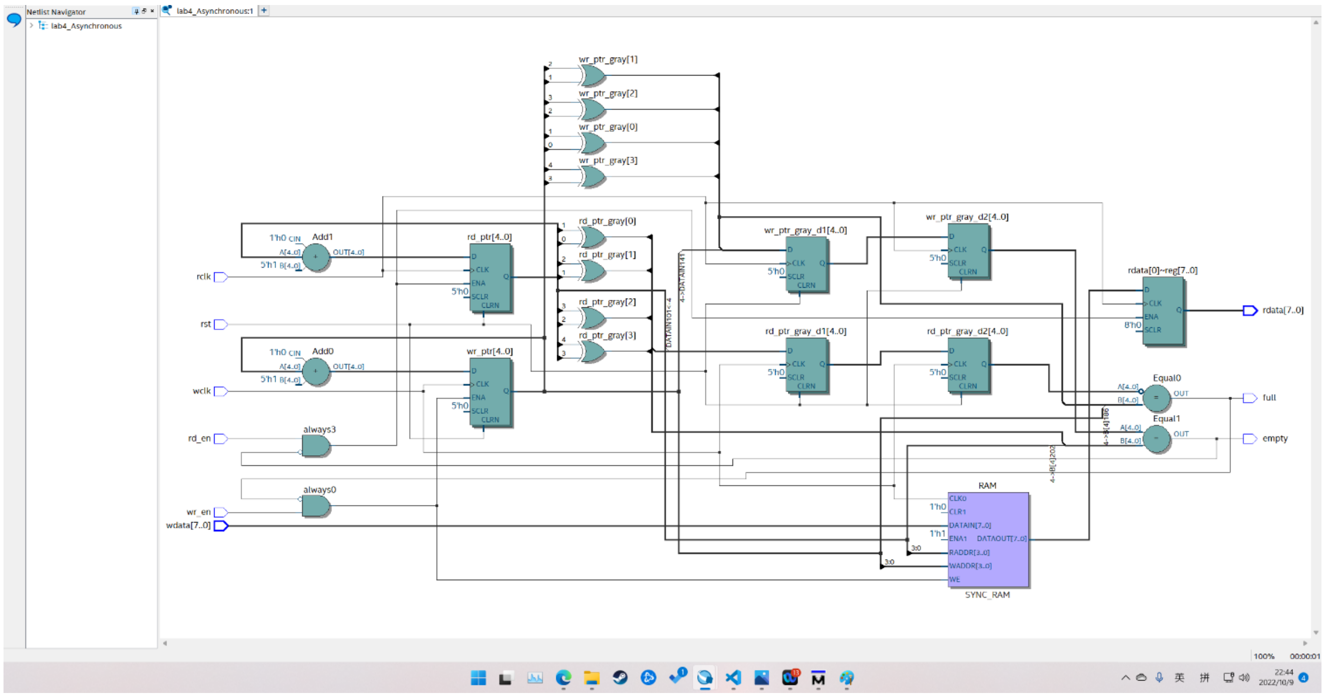
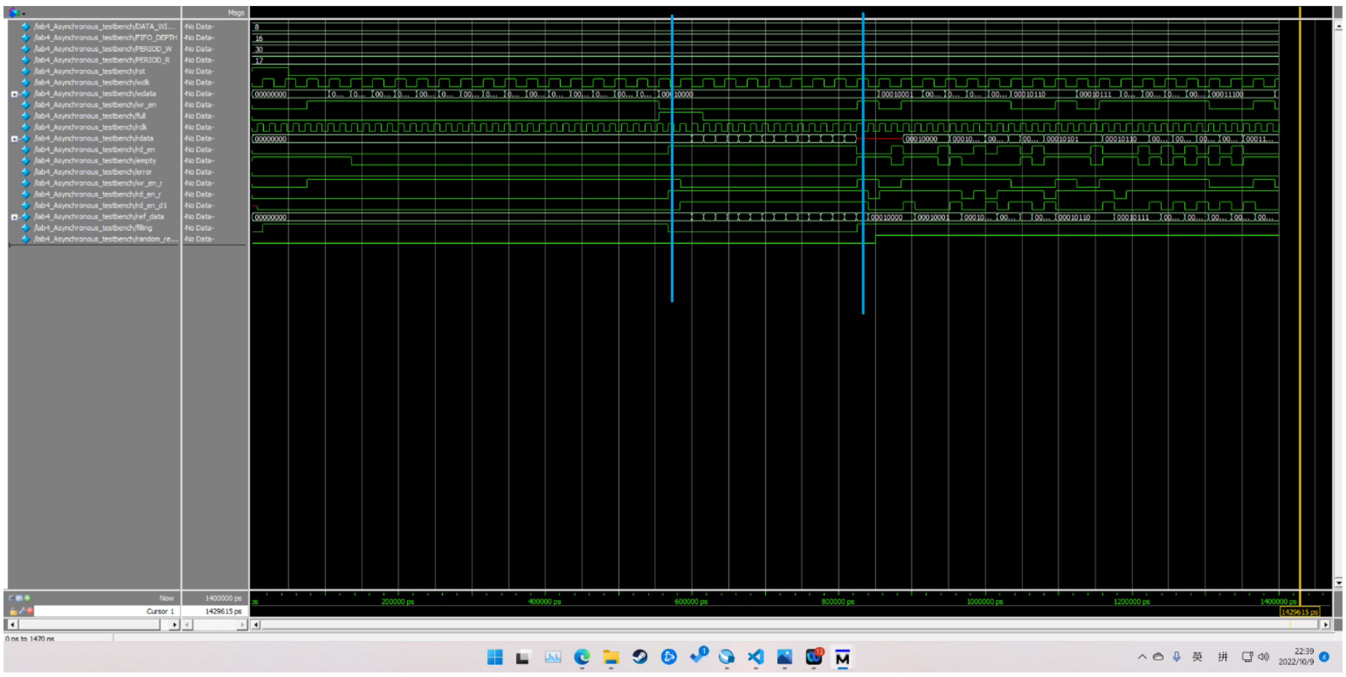
```

Asynchronous RTL



Asynchronous waveform



The full and empty is same as synchronous. Asynchronous focus on different clock in reading and writing. This uses grey code. Gray code pointers that are synchronized into the opposite clock domain before generating synchronous FIFO full or empty status signals. The three sections are writing until full, reading until empty, and reading and writing randomly. The waveform is as expected.