I spent 3.5h for this lab

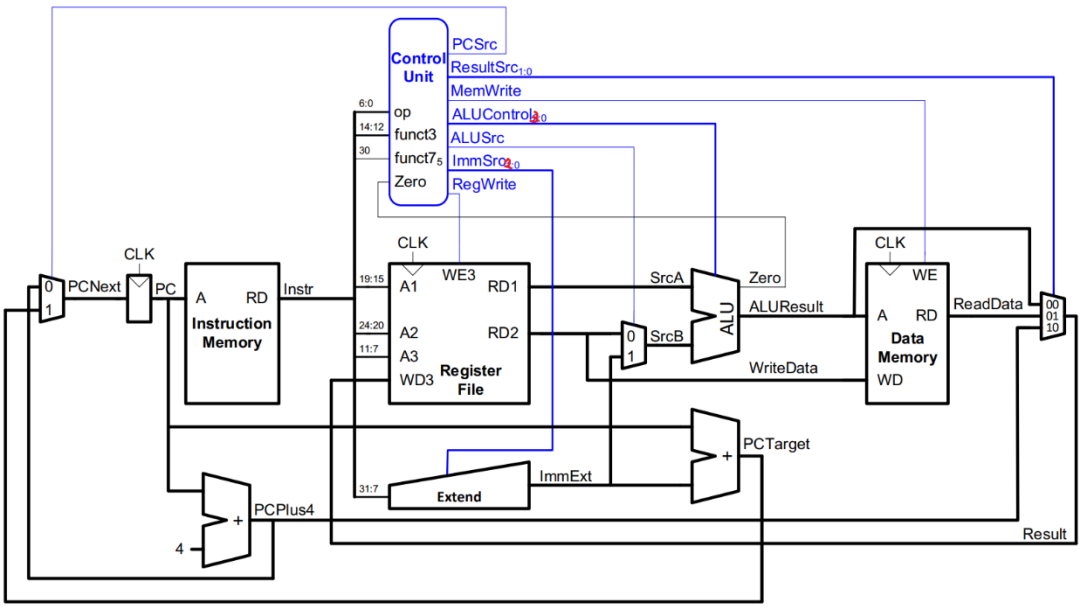


Figure 1: RISC-V single-cycle processor

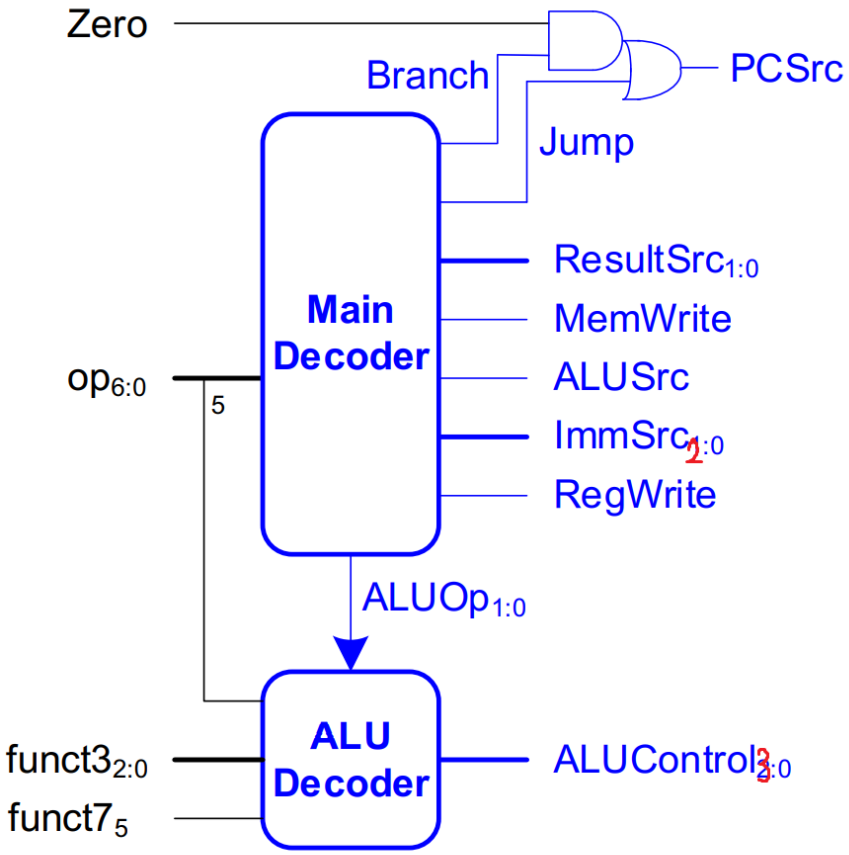


Figure 2: RISC-V single-cycle processor control unit

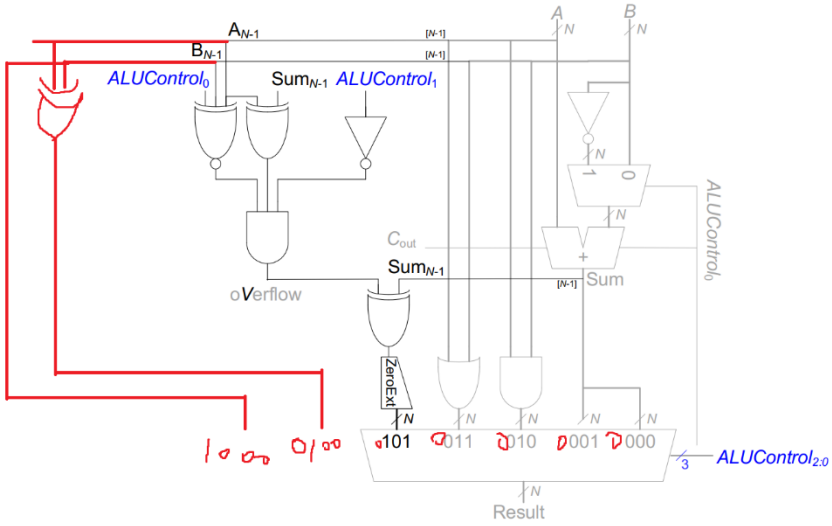


Figure 3: ALU

Table 1. Main Decoder Truth Table

Instruction	Opcode	RegWrite	ImmSrc	ALUSrcA	ALUSrcB	MemWrite	ResultSrc	Branch	ALUOp	Jump
lw	0000011	1	00	0	1	0	01	0	00	0
sw	0100011	0	01	0	1	1	xx	0	00	0
R-type	0110011	1	xx	0	0	0	00	0	10	0
beq	1100011	0	10	0	0	0	xx	1	01	0
I-type ALU	0010011	1	00	0	0	0	00	0	10	0
jal	1101111	1	11	x	x	0	10	0	xx	1

lui 0110111 1 100 x 1 0 00 0 11 0

Table 2. ALU Decoder Truth Table

$ALUOp_{1:0}$	$funct3_{2:0}$	$\{op_5, funct7_5\}$	$ALUControl_{2:0}$	Operation
00	x	x	000	Add
01	x	x	001	Subtract
10	000	00, 01, 10	000	Add
	000	11	001	Subtract
	010	x	101	SLT
	110	x	011	OR
	111	x	010	AND

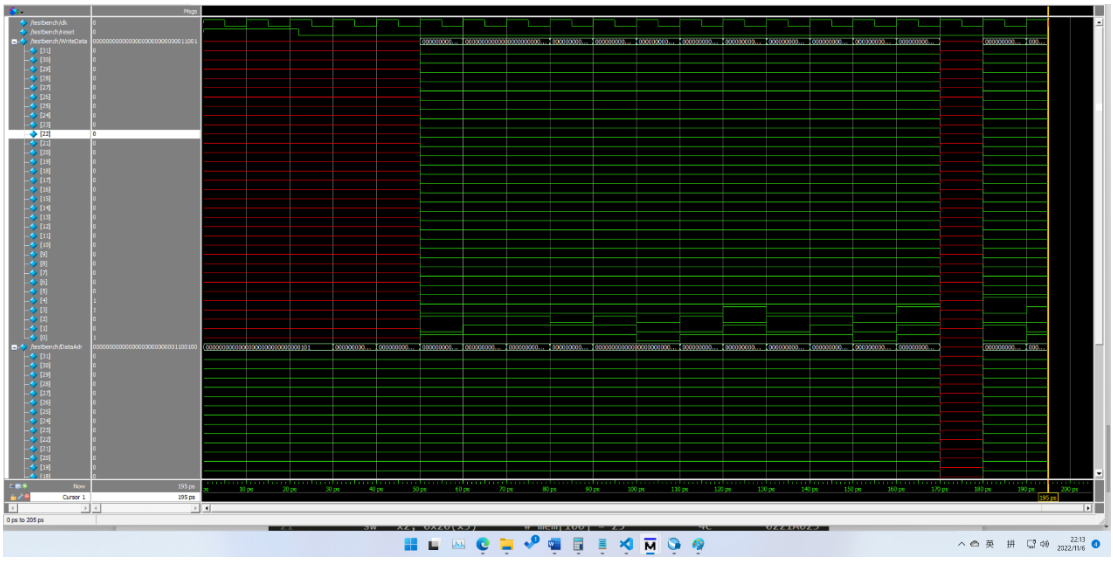
100 x 0100 xor
11 x x 1000 lui

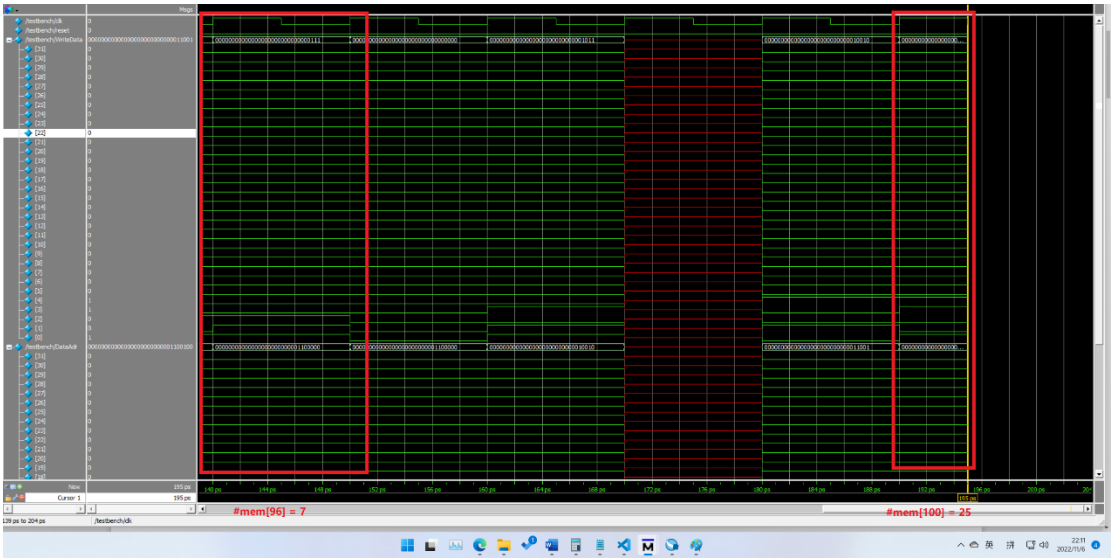
Table 3. *ImmSrc* encoding

ImmSrc	*ImmExt*	Type	Description
00	{{20{*Instr*[31]}}, *Instr*[31:20]}	I	12-bit signed immediate
01	{{20{*Instr*[31]}}, *Instr*[31:25], *Instr*[11:7]}	S	12-bit signed immediate
10	{{20{*Instr*[31]}}, *Instr*[7], *Instr*[30:25], *Instr*[11:8], 1'b0}	B	13-bit signed immediate
11	{{12{*Instr*[31]}}, *Instr*[19:12], *Instr*[20], *Instr*[30:21], 1'b0}	J	21-bit signed immediate

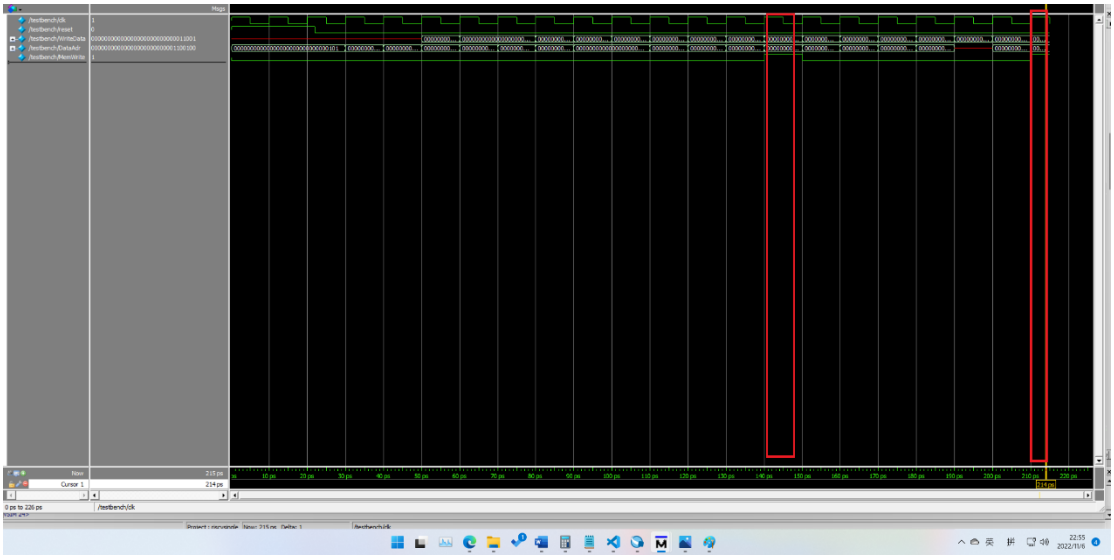
100 {{12{instr[31]}}, instr[30:20], instr[19:12], 12'b0} U 21-bit signed immerdiate

Code sent by slack

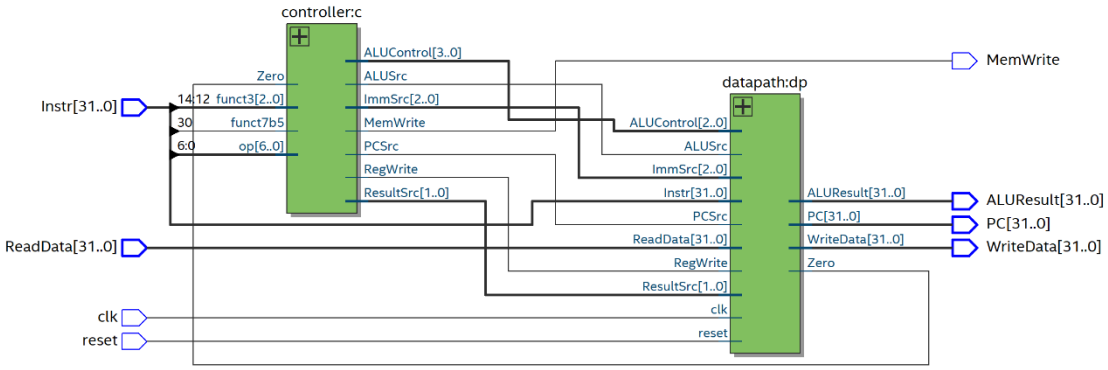




This is original.



This is modified. Both as expected and same.


controller:c
ALUControl[3..0]
Zero
ALUSrc
Instr[31..0]
14:12
funct3[2..0]
ImmSrc[2..0]
30
funct7b5
MemWrite
6:0
op[6..0]
PCSrc
RegWrite
ResultSrc[1..0]
datapath:dp
ALUControl[2..0]
ALUSrc
ImmSrc[2..0]
Instr[31..0]
ALUResult[31..0]
PCSrc
PC[31..0]
ReadData[31..0]
ReadData[31..0]
WriteData[31..0]
RegWrite
Zero
ResultSrc[1..0]
clk
clk
reset
reset
MemWrite
ALUResult[31..0]
PC[31..0]
WriteData[31..0]