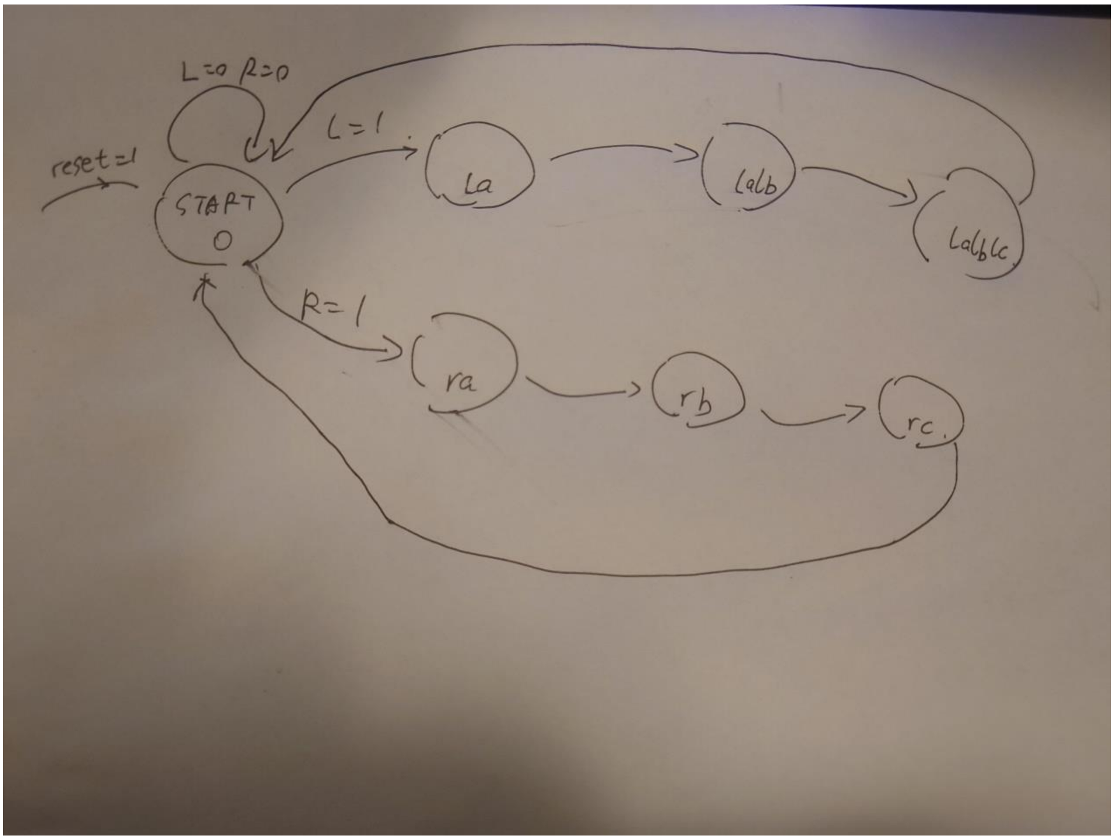
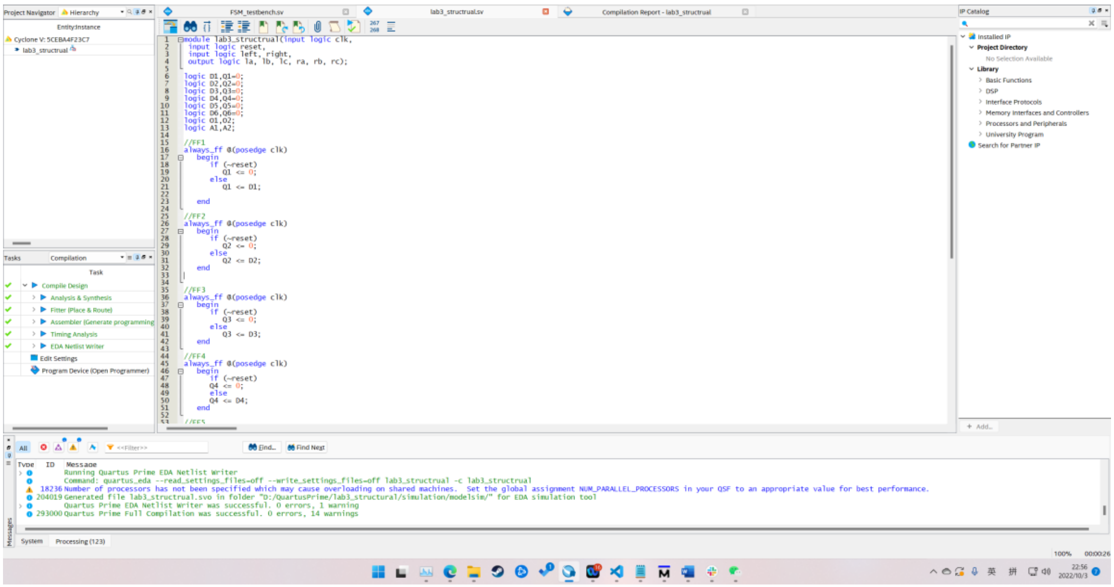
1. 2h is used.
2.



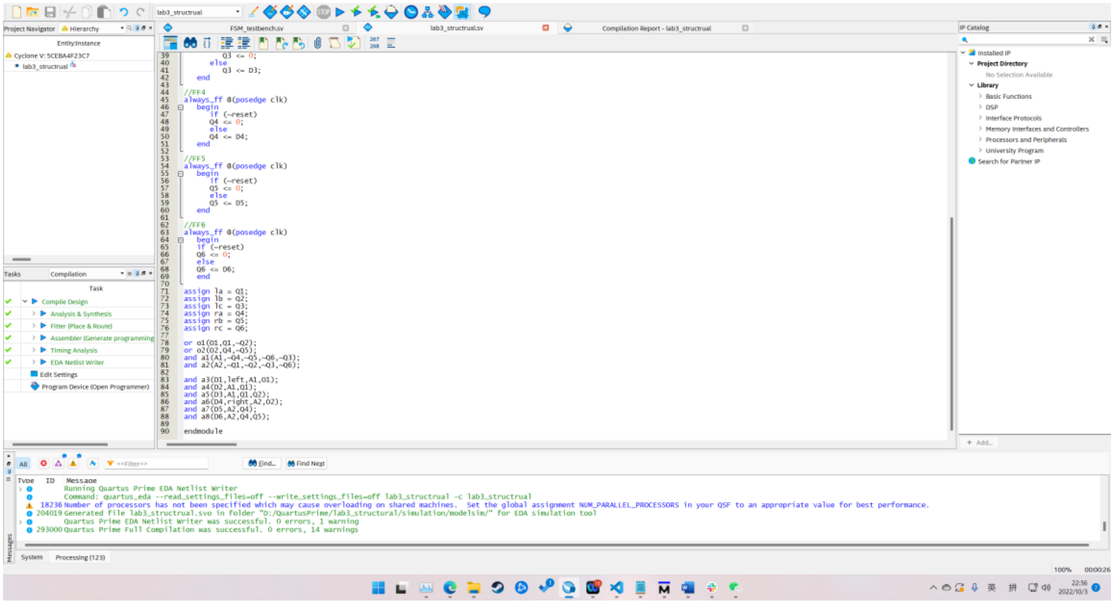
When L and R is 0, there is no light. When L = 1 or R = 1, the FSM goes through 3 states, and goes back to start.

3.



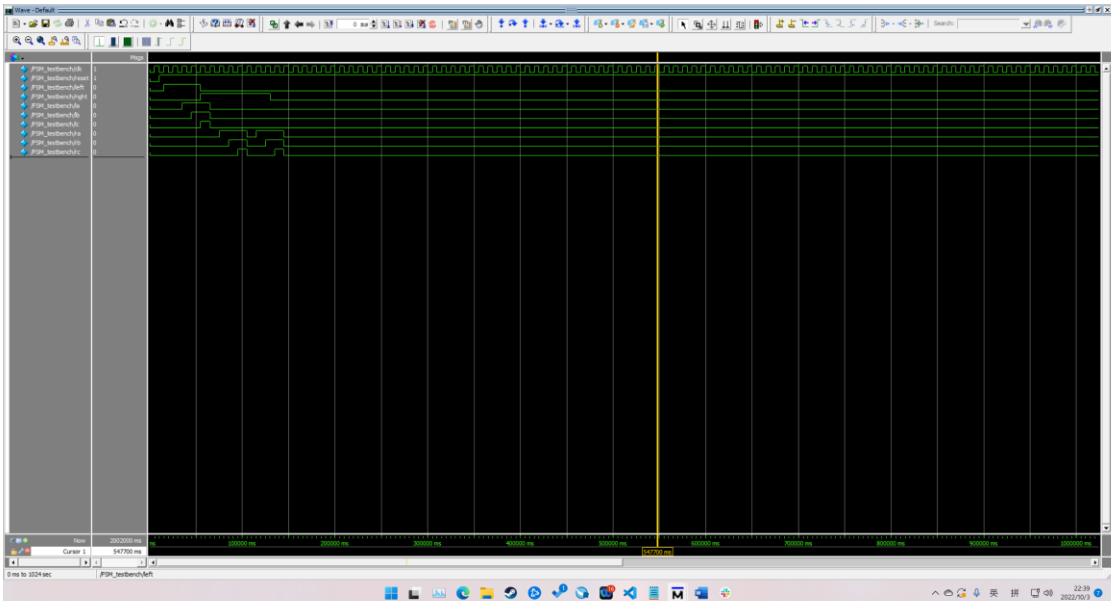
```
module lab3_structrual(input logic clk,
 input logic reset,
 input logic left, right,
 output logic la, lb, lc, ra, rb, rc);

logic D1,Q1=0;
logic D2,Q2=0;
logic D3,Q3=0;
logic D4,Q4=0;
logic D5,Q5=0;
logic D6,Q6=0;
logic O1,O2;
logic A1,A2;

//FF1
always_ff @(posedge clk)
   begin
      if (~reset)
         Q1 <= 0;
      else
         Q1 <= D1;

   end

//FF2
always_ff @(posedge clk)
   begin
      if (~reset)
         Q2 <= 0;
      else
         Q2 <= D2;
   end


//FF3
always_ff @(posedge clk)
   begin
      if (~reset)
         Q3 <= 0;
      else
         Q3 <= D3;
   end

//FF4
always_ff @(posedge clk)
   begin
      if (~reset)
      Q4 <= 0;
      else
      Q4 <= D4;
   end

//FF5
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab3_structrual -c lab3_structrual
      18236  Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
      204019 Generated file lab3_structrual.svo in folder "D:/QuartusPrime/lab3_structural/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
      293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```



```
         Q3 <= 0;
      else
         Q3 <= D3;
   end

//FF4
always_ff @(posedge clk)
   begin
      if (~reset)
      Q4 <= 0;
      else
      Q4 <= D4;
   end

//FF5
always_ff @(posedge clk)
   begin
      if (~reset)
      Q5 <= 0;
      else
      Q5 <= D5;
   end

//FF6
always_ff @(posedge clk)
   begin
   if (~reset)
   Q6 <= 0;
   else
   Q6 <= D6;
   end

assign la = Q1;
assign lb = Q2;
assign lc = Q3;
assign ra = Q4;
assign rb = Q5;
assign rc = Q6;

or o1(O1,Q1,~Q2);
or o2(O2,Q4,~Q5);
and a1(A1,~Q4,~Q5,~Q6,~Q3);
and a2(A2,~Q1,~Q2,~Q3,~Q6);

and a3(D1,left,A1,O1);
and a4(D2,A1,Q1);
and a5(D3,A1,Q1,Q2);
and a6(D4,right,A2,O2);
and a7(D5,A2,Q4);
and a8(D6,A2,Q4,Q5);

endmodule
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab3_structrual -c lab3_structrual
      18236  Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
      204019 Generated file lab3_structrual.svo in folder "D:/QuartusPrime/lab3_structural/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
      293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```

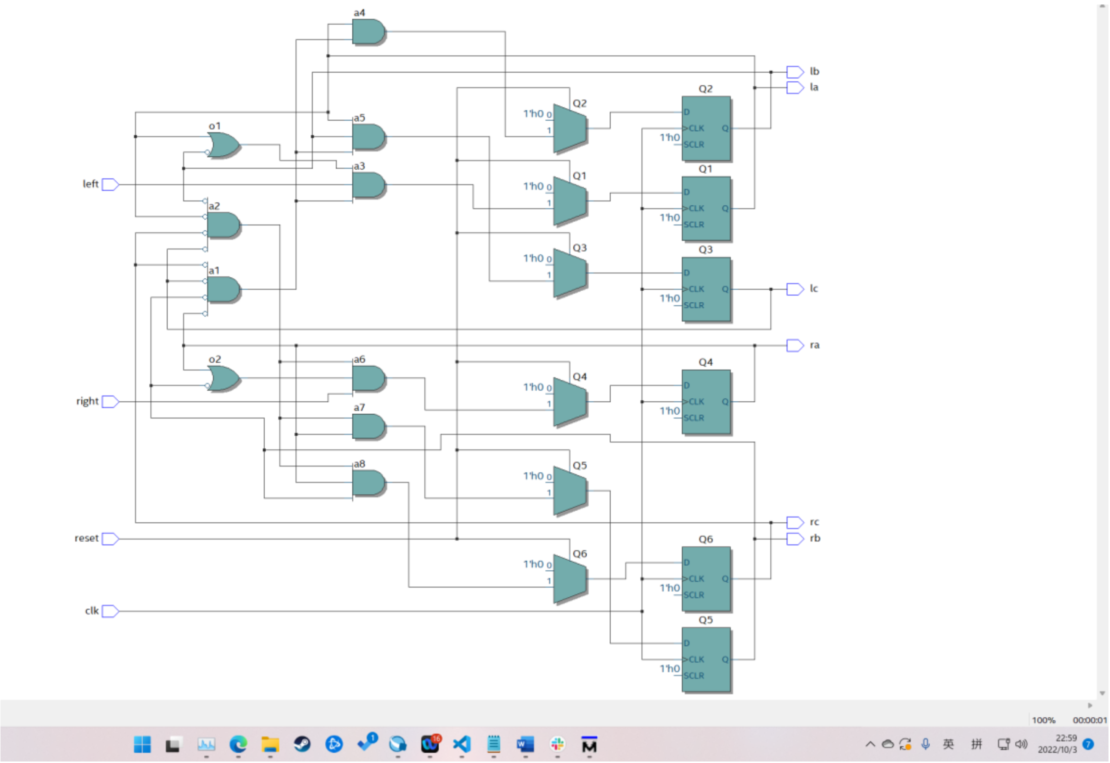


	Msgs
/FSM_testbench/clk	1
/FSM_testbench/reset	1
/FSM_testbench/left	0
/FSM_testbench/right	0
/FSM_testbench/la	0
/FSM_testbench/lb	0
/FSM_testbench/lc	0
/FSM_testbench/ra	0
/FSM_testbench/rb	0
/FSM_testbench/rc	0

Now 2002000 ms
Cursor 1 547700 ms

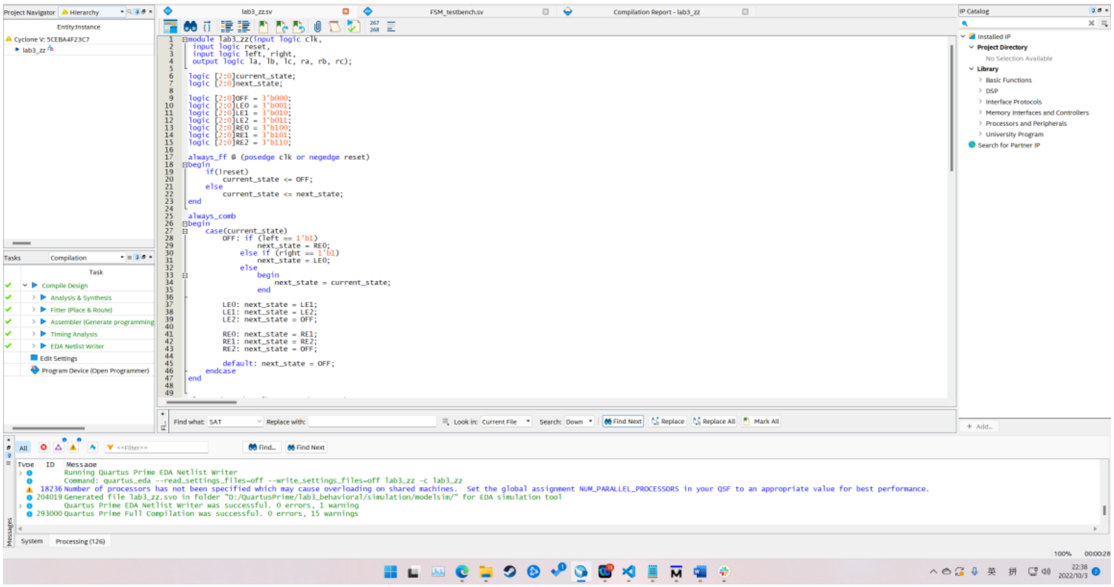
0 ms to 1024 sec /FSM_testbench/left

It is expected in the waveform. When the input is left or right, they will light up in sequence and shutdown for one period.



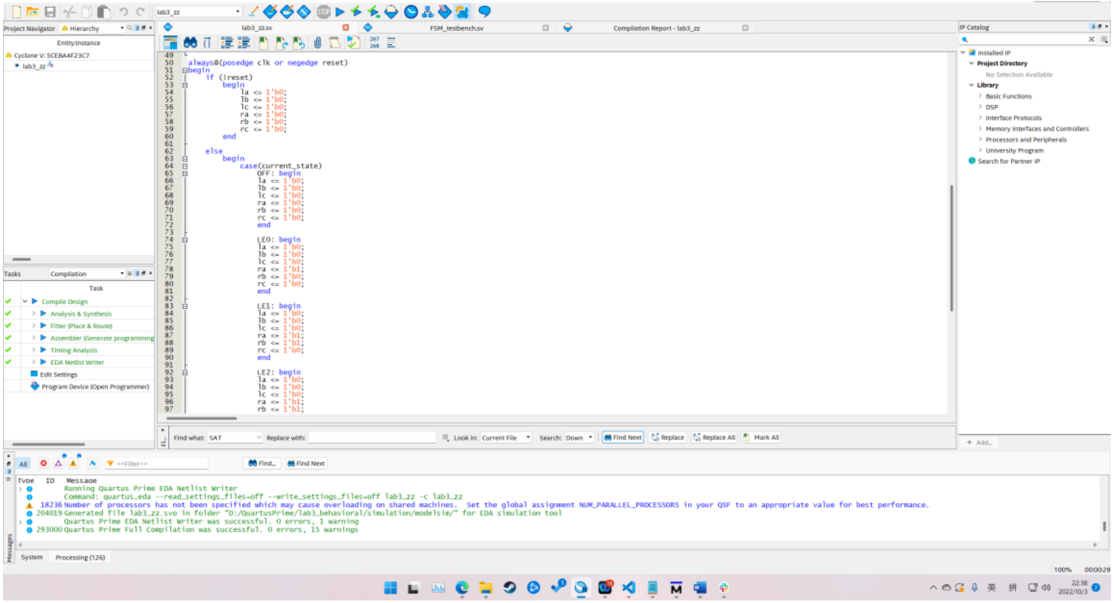
RTL is done by 5 D-FFs.

Behavioral:



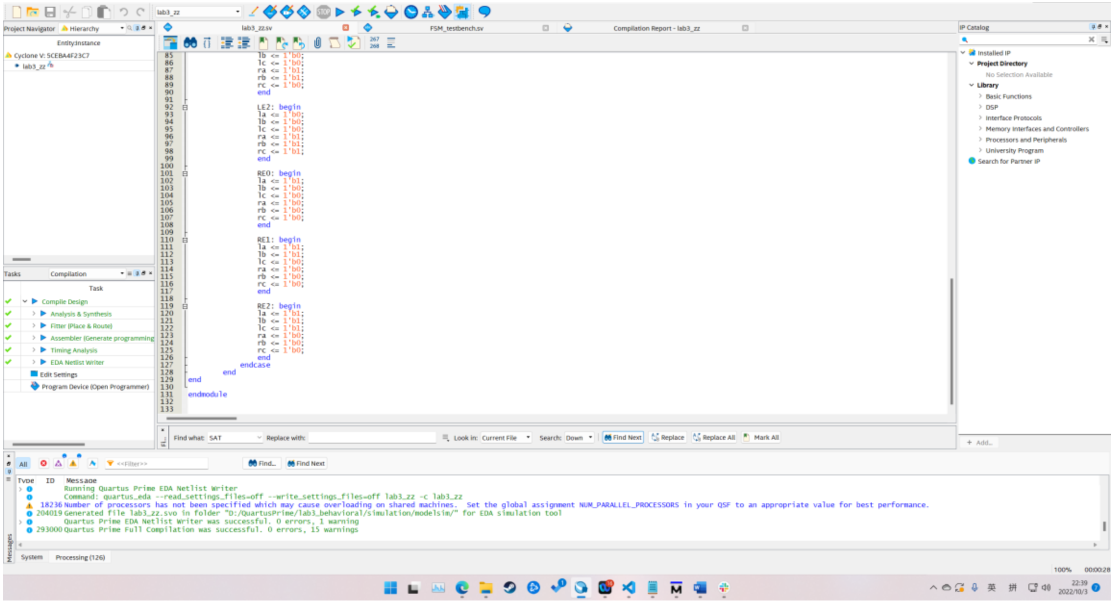
```
module lab3_zz(input logic clk,
 input logic reset,
 input logic left, right,
 output logic la, lb, lc, ra, rb, rc);

logic [2:0]current_state;
logic [2:0]next_state;

logic [2:0]OFF = 3'b000;
logic [2:0]LE0 = 3'b001;
logic [2:0]LE1 = 3'b010;
logic [2:0]LE2 = 3'b011;
logic [2:0]RE0 = 3'b100;
logic [2:0]RE1 = 3'b101;
logic [2:0]RE2 = 3'b110;

always_ff @ (posedge clk or negedge reset)
begin
    if(!reset)
        current_state <= OFF;
    else
        current_state <= next_state;
end

always_comb
begin
    case(current_state)
        OFF: if (left == 1'b1)
                next_state = RE0;
            else if (right == 1'b1)
                next_state = LE0;
            else
                begin
                    next_state = current_state;
                end

        LE0: next_state = LE1;
        LE1: next_state = LE2;
        LE2: next_state = OFF;

        RE0: next_state = RE1;
        RE1: next_state = RE2;
        RE2: next_state = OFF;

        default: next_state = OFF;
    endcase
end
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab3_zz -c lab3_zz
     18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
    204019 Generated file lab3_zz.svo in folder "D:/QuartusPrime/lab3_behavioral/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
    293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings
```



```
always@(posedge clk or negedge reset)
begin
    if (!reset)
        begin
            la <= 1'b0;
            lb <= 1'b0;
            lc <= 1'b0;
            ra <= 1'b0;
            rb <= 1'b0;
            rc <= 1'b0;
        end

    else
        begin
            case(current_state)
                OFF: begin
                la <= 1'b0;
                lb <= 1'b0;
                lc <= 1'b0;
                ra <= 1'b0;
                rb <= 1'b0;
                rc <= 1'b0;
                end

                LE0: begin
                la <= 1'b0;
                lb <= 1'b0;
                lc <= 1'b0;
                ra <= 1'b1;
                rb <= 1'b0;
                rc <= 1'b0;
                end

                LE1: begin
                la <= 1'b0;
                lb <= 1'b0;
                lc <= 1'b0;
                ra <= 1'b1;
                rb <= 1'b1;
                rc <= 1'b0;
                end

                LE2: begin
                la <= 1'b0;
                lb <= 1'b0;
                lc <= 1'b0;
                ra <= 1'b1;
                rb <= 1'b1;
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab3_zz -c lab3_zz
     18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
    204019 Generated file lab3_zz.svo in folder "D:/QuartusPrime/lab3_behavioral/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
    293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings
```



```
                lb <= 1'b0;
                lc <= 1'b0;
                ra <= 1'b1;
                rb <= 1'b1;
                rc <= 1'b0;
                end

                LE2: begin
                la <= 1'b0;
                lb <= 1'b0;
                lc <= 1'b0;
                ra <= 1'b1;
                rb <= 1'b1;
                rc <= 1'b1;
                end

                RE0: begin
                la <= 1'b1;
                lb <= 1'b0;
                lc <= 1'b0;
                ra <= 1'b0;
                rb <= 1'b0;
                rc <= 1'b0;
                end

                RE1: begin
                la <= 1'b1;
                lb <= 1'b1;
                lc <= 1'b0;
                ra <= 1'b0;
                rb <= 1'b0;
                rc <= 1'b0;
                end

                RE2: begin
                la <= 1'b1;
                lb <= 1'b1;
                lc <= 1'b1;
                ra <= 1'b0;
                rb <= 1'b0;
                rc <= 1'b0;
                end
            endcase
        end
end

endmodule
```

```
Type  ID     Message
             Running Quartus Prime EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab3_zz -c lab3_zz
     18236 Number of processors has not been specified which may cause overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
    204019 Generated file lab3_zz.svo in folder "D:/QuartusPrime/lab3_behavioral/simulation/modelsim/" for EDA simulation tool
             Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
    293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings
```