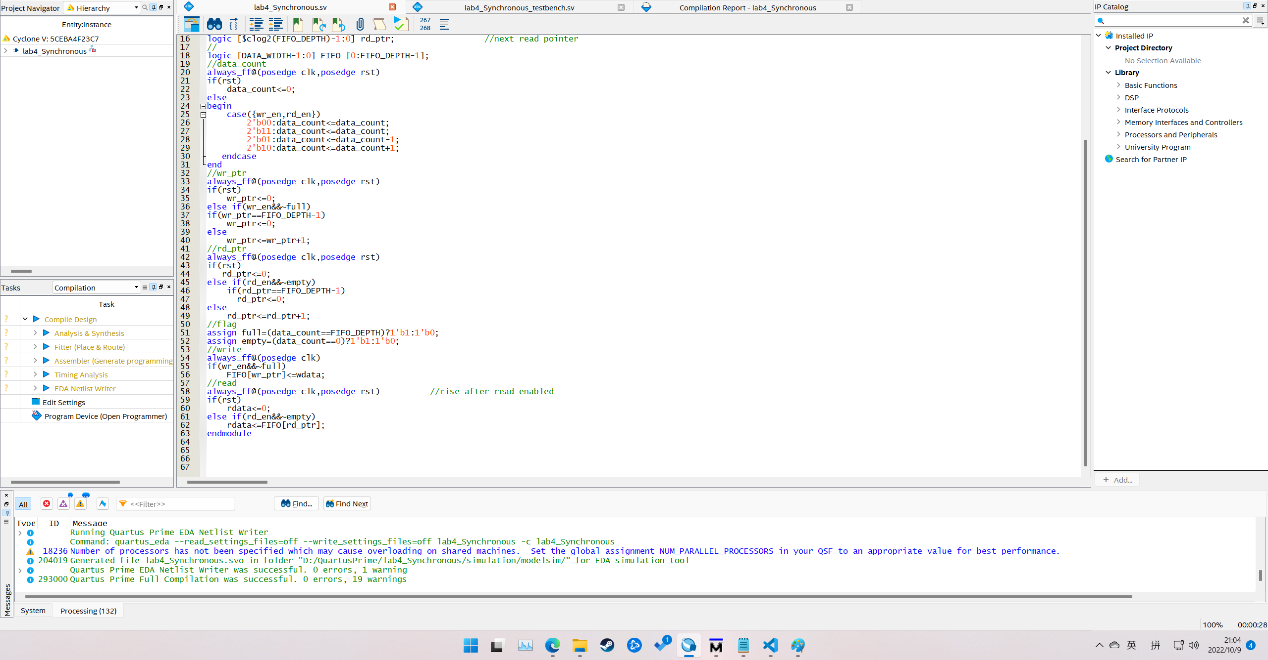
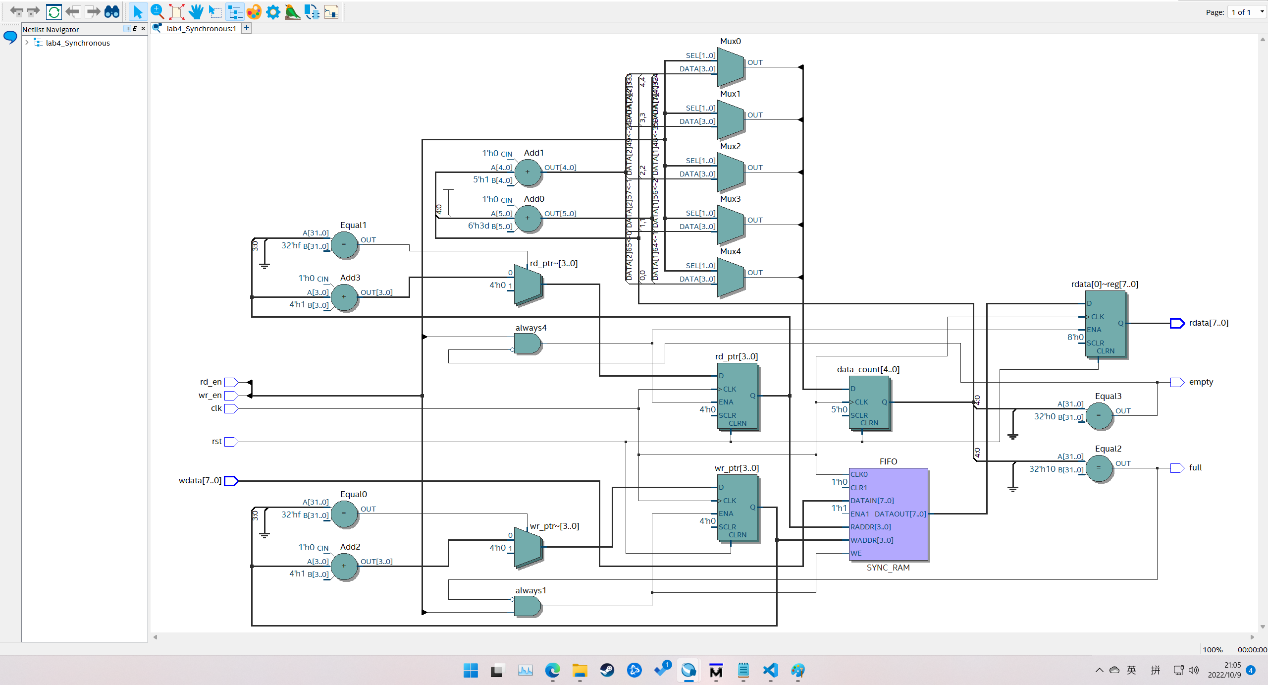
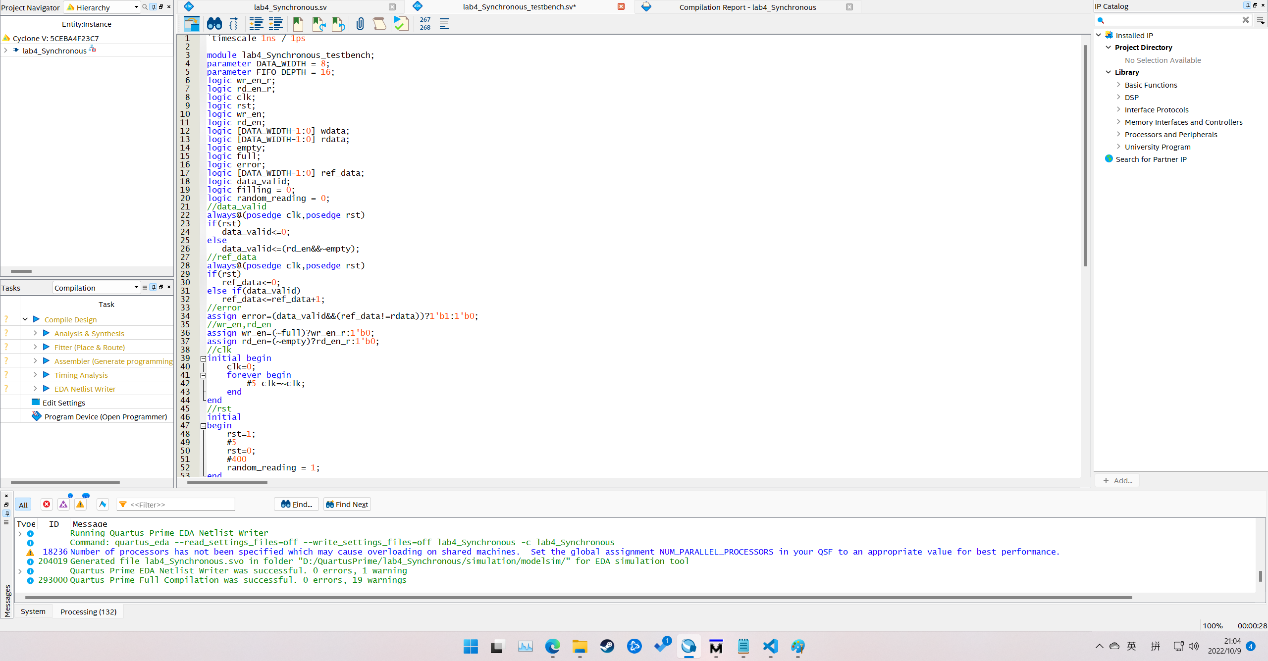
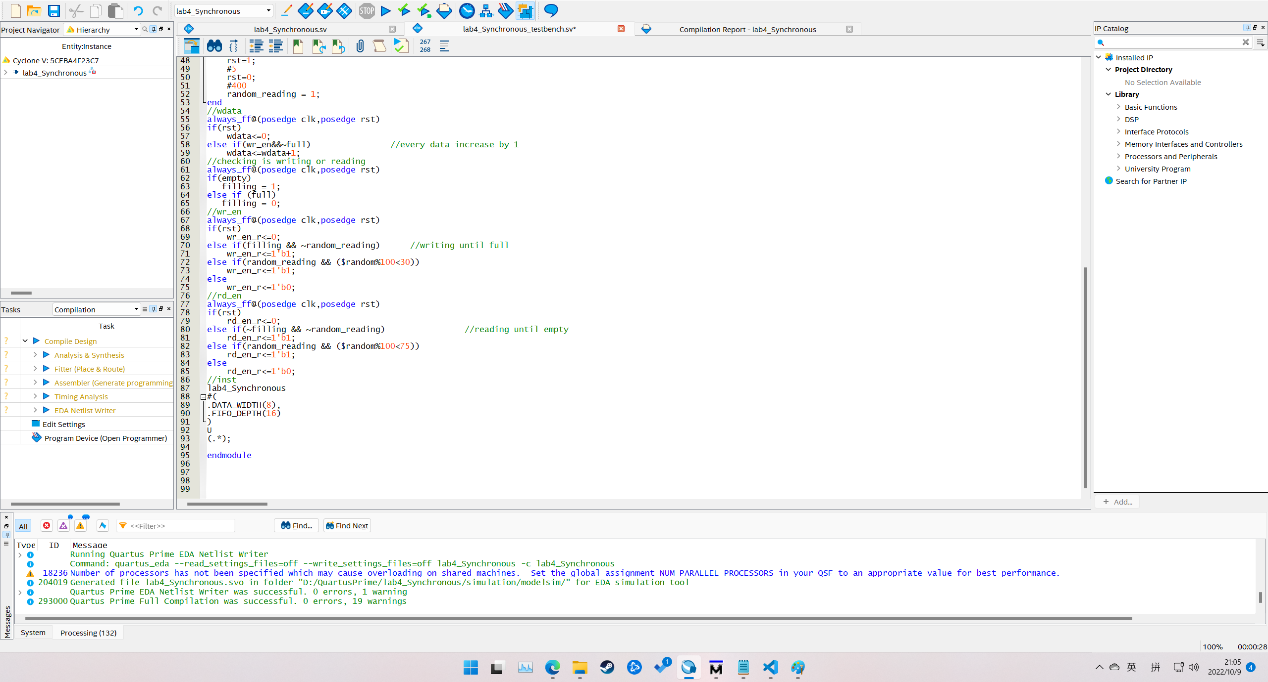
This lab uses 4 hours.

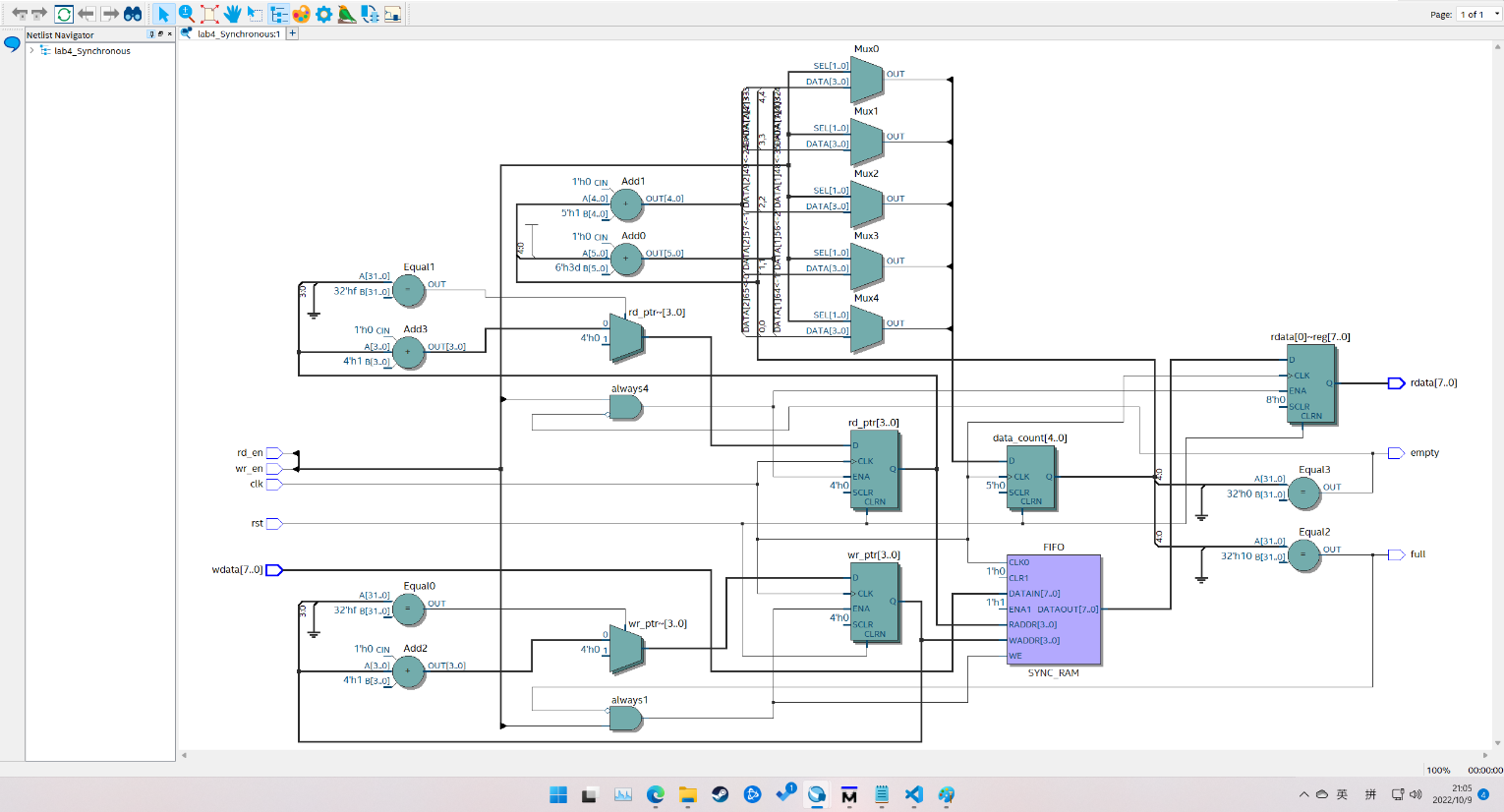
Synchronous code



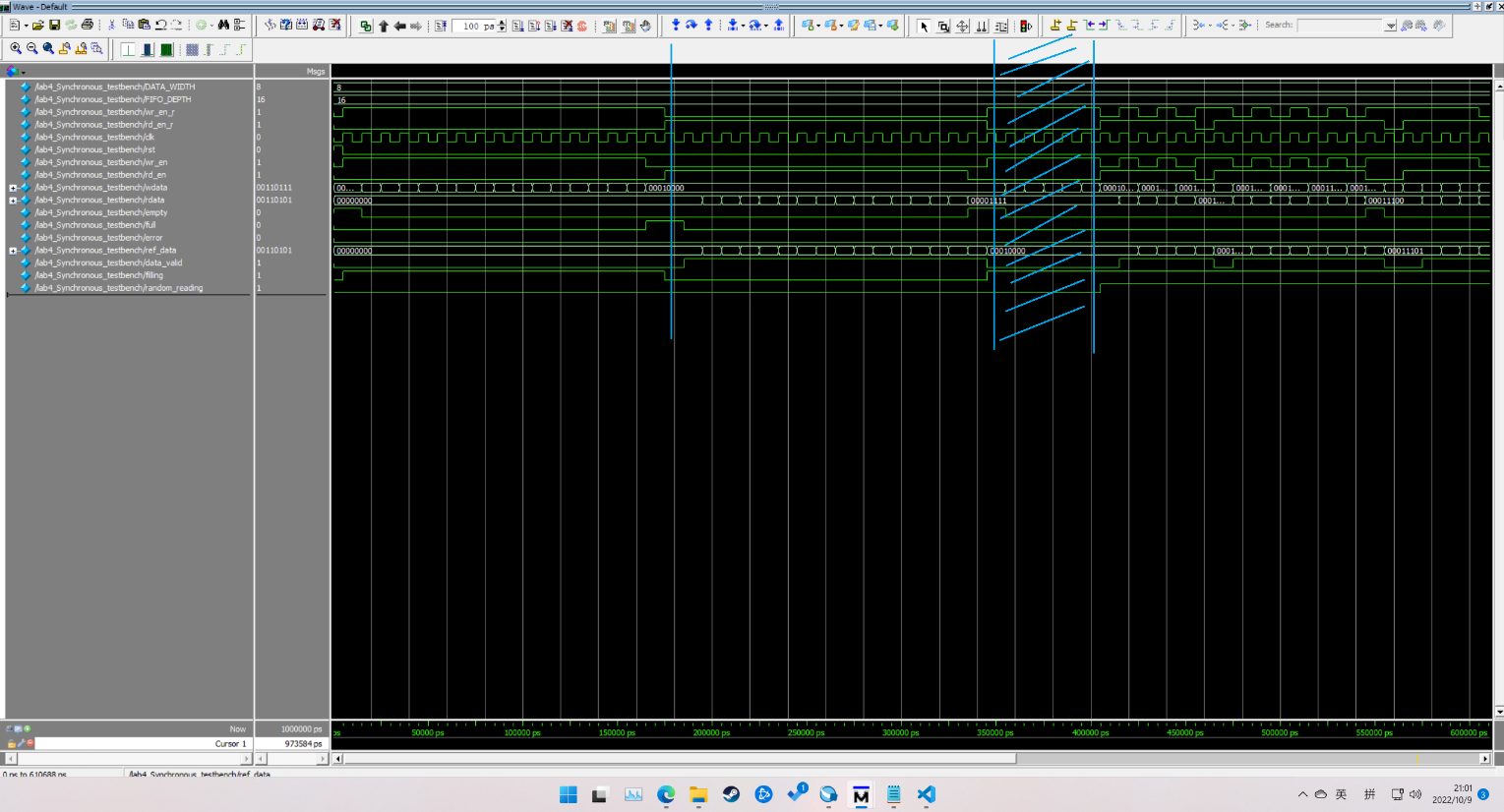
Synchronous testbench



Synchronous RTL

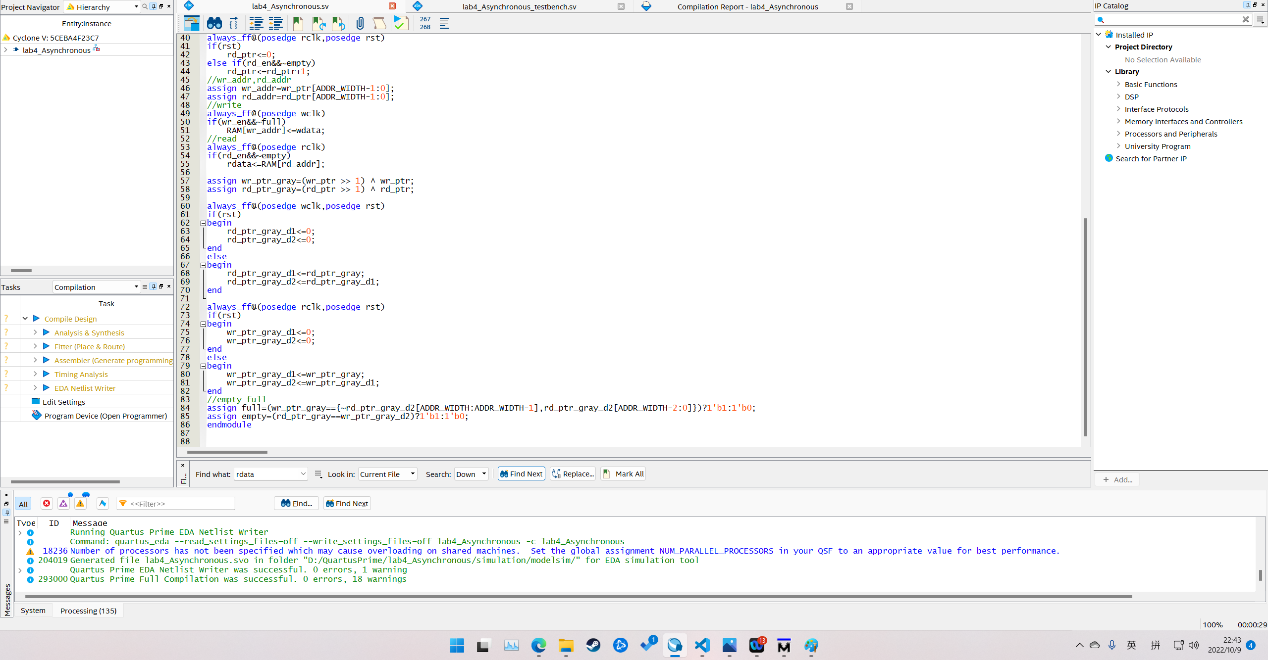
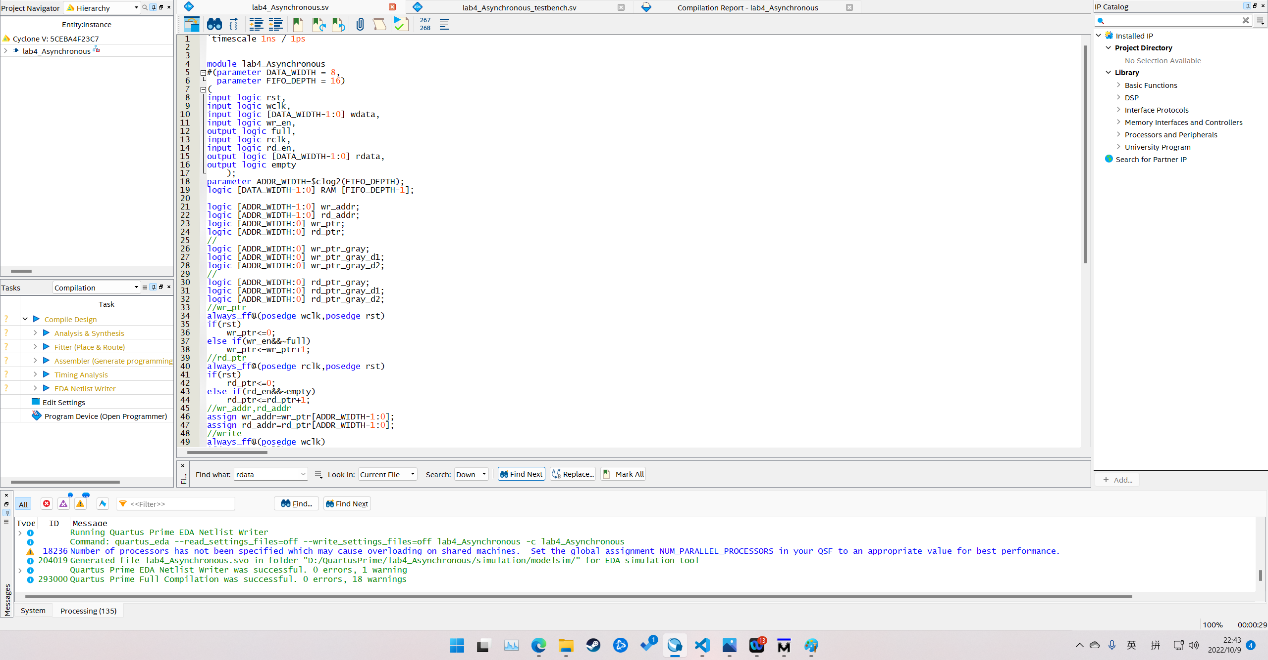


Synchronous waveform

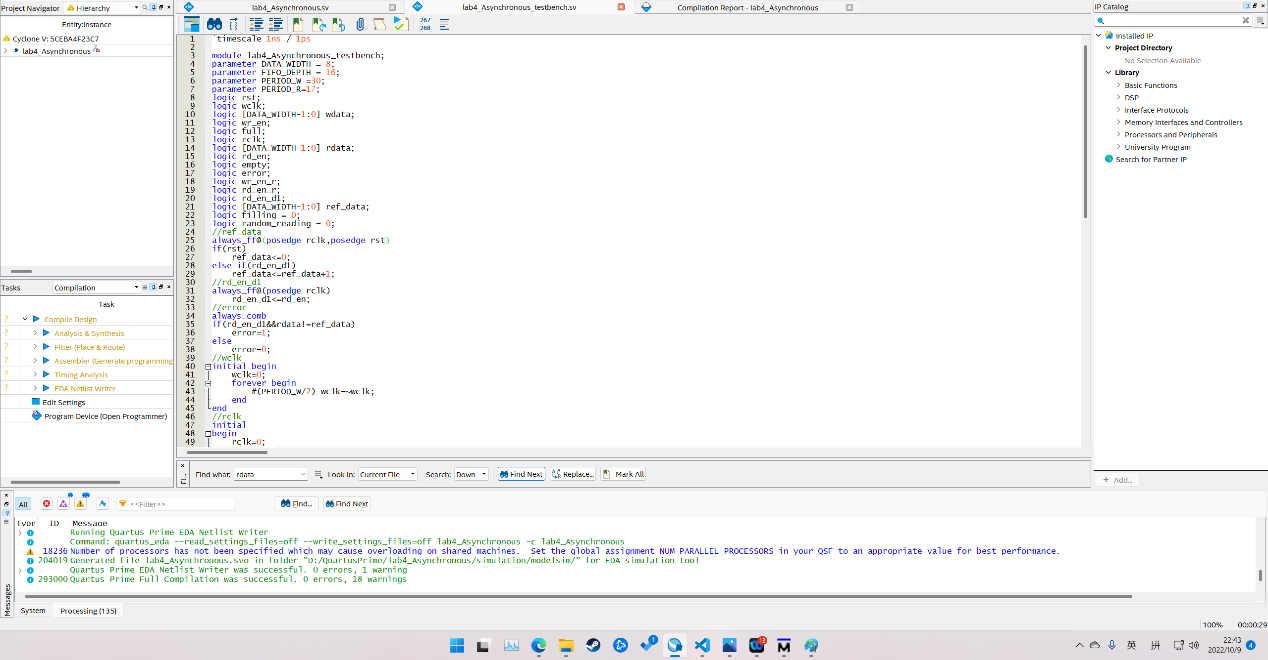


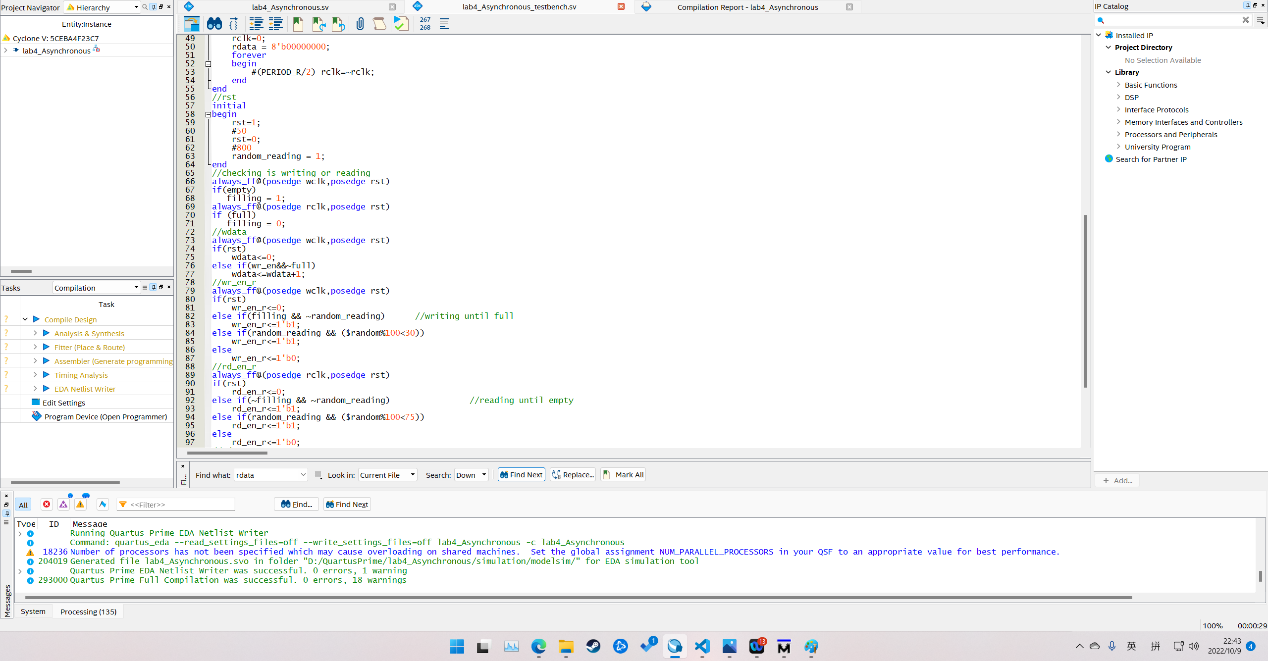
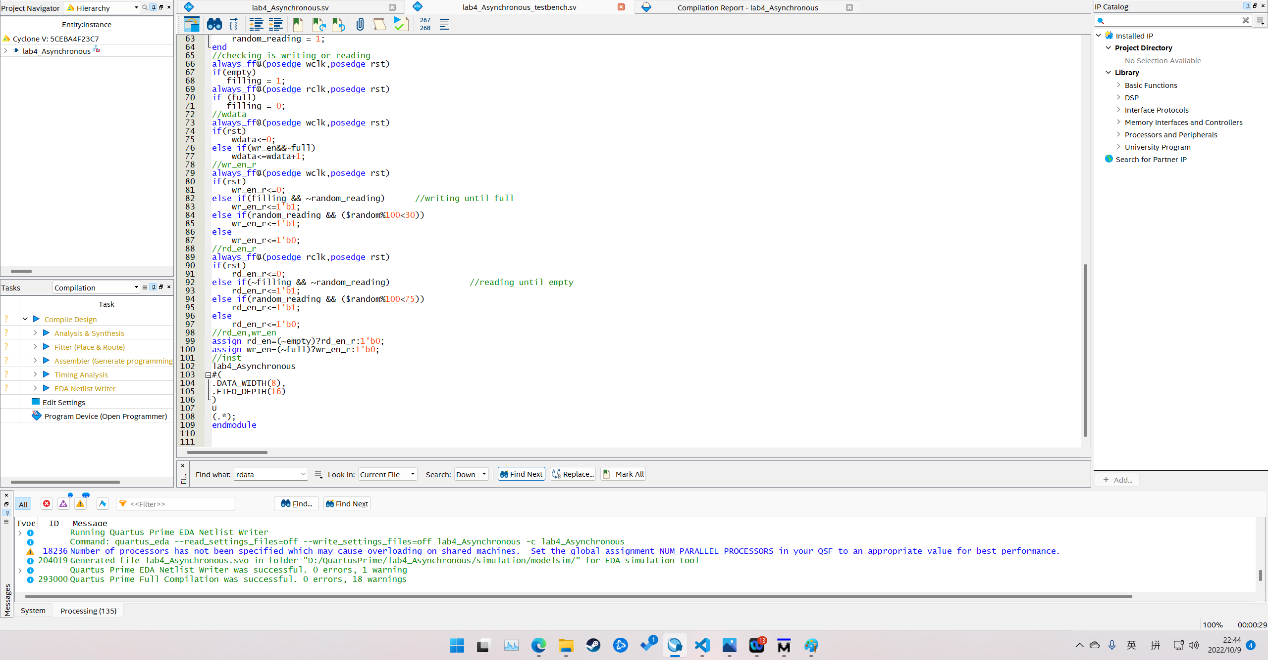
The first section is let FIFO write from 0 to 16. At first, empty is high, after first data is written, it is low. When data is 16, the FIFO is full, so full is high. Then in the second section, FIFO reads data, from 0 to 16. Then empty is high again. In third section, the FIFO randomly reads and writes. So both read and write would trigger randomly. The waveform is as expected.

Asynchronous code

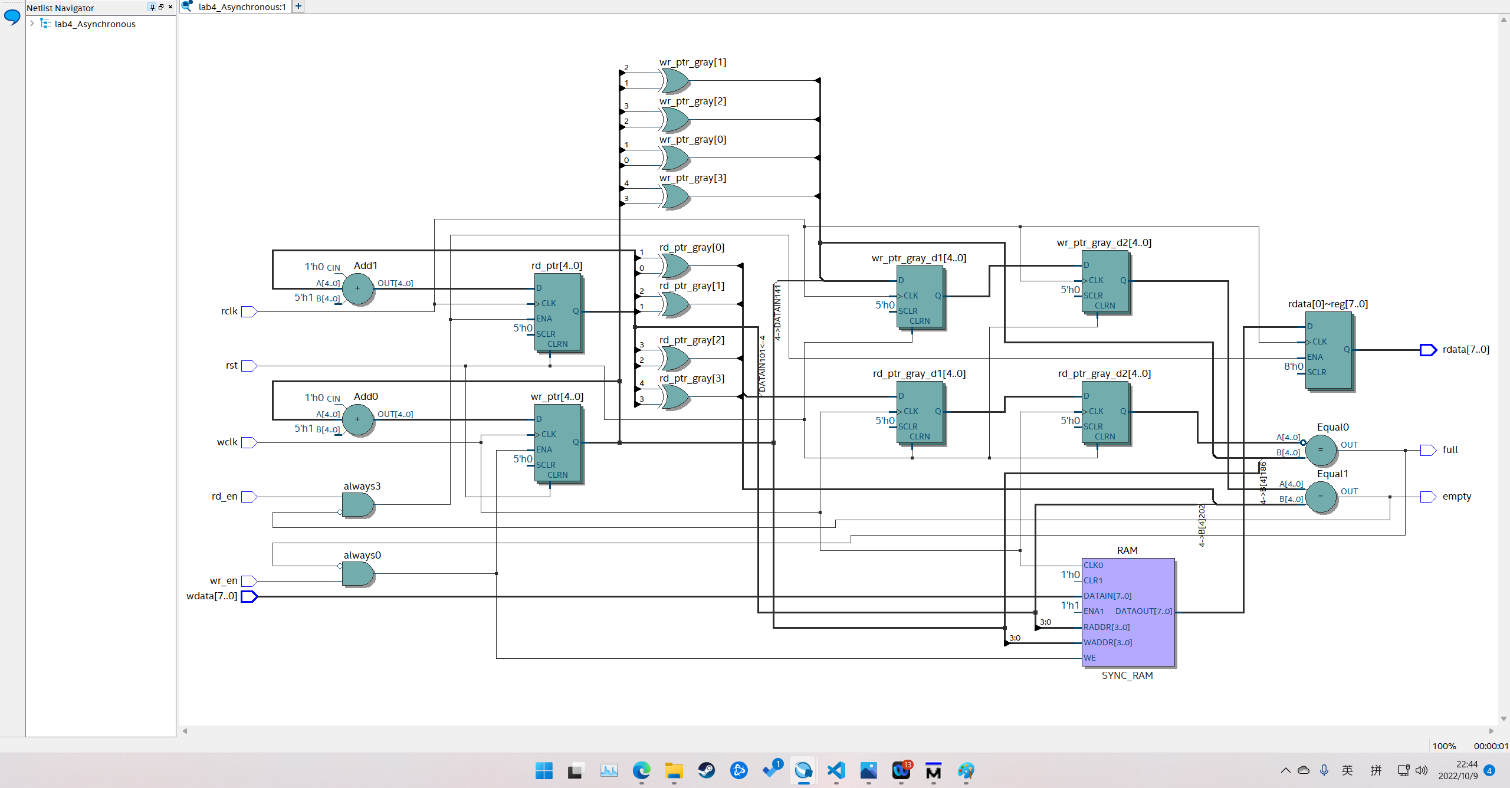


Asynchronous testbench

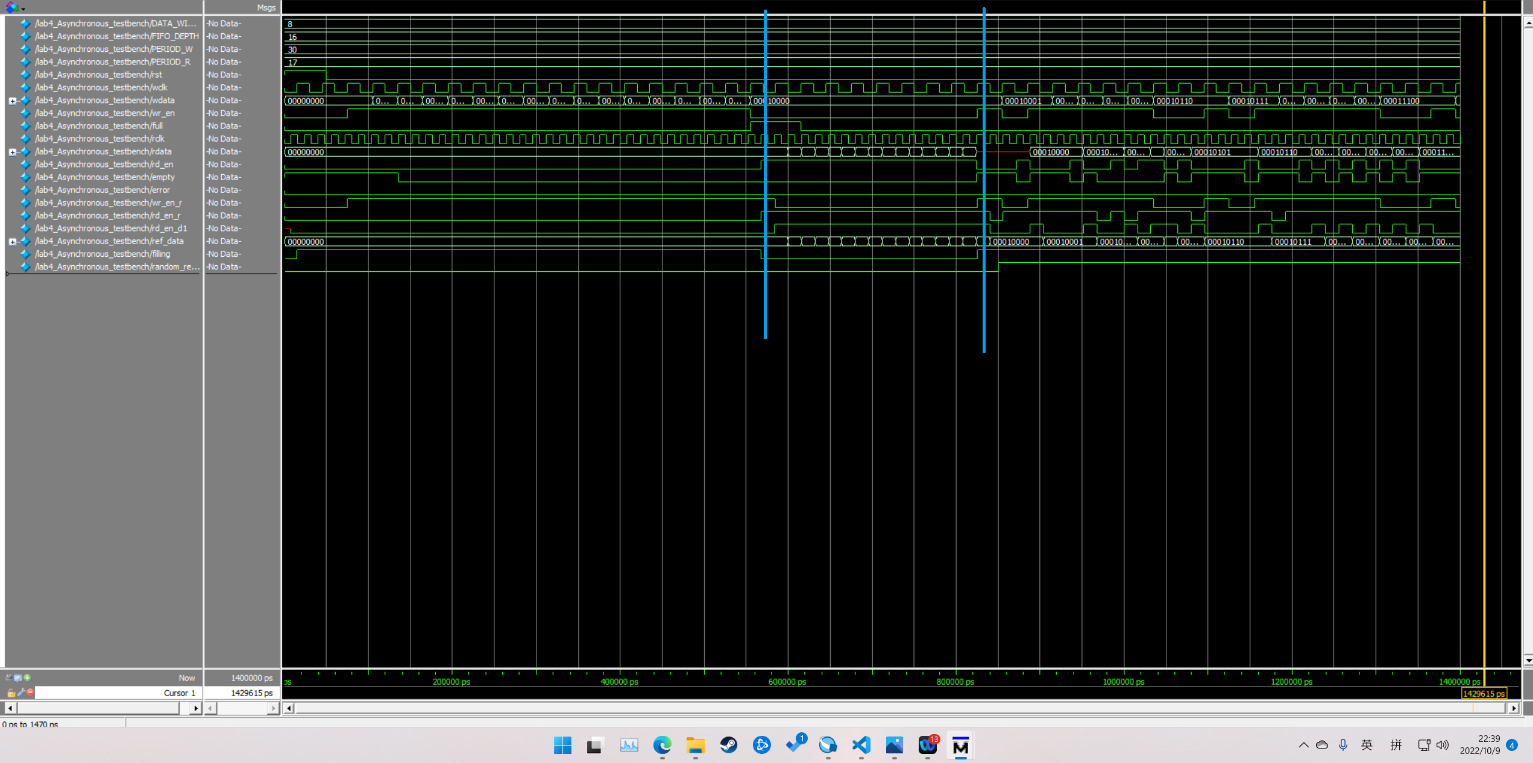




Asynchronous RTL



Asynchronous waveform



The full and empty is same as synchronous. Asynchronous focus on different clock in reading and writing. This uses grey code. Gray code pointers that are synchronized into the opposite clock domain before generating synchronous FIFO full or empty status signals. The three sections are writing until full, reading until empty, and reading and writing randomly. The waveform is as expected.