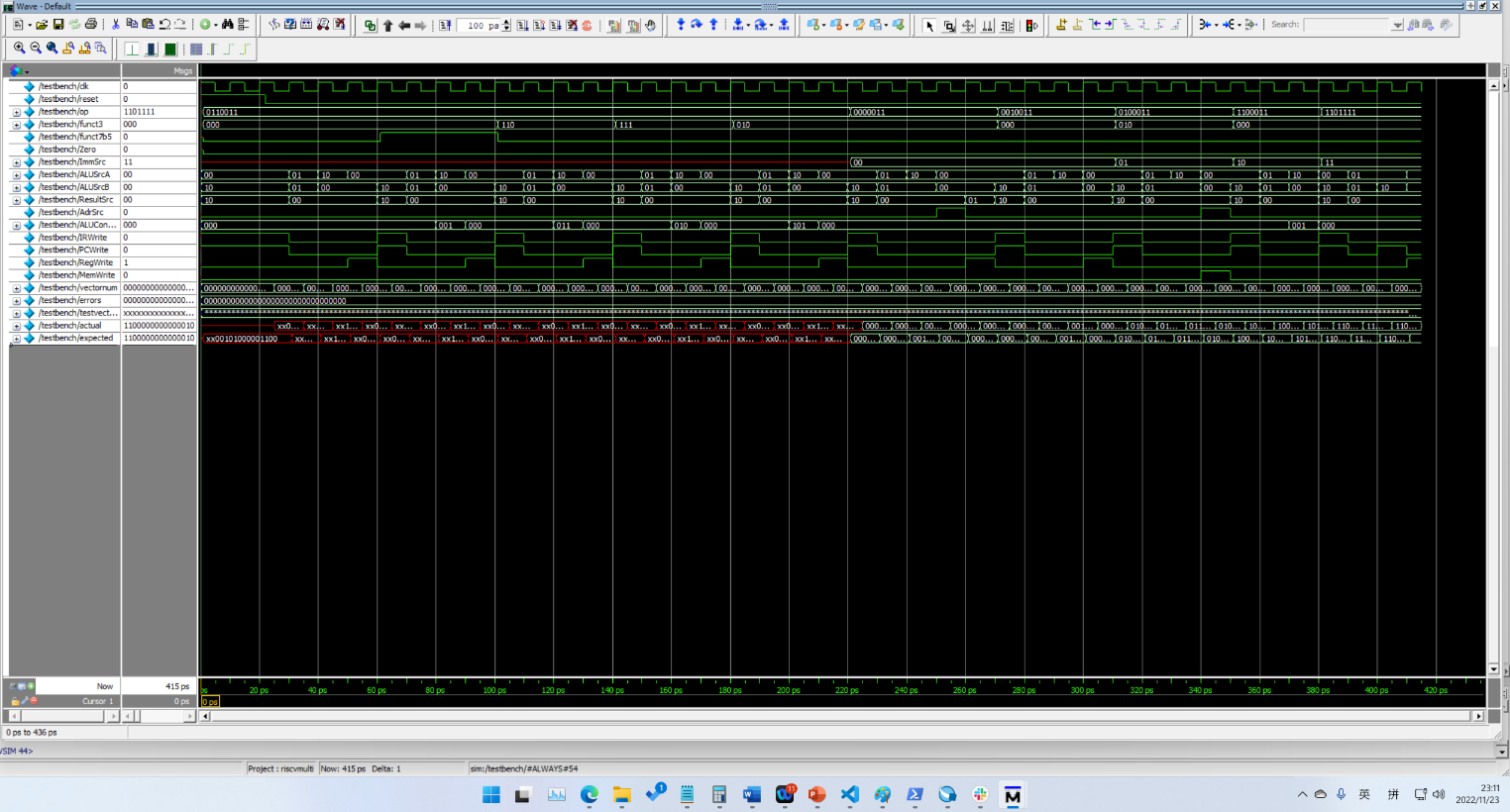
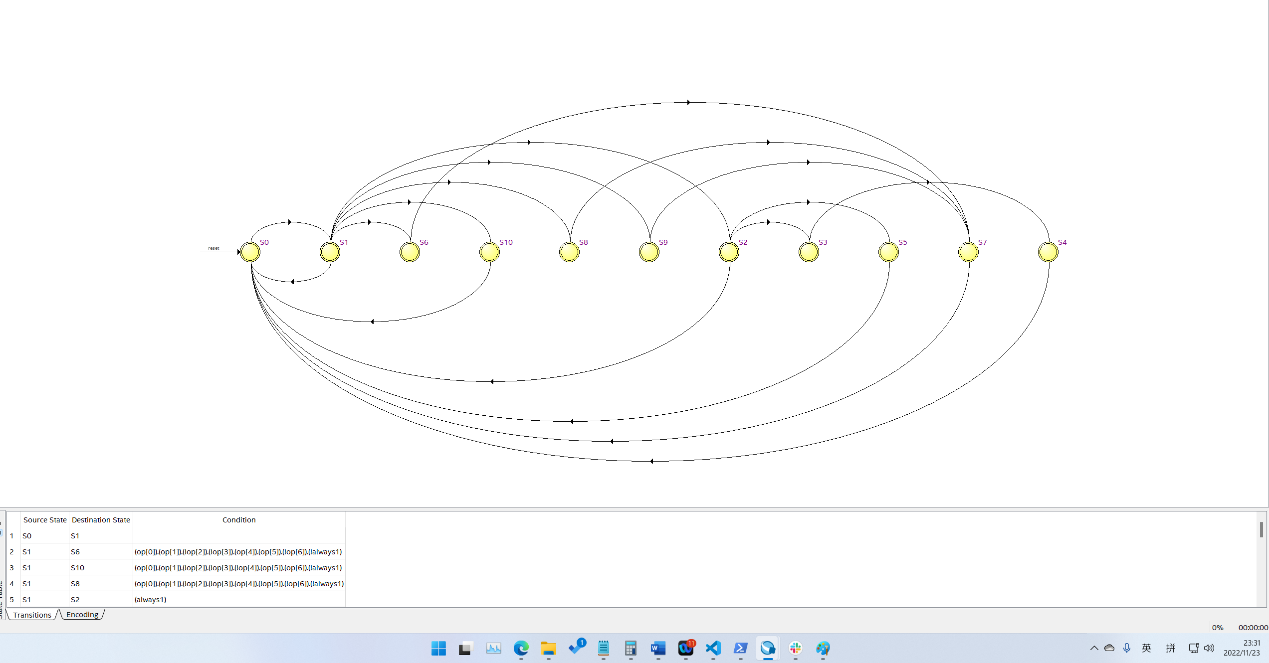
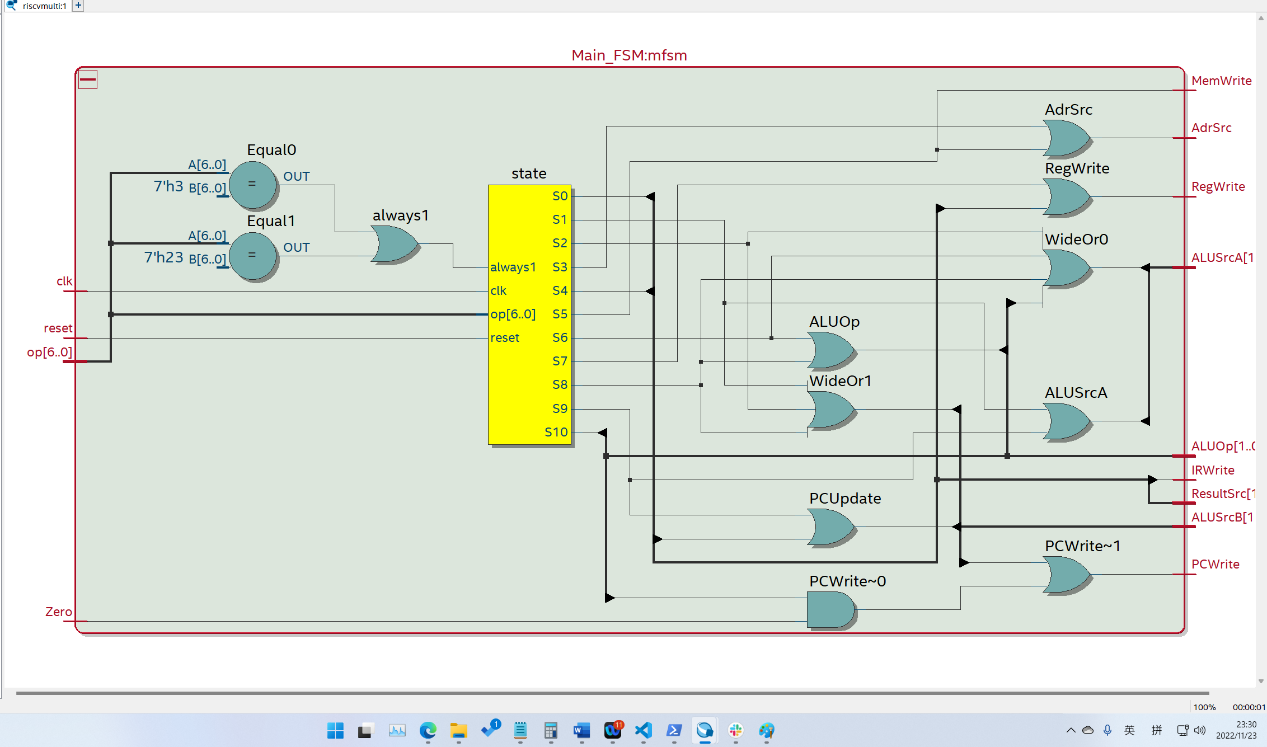
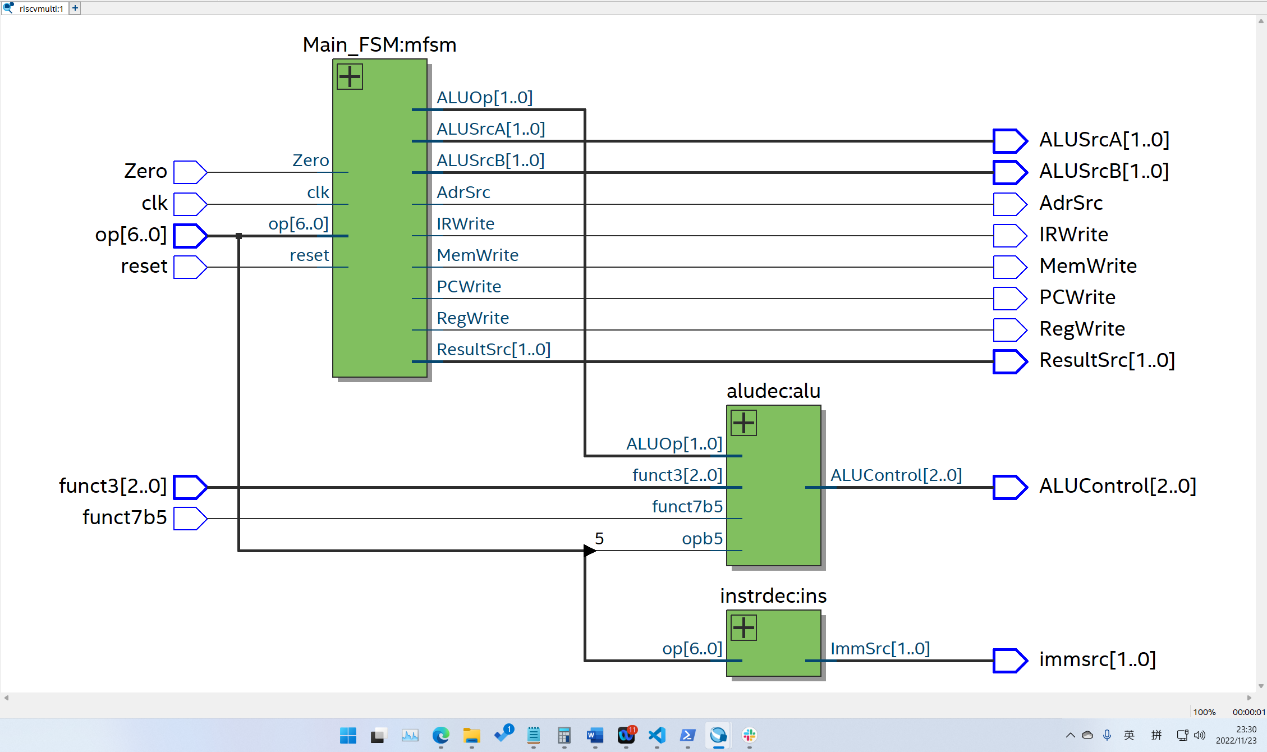
I spent 4h.

The FSM write enable signals (RegWrite, MemWrite, IRWrite, PCUpdate, and Branch) are 0 if not listed in a state. Other signals are don’t care if not listed in a state. Then fetch the input, decode it and goes to memadr if it is lw. Then memread and memwb. Then PC+4 and go back to fetch. In memadr, if it is sw, goes to memwrite and then goes back to fetch as before. For R-Type, data goes into ALU with ALUSrcB 00 from register and then aluwb. For I-Type, data goes into ALU with ALUSrcB 01 from extend and then aluwb. For the decoding state, Read Registers and Calculate Target Address (PC+imm). If the op is beq, compare registers and Send Target PC (ALUOut) to PCNext. If op is jal, calculate PC + 4 and Send Target Address (ALUOut) to PCNext.



It has passed the test vector. The test vector is red in front is because there are 2 xx, the data is as expect, the terminal has no error output.



The alu and instrdec is provided in the lab, so RTL schematics is not shown.