Lab 1: Power Management

ESE519/IPD519: Introduction to Embedded Systems
University of Pennsylvania

In this document, you'll fill out your responses to the questions listed in the Lab 1 Manual. Please fill out your name and link your Github repository below to begin. Be sure that your code on the repo is up-to-date before submission!

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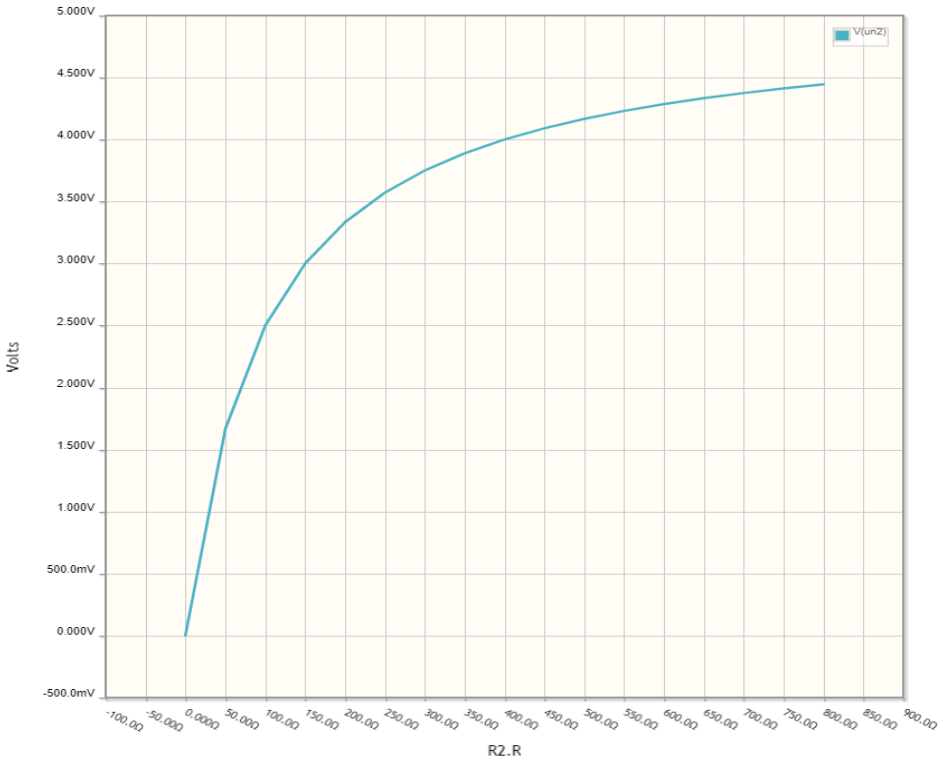
GitHub Repository: https://github.com/o0wkr0o/ESE519-Lab1/

IR1+IR2 = VCC

1. I = VCC/(R1+R2)
   Vnode1 = VR2 = 5*100/(100+100)=2.5(V)
2.
   Vnode1 = VR2 = 5*850/(100+850)=4.47(V)

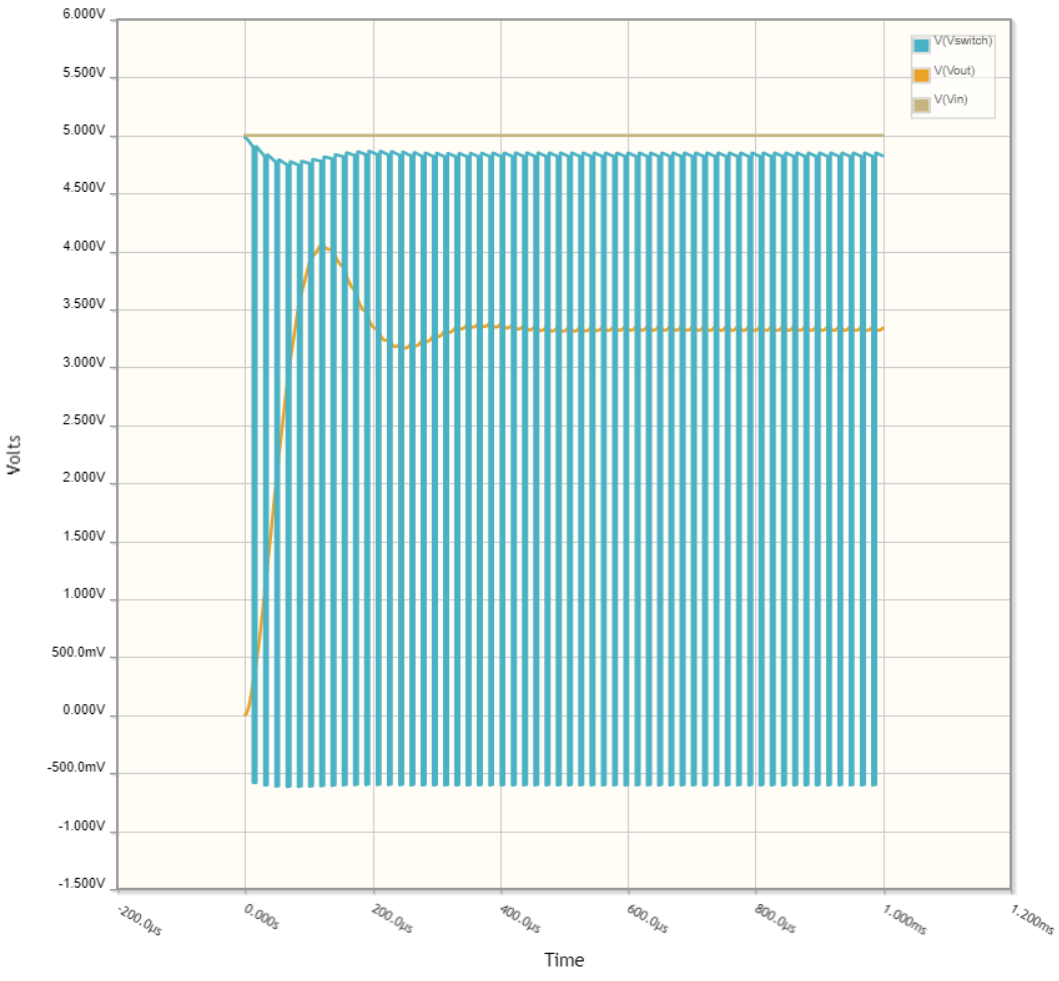


4.
1) provide different voltage for device that require different voltage, for example chargers for different devices
2) provide different voltages for the MOSFET to control the gate voltage for close or open in order to control the circuit.
3) use it as a potentiometer to control the voltage so that the volume on the output will change accordingly.

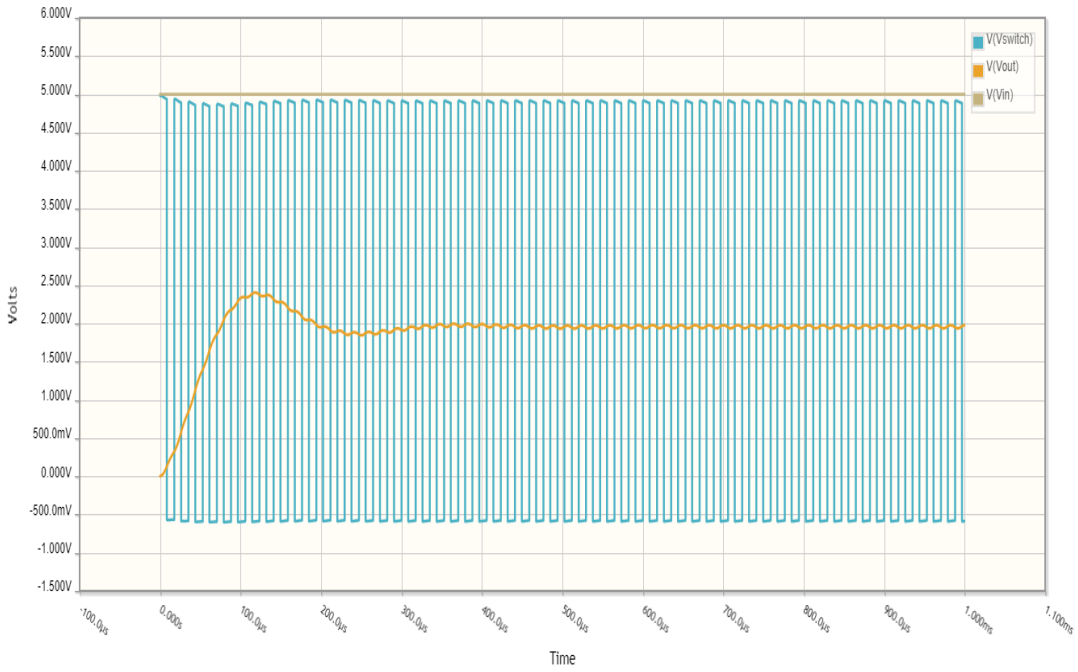
5. As the CLK is high, the MOSFET is off, and as the CLK is low, the MOSFET will be on. And the MOSFET is active then the pulse is low.

6. In order to get 3.3V, we need the duty cycle to be around 52%. As for 2V, we need the duty cycle to be 26.3%. The measurement was a bit off, but it still makes sense since I think it's still sitting within the tolerance. And in real life, there are more factors that may influence the results, so it could be more different in results than simulation.

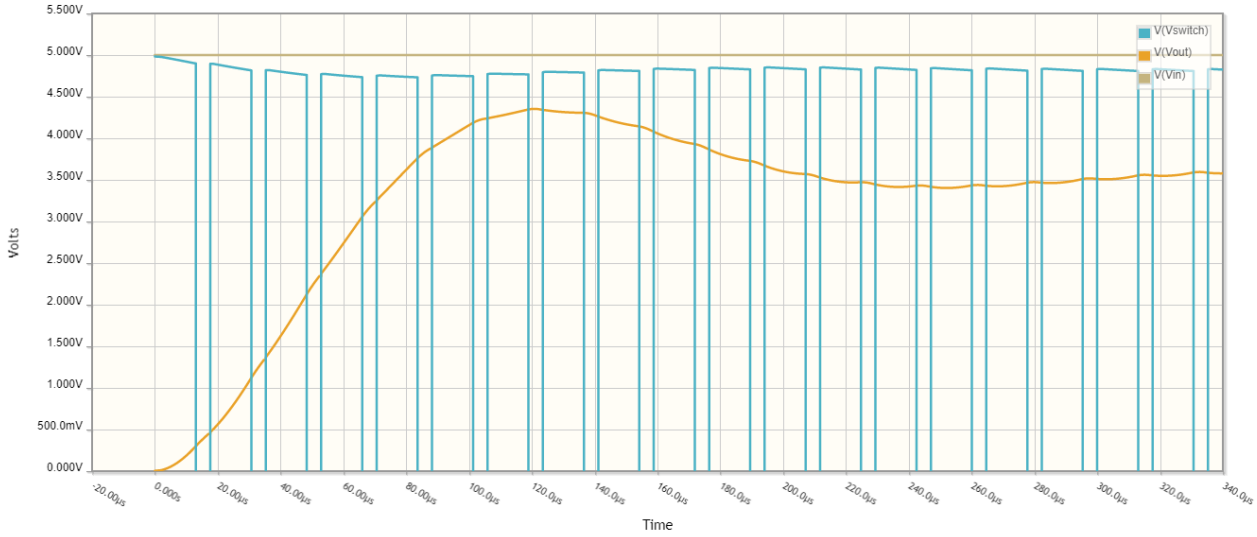
7. 3.3V



2V

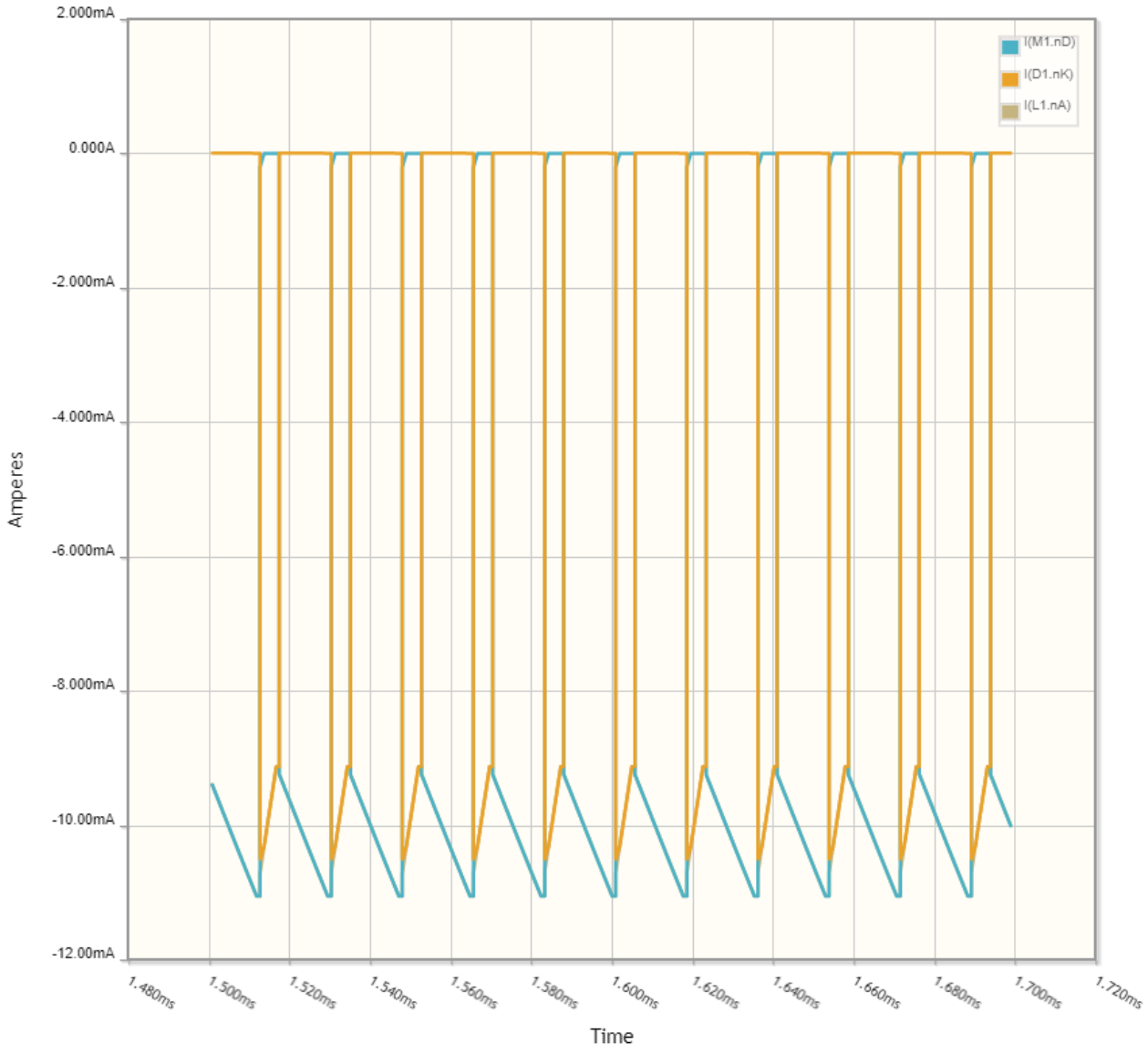


8.



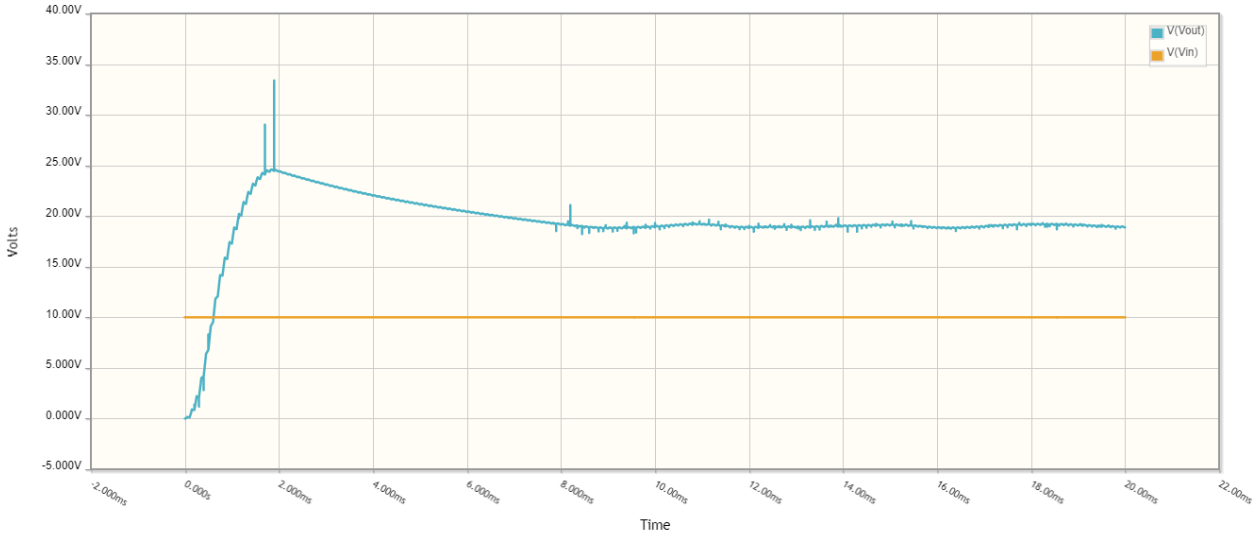
Because we have capacitor and inductor in the circuit, there is definitely the charge and discharge stage in the circuit, which will influence the output voltage. And by changing those two items values, we could identify the results for what we need for design.

9.



10. Since we have a KCL circuit, IL1+ID1 = IM1 according to the circuit diagram, so as the parameters were related to their electrical properties (Capacitor and Inductor), this is the result that made sense to the circuit diagram.

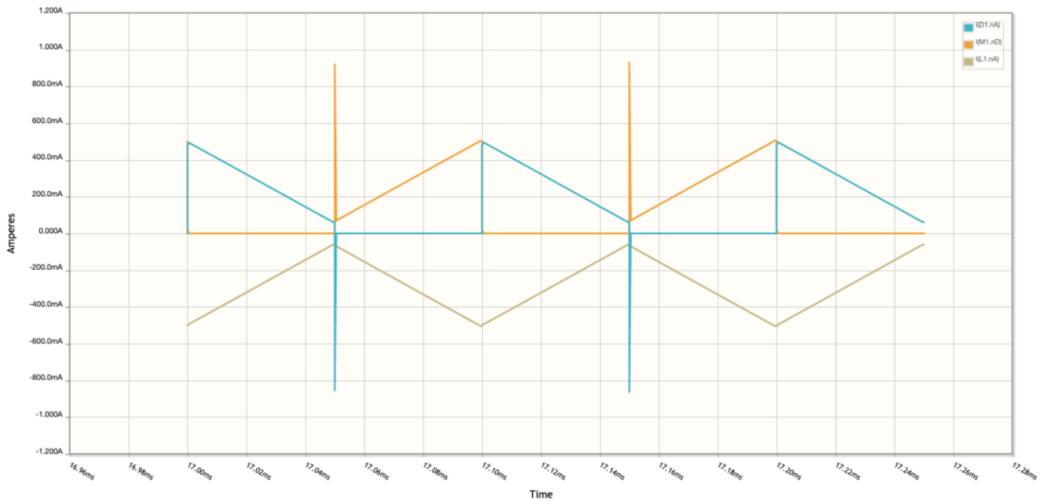
11.



12. Yes it is. Since we had the voltage boosted up. But those straight peaks are sort of unexpected, which could be the simulation vs calculation difference.

13. Since we had 20m as step time and 1u for the interval of the time, which is larger than what we had in the previous problem for the total amount of time steps. Also, we had a large overshoot on voltage compared to the previous one, so it will acquire more time to recover. But the main reason is definitely the amount of time points.

14.



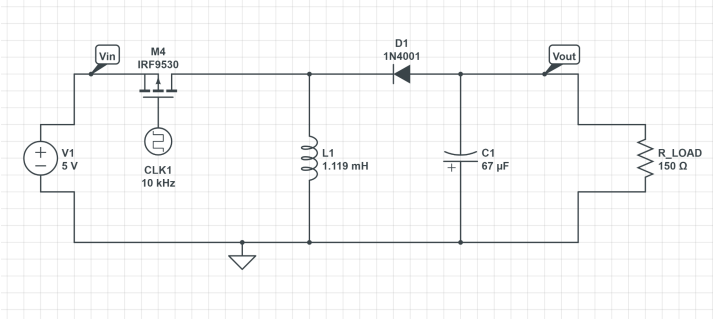
15. As our equation for KCL is still valid, with ID1(nA) + IM1(nD) + IL1(nA), the simulation data still makes sense as the sum of those circuits' current is 0.

16.

Jack	USB	Power Source?	NODE1	NODE2	NODE3
0V	5V	USB	-928.8uV	4.999V	3.3V
10V	0V	Jack	5.001V	5V	3.3V
10V	5V	Jack	5.001V	5V	3.3V
3V	3V	USB	-928.8uV	4.999V	3.3V

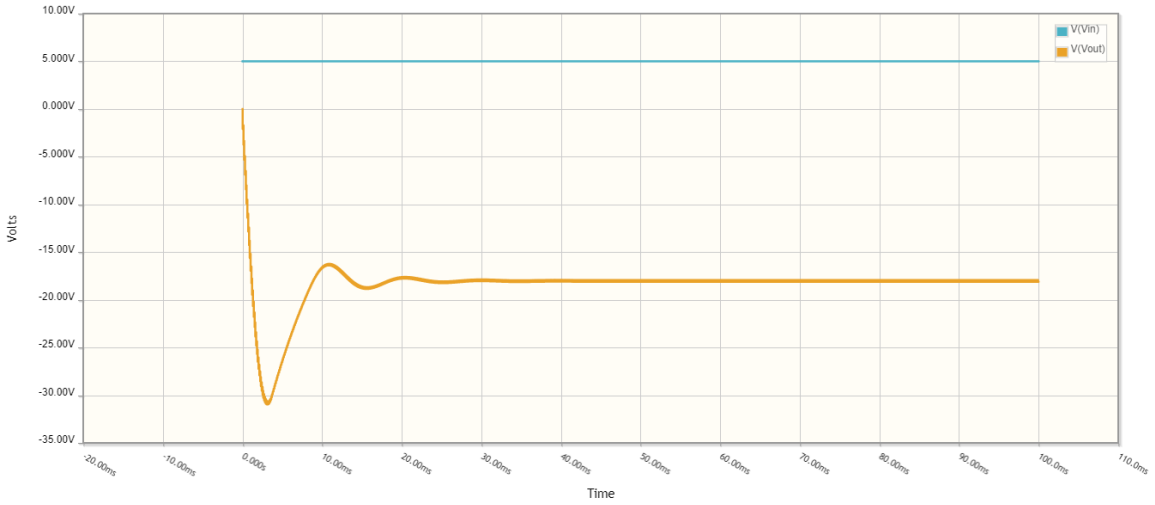
17. Because if we decide to use non-inverting-input without a voltage divider, then what will happen is that the input voltage won't be able to be 3.3V, instead, it will be larger than 3.3V all the time. As a result, the circuit will not run as we implemented.

18.



https://www.circuitlab.com/circuit/b2e34jc7wz5q/circuit-for-q18-ese519lab1/

20.



21. MOSFET are more for high power use and is more expensive than BJT, but BJT also have three terminals as MOSFET