```
module mux2_1 (x,y,v,d);
output reg x , y , v ;
input [3:0] d;
always@(d)
begin
x = d[2] | d[3];
y = d[1] | d[3];
v = d[0] | d[1] | d[2] | d[3];
end
endmodule
module test_mux;
reg [3:0]d;
mux2_1 mux (x, y, v,d);
initial
begin
d[0]=0;d[1]=0;d[2]=0;d[3]=0;
  #10 d[0]=1; d[1]=0; d[2]=0; d[3]=0;
  #10 d[0]=0; d[1]=1; d[2]=0; d[3]=0;
  #10 d[0]=0; d[1]=0; d[2]=1; d[3]=0;
```

```
end
initial
begin
$display(" time out x y v");
monitor(time, " \%b \%b \%b", x, y, v);
end
initial
begin
$dumpfile("mux_t.vcd");
$dumpvars;
end
```

endmodule

#10 d[0]=0; d[1]=0; d[2]=0; d[3]=1;

