**Computer Organization**

**HDL simulator you used (ModelSim or Xilinx):**

**ModelSim**

**The input fields of each pipeline register:**

**IFID:** **clk\_i, rst\_n, pc\_addr\_i , pc\_instr\_i**

**IDEX:** **clk\_i, rst\_n, pc\_addr\_i , aluop\_i , alusrc\_i , regdst\_i , memread\_i , , memwrite\_i , branch\_i, branchtype\_i , memtoreg\_i , rs\_addr\_i , rt\_addr\_i , rs\_data\_i , rt\_data\_i , sign\_data\_i , RegWrite\_i , , opcode\_i, z\_data\_i**

**EXMEM:** **clk\_i, rst\_n , memread\_i , memwrite\_i , branch\_i , zero\_i , memtoreg\_i , alu\_i , rt\_i , rd\_addr\_i , branch\_data\_i , RegWrite\_i ,**

**MEMWB:** **clk\_i, rst\_n, dm\_i, alu\_i , memtoreg\_i , rd\_addr\_i , RegWrite\_i ,**

**Compared with lab4, the extra modules:**

**IFID IDEX EXMEM MEMWB reg , pc\_src2 the mux2to1 before pc**

**Problems you met and solutions:**

**全部線都要重接，變數名稱打錯，線太多等線太多所造成的問題**

**Ans:線剛接出來時名稱後面接1，經過一reg變2，依此類堆**

**Summary:**

**因為還沒做fordwarding，bubble，所以這次還沒碰到一些hazard**

