**Computer Organization**

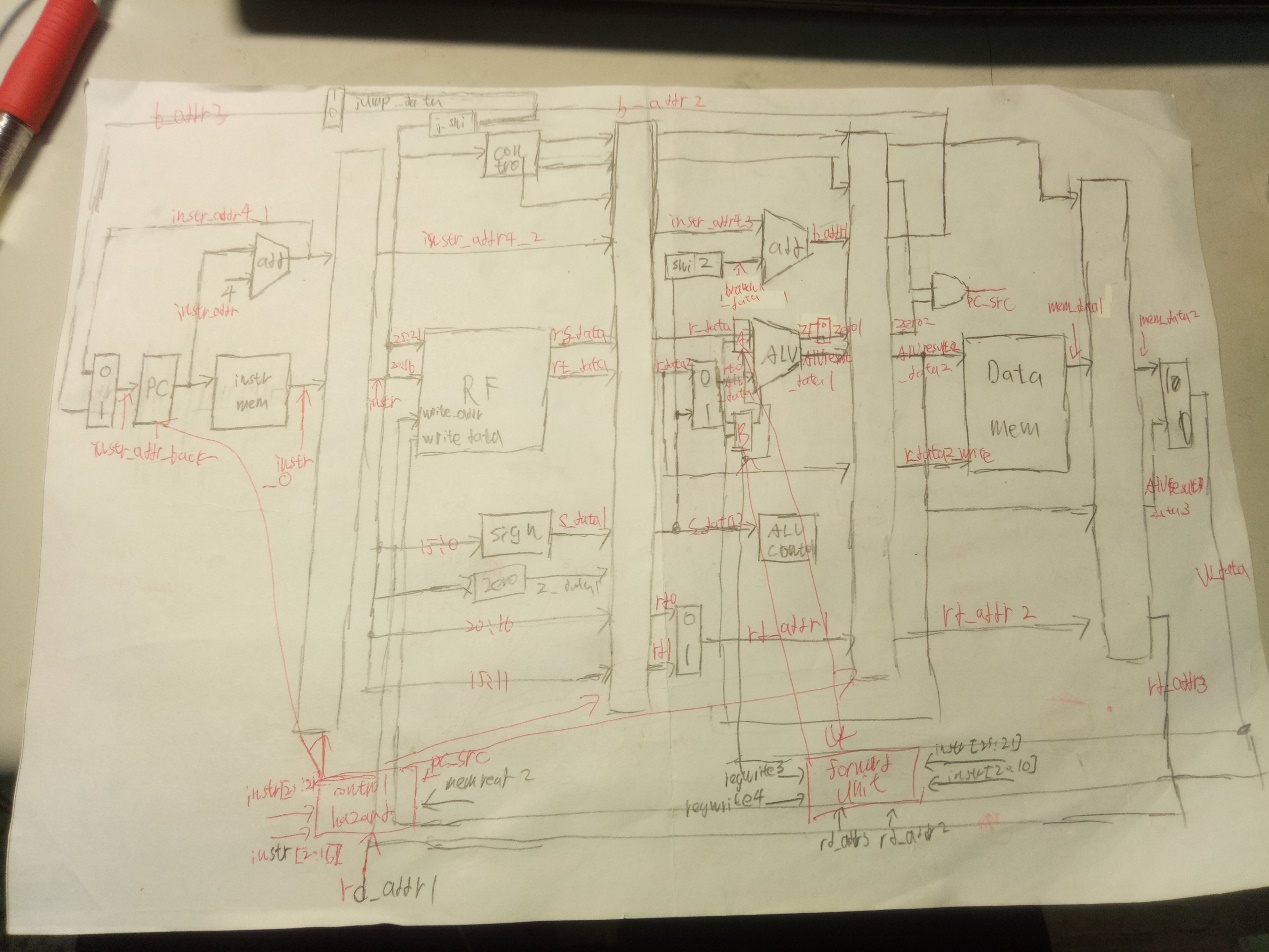
**HDL simulator you used:**

**modelsim**

**Finished part:**

**A b c**

**Architecture diagrams:**

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**Hardware module analysis:**

**Forward unit:決定Alu input 來源來自WB OR MWM OR ID**

**Data hazard:若偵測到LW 暫停IF一個CYCLE 若偵測到BRANCH OR JUMP FLUSH掉前三個PIPLINE REG**

**Problems you met and solutions:**

**注意線有沒有接對**

**Summary:**

照課本處理DATA HAZARD