

Residual Metallic Contamination of Transferred Chemical Vapor Deposited Graphene

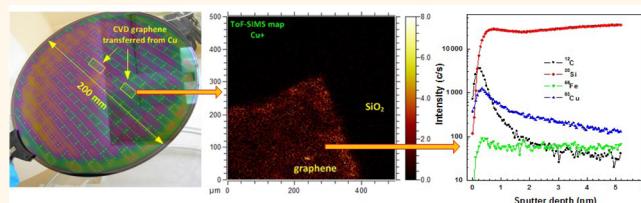
Grzegorz Lupina,^{*,†} Julia Kitzmann,[†] Ioan Costina,[†] Mindaugas Lukosius,[†] Christian Wenger,[†] Andre Wolff,[†] Sam Vaziri,[‡] Mikael Östling,[‡] Iwona Pasternak,[§] Aleksandra Krajewska,[§] Wlodek Strupinski,[§] Satender Kataria,[⊥] Amit Gahoi,[⊥] Max C. Lemme,[⊥] Guenther Ruhl,^{||} Guenther Zoth,^{||} Oliver Luxenhofer,^{||} and Wolfgang Mehr[†]

[†]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany, [‡]School of ICT, KTH Royal Institute of Technology, Isafjordsgatan 22, 16440 Kista, Sweden,

[§]Institute of Electronic Materials Technology, Wolczynska 133, 01-919 Warsaw, Poland, [⊥]University of Siegen, Hölderlinstr. 3, 57076 Siegen, Germany,

^{||}Infineon Technologies AG, Regensburg 93049, Germany, and [¶]Infineon Technologies Dresden GmbH, Dresden 01099, Germany

ABSTRACT Integration of graphene with Si microelectronics is very appealing by offering a potentially broad range of new functionalities. New materials to be integrated with the Si platform must conform to stringent purity standards. Here, we investigate graphene layers grown on copper foils by chemical vapor deposition and transferred to silicon wafers by wet etching and electrochemical delamination methods with respect to residual submonolayer metallic contaminations. Regardless of the transfer method and associated cleaning scheme, time-of-flight secondary ion mass spectrometry and total reflection X-ray fluorescence measurements indicate that the graphene sheets are contaminated with residual metals (copper, iron) with a concentration exceeding 10^{13} atoms/cm². These metal impurities appear to be partially mobile upon thermal treatment, as shown by depth profiling and reduction of the minority charge carrier diffusion length in the silicon substrate. As residual metallic impurities can significantly alter electronic and electrochemical properties of graphene and can severely impede the process of integration with silicon microelectronics, these results reveal that further progress in synthesis, handling, and cleaning of graphene is required to advance electronic and optoelectronic applications.



KEYWORDS: CVD graphene · transfer · metallic contaminations · ToF-SIMS · TXRF

Graphene has a great potential to provide a performance boost for the next generation of high-frequency electronic and photonic devices.^{1–7} In view of these applications, chemical vapor deposition (CVD) on metal surfaces is currently one of the most relevant graphene synthesis techniques delivering large-area and good-quality material.⁸ Practical use of transferred CVD graphene in electronic and photonic devices will likely require a co-integration of the new material with the existing semiconductor device manufacturing platforms. For example, CVD graphene will have to comply with very stringent purity standards. A large research effort has been dedicated so far to study residual polymer impurities resulting from graphene transfer.⁸ Significantly less attention has been paid to potential submonolayer metallic contamination of graphene

associated with the growth on and transfer from metal catalysts, such as Cu or Ni. Since trace impurities in silicon can result in detrimental effects on the performance of electronic devices, detection and control of metal contaminants in Si-integrated circuit manufacturing are of critical importance to achieve high product yield. The effects of metal contamination (e.g., Cu, Ni, Fe) include junction leakage current increase and lifetime and dielectric strength degradation.⁹ Even at very low concentrations (10^{10} – 10^{11} atoms/cm²), trace metals pose a serious threat to Si devices.¹⁰ Since CVD graphene is usually synthesized on metallic surfaces, the growth and transfer processes can potentially cause residual contamination of graphene sheets. Although graphene is reported to be an effective barrier against Cu diffusion,¹¹ residual Cu atoms from contaminated graphene can potentially

* Address correspondence to lupina@ihp-microelectronics.com.

Received for review February 26, 2015 and accepted April 8, 2015.

Published online April 08, 2015
10.1021/acsnano.5b01261

© 2015 American Chemical Society

out-diffuse toward the substrate in the course of further device processing and result in degradation of device parts located beneath graphene. This can be expected based on the ability of Cu atoms (ions) to diffuse (drift) through dielectrics under thermal or electrical stress.^{12,13} Residual metals released during device processing can also cause cross-contamination of sensitive manufacturing tools. Finally, it has been demonstrated that residual metallic impurities can significantly alter electronic and electrochemical properties of graphene.^{14–16} It has been also shown that, even if nuclear purity graphite is used as the source material for graphene synthesis, the latter can be contaminated with impurities originating from chemical reagents used for processing.¹⁷

The presence of metallic impurities on graphene transferred from Cu substrates was recently confirmed using various techniques such as inductively coupled plasma mass spectrometry, X-ray energy-dispersive spectroscopy, energy electron loss spectroscopy, and X-ray photoelectron spectroscopy (XPS) in several publications.^{14,18,19} It has been shown that a wet Cu etching combined with a modified standard clean 2 (SC-2) used in Si device manufacturing²⁰ reduces the concentration of residual metals below the detection limit of XPS tools,¹⁹ being about 0.1 atom %.²¹ However, to verify if stringent purity standards of Si-integrated circuit (IC) manufacturing lines are met, investigations with more sensitive techniques are required.²²

RESULTS AND DISCUSSION

The facts listed above motivate our study of residual transfer-related metallic contamination (Cu, Fe, etc.) of large-area CVD graphene. We investigate different transfer methods involving different polymer support films combined with various strategies of detaching graphene from the metal catalyst substrate (using different Cu etchants and electrochemical delamination). We use time-of-flight secondary ion mass spectrometry (ToF-SIMS) and total reflection X-ray fluorescence (TXRF) to obtain elemental fingerprints of residual contamination with a sensitivity better than 10^9 atoms/cm². ToF-SIMS offers the capability of high-resolution elemental or molecular fragment mapping; however, due to the strongly varying matrix-dependent ionization cross sections, it is very difficult to quantify the measured elemental concentrations. TXRF, on the other hand, is easily quantifiable but does not yield spatial resolution. Thus, we calibrated ToF-SIMS using reference graphene samples measured by TXRF before. In this way, we experimentally demonstrate that even extensive wet chemical cleaning procedures fail to remove residual Cu completely, and that there is a trade-off between the purity of the fragile graphene layer and its structural integrity. Furthermore, our results indicate that Cu impurities transferred along with graphene onto Si wafers can negatively affect the

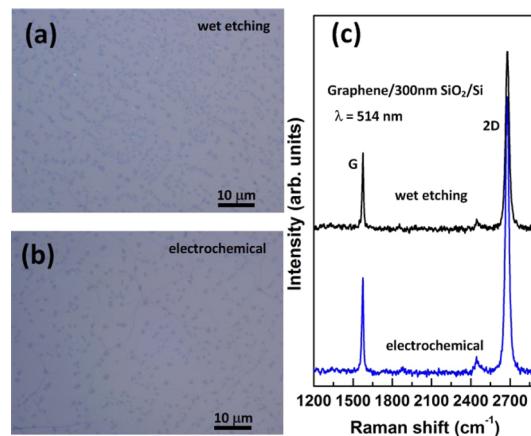


Figure 1. Comparison of graphene layers transferred using wet etching and electrochemical delamination. (a,b) Optical microscope images. Dark spots are multilayer graphene islands. (c) Corresponding Raman spectra.

minority carrier diffusion length in the Si substrate. Experiments presented here were performed on graphene samples grown and transferred in several different laboratories. The set was complemented with samples grown and transferred by commercial graphene material manufacturers and suppliers.

About $1 \times 1 \text{ cm}^2$ pieces of CVD graphene on Cu foils (for details, see Methods) were transferred onto three kinds of substrates: 300 nm SiO₂/Si(100), p-Si(100) wafers covered with native SiO₂, or patterned p-Si(100) substrates with Si pillars embedded into SiO₂. Different polymers such as poly(methyl methacrylate) (PMMA) and polystyrene (PS) were used as supports during the transfer process. There was no clear influence of the type of polymer on the concentration of residual metallic impurities. Unless explicitly stated otherwise, data reported here refer to PMMA-supported transfer. To detach the graphene layer from the Cu substrate, electrochemical delamination (EC)²³ and wet etching^{24,25} using ammonium persulfate (APS), FeCl₃, and H₂SO₄ solutions were performed (see Methods).

The quality of the transfer process for each sample was controlled with optical microscopy (OM) and Raman spectroscopy. Figure 1a,b shows OM images of graphene layers transferred onto 300 nm SiO₂/Si using wet etching and electrochemical delamination. Figure 1c shows the corresponding representative Raman spectra. In general, both transfer techniques result in good-quality graphene with a low amount of cracks and holes and a low-intensity Raman D band (see also Supporting Information, Figures S1 and S2). For ToF-SIMS measurements, the $1 \times 1 \text{ cm}^2$ graphene patches were inspected with OM and Raman spectroscopy and the areas with the best quality (*i.e.*, low amount of holes and particles, low Raman D band) were selected for further investigation.

Figure 2 presents an illustrative example of ToF-SIMS investigations performed on a graphene layer transferred

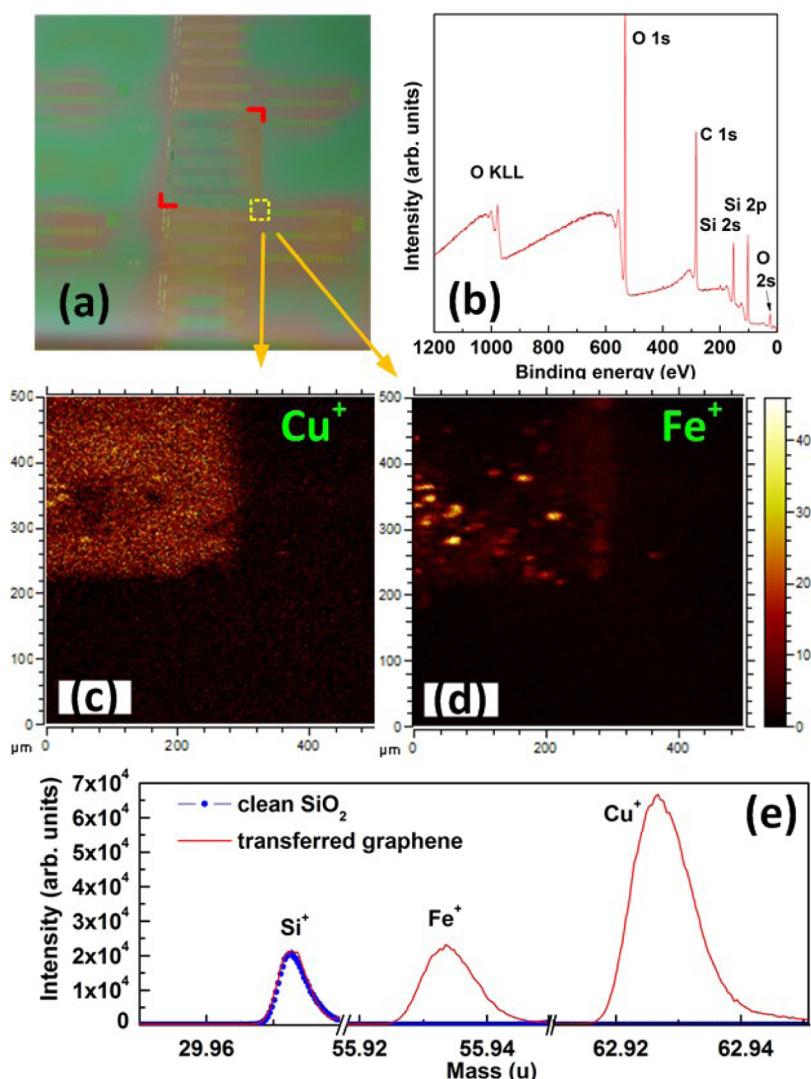


Figure 2. Residual metallic contaminations on CVD graphene. (a) Photograph of $\sim 1 \times 1 \text{ cm}^2$ large graphene flake transferred to a patterned Si chip. (b) XPS overview scan on the area covered by graphene. (c,d) ToF-SIMS $^{63}\text{Cu}^+$ and $^{56}\text{Fe}^+$ maps on the corner of the graphene layer. ToF-SIMS mass spectra in selected regions acquired on transferred graphene and on a clean SiO_2 reference sample (e). Spectra are normalized to the intensity of the ^{30}Si peak.

onto a patterned substrate (Figure 2a) using an FeCl_3 -based wet etching method. While XPS (Figure 2b) does not detect any metallic species on the surface, the ToF-SIMS maps (Figure 2c,d) acquired in the bunched mode show clear evidence of Cu and Fe residuals on the areas covered with graphene (see Supporting Information for additional XPS results). Comparison of ToF-SIMS mass spectra for a thermally grown 300 nm SiO_2/Si substrate without and with graphene (Figure 2e) proves that the presence of residual metals is related to the graphene transfer process. In general, the regions close to the edge of the graphene flake appear to be more heavily contaminated, showing relatively large agglomerations of metallic impurities. This can be caused by the mechanical deformation of the PMMA/graphene/Cu stack during cutting of the graphene/Cu stack into smaller pieces. As the edge regions were found to be nonrepresentative of the sample, all

further measurements were performed on the areas located at least $500 \mu\text{m}$ away from the graphene edge to enable reliable analysis and meaningful comparison between different samples.

An example of such a measurement on five different spots across the sample is illustrated in Figure 3a. Mass spectra in the $^{56}\text{Fe}^+$ and $^{63}\text{Cu}^+$ regions (Figure 3b) indicate that the intensity of the Cu^+ and Fe^+ signals is relatively uniform. Also, the individual ToF-SIMS maps acquired at different positions indicate, in contrast to the edge regions, a homogeneous distribution of metallic contaminants within the mapping area of $500 \times 500 \mu\text{m}^2$ (Figure 3c). Larger Cu agglomerates were observed only occasionally.

Figure 4 summarizes the Cu surface concentration values measured with ToF-SIMS calibrated to TXRF for graphene samples obtained by different detachment methods. We found that there is a broad distribution of

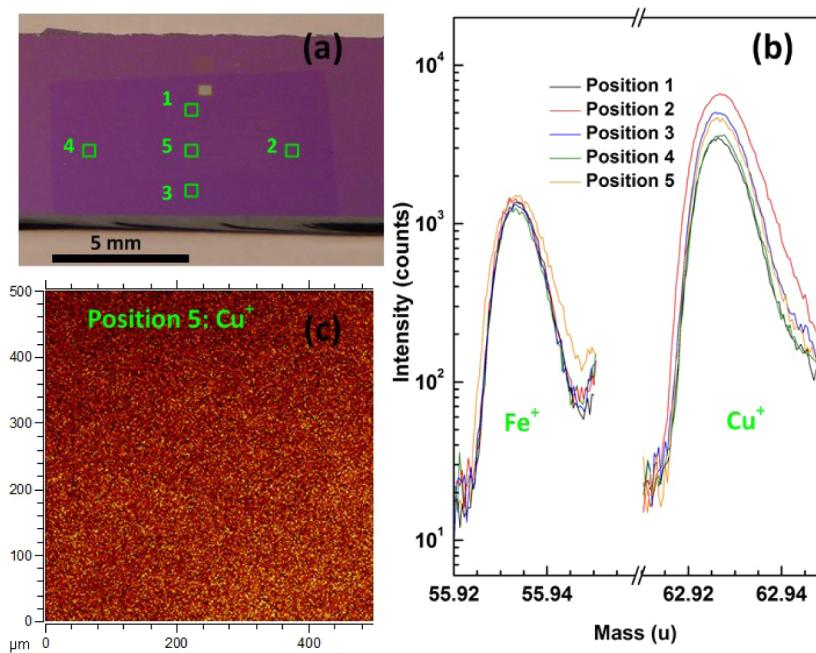


Figure 3. Distribution of metallic contaminants on the surface. (a) Optical microscope image of a graphene layer transferred onto a 300 nm SiO_2/Si substrate. (b) ToF-SIMS mass spectra in $^{56}\text{Fe}^+$ and $^{63}\text{Cu}^+$ regions acquired at different points across the sample. Positions refer to the areas marked in panel (a). (c) 500 \times 500 μm^2 ToF-SIMS map of Cu^+ in the center of the sample. Measurements in panel (b) have been normalized to the $^{30}\text{Si}^+$ peak intensity.

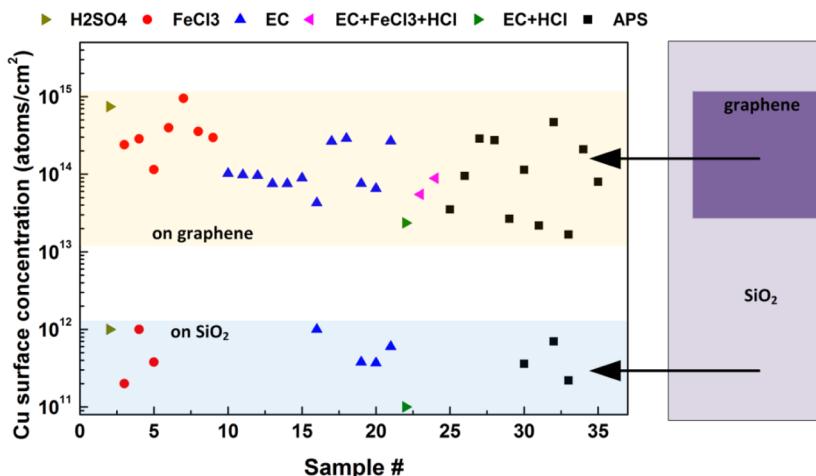


Figure 4. Comparison of surface concentration of Cu for different transfer methods. Measurements on graphene were performed in the center of the flake. Control measurements on the SiO_2 substrate were performed \sim 0.5–1 mm away from the edge of the graphene flake.

Cu surface concentration values ranging from 10^{13} to 10^{15} atoms/cm² for various graphene sources and transfer techniques. Furthermore, the amount of Cu residuals does not strongly depend on the type of the Cu etchant. Separate experiments confirmed that the chemicals used (VLSI grade) in various transfer processes were free of Cu traces (within detection limit of ToF-SIMS). The lowest concentrations of residual Cu are found on samples etched in APS. However, this group of samples shows also the largest distribution of results. On samples etched in FeCl_3 apart from Cu, a significant amount of Fe residuals was found. Although the latter can be quite effectively removed by the

modified SC-2 clean,¹⁹ the FeCl_3 -based etchant does not present any advantage over APS and electrochemical delamination in terms of residual Cu. For this reason, only Fe-free detachment methods were used in further experiments. Interestingly, very similar amounts of Cu were found on graphene layers prepared by electrochemical delamination and wet etching. For some types of starting graphene material, electrochemical delamination produced heavily contaminated graphene samples (Supporting Information, Figure S4). This suggests that the delamination process should be adjusted to a given graphene type to obtain a clean detachment. Subsequent treatment of

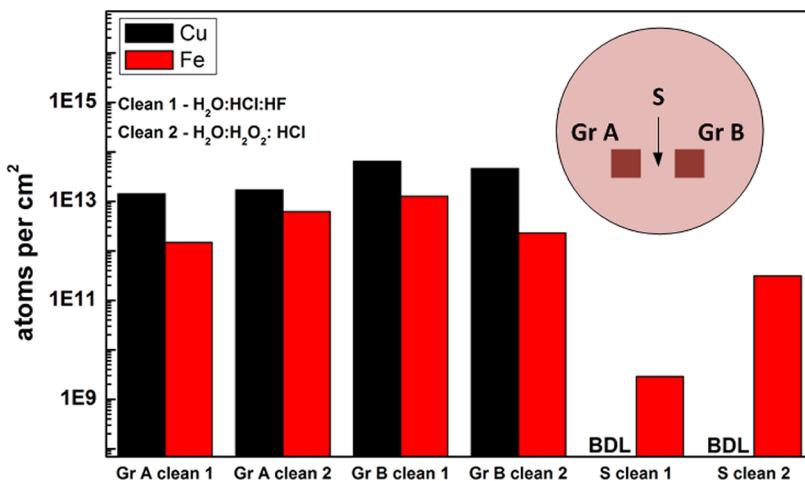


Figure 5. Surface concentration of Cu and Fe impurities measured by TXRF for two graphene samples from different sources (Gr A and Gr B) transferred onto 200 mm wafers using optimized transfer/cleaning protocols. BDL (below detection limit) indicates that no Cu impurity was detected in the neighborhood of the graphene patches (indicated by arrow, S).

delaminated graphene in, for example, HCl solutions usually reduced slightly the residual Cu amount to a level below 5×10^{13} atoms/cm². However, samples with a Cu impurity level lower than 10^{13} atoms/cm² could not be obtained with any of the mentioned methods. At the same time, measurements on the SiO₂ substrate in the direct neighborhood of the flake (~ 0.5 –1 mm away from the graphene edge) indicated contamination of 10^{11} – 10^{12} Cu atoms/cm².

Figure 5 presents results obtained for optimized transfer and cleaning protocols, thus constituting the cleanest graphene samples obtained in this work on 200 mm wafer substrates. Here, APS was used to etch Cu foil, and the PMMA/graphene stack was rinsed several times in DI H₂O. Subsequently, samples were placed in a HCl-based cleaning solution to remove metallic residuals from graphene. Finally, graphene with PMMA was moved to a large volume container with DI H₂O and transferred to the target wafer. Special care was taken to eliminate all metallic tools (tweezers, scissors, etc.) from the transfer process. The concentration of Cu in the neighborhood of the graphene patches (indicated by arrow, S) is below the detection limit (BDL), indicating that the process does not contaminate the wafer with Cu beyond areas covered with graphene (for example, by redeposition during the final rinsing step). At the same time, the concentration of Cu impurities on the areas covered with graphene stills exceeds 1×10^{13} atoms/cm². Moreover, significant amounts of Fe residuals are found both on graphene and on the uncovered SiO₂ surface.

Given this evidence, it can be speculated that at least part of residual Cu may be “enclosed” into the graphene layer, making it inaccessible for Cu etchants. Sublimation of Cu during the graphene growth process and formation of graphene wrinkles during cooling^{26,27} could, for example, result in Cu atoms being trapped in graphene pockets isolated from the

Cu substrate. We also did not find a clear correlation between the Cu foil temperature during graphene growth and the amount of impurities after growth (Supporting Information, Figure S8). Similarly, we were unable to resolve any accumulations of Cu atoms which could be associated with grain boundaries, wrinkles, graphene adlayers, or any other morphological features. An example of such attempt is illustrated in Figure 6, which shows a secondary ion (SI) image and a corresponding ToF-SIMS $^{63}\text{Cu}^+$ map acquired in the burst alignment mode on the area of $20 \times 20 \mu\text{m}^2$. Bright dots visible in the SI image (Figure 6a) correlate well with the multilayer islands visible in the optical microscope images (compare Figure 1). In the $^{63}\text{Cu}^+$ map (Figure 6b) acquired on the same position, these areas (examples marked with green circles) appear to have lower surface concentration of Cu than the monolayer graphene regions between the islands (red circles). This, however, may also be a consequence of the fact that in this mapping mode information is collected from the topmost surface layer only. As a result, Cu impurities under thicker graphene islands do not contribute to the acquired Cu distribution image as strongly as those located below monolayer graphene regions. Yet, we found it difficult to resolve this with a sequence of mapping–sputtering steps (Supporting Information, Figure S5).

In an attempt to further reduce the surface concentration of Cu, we investigated the effect of prolonged etching time in APS. According to these experiments, there is a significant difference in the amount of Cu present on the surface of samples etched for 8 and 72 h, as shown in Figure 7a. Surface concentration of Cu decreases as the result of longer etching time by 50%. This apparent improvement in purity comes, however, at the expense of graphene layer integrity. As illustrated by optical microscope images in Figure 7b,c, prolonged contact with the Cu etchant results in the

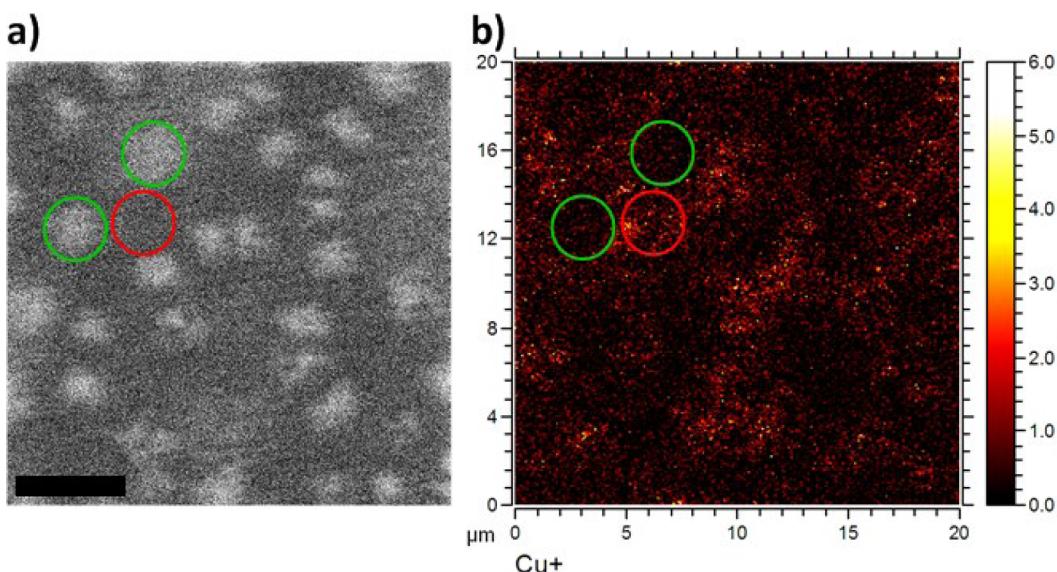


Figure 6. High lateral resolution ToF-SIMS imaging on optimized samples. (a) Secondary ion image showing multilayer graphene islands (bright spots) on monolayer graphene (dark background). The scale bar is $5\text{ }\mu\text{m}$. (b) Surface map of $^{63}\text{Cu}^+$ on the same region showing a correlation between the position of the islands and the surface concentration of Cu. Green and red circles mark the corresponding positions on both images.

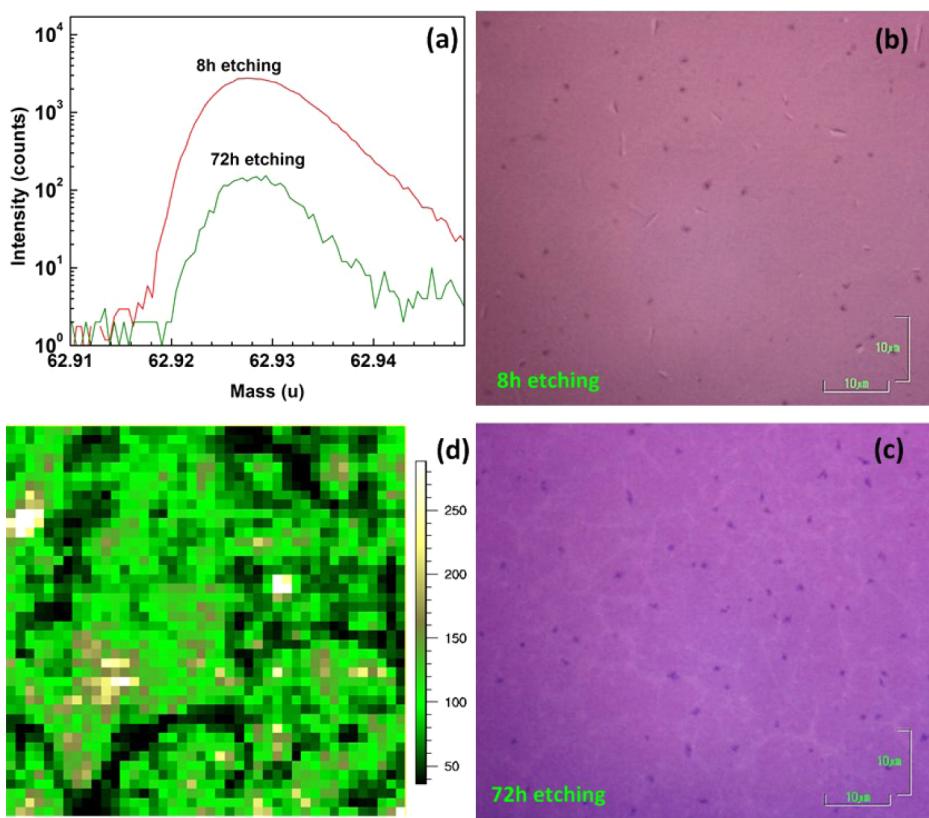


Figure 7. Investigation of prolonged wet etching time on the concentration of Cu residuals and the quality of graphene layers. (a) ToF-SIMS mass spectra in the ^{63}Cu region for samples with different etching time in APS solution. (b,c) Optical microscope images of graphene layers transferred to SiO_2 substrates after 8 and 72 h etching. (d) Raman 2D peak intensity mapping on a sample etched for 72 h. Mapped area is $20 \times 20\text{ }\mu\text{m}^2$.

appearance of cracks visible as a network of bright lines in Figure 7c. Graphene seems to be washed away in these areas, and the layer becomes discontinuous. This conclusion is in line with Raman map measurements

performed on the sample etched for 72 h (Figure 7d). The intensity of the 2D peak vanishes in some areas (black), reproducing a network of lines observed in optical images. Although it appears to be cleaner

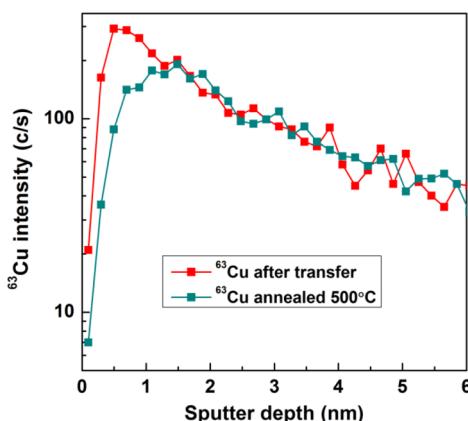


Figure 8. Influence of annealing on the amount of Cu residuals. Sample transferred onto native SiO₂/Si substrate was annealed in UHV at 500 °C for 30 min. Sputtering was performed with 0.5 keV Cs ions.

according to ToF-SIMS, the graphene layer clearly becomes patchy after prolonged etching.

On the basis of the above observations, one can conclude that at least a part of the residual Cu atoms is trapped within the graphene layer and remains insensitive to etching and cleaning treatments. In this way, CVD graphene is transferred to the target substrate along with trace amounts of metallic contaminations. To assess if the residual metal is mobile and may out-diffuse during subsequent thermal treatment, we performed several annealing experiments followed by ToF-SIMS and minority charge carrier diffusion length measurements.

Figure 8 shows ToF-SIMS Cu⁺ profiles from a graphene sample transferred onto a native SiO₂/Si substrate and annealed subsequently at 500 °C in ultrahigh vacuum (UHV) (10⁻⁸ mbar) for 30 min. Comparison of profiles taken before and immediately after annealing indicates that the thermal treatment resulted in a substantial reduction of the Cu concentration on the surface. This may imply a partial release of the Cu atoms from graphene and their diffusion into the underlying Si, in line with the ability of Cu ions to penetrate thin SiO₂ layers.²⁸

Minority charge carrier diffusion length (or the corresponding carrier lifetime) measurement is extremely sensitive to the smallest amounts of impurities and, hence, is an ultimate method for characterization of material quality and process control. It is widely used in silicon IC manufacturing for monitoring heavy metal contamination and key IC processing steps. The minority carrier lifetime is defined as the average time it takes an excess minority carrier to recombine. Low minority carrier lifetimes (low diffusion lengths) can be indicative of metal contamination. In particular, Cu precipitates were reported to be extremely efficient minority carrier recombination sites.²⁹ To investigate the potential influence of the residual Cu on the minority carrier lifetime in the Si substrate, two pieces

of graphene from different suppliers were transferred onto a p-type Si(100) wafer covered with native SiO₂ (Figure 9a). After transfer, the wafers with graphene were annealed at 600 °C for 5 min in N₂. Subsequently, carrier diffusion length was measured point-by-point to create a map of the wafer shown in Figure 9b.

The diffusion length map (Figure 9b) has been measured after optical activation of Cu and Fe impurities.³⁰ It clearly shows a significantly reduced diffusion length at exactly the two regions where the graphene flakes have been deposited (the strongly reduced diffusion length at the edge of the wafer is due to an unintentional contamination of the wafer edge and is not further considered). At these spots, the diffusion length is about 300–350 μm compared to about 500 μm of a reference region at the wafer center. After storage of the sample at room temperature for several days, a repeated diffusion length measurement showed a nearly complete recovery of the diffusion length at the two spots to values close to the values of the reference region. Further measurements after optical or thermal treatment (200 °C/5 min) resulted again in a significantly reduced diffusion length at the two regions. This reduction is again reversible as further measurements showed. From these observations, the following conclusion can be drawn. A relatively small part of the diffusion length drop is due to Cu impurities (small precipitates) that usually form after optical activation of Cu-contaminated p-type Si and that reduce the diffusion length of minority carriers. This reduction is not reversible.³⁰ The major part of the diffusion length reduction stems from Fe impurities because we observe the typical recovery of the diffusion length during storage at room temperature and the reversible reduction after repeated optical or thermal activation of Fe impurities.³¹ From the diffusion length change, an Fe concentration in the range of 10¹⁰ atoms/cm⁻³ can be estimated. We note that samples for this experiment were prepared by etching Cu in APS (FeCl₃-free transfer process) and that the origin of the Fe contamination is currently unknown. One of the possibilities is unintentional contamination during the graphene growth process or handling, as shown by our control measurements on as-shipped samples prior to transfer (Supporting Information, Figure S9).

ToF-SIMS profiles shown in Figure 9c, taken from one of the places covered by graphene (indicated by purple arrow in Figure 9b), appear to corroborate this claim. The ⁶³Cu profile after annealing shows a high concentration in the top few nanometers and approach the iron concentration in the bulk. In analogy to the case illustrated in Figure 8, the concentration of Cu at the surface decreased by about 40–50% as a result of the annealing treatment. Results of a reference experiment in which the native SiO₂/Si surface was intentionally contaminated with Cu to a nominal level of about 5 × 10¹⁴ atoms/cm² indicates that unbound Cu diffuses

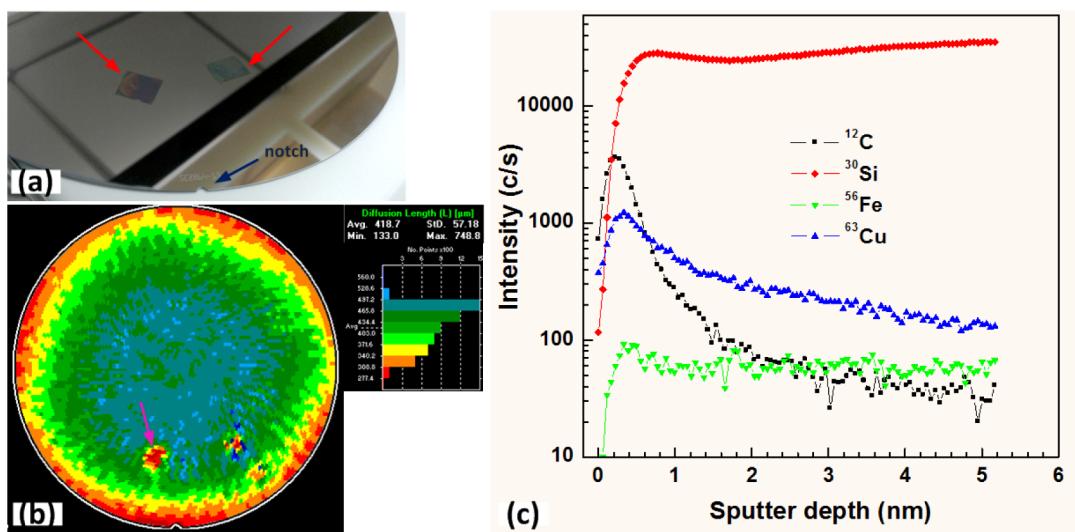


Figure 9. (a) Photograph of graphene layers transferred onto a native $\text{SiO}_2/\text{Si}(100)$ wafer. Photograph taken before PMMA removal; red arrows indicate the graphene locations. (b) Minority carrier diffusion length measurements on a p-type Si wafer with graphene flakes after annealing at $600\text{ }^\circ\text{C}$ for 5 min and optical activation of impurities.³⁰ (c) ToF-SIMS sputter profile on the graphene flake indicated by purple arrow in panel (b). Sputter depth profiling was performed with 1 keV O_2 ions.

easily into Si and its concentration drops by 2 orders of magnitude after being subjected to a similar thermal budget (Supporting Information, Figure S6). The amount of Fe and Cu found in the graphene on the surface is more than enough to explain the diffusion length measurements in the bulk after annealing. Therefore, no clear quantitative conclusion can be drawn about the mobility of the contaminations. However, it can clearly be stated that Cu and Fe contaminations in graphene are, in principle, mobile to a significant amount. Due to the fact that much lower Cu surface contaminations ($\sim 10^{12}$ atoms/cm 2) can cause a far stronger degradation of minority carrier diffusion length in n-type Si than in p-type Si,²⁹ results presented here call for more attention and further studies in this direction.

CONCLUSIONS

In semiconductor device manufacturing platforms, contamination control is absolutely essential because even small amounts of impurities can result in altered device parameters, reliability, and yield problems. This is reflected, for example, in the stringent specifications for high-purity raw materials. Here, we investigated the purity of large-area CVD graphene transferred from Cu to SiO_2/Si substrates with particular attention to a submonolayer Cu contamination. Our experiments show that, regardless of the transfer method

and subsequent cleaning, trace amounts of metals ($\sim 10^{13}$ – 10^{14} atoms/cm 2) are found on CVD graphene transferred to the target wafer. In the back-end-of-line (BEOL) integration of graphene devices,³ such contaminations may not play a significant role as most of the modern BEOL metallization layers are Cu-based. However, even such small amounts may be relevant when front-end-of-line (FEOL) integration approaches for electronic and photonic devices in Si IC fabrication lines are considered. In such a case, metallic impurities can lead to the contamination of Si devices and cross-contamination of fabrication tools. We find that a part of the residual Cu atoms can be released upon thermal treatment and out-diffuse, affecting the minority carrier diffusion length in the Si substrate. According to our findings, the amount of impurities on graphene varies depending on the source of graphene and, as a consequence, may be dependent on the CVD process used for graphene synthesis. These results call for more attention to the topic of submonolayer metallic contaminations of graphene and its influence on the performance of devices based on this new material. Clearly, further improvements in the transfer and cleaning technology are required to provide material of high quality and purity as demanded by microelectronic applications. This also includes the investigation of alternative metal catalyst-free paths for the fabrication of graphene directly on insulators and semiconductors.^{32–34}

METHODS

Sample Preparation. In the experiments described above, we used either various types of commercially available graphene on Cu or graphene grown in our laboratories. In the latter case, 4 cm \times 2 cm pieces of 25 μm thick Cu foil (AlfaAesar) were ultrasonically cleaned in acetone and was rinsed using isopropyl

alcohol (IPA). The foil was loaded in a nano-CVD chamber (Moorefield, UK). The chamber was purged five times using 200 sccm of Ar gas, and the chamber pressure was brought to less than 10 mTorr using a scroll pump. The Cu foil was then heated to $900\text{ }^\circ\text{C}$ in Ar (190 sccm) and H_2 (10 sccm) atmosphere in 2 min. Cu foil was kept under the same conditions for another

2 min. The temperature was then increased to 950 °C in 60 s. Then the chamber pressure was increased to 10 Torr using an Ar (80 sccm) and H₂ (20 sccm) mixture. At these conditions, Cu foil was annealed for 10 min at 950 °C. Graphene growth was carried out at 950 °C for 30 min using 5 sccm of CH₄. After growth, the chamber was cooled to room temperature in 90 min under Ar atmosphere.

To transfer graphene, PMMA or PS solution was spin-coated on the graphene/Cu stack. The graphene layer on the backside of the foil was removed by oxygen plasma etching. Ammonium persulfate (20–50 mg/mL in water), iron(III) chloride (80–120 mg/mL in water), and a 2:1:1 solution of H₂O/H₂SO₄/H₂O₂ were used to wet etch copper. The polymer/graphene stack was moved to distilled water several times to rinse the etchant residue. Electrochemical delamination was performed using NaOH or KCl as the electrolyte. The detached polymer/graphene stack was subsequently transferred to the target substrate and immersed in an acetone bath to remove polymer support, and finally, the wafer with graphene was rinsed in IPA.

For a reference, we also measured CVD graphene grown and transferred by graphene material manufacturers and suppliers. These layers showed good crystalline quality and a comparable level of metallic impurities as reported here.

Characterization. Raman spectra were acquired with a Renishaw InVia micro-Raman spectrometer equipped with a 514 nm (2.41 eV) wavelength excitation laser, an 1800 lines/mm grating, and 50× objective. High-resolution Raman mapping was performed with a 500 nm step size using a 100× objective. Large-area Raman mapping was performed with a 633 nm laser, an 1800 lines/mm grating, and a 50× objective.

ToF-SIMS measurements were conducted with a ToF-SIMS 5 instrument (ION-TOF, Münster, Germany) using 25 kV bismuth primary ions. The ToF-SIMS elemental mappings were acquired by operating the instrument in “burst alignment” (BA) and “high current bunched” (HCBU) mode. During the operation, the primary ion gun typically scans a field of view of 500 × 500 μm², applying a 1024 × 1024 pixel measurement raster. The BA mode offers a better lateral resolution on the cost of mass resolution. In order to exclude any mass interference, the HCBU was used. The charging effects due to the SiO₂ substrate were compensated by using an electron flood gun with an energy of 20 eV. The ToF-SIMS depth profiling was acquired in dual-beam mode by scanning the bismuth beam over an area of 500 × 500 μm², applying a 128 × 128 pixel measurement raster. An oxygen ion beam with an energy of 500 eV was used for material abrasion. This beam scanned an area of 700 × 700 μm². These parameters were chosen for best depth resolution. Since the results of such sputtering measurements provide spatially averaged information, only areas with homogeneous Cu coverage in the scanned area (excluding Cu accumulations and “pockets”) were selected.

To obtain absolute concentration of metallic residuals and to calibrate ToF-SIMS results, additional measurements were performed using TXRF. TXRF measurements were done on a Bruker AXS TREX 630 tool. A W K_α X-ray source operated at 40 kV and 40 mA was used at an incident angle of 0.05°. Analysis was performed on the areas covered by graphene and uncovered Si surface. To localize the graphene covered areas on the 200 mm Si wafer and to guide the TXRF analysis, differential work function imaging³⁵ using a QCept Technologies, Inc. ChemetriQ 5000 was applied (see Supporting Information, Figure S3).

XPS measurements were performed with a PHI VersaProbe II scanning XPS microprobe photoelectron spectrometer. Long integration times were applied to detect very low intensity metal peaks (if any).

Minority charge carrier diffusion length has been measured using a Semiconductor Diagnostics, Inc. FAaST 230 SPV tool.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Optical microscope images and Raman spectroscopy maps on delaminated and wet-etched graphene. Additional ToF-SIMS and XPS measurements. This material is available free of charge via the Internet at <http://pubs.acs.org>.

Acknowledgment. This work was supported by the EU project GRADE 317839, the DFG projects ME 4117/1 and LE 2440/1-1, and the ERC grant INTEGRADE (307311). Partial support by the EU FP7 grant no. 604391 (Graphene Flagship) is acknowledged. We acknowledge D. Kot of IHP for useful discussions and preparation of reference samples.

REFERENCES AND NOTES

- Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S. K.; Colombo, L. Electronics Based on Two-Dimensional Materials. *Nat. Nanotechnol.* **2014**, *9*, 768–779.
- Koppens, F. H. L.; Mueller, T.; Avouris, Ph.; Ferrari, A. C.; Vitiello, M. S.; Polini, M. Photodetectors Based on Graphene, Other Two-Dimensional Materials and Hybrid Systems. *Nat. Nanotechnol.* **2014**, *9*, 780–793.
- Han, S. J.; Valdes Garcia, A.; Oida, S.; Jenkins, K. A.; Haensch, W. Graphene Radio Frequency Receiver Integrated Circuit. *Nat. Commun.* **2014**, *5*, 3086–1–3086–6.
- Kim, K.; Choi, J.-Y.; Kim, T.; Cho, S.-H.; Chung, H.-J. A Role of Graphene in Silicon-Based Semiconductor Devices. *Nature* **2011**, *479*, 338–344.
- Bonaccorso, F.; Sun, Z.; Hasan, T.; Ferrari, A. Graphene Photonics and Optoelectronics. *Nat. Photonics* **2010**, *4*, 611–622.
- Mehr, W.; Dabrowski, J.; Scheytt, C.; Lippert, G.; Xie, Y.; Lemme, M.; Ostling, M.; Lupina, G. Vertical Graphene Base Transistor. *Electron Device Lett.* **2012**, *33*, 691–693.
- Vaziri, S.; Lupina, G.; Henkel, Ch.; Smith, A.; Lippert, G.; Mehr, W.; Lemme, M. A Graphene-Based Hot Electron Transistor. *Nano Lett.* **2013**, *13*, 1435–1439.
- Ferrari, A. C.; Bonaccorso, F.; Falko, V.; Novoselov, K. S.; Roche, S.; Boggild, P.; Borini, S.; Koppens, F.; Palermo, V.; Pugno, N.; et al. Science and Technology Roadmap for Graphene, Related Two-Dimensional Materials and Hybrid Systems. *Nanoscale* **2015**, *7*, 4598–4810.
- Hattori, T., Ed. *Ultraclean Surface Processing of Si Wafers*; Springer Verlag: Berlin, 1998.
- Vermeire, B.; Lee, L.; Parks, H. G. The Effect of Copper Contamination on Field Overlap Edges and Perimeter Junction Leakage Current. *IEEE Trans. Semicond. Manuf.* **1998**, *11*, 232–238.
- Hong, J.; Lee, S.; Lee, S.; Han, H.; Mahata, Ch.; Yeon, H.-W.; Koo, B.; Kim, S.-I.; Nam, T.; Byun, K.; et al. Graphene as an Atomically Thin Barrier to Cu Diffusion into Si. *Nanoscale* **2014**, *6*, 7503–7511.
- He, M.; Novak, S.; Vanamurthy, L.; Bakhru, H.; Plawsky, J.; Lu, T.-M. Cu Penetration into Low-k Dielectric during Deposition and Bias-Temperature Stress. *Appl. Phys. Lett.* **2010**, *97*, 252901-1–252901-3.
- He, M.; Lu, T.-M. *Metal–Dielectric Interfaces in Gigascale Electronics: Thermal and Electrical Stability*, Springer Series in Materials Science 157; Springer Science+Business Media LLC: New York, 2012.
- Ambrosi, A.; Pumera, M. The CVD Graphene Transfer Procedure Introduces Metallic Impurities Which Alter the Graphene Electrochemical Properties. *Nanoscale* **2014**, *6*, 472–476.
- Ambrosi, A.; Chua, C. K.; Khezri, B.; Sofer, Z.; Webster, R. D.; Pumera, M. Chemically Reduced Graphene Contains Inherent Metallic Impurities Present in Parent Natural and Synthetic Graphite. *Proc. Natl. Acad. Sci. U.S.A.* **2012**, *109*, 12899–12904.
- Pumera, M.; Ambrosi, A.; Chng, E. L. K. Impurities in Graphenes and Carbon Nanotubes and Their Influence on the Redox Properties. *Chem. Sci.* **2012**, *3*, 3347–3355.
- Wong, C. H. A.; Sofer, Z.; Kubesova, M.; Kucera, J.; Matejkova, S.; Pumera, M. Synthetic Routes Contaminate Graphene Materials with Whole Spectrum of Unanticipated Metallic Elements. *Proc. Natl. Acad. Sci. U.S.A.* **2014**, *111*, 13774–13779.
- Aleman, B.; Regan, W.; Aloni, S.; Altoe, V.; Alem, N.; Girit, C.; Geng, B.; Maserati, L.; Crommie, M.; Wang, F.; et al. Transfer-Free Batch Fabrication of Large-Area Suspended Graphene Membranes. *ACS Nano* **2010**, *4*, 4762–4768.

19. Liang, X.; Sperling, B. A.; Calizo, I.; Cheng, G.; Hacker, C. A.; Zhang, Q.; Obeng, Y.; Yan, K.; Peng, H.; Li, Q.; et al. Toward Clean and Crackless Transfer of Graphene. *ACS Nano* **2011**, *5*, 9144–9153.
20. Kern, W.; Puotinen, D. A. Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology. *RCA Rev.* **1970**, *31*, 187–206.
21. Shard, A. G. Detection Limits in XPS for More Than 6000 Binary Systems Using Al and Mg K α X-rays. *Surf. Interface Anal.* **2014**, *46*, 175–185.
22. Colombo, L.; Wallace, R. M.; Ruoff, R. S. Graphene Growth and Device Integration. *Proc. IEEE* **2013**, *101*, 1536–1556.
23. Wang, Y.; Zheng, Y.; Xu, X.; Dubuisson, E.; Bao, Q.; Lu, J.; Loh, K. P. Electrochemical Delamination of CVD Grown Graphene Film: Toward the Recyclable Use of Copper Catalyst. *ACS Nano* **2011**, *5*, 9927–9933.
24. Suk, J. W.; Kitt, A.; Magnuson, C. W.; Hao, Y.; Ahmed, S.; An, J.; Swan, A. K.; Goldberg, B. B.; Ruoff, R. S. Transfer of CVD-Grown Monolayer Graphene onto Arbitrary Substrates. *ACS Nano* **2011**, *5*, 6916–6924.
25. Ryu, J.; Kim, Y.; Won, D.; Kim, N.; Park, J. S.; Lee, E.-K.; Cho, D.; Cho, S.-P.; Kim, S. J.; Ryu, G. H.; et al. Fast Synthesis of High-Performance Graphene Films by Hydrogen-Free Rapid Thermal Chemical Vapor Deposition. *ACS Nano* **2014**, *8*, 950–956.
26. Li, X.; Cai, W.; An, J.; Kim, S.; Nah, J.; Yang, D.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; et al. Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils. *Science* **2009**, *324*, 1312–1314.
27. Mattevi, C.; Kim, H.; Chhowalla, M. A Review of Chemical Vapour Deposition of Graphene on Copper. *J. Mater. Chem.* **2011**, *21*, 3324–3334.
28. Hozawa, K.; Yugami, J. Copper Diffusion Behavior in SiO₂/Si Structure during 400°C Annealing. *Jpn. J. Appl. Phys.* **2004**, *43*, 1.
29. Istratov, A. A.; Weber, E. R. Physics of Copper in Silicon. *J. Electrochem. Soc.* **2002**, *149*, G21–G30.
30. Henley, W. B.; Ramappa, D. A.; Jastrzebski, L. Detection of Copper Contamination in Silicon by Surface Photovoltaic Diffusion Length Measurements. *Appl. Phys. Lett.* **1999**, *74*, 278–280.
31. Zoth, G.; Bergholz, W. A Fast, Preparation-Free Method To Detect Iron in Silicon. *J. Appl. Phys.* **1990**, *67*, 6764–6771.
32. Wie, D.; Peng, L.; Li, M.; Mao, H.; Niu, T.; Han, C.; Chen, W.; Wee, A. T. S. Low Temperature Critical Growth of High Quality Nitrogen Doped Graphene on Dielectrics by Plasma-Enhanced Chemical Vapor Deposition. *ACS Nano* **2015**, *9*, 164–171.
33. Lippert, G.; Dabrowski, J.; Schroeder, T.; Yamamoto, Y.; Herziger, F.; Maultzsch, J.; Baringhaus, J.; Tegenkamp, Ch.; Carmen Asensio, M.; Avila, J.; et al. Graphene Grown on Ge(001) from Atomic Source. *Carbon* **2014**, *75*, 104–112.
34. Lee, J.-H.; Lee, E. K.; Joo, W.-J.; Jang, Y.; Kim, B.-S.; Lim, J. Y.; Choi, S.-H.; Ahn, S. J.; Ahn, J. R.; Park, M.-H.; et al. Wafer-Scale Growth of Single-Crystal Monolayer Graphene on Reusable Hydrogen-Terminated Germanium. *Science* **2014**, *344*, 286–289.
35. Park, J.; Cho, S.; Hawthorne, J. Electrochemical Induced Pitting Defects at Gate Oxide Patterning. *IEEE Trans. Semicond. Manuf.* **2013**, *26*, 315–318.