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Nonvolatile Memory Cells Based on MoS_2/Graphene Heterostructures

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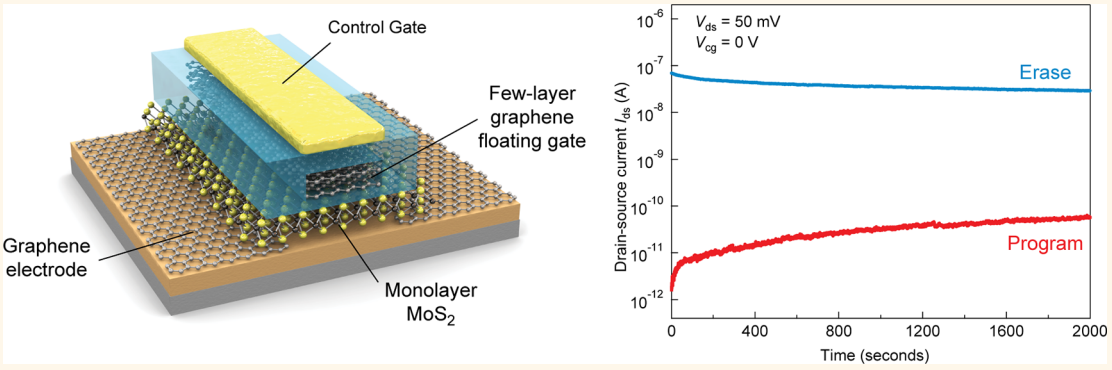
ABSTRACT



Memory cells are an important building block of digital electronics. We combine here the unique electronic properties of semiconducting monolayer MoS_2 with the high conductivity of graphene to build a 2D heterostructure capable of information storage. MoS_2 acts as a channel in an intimate contact with graphene electrodes in a field-effect transistor geometry. Our prototypical all-2D transistor is further integrated with a multilayer graphene charge trapping layer into a device that can be operated as a nonvolatile memory cell. Because of its band gap and 2D nature, monolayer MoS_2 is highly sensitive to the presence of charges in the charge trapping layer, resulting in a factor of 10^4 difference between memory program and erase states. The two-dimensional nature of both the contact and the channel can be harnessed for the fabrication of flexible nanoelectronic devices with large-scale integration.

KEYWORDS: two-dimensional materials · dichalcogenides · MoS_2 · graphene · nanoelectronics · memory · heterostructures

Two-dimensional materials, such as graphene and single layers of boron nitride (BN) or molybdenum disulfide (MoS_2), are the thinnest known materials with electronic properties that can be advantageous for a wide range of applications in nanotechnology.[1−6] Being only one layer thick, they represent the ultimate limit of scaling in the vertical direction and could offer reduced power dissipation because of smaller short channel effects.[7] They can also be regarded as a complete material library containing all the components necessary for building electronic circuits in which insulating BN could act as the substrate and gate dielectric barrier,[6] graphene as an interconnect while MoS_2 or another 2D semiconductor could play the role of a semiconducting channel.[4] Because graphene is semimetallic, it could form the ideal contact to 2D semiconductors, capable of supporting large current densities,[8] exceeding 10^9 A/cm^2 (ref 9). Furthermore, the lack of dangling bonds at the interface between graphene and 2D semiconductors would suppress the appearance of interface states and charge traps. As the graphene's work function can be electrostatically or chemically tuned,[10] it could also be adapted to a wide variety of 2D semiconductors with different work functions and band gaps. In this work, we demonstrate the integration of a 2D semiconductor in the form of monolayer MoS_2 with graphene electrodes. The basic device functions as a field-effect transistor, with ohmic contacts and performance comparable to similar devices with metal contacts.[4] Furthermore, this device can serve as a prototype for more advanced devices based on a 2D architecture. We demonstrate this by adding a charge trapping layer in the form of a multilayer graphene floating gate, resulting in a new heterostructure capable of operating as a nonvolatile memory cell.

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The use of 2D materials could offer immediate practical advantages for the realization of memory devices based on the floating gate transistor structure.[11] In current flash memory technology, serious hurdles need to be overcome to advance device miniaturization, both in the lateral and vertical directions. Vertical scaling leads to reduction of the program/erase voltages but is limited by the requirement of charge retention on the floating gate, which sets the limit for a minimum tunneling oxide thickness (~5 nm). On the other hand, lateral scaling, driven by the quest for higher data storage capability, is seriously limited by the capacitive coupling between the drain electrode and the floating gate, which results in a longer penetration of the drain field in the transistor channel[12] as the device is scaled. Furthermore, interference between neighboring cells leads to an undesirable spread in the threshold voltages of the devices.[13] The effect of capacitive interference can be significantly diminished through the reduction of the floating gate thickness,[14] while the reduction of electrode thickness can diminish the coupling between the electrodes and the floating gate. Because of this, it is extremely interesting to investigate the suitability of 2D materials for use in memory devices where they could replace traditional choices for semiconducting channels, interconnects, and charge trapping layers.

RESULTS AND DISCUSSION

Figure 1 shows the structure of our memory device, composed of two transistors fabricated on the same monolayer MoS_2 flake placed over graphene stripes acting as source and drain electrodes. A piece of multilayer graphene (MLG), 4−5 layers thick, separated by a 6 nm thick tunneling oxide layer (HfO_2) from the monolayer MoS_2 channel acts as the floating gate. We chose multilayer graphene as the floating gate because of its work function (4.6 eV) which is not sensitive to the number of layers and results in a deep potential well for charge trapping and improved charge retention. Furthermore, the low conductivity along the vertical *c*-axis suppresses detrimental ballistic currents across the floating gate,[15] while a higher density of states (>4.4 × 10^{13} cm^{-2} eV^{-1}) with respect to its single-layer counterpart (8 × 10^{12} cm^{-2} eV^{-1})[16] would allow more charge to be stored on it resulting in a larger memory window. The floating gate is further capped by a 30 nm thick blocking oxide layer at the top. The conductivity of the MoS_2 channel depends on the amount of charge stored in the floating gate (FG) and is modulated by the voltage V_{cg} applied to the control gate electrode (CG), which can also be used to vary the amount of charge stored on the floating gate.

The fabrication process includes three transfer steps.[17] Figure 1C shows the appearance of the device at several stages of the fabrication procedure. We start by growing graphene using chemical vapor deposition (CVD)[18] and transferring it onto a silicon substrate with

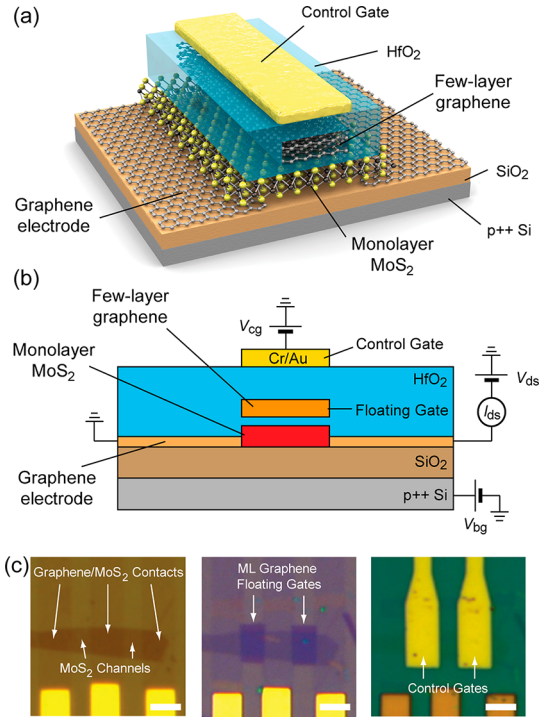

Figure 1. MoS_2/graphene heterostructure memory layout. (a) Three-dimensional schematic view of the memory device based on single-layer MoS_2. (b) Schematics of a heterostructure memory cell with a single-layer MoS_2 semiconducting channel, graphene contacts and multilayer graphene (MLG) floating gate. The MLG floating gate is separated from the channel by a thin tunneling oxide (*ca.* 1 nm Al_2O_3 + 6 nm HfO_2) and from the control gate by a thicker blocking oxide (1 nm Al_2O_3 + 30 nm HfO_2). (c) Optical micrographs of two graphene/MoS_2 heterostructure transistors fabricated on the same MoS_2 monolayer flake at various stages of fabrication. Left: single-layer MoS_2 transferred over an array of graphene stripes patterned on oxidized silicon chips and contacted with metal leads (Cr/Au: 10/50 nm); middle: the same device after deposition of the tunneling oxide and transfer/patterning of MLG floating gates; right: final device after the deposition of the blocking oxide and definition of the control gate electrodes (Cr/Au: 10/50 nm). Scale bars: 3 μm.

a 270 nm thick thermally grown silicon-dioxide (SiO_2) layer. Graphene is patterned into stripes and contacted with metal leads. MoS_2 is then exfoliated on another SiO_2/Si substrate covered with a sacrificial polymer layer. Individual layers are detected using optical microscopy[19] and transferred[20] on top of the graphene stripes that form the source and drain electrodes in direct contact with monolayer MoS_2. Fabrication continues with the deposition of the tunneling oxide layer on top of the MoS_2/graphene heterostructure, in the form of a 6 nm thick HfO_2 film grown using atomic layer deposition (ALD). We use a thermally oxidized Al seed layer[21] to facilitate the ALD deposition over graphene and MoS_2. Multilayer graphene flakes 1.5 nm thick are transferred onto the tunneling oxide and positioned above the MoS_2 flakes. Finally, the floating gate is capped by a 30 nm thick HfO_2 layer followed by the deposition of the control gate.

Figure 2a shows the small-bias current *versus* bias voltage (I_{ds} − V_{ds}) characteristic of one of our floating

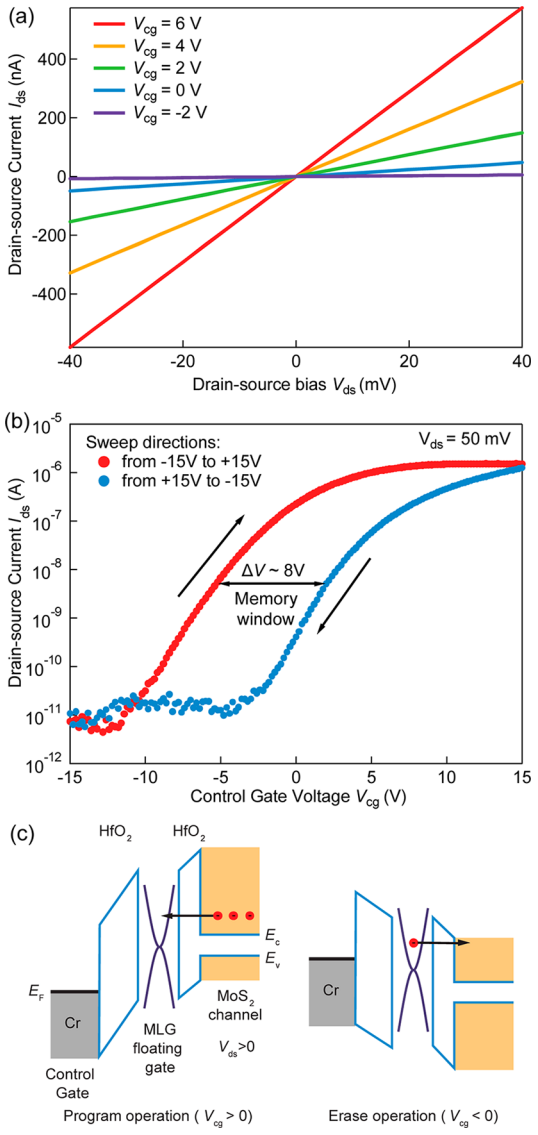

Figure 2. Device characteristics and charge trapping in the device. (a) Output characteristics (drain-source current I_{ds} *vs* drain-source voltage V_{ds}) of the floating gate transistor in the ON state, for different control gate biases V_{cg}. The curve linearity at small V_{ds} indicates that graphene acts as a ohmic contact to monolayer MoS_2. (b) Transfer characteristic (drain-source current I_{ds} *vs* control-gate voltage V_{cg}) of the floating gate transistor, acquired along two different control-gate voltage sweep directions. The large hysteresis of ~8 V is related to accumulation of charge in the MLG floating gate. The voltage sweep rate was 1.4 V/s. (c) Simplified band diagram of the memory device in program and erase states. Application of a positive control gate voltage V_{cg} programs the device. Electrons tunnel from the MoS_2 channel through the 6 nm thick HfO_2 and accumulate on the multilayer graphene floating gate. Application of a negative control gate voltage V_{cg} depletes the floating gate and resets the device.

gate transistors acquired for different values of the control gate voltage V_{cg}. The symmetry of the curves with respect to the origin and their linear behavior indicates the formation of ohmic contacts between graphene and monolayer MoS_2. This is due to a tunable and favorable graphene work function.[10] The relatively large current, on the order of 500 nA for a 40 mV bias, corresponding to a total series resistance of 125 kOhm shows that efficient charge injection from graphene to MoS_2 is possible even though the distance between the two is close to the interlayer distance in graphite (3.4 Å). This is in agreement with density functional theory-based calculations of the electronic structure of graphene/MoS_2 hybrids showing that charge transfer between graphene and MoS_2 is possible in spite of a lack of interaction and the relatively large interlayer separation.[22]

As this device is in two-contact configuration, we can only estimate the upper limit for the contact resistance from the highest recorded channel current during the gate voltage sweep shown on Figure 2a. From I_{ds} = 1.5 μA, a bias voltage V_{ds} = 50 mV, and channel width of 3 μm, we estimate the upper limit for the contact resistance of 50 k$\Omega\cdot\mu$m. Future four-contact and transfer-length measurements will result in a more accurate measurement of contact resistance in this material combination. This value could be further reduced by chemical doping, local electrostatic control or the use of flat substrates. The use of graphene as a contact material for 2D semiconductors in place of thicker metallic films is expected to be advantageous as it allows fabricating devices and circuits[23] in a truly 2D architecture, using for example roll-to-roll printing and with reduced parasitic interference between neighboring devices and increased resistance to short-channel effects.[7] Work-function tunability[10] of graphene will allow it to be adapted to a wide variety of 2D materials. Furthermore, because it is chemically inert and mechanically flexible, graphene is the ideal noninvasive contact to other 2D materials.

The information storage capability of our device can be deduced from the transfer characteristics (drain current I_{ds} *versus* control-gate voltage V_{cg}), shown in Figure 2b, acquired in two sweeping directions, from negative to positive voltages (blue) and in the opposite sweep direction (red). The large hysteresis, characterized by a maximum voltage shift ΔV of approximately 8 V, is related to the charging/discharging of the floating gate in response to the control gate voltage. As the control gate voltage is swept toward high positive values (red curve), Fowler-Nordheim electron tunneling occurs from the channel into the floating gate through the HfO_2 oxide barrier, Figure 2c.[24] At this stage, electrons are accumulated in the floating gate and the device is in the program state. Accumulation of electrons in the floating gate results in a positive shift of the threshold voltage. This is observable from the blue curve, where the control gate voltage is swept in the opposite direction. As the control gate voltage V_{cg} reaches negative values, electrons are transferred back from the floating gate to the channel. For sufficiently high fields the floating gate is fully discharged, resulting in the erase state. For the purpose of reading the

memory state, zero voltage should be applied to the control gate (V_{cg} = 0). This would result in high drain current in the erase state and low drain current current in the program state.

Other hysteresis mechanisms[25] could be present in the device, but they can be ruled out as potential sources of such a high memory effect. Trapping states related to charge impurities present at the semiconductor/dielectric interface cannot generate a permanent threshold voltage shift. As shown in Figure 3a, we can generate permanent current/threshold voltage states characterized by varying memory windows ΔV by modulating the amount of charge stored in the floating gate. To calculate the threshold voltage shift, we define a reference erase state by assuming that the floating gate is not likely to accumulate positive charge (see Supporting Information). The floating gate can be depleted of all residual charge by sweeping the control gate voltage from 0 V to a low negative voltage, denoted as $V_{cg,min}$ (<−5 V). This places the device in the erase state. Immediately after floating gate depletion, we sweep the control gate voltage in the negative-to-positive direction, starting from $V_{cg,min}$ = −18 V, resulting in the black dashed line in Figure 3a, characterized by a threshold voltage $V_{th} \approx 0$ V. Repeating this voltage sweep results in a set of curves with no observable dependence of the V_{th} on the different values tested for $V_{cg,min}$.[17] This indicates that the multilayer graphene floating gate is not likely to accumulate positive charge (holes) in response to a negative voltage applied to the control gate. Hence, a reference *E* state with $V_{th} \approx 0$ V could be defined, corresponding to approximately zero charge stored in the FG. We can now reach different program (*P*) states by performing successive V_{cg} sweeps, stopping at gradually increasing maximum values of $V_{cg,max}$. Figure 3a shows a family of curves acquired in this way, corresponding to different program states characterized by their own memory windows. The threshold voltage shift ΔV (memory window), measured from the reference *E* state, is strongly dependent on the maximum control gate voltage, as can be inferred from the inset graph in Figure 3a. A maximum control gate voltage of +18 V results in a memory window exceeding 8 V. Gate leakage during these measurements is less than 10 pA and is within the noise limits of our instrument (see Supporting Information).

We estimate the amount of charge stored on the floating gate from the expression $n = (\Delta V \times C_{FG-CG})/q$, based on the charge balance equation,[26] where q is the electron charge, ΔV is the difference in the threshold voltage for read and erase states, while the C_{FG-CG} is the capacitance between the floating gate and the control gate, modeled as $C_{FG-CG} = \varepsilon_0\varepsilon_{bl}/d_{bl}$, with ε_0 the vacuum permittivity, ε_{bl} the relative dielectric constant of the HfO_2 blocking layer (~19), and d_{bl} its thickness (~30 nm). This results in a density of stored electrons

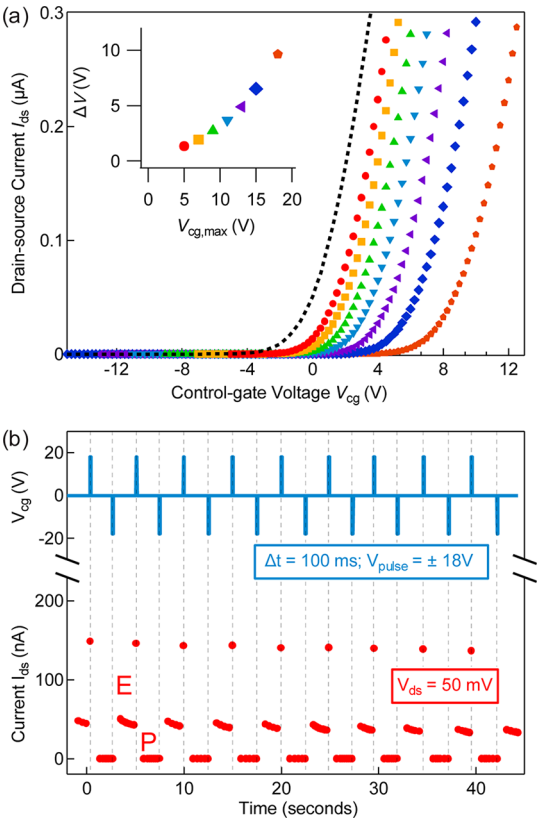

Figure 3. Memory states. (a) Dependence of the memory window on the control-gate voltage. Symbols: transfer characteristics (drain-source current I_{ds} *vs* control-gate voltage V_{cg}) of the floating gate transistor acquired from positive to negative control gate voltages V_{cg}, for different $V_{cg,max}$ (plotted in the inset). The drain-source voltage V_{ds} is fixed to 50 mV. Dashed line: transfer curve of the device in the erase state, corresponding to no charge stored on the floating gate. The inset graph shows the dependence of the memory window, related to charging of the floating gate, on the maximum voltage applied to the control gate. (b) Switching between erase (*E*, high current, device ON) and program (*P*, low current, device OFF) states induced by the application of alternating V_{cg} pulses (±18 V for 100 ms) with a time interval of 2.3 s. The application of a positive V_{cg} pulse (*E* → *P*) induces a drain-source current I_{ds} peak (130−150 nA) due to the increase of the charge density in the MoS_2 channel during the pulse.

on the order of ~2.8×10^{13} cm^{-2}. In agreement with Mishra *et al.*[14] and Hong *et al.*[27] we conclude that MLG, due to its higher density of states than in graphene, allows a larger memory window with strong potential for multilevel data storage.

We now test the dynamic behavior of our device, reported in Figure 3b. Switching between program and erase states is achieved through the application of voltage pulses to the control gate electrode, with the source grounded and the drain biased at 50 mV. The device is initially in the *E* state, corresponding to the ON current level. A positive voltage pulse (+18 V) with the duration of 100 ms leads to both accumulation of charge in the transistor channel, indicated by the ~150 nA current spike and to tunneling of electrons into the floating gate. When the control gate voltage is

reset to 0 V, the device remains in its program state, holding a stable OFF current. The application of a symmetric negative pulse (−18 V, 100 ms duration) 2.3 s later restores the initial erase state. We performed an endurance test measurement for our memory device, observing a well-defined and reproducible *P/E* switching for over 120 cycles. The slow decay of the ON current is presumably due to trapping mechanisms related to charge impurities present at the semiconductor/dielectric interface, as observed elsewhere.[25]

The stability of *E* and *P* states, crucial for nonvolatile information storage, was further investigated by monitoring their time-resolved behavior at a constant drain-source bias of 50 mV, reported in Figure 4. During the entire observation time, the corresponding erase state current was measured to be in the range 10^{-8}–10^{-7} A, with an exponential decay saturating to about 20 nA. After this measurement, the memory was programmed to the program state through a voltage pulse (V_{cg} = +18 V, duration 3 s), resulting in the OFF state of the drain current I_{ds}. Although slowly increasing with time, the I_{ds} current remained in the 10^{-12}–10^{-10} A range during at least 2000 s. Room for improvement can be identified in both lowering the density of charge impurities in and around the channel in order to stabilize the erase-state current and in improved engineering of the tunneling oxide layer to increase the retention performance.

For the program and erase states we measured a maximal program/erase (*P/E*) current ratio exceeding 10^4. Such a remarkable *P/E* current ratio not only allows easy readout of the device state, but also allows multilevel storage, where more than one bit of information could be stored in the memory cell in the form of several distinct floating-gate charge levels.

As the final step of our device characterization procedure, we studied the memory charge retention characteristics (Figure 4b), which are related to both the nature of the tunneling barrier and to the work function of the MLG. The latter determines the depth of the potential well for the electrons stored in the floating gate. After programming the memory through a positive pulse (V_{cg} = +18 V during 3 s), we measured the threshold voltage at different time intervals, determined using a linear fit of the transfer characteristics, as shown in the inset of Figure 4b. These curves were acquired in a narrow range of control voltage V_{cg}, from 0 to +12 V, in order to prevent undesired electron depletion/injection occurring at the floating gate. Successive voltage sweeps carried out immediately one after the other resulted in similar V_{th} values, confirming the fact that the measurement itself was not perturbing the system. We observe a threshold voltage variation from 7.5 to 5 V during a time period of 10^4 seconds. Assuming that the reference erase state is characterized by $V_{th} \approx 0$ V, we estimate that, after 10 years, 30% of the initial charge would still be stored on the floating gate. This result proves that the charge leakage from

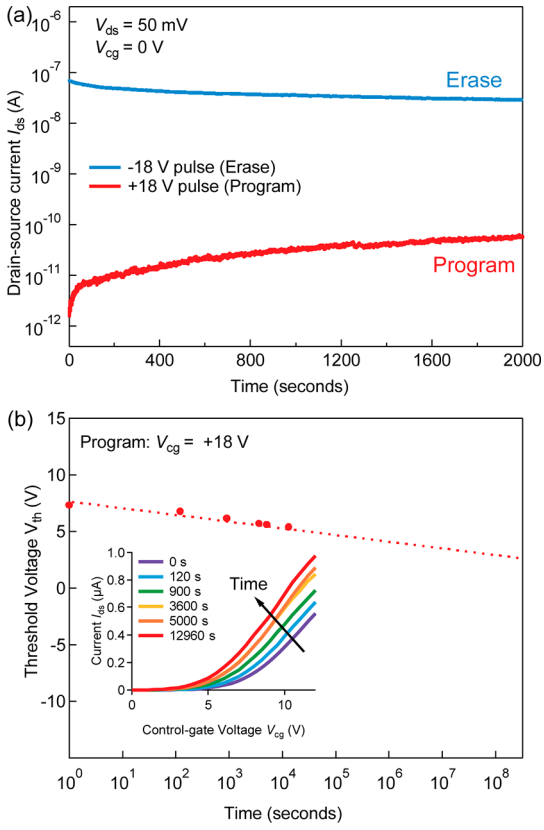

Figure 4. Device dynamics and charge retention. (a) Temporal evolution of drain-source currents (I_{ds}) in the erase (ON) and program (OFF) states. The curves are acquired independently for the program (10^{-8}–10^{-7} A) and erase (10^{-12}–10^{-10} A) current states and plotted on a common time scale. The drain-source bias voltage is 50 mV and the duration of the control-gate voltage (V_{cg}) pulse is 3 s. (b) Time-resolved behavior of the device threshold voltage after application of the programming voltage pulse (+18 V for 3 s). Threshold voltage was determined from linear fits to transfer curves (inset) in the linear regime. We estimate that after 10 years the device retains 30% of the charge stored on the floating gate.

the floating gate is slow on the time-scale of years and that the combination MoS_2/MLG indeed has a potential for application in nonvolatile memory technology. The value extracted for charge retention appears encouraging, considering that this is the first prototype of its kind. Further improvement can be achieved by means of a thorough engineering of the blocking oxide layer, using for instance novel insulating 2D crystals, such as BN or 2D oxides.[28]

CONCLUSION

We have demonstrated a new type of heterostructures based on 2D materials in which we use graphene as an ohmic contact to monolayer MoS_2 in a field-effect transistor geometry, paving the way toward the realization of truly 2D device architectures. The final device includes a multilayer graphene floating gate and operates as a nonvolatile memory cell. This demonstrates that it is possible to design memory devices using 2D building blocks, including contacts, floating gate, and

the semiconducting channel. Moreover, the excellent mechanical properties of 2D semiconductors such as MoS_2 (ref 29) can be exploited for fabrication of transistor circuits and memory devices on flexible substrates, with a naturally emerging range of related applications. Such devices could be produced massively and inexpensively using liquid-scale processing[30] or roll-to-roll printing[31] of CVD-grown material.[32,33]

METHODS

Single layers of MoS_2 are exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide) using the scotch-tape micromechanical cleavage technique method pioneered for the production of graphene.[1] AFM imaging was performed using the Asylum Research Cypher AFM. Electrical characterization of the memory device was performed in ambient conditions at room temperature using an Agilent E5270B parameter analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Detailed description of the device fabrication procedure and additional characterization of the device. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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