electronic circuit and packaging designers. The palladium-silver end-cap terminals normally supplied were, in fact, advertised as being solderable with minimum leaching of silver into the solder.

Upon a detailed investigation of a capacitor failure it was discovered that a crack had occurred under the end termination of a capacitor and, furthermore, that this crack could not be detected from the outside. Indeed, very careful cross sectioning was required, followed by equally careful microscopic examination. Further investigation led to the conclusion that the crack thus discovered was not an isolated instance of this phenomenon.

This paper, and the experimental data it reports, will show that capacitor attachment to alumina substrates using solder causes the capacitors to crack, but that these cracks rarely result in complete electrical failure of the capacitor. The paper will also show that preheating the substrate to a specific temperature during the soldering operation will minimize the cracking phenomenon. While some inferences may be drawn as to the mechanism causing the cracking, the elucidation of this mechanism was not the purpose of the study to be reported here. The elimination of cracking by using conductive epoxy for attaching ceramic-chip capacitors to alumina substrates will be shown.

Bulk lifetime determination of MOS structures by a voltage step response method. C. TRULLEMANS and F. VAN DE WIELE. *Solid-St. Electron.* **21,** 561 (1978). The time dependance of the current flowing through a MOS capacitor switched from an inversion state to a deeper inversion state is described by a simple model. A method is derived for determining the bulk lifetime from dynamic current measurements alone.

Threshold voltage instability of MOS field effect transistors. SESHA R. SHANKAR, RAJ P. MISRA and HENRY T. RAND. *Microelectron. Reliab.* **17,** 305 (1978). This paper presents the results of accelerated life tests performed on *p*-channel enhancement mode MOSFETs, the test conditions being storage at 140°C, with and without gate bias. It is observed that with positive gate bias, $|V_T|$ drifts upwards, and with negative gate bias also, the $|V_T|$ drift is upwards at least after a hundred hours. In the latter case, the augmentation of positive ion density in the oxide regions near the oxide–semiconductor interface is postulated, and the results presented are explained in terms of this postulation.

Adaption aux ensembles des condensateurs a dielectrique polypropylene metallise. C. FEY. *Revue Technique Thomson-CSF* **10,** (1) 147 (March 1978). (In French.) It is possible to predict, with a good measure of agreement with experiment, the temperature rise in metallized polypropylene film capacitors, notably in respect of heat exchanges with the exterior. The theoretical calculations are usually simple and can be computer-assisted if necessary and will allow evaluating the effects of different dimensional parameters.

CMOS reliability. L. J. GALLACE, H. L. PUJOL and G. L. SCHNABLE. *Microelectron. Reliab.* **17,** 287 (1978). Complementary metal-oxide–silicon (CMOS) integrated circuits have had a major impact on the electronics industry, and have created new areas of application for digital circuits. CMOS digital circuits, because of a number of very significant circuit advantages, including low power dissipation, high noise immunity and wide operating-voltage range, have become a very widely used logic family.

The RCA series of CMOS devices, first introduced as the COS/MOS CD4000 series in 1968, has gained wide acceptance. The introduction, in 1971, of plastic-encapsulated CMOS integrated circuits was instrumental in achieving even wider acceptance of the popular CD4000-series devices.

The COS/MOS product line today includes more than 100 standard parts in the CD4000A series, parts that are used worldwide in applications ranging from such special uses as battery-operated watch circuits to many functions in the aerospace, computer, automotive and consumer industries. In addition, a new product line has been introduced, the CD4000B series, which has improved features such as a higher operating-voltage range (3–20 V), standardized output drive, symmetrical transition time and improved electrostatic-discharge (ESD) protection networks.

This report, which presents new data on the reliability of CMOS integrated circuits, is divided into four major sections: the first section is a review of background information on MOS integrated-circuit reliability, the second section presents new experimental results of comprehensive studies of the reliability of RCA CMOS (or COS/MOS) integrated circuits, the third section is a discussion of application considerations and outlines RCA electrical specifications for COS/MOS integrated circuits and the fourth section is a review of the effects of some of the trends occurring in the CMOS industry. Some generalizations and conclusions concerning CMOS reliability are included in the fourth section.

Developments likely to improve the reliability of plastic encapsulated devices. R. O. JONES. *Microelectron. Reliab.* **17,** 273 (1978). The development of plastic encapsulated silicon devices with their considerable cost reduction over their hermetic counterparts, due to both cheaper components and better suitability to mechanization of assembly processes, has led to other failure mechanisms on reliability testing.

Instead of the silicon die being in contact with a dry gas in a sealed enclosure, the plastic material is in intimate contact with the die and further the plastic is not an hermetic seal. This leads to additional mechanical stresses in the structure, degradation of the die surface parameters due to the relatively impure environment and extra hazards due to ingress of the outside atmosphere onto the silicon die.

We will attempt to discuss some of the important failure mechanisms in plastic encapsulated devices as observed on endurance testing and how these are modified by changes in plastic material, die passivation and the metal contacts between the die and grid frame. All the effects are wearout mechanisms and will be given as time for a given percentage failure rather than as percentage per 1000 hr.

3. CIRCUIT AND SYSTEMS RELIABILITY, MAINTENANCE AND REDUNDANCY

Screening methods and experience with MOS memory. R. V. PAPPU, E. HARRIS and M. YATES. *Microelectron. Reliab.* **17,** 193 (1978). This paper describes the experience of Bell-Northern Research and Northern Telecom Ltd. with MOS dynamic RAMS in high reliability switching systems. Various failure mechanisms of the MOS memory devices and the screening procedures, implemented in Northern Telecom Ltd. to weed out weak devices, are explained. The resultant device drop-out rates in manufacturing and the effect of this comprehensive pre-conditioning on the field failure rate of MOS memory cards are discussed.

Effects of design automation on the reliability and maintainability design of electronic systems. J. E. ARSENAULT and P. DESMARAIS. *Microelectron. Reliab.* **17,** 143 (1978). The ability to design required reliability and maintainability perform-