A system is described for locating faulty integrated circuits on a printed circuit card under the guidance of computer programmed in accordance with the circuit being tested. The disclosed system includes a current pulsing network allowing digital selection, as by the computer, of reference voltage levels at which current is injected into the circuit being tested.

4837552

NON-VOLATILE FAULT DISPLAY WITH MAGNETIC RESET SWITCH FOR ADAPTIVE BRAKING SYSTEM

Patrick J Vandemotter, Merlyn Hutchins, Jon S Canale, Kenneth R Koyan assigned to Allied-Signal Inc

A fault indicating mechanism for an electronic system, such as a vehicle adaptive braking system, includes a series of visual indicators, such as light emitting diodes, on one surface of the housing within which the electronic components comprising the system are sealed. Each of the indicators is activated in response to a predetermined malfunction sensed in the system, such as a defective speed sensor, defective modulator, or a defect in the electronic circuitry. A magnetically responsive switch is sealed within the housing adjacent the indicators, but is not visible from the exterior of the housing. The indicators are reset when the system is repaired by the mechanic who holds a common magnet against the housing adjacent the switch. When the switch is activated by a magnet, all of the indicators flash on and are then turned off. A nonvolatile RAM stores malfunctions sensed by the system when the system is powered down, so that all malfunctions are again indicated immediately when the system is powered up.

4837764

PROGRAMMABLE APPARATUS AND METHOD FOR TESTING COMPUTER PERIPHERALS

Vincent J Russello assigned to Bunker Ramo Corporation

An apparatus and method for testing the condition of computer peripherals is provided. The apparatus is portable and enclosed in a housing and comprises a microprocessor, first nonvolatile memory means having stored therein an operating system routine, at least one working memory means for storing an instruction set defining a test protocol, at least one peripheral connector means for operatively connecting said apparatus with a peripheral to be tested in accordance with said protocol, at least one data source connector means for operatively connecting an external data source to said apparatus, a keyboard for receiving user commands for controlling the operation of said microprocessor and sending said user commands to said microprocessor, a display, and second nonvolatile memory means having permanently stored therein a debuffer routine for responding to user commands input through the keyboard to instruct the microprocessor to store an instruction set in working memory defined by data input from said external data source and test said peripheral in accordance with the protocol set forth in said instruction set.

4837765

TEST CONTROL CIRCUIT FOR INTEGRATED CIRCUIT

Takamas Suzuki, Tokyo, Japan assigned to NEC Corporation

For shortening the time period needed for test of component function blocks fabricated on a semiconductor chip and detecting a circuit trouble, there is disclosed a test control circuit for an integrated circuit having a plurality of component blocks including at least two component blocks responsive to respective data signals or a common test signal and achieving predetermined functions, respectively, to produce respective output signals based on the respective data signals or the common test signal, the predetermined functions being identical with one another, comprising (a) a control signal generating circuit responsive to a command signal and capable of producing at least two prohibiting signals applied to the at least two component blocks, respectively (b) a mode selecting circuit responsive to a test mode signal and causing the at least two component blocks to respond to the common test signal, and (c) a logic circuit carrying out a logical operation for the output signals supplied from the at least two component blocks and producing an output signal, wherein each of the at least two component blocks suspends the production of the output signal based on the common test signal in the presence of said prohibiting signal, so that the at least two component blocks are examined in the absence of the prohibiting signal and the logic circuit is examined in the presence of the prohibiting signal.

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