Low-Power and Small-Sized Scan Driver Using Amorphous Oxide TFTs

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Abstract

This paper presents a low-power and small-sized scan driver using amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs). Power consumption of the proposed scan driver is reduced by eliminating unnecessary charging current of the scan line and reducing the voltage swing of clock signals. In the proposed scan driver, area of the output stage, which requires large-sized driving TFTs, is also reduced by merging TFTs for charging and discharging the scan line into one TFT and using non-overlapping clock signals. Compared to the previous scan driver, power consumption and area of the output stage of the proposed scan driver is reduced by 21% and 40%, respectively. The proposed scan driver has power consumption of 27.4 μW per stage at the operating frequency of 46 kHz and the area per stage is 1153×192 μm².

1. Introduction

A hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) is widely used for the backplanes of the liquid crystal display (LCD). As flat panel displays (FPDs) with high resolution become larger and use fast driving method for high image quality, the mobility of the a-Si:H TFT is not enough for backplanes in FPDs [1]. Amorphous Indium Gallium Zinc Oxide (a-IGZO) TFT is getting a lot of attention as the best candidate of TFT backplane technologies due to its high mobility and good uniformity of electrical properties compared to the a-Si:H [1-4]. Therefore, the LCD backplane using the a-IGZO TFT can be implemented in large size display and can be driven at high frame rate.

Most of a-IGZO TFTs are n-type devices and have a negative threshold voltage (Vth) [4], and this causes high off-state current. Recently, several papers about integrated scan driver on the backplane using a-IGZO TFTs are reported [5-7]. These papers are using additional signals or compensation circuits to reduce the leakage current. These previous scan drivers, which require additional off-state voltage (VSS), have unnecessary charging and discharging current of the scan line. Figure 1 shows the output signal of the previously reported scan driver [5]. As shown in Figure 1, during the transition of the output signal between 'LOW' and 'HIGH', the output signal is passing through the low state voltage of clock signal (V_L), and this phenomenon requires additional charging and discharging current. These unnecessary charging and discharging current increase the power consumption of the scan driver. In addition, previously reported integrated scan drivers [6, 7] have large size pull-up and pull-down TFTs for the charging and discharging the scan line. Because they have to drive the large scan line loads, these TFTs are designed relatively larger than other TFTs in scan driver and these large TFTs occupy half of the area of the scan driver.

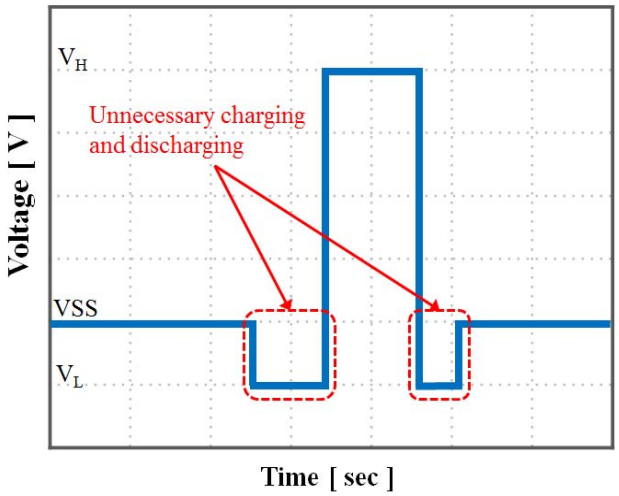

Figure 1. Output signal of previously reported scan driver

In this paper, we propose an integrated scan driver with low-power consumption and small area using a-IGZO TFTs. The power consumption is reduced by eliminating unnecessary charging current of the scan line and reducing the voltage swing of clock signals using the same voltage level for V_L of clock signal and VSS in output stage. In addition, we reduce the number of large size TFTs by merging TFTs for charging and discharging the scan line into one TFT using non-overlapping clock signals to reduce the area of scan driver.

2. Proposed scan driver circuit.

Figure 2 shows the schematic diagram of the proposed scan driver. This circuit is composed of three stages which are a DC generation stage, a control signal generation stage and an output stage. The DC generation stage generates internal supply voltage using clock signals for voltage source of an inverter in the control signal generation stage. The control signal generation stage generates control signals for the output stage. The output stage charges and discharges the large load of the scan line.

The proposed circuit is composed of 13 TFTs and 2 capacitors. The channel length of TFTs in scan driver is 7 μm except T5. The channel length of T5 is 40 μm for using as load resistor of the pseudo NTFT inverter circuit. The channel widths of TFTs are 7 μm (T5), 10 μm (T3, T4, T6 and T11), 30 μm (T8), 50 μm (T1, T2 and T7), 100 μm (T10, T12 and T13), and 600 μm (T9). T9 is relatively large to charge and discharge the scan line load. In order to reduce the area of output stage, we merged the functions of pull-up and pull-down TFTs into T9. As a result, we reduced 40% area of output stage.

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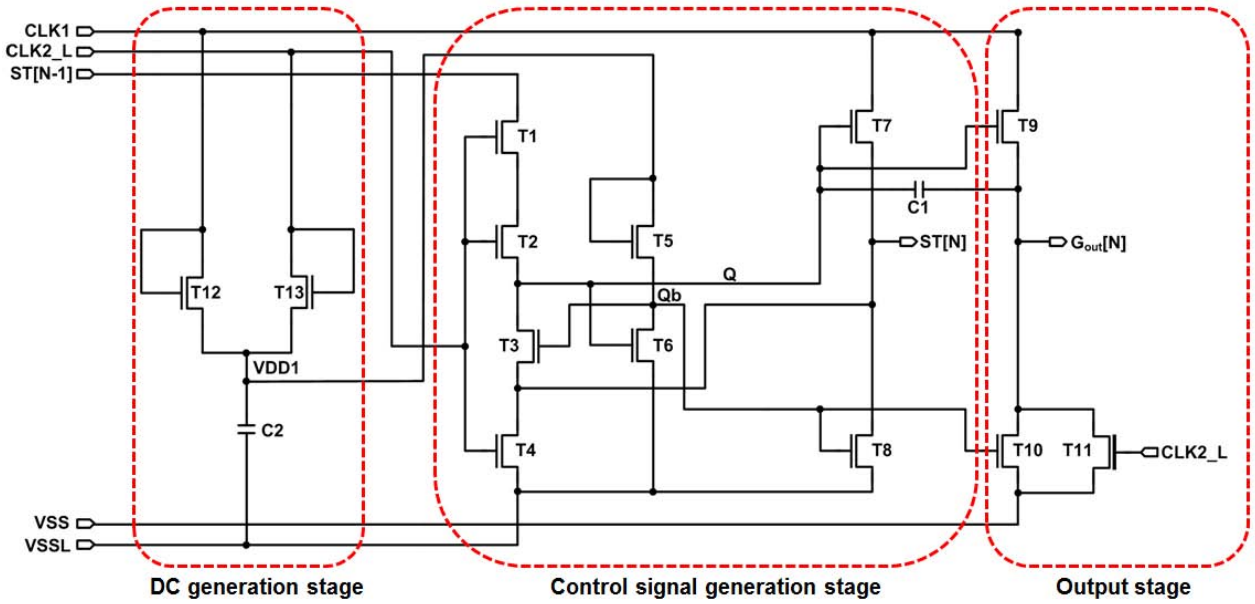


Figure 2. Schematic diagram of proposed scan driver

In addition, Low level of the signals using in control signal generation stage is lower than the signals using in the output stage to completely turn off the TFTs in the output stage by applying negative voltage to V_{GS} of TFTs. Clock signals for the output stage and the control signal generation stage are separated to reduce the power consumption. Low voltage of the clock signal using in the control signal generation stage and the output stage is set to VSSL and VSS, respectively. It removes the unnecessary charging and discharging of scan line.

Figure 3 and 4 show the block diagram and the timing diagram of the proposed scan driver. Three kinds of voltages are used which are VSS of -5V, VSSL of -10V, V_H of 15V.

V_L of two clock signals (CLK1_L and CLK2_L) in the control signal generation stage are -10V and two clock signals (CLK1 and CLK2) in the output stage are -5V. CLK1 and CLK1_L, CLK2 and CLK2_L have the same phase, respectively. CLK1 and CLK2 are inverted non-overlapping clocks

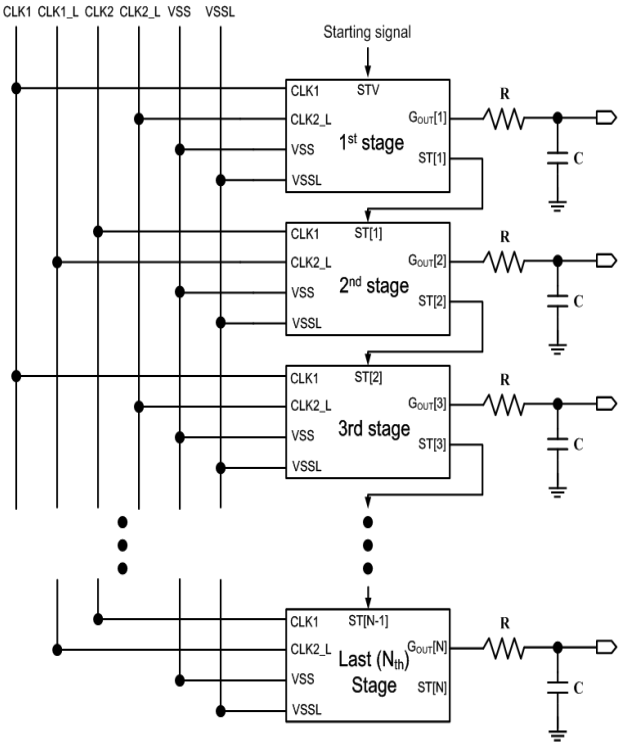


Figure 3. Block diagram of N-stage proposed scan driver

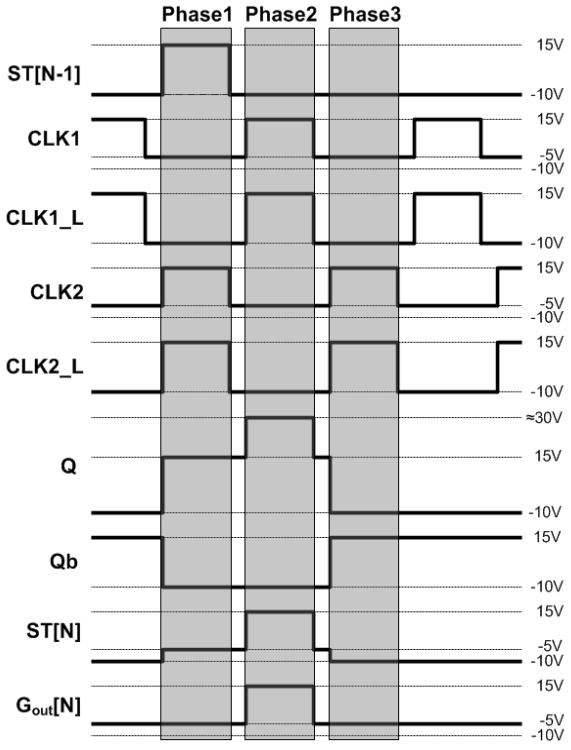


Figure 4. Timing diagram of proposed scan driver

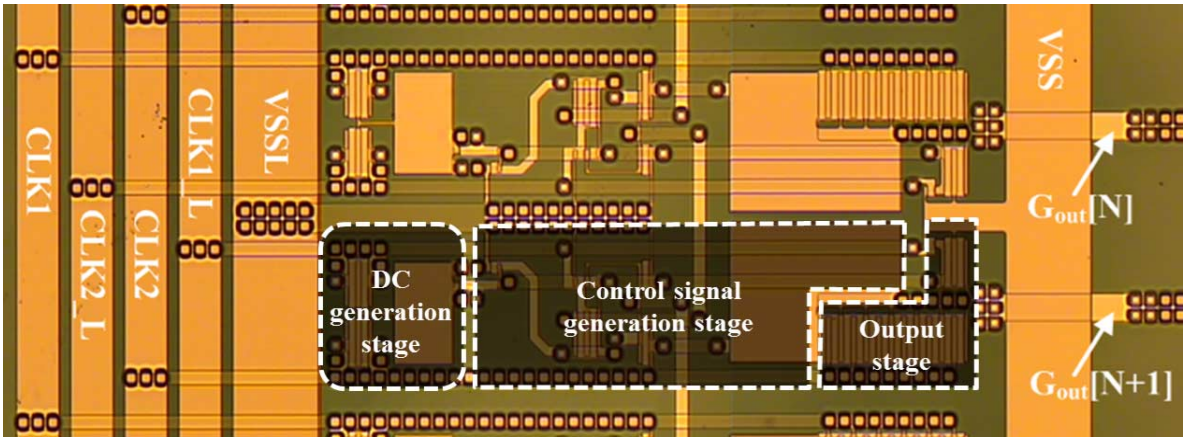


Figure 5. Microscope image of proposed scan deriver

The proposed scan driver has three operation phases which are pre-charging phase, driving phase, and holding phase. In the pre-charging phase, CLK2_L becomes 'HIGH' and output signal of previous stage (ST[N-1]) is applied to node Q of present stage through T1 and T2. Node Q is charged to V_H. In the driving phase, node Q is boosted up to almost two times of V_H by C1 when CLK1 becomes 'HIGH' so that the output signals (ST[N] and Gout[N]) can be fully charged up to V_H through T7 and T9, respectively. After that CLK1 becomes 'LOW', output signals are discharged through the same TFTs, T7 and T9. In this phase, it is important to maintain the voltage of node Q which is in floating state. We connect the node of ST[N] to the node between source of T3 and drain of T4 to reduce the leakage current. Leakage current at node Q is reduced by reducing the voltage difference between drain and source of T3. In the holding phase, node Q is discharged to VSSL when CLK2_L becomes 'HIGH'. Node Qb, an inverted signal of node Q by the inverter which is composed of T5 and T6, changes to 'HIGH', then T8 and T10 turn on to maintain ST[N] and G_{out}[N] as VSSL and VSS, respectively, for the stable operation.

3. Measurement results and discussion

We fabricated the proposed scan driver with ten stages using a-IGZO TFT on the glass substrate. Figure 5 shows the microscope image of the proposed scan driver. The area of scan driver per stage is 1153×192 μm^2. Considering a large size TFT-LCD, 10 kΩ resistor and 150 pF capacitor are connected to the output node as the load of the scan line. Table 1 shows the measurement conditions. We measured the power consumption of proposed scan drivers using CLK1, CLK2, CLK1_L and CLK2_L signals with same V_L (conventional method), and using clock signals with different V_L (proposed method) in order to compare the performance of the proposed scan driver.

Table 1. Measurement conditions

parameter	conventional method	proposed method
VSS (V)	-5	-5
VSSL (V)	-10	-10
CLK1, CLK2 (V)	-10 ~ 15	-5 ~ 15
CLK1_L, CLK2_L (V)		-10 ~ 15

Figure 6 shows the measured waveforms of input and output signals in the proposed scan driver at operating frequency of 46 kHz. This measurement results demonstrate that the proposed scan driver is working successfully.

Figure 7 (a) and (b) show output signals of scan driver in conventional method and (b) shows output signals of scan driver in proposed method for comparison. The scan drivers in conventional method use the same clock signals for the control signal generation stage and the output stage. The clock signals have lower V_L than VSS in output stage. It causes the unnecessary charging and discharging of the scan line. This results in increasing of the dynamic power consumption of the clock signals.

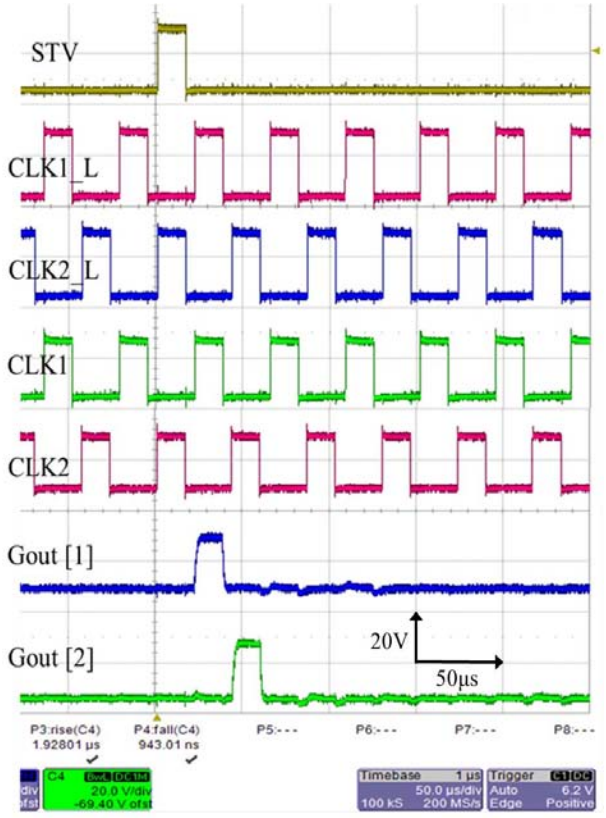
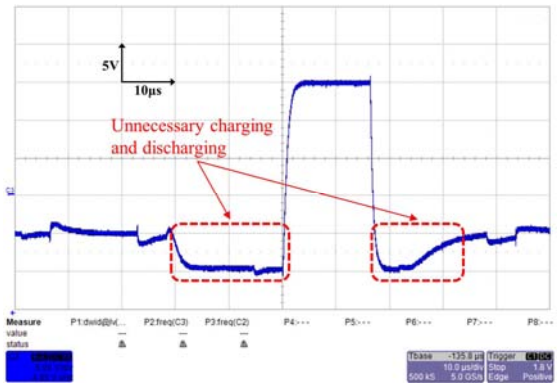
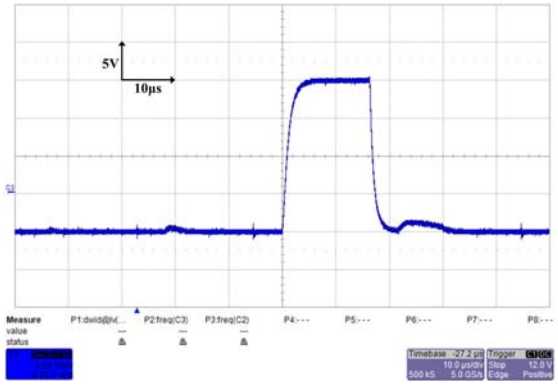


Figure 6. Measured waveforms of input and output signals



(a)



(b)

Figure 7. Output signals of proposed scan driver using (a) conventional method and (b) proposed method

The measured power consumptions per one stage are 34.7 μW in conventional method and 27.4 μW in proposed method at the operating frequency of 46 kHz, respectively. The power consumption is reduced 21% using different clock signals by eliminating unnecessary charging and discharging of scan line and reducing the swing range of clock signals. Figure 8 shows the measured last stage output waveform of the proposed scan driver at 178 kHz. This result shows that the proposed scan driver is enough to drive FULL HD 120 Hz TFT-LCD.

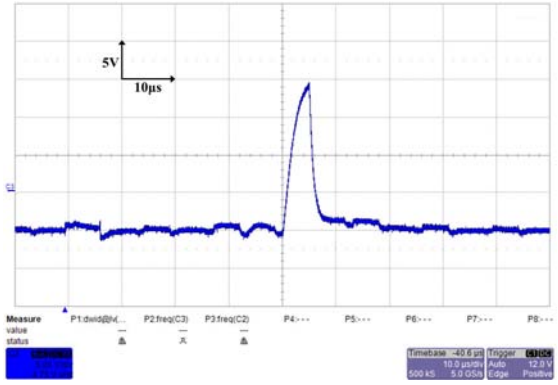


Figure 8. Output signal of proposed scan driver at 178 kHz

4. Summary

This work presents a scan driver using a-IGZO TFTs which composed of 13 TFTs and 2 capacitors. Performance of the proposed scan driver is verified by measurement results. The proposed scan driver has power consumption of 27.4 μW per stage at the operating frequency of 46 kHz and the area per stage is 1153×192 μm^2. The proposed scan driver reduces the 21% power consumption compared with previous structure by eliminating the unnecessary charging and discharging current of the scan line and reducing the swing range of clock signals. In addition, 40% area of output stage are reduced by merging the functions of pull up and pull down TFTs into one TFT for charging and discharging of scan line. As a result, we implemented low-power and small-sized scan driver using a-IGZO TFTs. Therefore the proposed methods can be usefully used to design scan driver using oxide TFTs.

5. References

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