Gating of Enhanced Electron-Charging Thresholds in Self-Assembled Nanoparticle Films

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Films of butanedithiol interconnected nanoparticles can exhibit a percolation-driven insulating to metal transition. To explore properties of materials with interpolating behavior, we have measured conductance of these films with systematically varying thickness. Films below a certain threshold coverage exhibit thermally assisted conductance and conductance suppression near zero bias indicative of single-electron-charging barriers. In analogy with semiconductors, we show that these films permit transistor-type gating of film conductivity.

Realization of self-assembled nanoparticle-based transistors[1,2] has been an important step in the development of single electron devices.[3−7] Self-assembly affords a wide choice of presynthesized nanocomponents suitable for use in device fabrication, including components potentially much smaller than those fabricated by microlithography.[1,8−12] Significantly, it is also a highly parallel approach enabling a bridging of nano- and macroscopic scales.

We describe here electrical measurements of macroscopic self-assembled films comprising metal nanoparticles (NPs) linked with insulating molecules.[9,13−18] NPs are commonly referred to as "artificial atoms"[19] and can be viewed as building blocks for the macroscopic self-assembled films. Assemblies of NPs can then be considered as "artificial materials". Assembly properties can be conveniently described using nanoparticles and molecular linkers as a basis, just as properties of materials can be well understood using atoms as a basis. We have shown in a previous study that self-assembled NP films can give rise to single-electron-charging effects with very large threshold voltages arising from their NP substructure.[15] Energy barriers arise fundamentally from single electron charging and are broadened by a natural tendency of such materials to form large, disordered arrays of NP clusters. We show here that such self-assembled NP films can be used as a critical element in field effect transistors (FETs), albeit with much smaller ON/OFF conductance ratios than commercial semiconductor-based devices. Our results highlight the versatility of self-assembled materials both to exhibit a wide range of electric behavior controllable through film composition and thickness[20−22] and to exhibit robust, gate-field sensitive single electron effects even at macroscopic scales.

Gold NPs were synthesized following a modified Brust method (see Supporting Information).[9,17,23] Briefly, nanoparticles are formed by reducing tetraoctylammonium-stabilized hydrogen tetrachloroaurate with sodium borohydride in toluene. This procedure yields particles with average diameters in a 5−8 nm range as determined by transmission electron microscopy.[17] Solutions were stable against aggregation for at least several months. Figure 1a shows device preparation procedures. A heavily doped silicon wafer was annealed at 1000 °C for 20 h in oxygen to grow gate oxides. Next, a central ∼1 mm wide trench was etched in the oxide with a 5% HF/H_2O solution, and a thin oxide was then grown on the entire surface by annealing the wafer at 900 °C for 30 min in oxygen. Expected thicknesses for the trench and remaining oxides were ∼10 to 30 nm and 300 nm, respectively. A molecularly linked gold NP film was self-assembled on the oxide surface by immersing the wafer in a solution of 2% 3-aminopropyldiethoxymethylsilane in toluene at 80 °C for 20 min and then by alternately immersing the wafer in toluene solutions of gold NPs and 0.5 mM 1,4-butanedithiol. We allowed 4 h for the first and 1 h for subsequent immersions in the gold NP solution and 10 min for immersions in the dithiol solution. We observed aggregation of NPs on surfaces if films were dried after NP immersions. To avoid aggregation, we immediately exposed the films to excess butanedithiol solution after rinsing with solvent but without drying the films. Using indium, two copper wires were attached to the film on the thick oxide and one to the silicon for application of bias and gate voltages, respectively. For samples used to explore the evolution of film properties as a function of increasing NP/dithiol exposure cycles, indium electrodes (ca. 1×1 mm^2 in size) were soldered before the silanization and film self-assembly steps. We confirmed reproducibility by testing three samples for this measurement. We also tested 15 other samples prepared with four exposure cycles. For conductance measurements, one of the electrodes attached to the film was electrically grounded, and bias and gate voltages were applied relative to this grounded electrode. Of the 15 four-exposure samples, some had indium electrodes attached after oxide growth, others after silanization, and still others after completion of NP/dithiol exposure cycles. No qualitative difference was observed in plots of conductance versus bias and gate voltages. Differential conductance was numerically calculated from current-bias voltage measurements. NP films were stable over many bias voltage sweeps below ±3 V and temperature cycles between 77 and 300 K. These samples were also stable despite being stored for at least a few months.

Previous studies have shown using ultraviolet−visible spectroscopy and scanning electron microscopy that the above film preparation procedure adds an approximately constant amount of material per immersion cycle.[13] Figure 1c shows an ambient scanning tunneling microscope (STM) image of a film. The NPs in the STM image appear larger and more broadly distributed in size than they do in transmission electron microscope images. This is probably due to a convolution of rough surface topography and a broad STM tip, as well as the existence of

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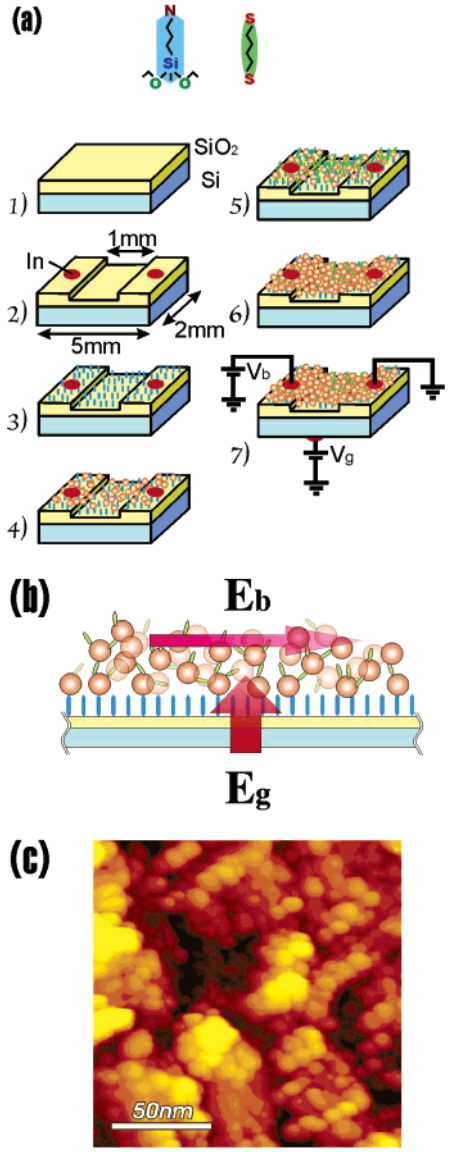

Figure 1. (a) Device fabrication procedures. A heavily doped silicon wafer with a patterned oxide layer is initially functionalized with an aminosilane. A film of molecularly linked nanoparticles is subsequently self-assembled on the wafer by immersing it alternately in toluene solutions of ~5 nm gold nanoparticles and butanedithiol. V_b and V_g represent bias and gate voltages, respectively. (b) Cross-sectional schematic of a prepared sample. Bias and gate electric fields are denoted by E_b and E_g, respectively. (c) A scanning tunneling microscope image of a self-assembled nanoparticle film. The film was self-assembled using four nanoparticle/butanedithiol exposure cycles. Tip bias and current set point were −1.2 V and 0.1 nA, respectively.

clusters of linked-NPs. Nevertheless, the image correctly shows that the film is morphologically disordered. The images are typically quite stable, implying good chemical adhesion of the NPs.

Before proceeding to three-terminal conductance measurements involving a gate electrode, we first performed several two-terminal measurements. Figure 2a shows a plot of logarithm of zero-bias differential conductance versus inverse temperature from 80 to 270 K. The sample probed was prepared on a glass slide using four NP/dithiol immersion cycles, and its resistance at room temperature was 625 kΩ. Figure 2a shows that differential conductance decreases by an order of magnitude with decreasing temperature (270 to 80 K), indicating nonmetallic behavior. The plot exhibits excellent agreement with

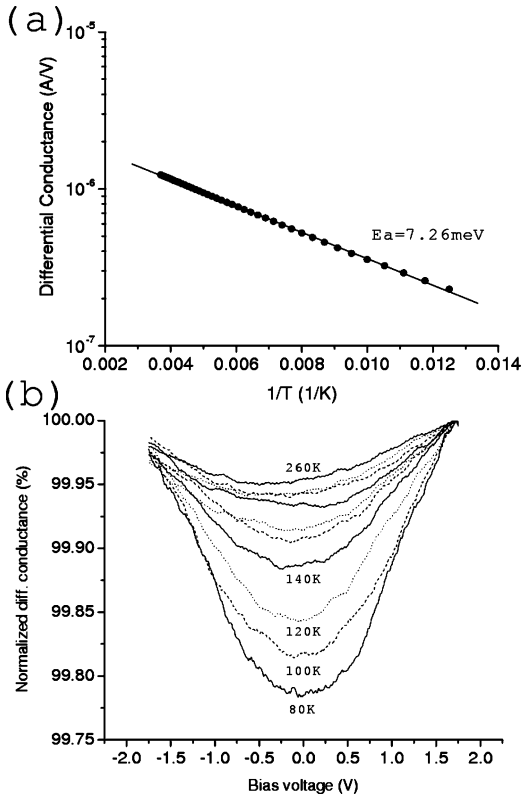

Figure 2. (a) Plot of zero-bias differential conductance versus temperature. Activation energy obtained by linear fitting is 7.26 meV. (b) Plots of normalized differential conductance versus bias voltage at various temperatures (20 K steps).

Arrhenius behavior with an activation energy of $E_a = 7.26$ meV. Repeating sample preparation and measurements several times, we found that film resistance at room temperature for various four immersion cycle samples ranged from 100 kΩ to 10 MΩ likely because of variation in local film morphology and percolation effects. Although film resistance is only very roughly controlled from sample to sample through the number of immersion cycles, it is possible to carefully control the resistances of a given sample through immersion time, for example. For a given sample, as more material is deposited, film resistance decreases. Detailed examples are provided below. We note that of 15 samples exhibiting nonmetallic temperature dependence, all 15 revealed similar conductance features also described in detail below.

Figure 2b shows normalized differential conductance versus bias voltage measurements at various temperatures for the same sample considered in Figure 2a. Each curve was obtained by dividing differential conductance curves by their respective values at 1.75 V.[24] At 80 K, there is a distinct, extremely broad (~2 V, 0.22%) suppression of differential conductance around zero-bias voltage. We found that the suppression gradually diminished with increasing temperature. Generally, addition of more NPs tends to increase film conductance[13,14] and reduce the suppression.[15] Several films grown on glass slides exhibited similar broad conductance suppressions near zero-bias voltages.[15] Samples subjected to a large number (approximately eight exposures) of immersion cycles and subsequently had indium electrodes attached consistently exhibited low room-temperature resistances (100~300 Ω) and increasing conductance with decreasing temperature (metallic-like behavior).

As is the case with evaporated granular metal films, charge transport through disordered molecularly linked NP films likely

involves many competing local processes, such as metallic charge transport, thermionic emission, thermally assisted tunneling, hopping, and so forth, as well as percolation phenomena.[16,25,26] Samples with sufficiently few exposures are necessarily insulating. With increasing NP exposure, films contain increasingly large "clusters" of molecularly linked NPs until at a percolation threshold there is at least one such linked cluster spanning the sample.[13] We have observed that samples over a certain threshold number of exposures exhibit metallic-like temperature dependences, implying that butanedithiol provides sufficient inter-NP electrical connectivity to permit metallic-like transport within a cluster.[16,17,20]

At intermediate exposures, capacitances between NP clusters give rise to single-electron-charging energy barriers. The barriers contribute to the observed thermally assisted transport[27] and account for observed current suppression around zero bias (Coulomb blockade).[15] An isolated ~5 nm sphere has a self-capacitance of ~0.5 aF and a charging energy of ~0.2 eV, much smaller than the observed suppression energy scale of ~2 eV. In practice, an NP in the film is capacitatively coupled to other NPs and its charging energy is expected to be even lower, exacerbating the discrepancy with the observed value. The larger observed value can be attributed to the fact that below the percolation threshold, current flows through the disordered film from cluster to cluster along quasi-one-dimensional pathways of lowest resistances.[28,29] For samples further below the percolation threshold, the number of clusters in a current-bearing pathway increases, cluster sizes decrease, the voltage drop between clusters increases (because of voltage division), and the energy an electron has to charge a given cluster drops.[15,28] As a result, Coulomb blockade threshold voltages, as gauged by the range of voltages over which current is suppressed, are expected to increase as observed.[15] Decreasing single cluster capacitances also contribute toward generating larger thresholds. The measured activation energy of $E_a = 7.26$ meV corresponds to a thermal energy of 84 K. Assuming a Coulomb charging energy threshold $E_{th} \sim e^2/2C$ that is on the order of E_a, C is ~10 aF and the voltage division argument suggests that the number of clusters is about 2 eV/7.26 meV or ~275. If we assume that all clusters are isolated, equally sized, and span the distance between the electrodes (~1 mm), then clusters are expected to be ~ 4 μm in diameter. The capacitance between such large clusters and the silicon substrate would be ~25 fF, which is much too large. A more likely picture is that current flows through pathways with metal-like clusters of various sizes, and the smallest capacitances through the pathways are about ~10 aF.

Several studies have reported the existence of single-electron-charging effects in other systems, including ordered ultrasmall tunnel-junction arrays,[30] spin/drop cast[31,32] or compressed NP superlattices,[33] and disordered granular metal films.[34] A key flexibility afforded by the self-assembly process is that it permits preparation of bulk materials with a broad range of behaviors. Despite their disordered morphology, electronic behaviors of molecularly linked films are controllable through independent choice of assembly components and the assembly process itself. The latter includes choice over parameters such as film thickness. Interestingly, below the linking percolation threshold, bulk NP film behavior is intermediate between insulating and metallic, since the films can support current flow yet the number of charge carriers is limited by single-electron-charging energy barriers and temperature. In the case of semiconductors, limited carrier densities are such that they can support unscreened DC electric fields and enable field-effect transistor operation.

To explore the possibility that NP films, too, can support a gate-field-induced change in conductance, we measured conductance of a given film with increasing NP/dithiol exposure cycles. Figure 3 shows a series of plots of differential conductance versus bias (V_b) and gate (V_g) voltages measured at 77 K. Data were obtained using one given sample prepared on SiO_2/degenerately doped p-type silicon and are displayed sequentially with increasing number of exposures. At low number of exposure cycles, we observe clear conductance suppression. Its amplitude decreases from ~50% to <0.5% with increasing number of exposures from two to eight (see percentages in color scale bars in Figure 3). We also observe suppression in the plots evolving from being vertical to diagonal in shape as the number of exposures increases to five, after which point the shape remains roughly unchanged. A gate effect results in a linear shift of conductance suppression minimum away from $V_b = 0$ and gives rise to the diagonal shape. These results were very reproducible. We tested three samples with varying number of exposures, and all exhibited a similar controlled evolution of conductance versus V_b and V_g. We also tested 15 other nonmetallic samples prepared using four exposures. All exhibited conductance suppression in the range of 1−10% and diagonal conductance plots similar in shape to that in Figure 3d. For a given sample, the data were reproducible from scan to scan. To exclude a possibility that the conductance features can be attributed to a leakage current through the gate oxide, we directly measured the leakage current at maximum gate voltage using a four-exposure sample and found that the leakage current was well below 50 pA, the level of our AC noise. The observation that similar suppressions were found on insulating glass slides also excludes leakage current as a possible cause. Further, conductance suppression weakened and frequently disappeared all together at higher temperatures (~175 K), consistent with thermally overcoming energy barriers. In a control measurement, we observed that the gate effect became significantly weaker if the oxide below the central part of film was thick (see Supporting Information). This observation eliminates a possibility that the gate effects arise from contact or edge effects at the source or drain electrodes. Source/drain contact and edge effects are localized at or near these contacts since gate-induced fringe fields extend on length scales on the order of ~300 nm around source or drain electrodes because of the oxide thickness. However, the modified central oxide was much further away (~500 μm).

To confirm both the existence of an energy barrier to electron flow and the controlled evolution of the barrier with film thickness, we measured zero-bias differential conductance versus temperature at $V_g = 0$ V for the sample considered in Figure 3. Arrhenius plots of the data are shown in Figure 4a. Each line corresponds to the sample at a different exposure number and is associated with a corresponding differential conductance plot in Figure 3. Zero-bias differential conductance systematically increases with increasing temperature indicating nonmetallic behavior. The data yield excellent fits to straight lines. Best-fit slopes and intercepts yield activation energies and conductance at a high-temperature limit ($T \rightarrow \infty$), as shown in Figure 4b and c, respectively. The activation energy decreases rapidly for the first few exposures and then more slowly beyond around six exposures. A tendency toward saturation is clearer in Figure 4c. We believe that the rapid drop in activation energy is due to a formation of larger metallic clusters in films. As films grow thicker with more exposures, these clusters grow and capacitance

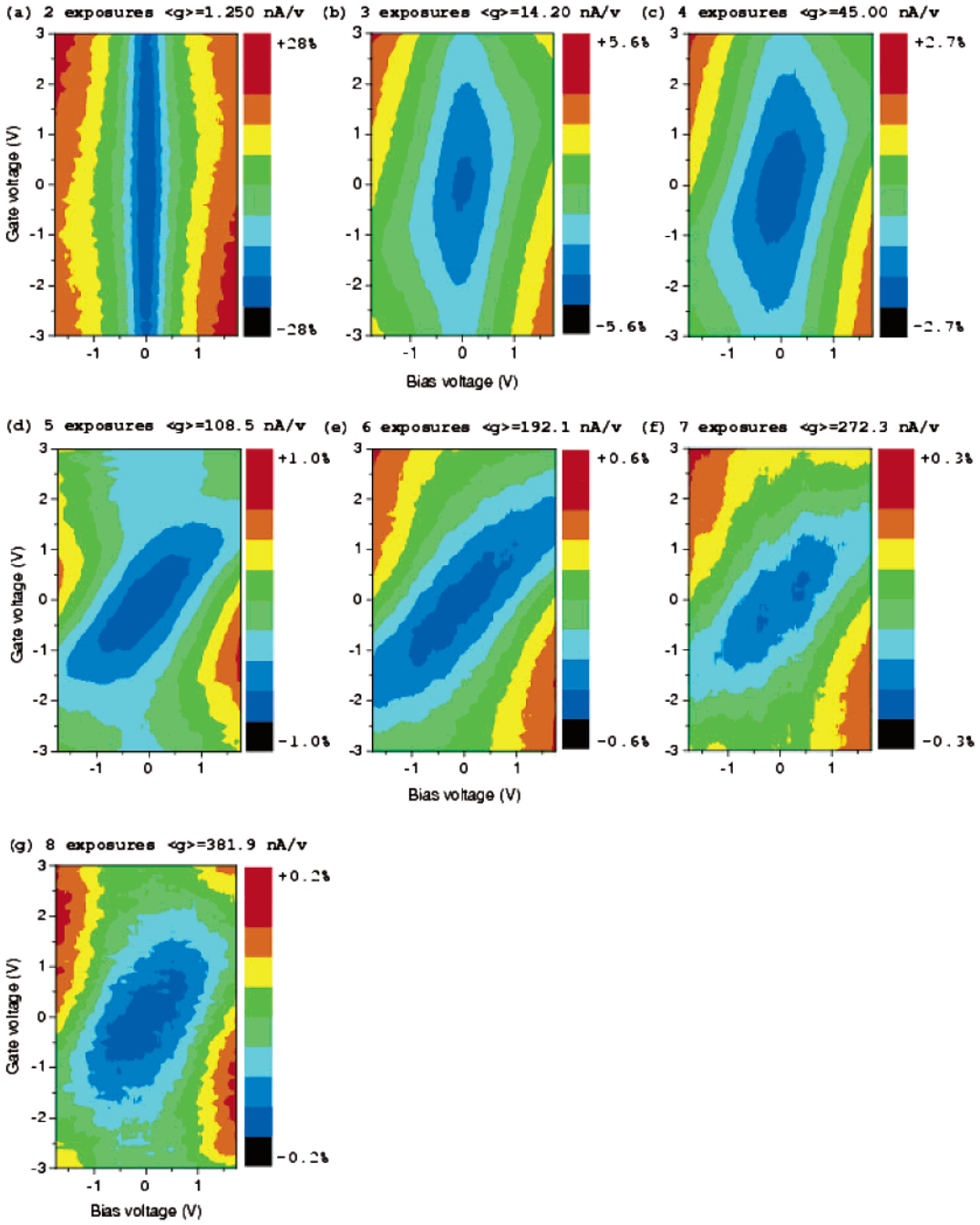

Figure 3. Differential conductance maps as a function of bias and gate voltages at 77 K. We exposed the same sample eight times to nanoparticle and dithiol solutions and measured surface plots after each exposure. Each conductance surface plots is labeled with its average conductance value, $\langle g \rangle$, which corresponds to 0% in the color scale.

between them increases so that the associated charging energy decreases.[35] The eventual saturation may be due to contact resistance.

The observed gate-tunability of differential conductance minima can be straightforwardly rationalized in a context of single-electron phenomena and Coulomb blockade. Since current through disordered films flows predominantly through quasi-1D pathways of least resistance,[28,29] we first consider idealized 1D pathways through arrays of clusters as shown in Figure 5. Clusters are capacitatively coupled, and tunneling between clusters is admitted by a resistor. As a result, the electrical behavior of such an array can be modeled using parallel resistor−capacitor combinations connected in series as shown. Because of the existence of a quantum of electronic charge, the charging energy-level spectrum associated with the array is discrete. In Figure 5, we have shown a situation in which Coulomb blockade energy gaps (Δ) between the highest occupied and lowest unoccupied charging energy levels are equal and symmetrically distributed with respect to the Fermi level. In practice, disorder in film morphology and fluctuations in local fields because of trapped charges will give rise to variations from this picture, as discussed below. When a bias voltage is applied across such an idealized array, it is divided equally along each junction, and charging energy levels are lowered by a fraction of the total voltage applied. At a threshold negative bias voltage, all of the lowest unoccupied charging energy levels cross the Fermi level and the system exits the Coulomb blockade region. There is an analogous threshold at positive bias voltages. When $V_g \neq 0$, all the charging energy

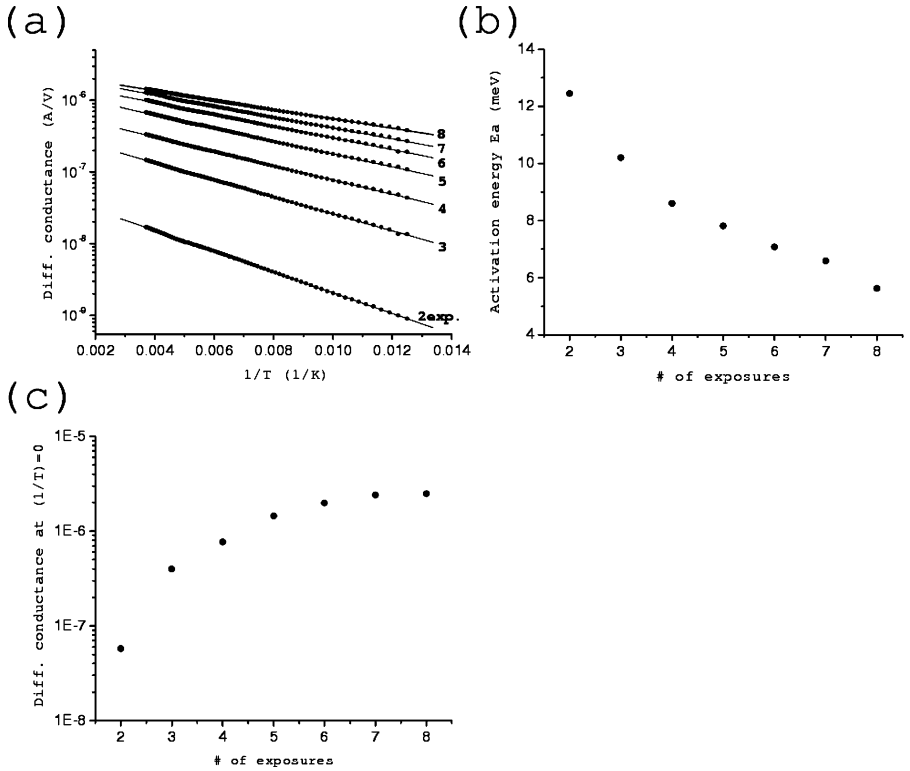

Figure 4. (a) Arrhenius plots of zero-bias differential conductance versus temperature measurements at $V_g = 0$ V for the same sample used in Figure 3. Each exposure is associated with a corresponding surface plot in Figure 3. (b) Activation energies and (c) conductance at a high-temperature limit ($T \rightarrow \infty$) obtained from the best fit lines in (a).

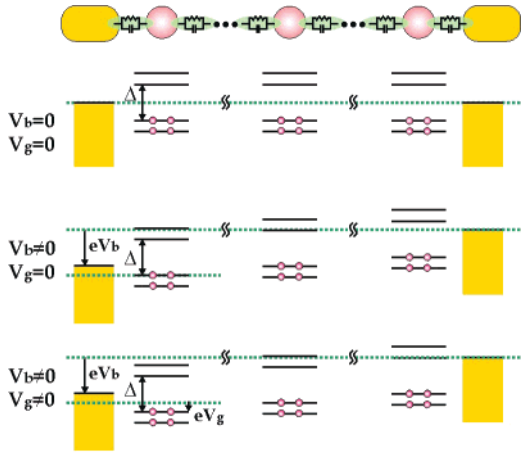

Figure 5. Schematic illustration of a resistor−capacitor model and a corresponding energy-level diagram for an idealized serial array of nanoparticle clusters. When bias and gate voltages (V_b and V_g) are both zero, the Fermi level is assumed to be located midway between equally sized Coulomb blockade energy gaps. An applied V_b is distributed among the capacitors providing an inclined potential, and an applied V_g shifts all charging energy levels of clusters equally.

levels shift by the same amount, eV_g, in turn shifting the Coulomb blockade threshold voltages.

If films had idealized energy values shown in Figure 5, we would expect to observe periodic diamond-shaped conductance suppressions (so-called Coulomb oscillation[36]) as we sweep gate voltage, owing to the presence of higher Coulomb energy states. The fact that samples showed diagonal current suppression, as in Figure 3d, suggests that morphological variations, which give rise to multiple parallel current pathways and clusters with a range of capacitances, also give rise to averaging over a distribution of charging energy levels. Such averaging will strongly diminish the contrast of Coulomb oscillations by reducing the number of bottlenecks at the corresponding gate voltage.

In such films, the temperature dependence of conductance near zero bias provides a practical measure for the charging energy since only thermally activated electrons may contribute to current flow. As metallic clusters in a film grow, capacitances between these clusters become larger. As a result, Coulomb blockade energy and the activation energy are lowered, as observed in Figure 4b. Simultaneously, electronic screening by the metallic clusters should increase and eventually weaken gate effects, as is observed. Our measurements do not provide a conclusive cause for the initial increase in gate influence with increasing gold NP/dithiol exposure cycles. We speculate that film morphology plays an important role. One possible scenario is that as the number of exposures increases, regions around current pathways become increasingly occupied with clusters which can become polarized and produce stronger local gating fields. Another scenario is that the strong feature near 0 V in thin films with few exposures may include a contribution from tunneling. Tunneling itself is not influenced by gate fields and can appear as a very strong increase in differential conductance with increasing magnitude of bias voltage. As film thickness increases and tunneling gaps are filled, a gate-tunable Coulomb blockade feature becomes more apparent.

Trapped charge distribution may give rise to important additional deviations from the idealized picture shown in Figure 5. Several previous studies have shown that quasi-trapped charges can dramatically alter contact potentials of surfaces under ambient conditions[37] and can alter charging threshold voltages of single electron devices even at temperatures as low as 4.2 K.[38] Averaging over a random distribution of charges will cause Coulomb blockade to vanish for some junctions. The film will nevertheless continue to exhibit broad blockade behavior because of bottleneck junctions with surviving block-

ade effects. A disordered energy landscape generated by a distribution of trapped charges is likely ubiquitous in practice. As a result, percolation effects that are critical in morphologically disordered, chemically self-assembled NP films discussed here are very likely of widespread importance, even in systems with a high degree of NP spatial ordering.[32,39]

In summary, we have demonstrated gate-tunability of enhanced Coulomb blockade effects in bulk films of molecularly linked NPs. Realization of these macroscopic single electron devices relied critically on a basic flexibility inherent in self-assembly as well as on an ability of this technique to bridge nano- and macroscopic scales. Future studies will exploit these techniques, particularly with respect to their ability to generate widely varying device behaviors and functionalities through straightforward changes in film composition and thickness.

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Supporting Information Available: Synthetic details for gold nanoparticle preparation, detailed experimental setup, and control measurements using thicker gate oxides are enclosed. This material is available free of charge via the Internet at http://pubs.acs.org.

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