Effect of Dielectric Roughness on Performance of Pentacene TFTs and Restoration of Performance with a Polymeric Smoothing Layer

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The morphology, structure, and transport properties of pentacene thin film transistors (TFTs) are reported showing the influence of the gate dielectric surface roughness. Upon roughening of the amorphous SiO_2 gate dielectric prior to pentacene deposition, dramatic reductions in pentacene grain size and crystallinity were observed. The TFT performance of pentacene films deposited on roughened substrates showed reduced free carrier mobility, larger transport activation energies, and larger trap distribution widths. Spin coating roughened dielectrics with polystyrene produced surfaces with 2 Å root-mean-square (rms) roughness. The pentacene films deposited on these coated surfaces had grain sizes, crystallinities, mobilities, and trap distributions that were comparable to the range of values observed for pentacene films deposited on thermally grown SiO_2 (roughness also ∼2 Å rms).

Introduction

Organic semiconductors are being explored for use in consumer electronics such as smart cards, radio frequency identification (RFID) tags,[1,2] display backplane driver circuits,[3−5] and sensors.[6] Polycrystalline films of pentacene, in particular, have shown electrical performance comparable to amorphous hydrogenated silicon (a-Si:H), making pentacene attractive for thin film transistor (TFT) applications.

During vapor deposition of organic semiconductor materials such as pentacene, film morphology and structure are controlled by process parameters including substrate temperature,[7−10] deposition rate,[11] and pentacene source purity.[12] Several groups have explored the correlation between grain size and charge mobility on SiO_2 gate dielectrics; generally, mobility increases with increasing grain size.[13,14] Mobilities in the range of 0.6−1.7 cm^2/V s have been achieved for large-grained pentacene films on SiO_2.[3,15,16] However, the opposite trend of mobility increasing with decreasing grain size has been shown for pentacene films deposited on SiO_2 coated with a monolayer of octadecyltrichorosilane (OTS). This dielectric surface treatment leads to mobilities ranging from 1.5 to >2 cm^2/V s.[17,18] Even higher mobilities have been achieved, with no clear correlation between mobility and grain size, for pentacene deposited on polyvinylphenol-coated silica ($\mu = 3$ cm^2/V s)[19] and poly(α-methylstyrene)-coated alumina ($\mu > 5$ cm^2/V s).[20] The conflicting results on the importance of grain size underscore the point that the connection between dielectric surface energy, film morphology, and electrical properties in pentacene is not fully understood.[21−26]

It is generally accepted, however, that the surface roughness of the gate dielectric is an important parameter that affects the electrical performance of organic semiconductor films in TFTs.[27,28] In recent work, rougher substrates have been shown to result in smaller grains and lower mobilities.[29] Here we report the electrical performance of pentacene TFTs based on SiO_2 dielectrics with root-mean-square (rms) roughnesses varying from 2 to 20 Å. Temperature-dependent measurements indicate that carrier trapping is more pronounced on rougher substrates, consistent with lower observed mobilities. Importantly, we show that spin coating of the rough dielectric surfaces with ∼100 Å of polystyrene "erases" the effects of roughness and restores the electrical performance of the pentacene layer. Our polystyrene-coated substrates have essentially the same smoothness as thermally grown SiO_2, and the electrical performance of pentacene TFTs on the polystyrene-treated substrates is comparable to devices on thermally grown SiO_2. The polymer coating strategy appears to be completely general and thus could be used to prime any dielectric surface before organic semiconductor deposition.[30] In particular, the polymer coating may be useful for smoothing low temperature dielectric materials that are necessary for flexible electronics but that typically exhibit rough surfaces.

Experimental Section

Heavily doped p-type silicon wafers were used as substrates for TFT fabrication. A 3000 Å thick thermal oxide grown on the polished side of the wafer functioned as the gate dielectric, and additional metallic layers deposited on the unpolished side of the wafer (Al and Au) formed the back-side gate contact. The SiO_2 dielectric was "roughened" in an STS Reactive Ion etcher maintained by the Nanofabrication Facility at the University of Minnesota (CF_4 at 40 sccm, O_2 at 4 sccm, 100 mTorr, 100 W, and 30−120 s run time). Polystyrene treatments on the SiO_2/Si wafers were supplied by 3M Company. A 0.1 wt % solution of polystyrene in toluene was applied by spin coating and followed with an oven bake at ∼120 °C for ∼30 min to remove residual solvent.[20] The polymer film thickness was ∼100 Å.

Pentacene purchased from Aldrich was purified by gradient sublimation[31] prior to evaporation in a vacuum system (pressure

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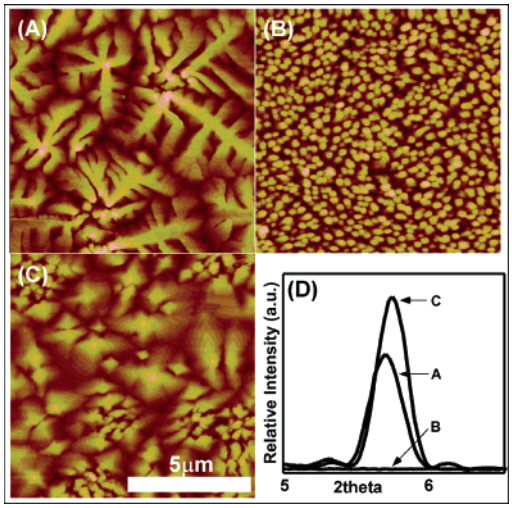

Figure 1. Tapping mode AFM images of pentacene films (~350 Å) on (A) "smooth" SiO_2, (B) "rough" SiO_2, and (C) polystyrene-coated "rough" SiO_2. XRD spectra (D) for the first-order reflection (001″) from these pentacene films.

$<10^{-6}$ Torr, $T_{substrate} = 25$ °C, and rate 0.01−0.3 Å/s). The pentacene source material was resistively heated to 130−150 °C, at which point the shutter was opened and the source was further heated to 170−200 °C. Evaporations were performed in this manner to obtain a low initial deposition rate and good molecular ordering in the first few layers of pentacene. Atomic force microscope (AFM) images were obtained using a Digital Instruments Dimension 3100 AFM with NanoScope Software and MikroMasch noncontact silicon cantilevers in tapping mode. The structure of the films was characterized by X-ray diffraction (XRD) measurements using a Philips/PANalytical X'pert PRO high-resolution diffractometer.

After organic film deposition and characterization, source and drain top contacts (~500 Å gold) were thermally evaporated (pressure $<10^{-6}$ Torr and rate = 0.1−1 Å/s) through a shadow mask (channel length (L) ~200 μm and width (W) ~2000 μm). Electrical characterization was performed in a Desert Cryogenics probe station with a base pressure of 5×10^{-7} Torr. Source and drain voltages were applied with Keithley 236 and 237 source measure units, respectively. Gate voltages were applied with a Keithley 6517A electrometer. Source and drain currents were independently monitored by the 236 and 237, respectively, to evaluate potential leaks in the devices. All three units shared a common ground with an input impedance of 10^{14} Ω. Temperature was controlled via a Lakeshore L-331 controller between 80 and 295 K. Measurements were taken in the dark.

Results and Discussion

Four types of organic thin film transistors (OTFTs) were fabricated and include pentacene on (A) "smooth" SiO_2 (roughness ~2 Å rms), (B) "rough" SiO_2 (roughness ~15 Å rms), (C) polystyrene-treated "rough" SiO_2, and (D) polystyrene-treated "smooth" SiO_2 (note that for samples C and D roughness after polystyrene treatment was ~2 Å rms).[32] Figure 1 shows AFM images of the film morphology of pentacene films (~350 Å thick) on the aforementioned dielectric surfaces A−C. Sample A exhibited terraced, dendritic growth typical of pentacene films on amorphous SiO_2. Sample B confirmed that a pentacene film deposited on rough SiO_2 exhibits small, nodular grains with no visible crystalline faceting.[27] Samples C and D exhibited terraced grains similar to those of the pentacene film on "smooth" SiO_2 (A) with subtle differences (grains appeared smaller, flatter, and less dendritic). These morphologies were seen for four separate pentacene runs on dielectrics of types A−D. Sample D was included in the pentacene runs as a control sample. Also included were various roughnesses of SiO_2 for which we observed that, as the roughness of the SiO_2 was gradually increased, the grain size observed by AFM decreased, as seen elsewhere.[29] In the early stages of pentacene growth, an island nucleation density similar to that of the smooth (as grown) SiO_2 was seen on the rough SiO_2; however, the shape of the monolayer islands was more dendritic on the rough dielectric. During the initial stages of pentacene film growth on the polymer-treated substrates, an increased island nucleation density was observed in comparison to the nucleation density of pentacene islands on smooth SiO_2. Therefore, although the rms roughness of the smooth SiO_2 and polystyrene treatment are comparable, differences in resulting film nucleation density and grain size indicate that surface energy also has an effect on film morphology.

X-ray diffraction (XRD) of pentacene films was performed to determine intermolecular layer spacing. The diffraction spectrum of pentacene deposited on smooth SiO_2 confirms the presence of the "thin film" phase peak at $2\theta = 5.7°$, corresponding to a $d_{001''}$ spacing of 15.4 Å.[9,15,33] Presence of the "bulk" phase of pentacene ($d_{001'} = 14.4$ Å)[34] was not observed for films reported here; however, we do see the "bulk" phase for thicker pentacene films and films grown at higher substrate temperatures.[7,11] The XRD spectra of pentacene on rough SiO_2 (sample B) do not exhibit any crystalline peaks either in $2\theta-\omega$ coupled mode or by rocking the sample through ω with 2θ set to 5.7°. For pentacene film samples of gradually increasing SiO_2 roughness, X-ray diffraction peak intensity and number of higher order reflections decreased until the XRD spectra were featureless. Crystalline peaks corresponding to the "thin film" spacing of 15.4 Å and the presence of higher order peaks (up to 4 or 5) were observed for sample C similar to sample A. For samples A and C rocking curve widths were observed to be as low as 0.06°. This is attributed to good in-plane film uniformity, i.e., low mosaicity of grains.[35] Figure 1D shows an overlay of the first-order diffraction peaks for samples A, B, and C. Low-intensity, broad peaks symmetrically spaced about the first-order peak (at $2\theta = 5.3$ and 6.1°) are "finite size fringes" due to the good parallelism between molecular layers. The centroids of the (001″) peaks for samples A and C show a very small offset, which is within experimental precision (±0.02°). Further investigation, using higher precision scans, would be worthwhile to investigate any variation of the (001″) peak location.

Pentacene transistors were characterized in the linear and saturation regimes defined by standard MOSFET models,[36] and the electrical transport properties calculated included linear mobility (μ_{lin}), saturation mobility (μ_{sat}), onset voltage (V_0), threshold voltage (V_T), on-to-off current ratio (on/off), and subthreshold swing (S). Room temperature transfer parameters are summarized in Table 1, with each value averaged over four devices (for each sample type) fabricated over the course of 9 months (four separate pentacene runs). No special attention was paid to the amount of time samples were exposed to ambient conditions prior to electrical characterization (typically from 1 day to 2 weeks). The largest variation for any given set of samples was seen in V_0. This is likely due to impurities at the semiconductor−dielectric interface and can be attributed to process variability.

Sample A exhibited transport properties typical of a pentacene TFT on SiO_2 (Figure 2A). Sample B fabricated on the rough SiO_2 dielectric displayed an order of magnitude decrease in

TABLE 1: Room Temperature Transfer Characteristics

sample	μ_{sat} (cm^2/V s)	μ_{lin} (cm^2/V s)	V_0 (V)	V_T (V)	on/off	S (V/decade)
A (smooth SiO_2)	0.31	0.31	4	−10	5×10^8	1.4
B (rough SiO_2)	0.02	0.02	−19	−32	1×10^7	1.7
C (polymer coated)	0.94	0.62	2	−8	4×10^7	2.1

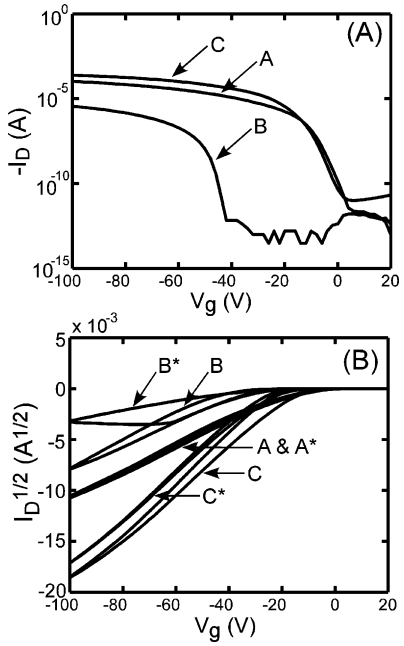

Figure 2. (A) Room temperature transfer characteristics of samples A, B, and C at $V_d = -50$ V. (B) $I^{1/2}$ vs V_G plotted for $V_d = -50$ V showing the hysteresis between forward and reverse gate sweeps at room temperature (A, B, and C) and 260 K (A*, B*, and C*).

linear (μ_{lin}) and saturation (μ_{sat}) mobilities and a significant negative shift in onset voltage (V_0), as shown in Table 1 and Figure 2A. The negative shift in V_0 and V_T for sample B can be attributed to an increase in the presence of traps at the interface between the pentacene film and the dielectric. Sample B also displayed significant hysteresis between forward and reverse gate voltage sweeps, indicating slow carrier detrapping rates within the film. Figure 2B shows an increase in trapping by the increase in hysteresis upon slight cooling of sample B to 260 K. Electrical characteristics of sample C were comparable to those of A, with a small increase in mobility. This illustrates that favorable transport characteristics can be obtained by application of a polymer smoothing layer on a rough dielectric surface. Sample films of pentacene on various roughnesses of SiO_2 were also electrically characterized. Figure 3 illustrates the sharp decrease in room temperature linear mobilities with increasing roughness of the dielectric, similar to that seen by Steudel et al.,[27] as well as the shift in onset voltage to more negative values with increasing dielectric roughness. There is a notable spread in mobilities for devices having a dielectric roughness <0.5 nm rms, indicating that process variables in addition to roughness were present and uncontrolled. For devices with roughness above 0.5 nm rms, it appears that dielectric roughness becomes a dominating factor in determining mobility.

The temperature dependence of electrical properties was evaluated from 80 to 295 K. For all of the pentacene devices tested, the subthreshold swing (S) increased and the on-to-off current ratio (on/off) decreased with decreasing temperature. A plot of linear mobilities versus temperature is given in Figure 4. The mobility of the devices decreases with temperature, which is indicative of activated transport. An Arrhenius plot was used to extract activation energies (E_A) of 26, 57, and 27 meV for

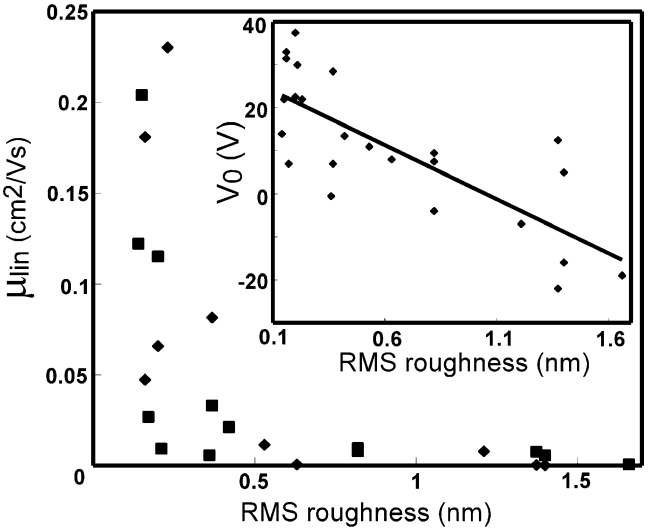

Figure 3. Plot of μ_{lin} vs rms roughness of SiO_2 dielectric. The diamonds represent pentacene TFTs deposited with a substrate temperature (T_{sub}) of 70 °C, and the squares represent $T_{sub} = 25$ °C. The inset shows the variation of onset voltage (V_0) with dielectric rms roughness for both substrate temperatures.

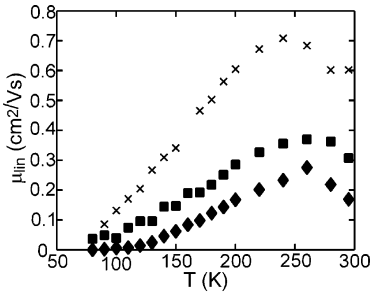

Figure 4. Plot of μ_{lin} vs T shown for samples A (squares), B (diamonds), and C (crosses).

samples A, B, and C, respectively, at $V_d = -5$ V. This trend in activation energies is consistent with a separate temperature run, using $I_d - V_g$ traces taken at $V_d = -10$ V to extract values for E_A. Calculated values of activation energies for the separate group of samples over the same temperature range were 6, 23, and 10 meV for samples of types A, B, and C, respectively. We observe a run-to-run variation of activation evergies ±10 meV; however, we do not observe the significantly higher activation energies reported elsewhere[37,38] or temperature-independent mobilities,[39] except for over a small range of high or low temperatures surrounding an activated region.[40] For sample B, we see a doubling of the activation energy in comparison to sample A and a return of the activation energy to nearly that of sample A with sample C.

It was also instructive to determine the variation in E_A over values of V_g in the linear (high V_g) region. For sample B, the range of E_A was greater than 10 meV, and for all other samples this variation was less than 5 meV (for both temperature runs). This indicates that the width of the trap distribution was also approximately doubled for the rough SiO_2 sample in comparison to the smooth SiO_2 sample and the polystyrene-treated TFT.

Figure 5 shows the variation in onset voltage (V_0) with temperature. Sample A shows a shift in V_0 to more negative

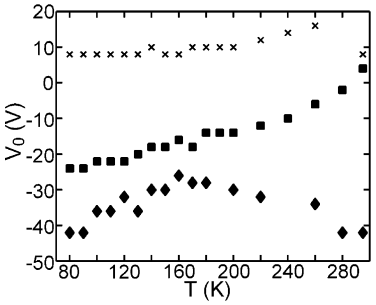

Figure 5. Plot of V_0 vs temperature for samples A (squares), B (diamonds), and C (crosses).

values with decreasing temperature, which we have observed in many separate temperature characterization runs of similar sample types. We attribute this shift to deep donor-like traps at the interface between the pentacene film and the dielectric. The polymer-treated sample, C, exhibits very little variation in V_0 with temperature, potentially indicating that very few deep traps are present. Sample B exhibits large negative V_0 values without any clear trend with decreasing temperature. This is consistent with deep donor-like traps.

Conclusion

We have demonstrated the effect of dielectric roughness on transport properties in pentacene TFTs and the ability to eliminate the detrimental roughness in order to restore desirable electrical properties. The smoothing layer procedure resulted in an order of magnitude improvement in charge mobility relative to the rough dielectric, and returned the mobility to a value comparable to that for the original smooth SiO_2. The doubling of E_A observed for the rough SiO_2 sample, in comparison to activation energies observed for both the smooth SiO_2 and the polymer-coated SiO_2, points strongly toward the important role of structural order on carrier trapping in pentacene. More work is needed to understand the correlation between surface chemistry and film morphology and the effect of dielectric roughness and surface energy on transport parameters. Further studies will include grazing incidence X-ray diffraction of pentacene/dielectric interfaces[41] to better understand the molecular ordering within the first few layers of the semiconductor where most electrical transport occurs in TFTs.

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References and Notes

(1) Drury, C. J.; Mutsaers, C. M. J.; Hart, C. M.; Matters, M.; de Leeuw, D. M. *Appl. Phys. Lett.* **1998**, *73*, 108−110.

(2) Baude, P. F.; Ender, D. A.; Haase, M. A.; Kelley, T. W.; Muyres, D. V.; Theiss, S. D. *Appl. Phys. Lett.* **2003**, *82*, 3964−3966.

(3) Klauk, H.; Gundlach, D. J.; Nichols, J. A.; Jackson, T. N. *IEEE Trans. Electron Devices* **1999**, *46*, 1258−1263.

(4) Sheraw, C. D.; Zhou, L.; Huang, J. R.; Gundlach, D. J.; Jackson, T. N.; Kane, M. G.; Hill, I. G.; Hammond, M. S.; Campi, J.; Greening, B. K.; Francl, J.; West, J. *Appl. Phys. Lett.* **2002**, *80*, 1088−1090.

(5) Mach, P.; Rodriguez, S. J.; Nortrup, R.; Wiltzius, P.; Rogers, J. A. *Appl. Phys. Lett.* **2001**, *78*, 3592−3594.

(6) Someya, T.; Katz, H. E.; Gelperin, A.; Lovinger, A. J.; Dodabalapur, A. *Appl. Phys. Lett.* **2002**, *81*, 3079−3081.

(7) Dimitrakopoulos, C. D.; Brown, A. R.; Pomp, A. *J. Appl. Phys.* **1996**, *80*, 2501−2508.

(8) Laquindanum, J. G.; Katz, H. E.; Lovinger, A. J.; Dodabalapur, A. *Chem. Mater.* **1996**, *8*, 2542−2544.

(9) Jentzsch, T.; Juepner, H. J.; Brzezinka, K. W.; Lau, A. *Thin Solid Films* **1998**, *315*, 273−280.

(10) Shtein, M.; Mapel, J.; Benziger, J. B.; Forrest, S. R. *Appl. Phys. Lett.* **2002**, *81*, 268−270.

(11) Bouchoms, I. P. M.; Schoonveld, W. A.; Vrijmoeth, J.; Klapwijk, T. M. *Synth. Met.* **1999**, *104*, 175−178.

(12) Jurchescu, O. D.; Baas, J.; Palstra, T. T. M. *Appl. Phys. Lett.* **2004**, *84*, 3061−3063.

(13) Horowitz, G.; Hajlaoui, M. E. *Adv. Mater. (Weinheim, Germany)* **2000**, *12*, 1046−1050.

(14) Knipp, D.; Murti, D. K.; Krusor, B.; Apte, R.; Jiang, L.; Lu, J. P.; Ong, B. S.; Street, R. A. *Mater. Res. Soc. Symp. Proc.* **2002**, *665*, 207−212.

(15) Lin, Y.-Y.; Gundlach, D. J.; Nelson, S. F.; Jackson, T. N. *IEEE Trans. Electron Devices* **1997**, *44*, 1325−1331.

(16) Klauk, H.; Jackson, T. N. *Solid State Technol.* **2000**, *43*, 63−64, 66−67, 72, 75−76.

(17) Lin, Y. Y.; Gundlach, D. J.; Nelson, S. F.; Jackson, T. N. *IEEE Electron Devices Lett.* **1997**, *18*, 606−608.

(18) Gundlach, D. J.; Kuo, C.-C.; Nelson, S. F.; Jackson, T. N. *IEEE 57th Device Research Conference Digest*; Santa Barbara, CA; IEEE Pub. Services: New York, 1999; pp 164−165.

(19) Klauk, H.; Halik, M.; Zschieschang, U.; Schmid, G.; Radlik, W.; Weber, W. *J. Appl. Phys.* **2002**, *92*, 5259−5263.

(20) Kelley, T. W.; Muyres, D. V.; Baude, P. F.; Smith, T. P.; Jones, T. D. *MRS Symp. Proc.* **2003**, *771*, 169−179.

(21) Salleo, A.; Chabinyc, M. L.; Yang, M. S.; Street, R. A. *Appl. Phys. Lett.* **2002**, *81*, 4383−4385.

(22) Kelley, T. W.; Boardman, L. D.; Dunbar, T. D.; Muyres, D. V.; Pellerite, M. J.; Smith, T. P. *J. Phys. Chem. B* **2003**, *107*, 5877−5881.

(23) Kobayashi, S.; Nishikawa, T.; Takenobu, T.; Mori, S.; Shimoda, T.; Mitani, T.; Shimotani, H.; Yoshimoto, N.; Ogawa, S.; Iwasa, Y. *Nat. Mater.* **2004**, *3*, 317−322.

(24) Pernstich, K. P.; Rashid, A. N.; Haas, S.; Schitter, G.; Oberhoff, D.; Goldmann, C.; Gundlach, D. J.; Batlogg, B. *Los Alamos Natl. Lab., Prepr. Arch., Condens. Matter* **2004**, 1−9, arXiv:cond-mat/0410014.

(25) Pernstich, K. P.; Goldmann, C.; Krellner, C.; Oberhoff, D.; Gundlach, D. J.; Batlogg, B. *Synth. Met.* **2004**, *146*, 325−328.

(26) Pernstich, K. P.; Haas, S.; Schitter, G.; Oberhoff, D.; Goldmann, C.; Gundlach, D. J.; Batlogg, B.; Rashid, A. N.; Schitter, G. *J. Appl. Phys.* **2004**, *96*, 6431−6438.

(27) Knipp, D.; Street, R. A.; Krusor, B. S.; Apte, R. B.; Ho, J. *Proc. SPIE−Int. Soc. Opt. Eng.* **2001**, *4466*, 8−19.

(28) Knipp, D.; Street, R. A.; Krusor, B.; Apte, R.; Ho, J. *J. Non-Cryst. Solids* **2002**, *299−302*, 1042−1046.

(29) Steudel, S.; De Vusser, S.; De Jonge, S.; Janssen, D.; Verlaak, S.; Genoe, J.; Heremans, P. *Appl. Phys. Lett.* **2004**, *85*, 4400−4402.

(30) Jin, Y.; Rang, Z.; Nathan, M. I.; Ruden, P. P.; Newman, C. R.; Frisbie, C. D. *Appl. Phys. Lett.* **2004**, *85*, 4406−4408.

(31) Laudise, R. A.; Kloc, C.; Simpkins, P. G.; Siegrist, T. *J. Cryst. Growth* **1998**, *187*, 449−454.

(32) A thorough investigation of the effects of spin coating on polymer roughness was not performed. Certain polymers, including polystyrene, typically gave very smooth layers, while other polymers were not further studied because a low roughness was not obtained.

(33) Mattheus, C. C.; Dros, A. B.; Baas, J.; Meetsma, A.; Boer, J. L. d. B.; Palstra, T. T. M. *Acta Crystallogr., Sect. C* **2001**, *C57*, 939−941.

(34) The polymorph of pentacene exhibiting a d_{001} spacing of 14.4 Å is normally termed the "bulk" phase of pentacene; however, the single-crystal structure of pentacene exhibits a d_{001} spacing of 14.1 Å. We have labeled the 14.4 Å spacing as the $d_{001'}$ spacing and the 15.4 Å spacing (most often termed the "thin film" phase) as the $d_{001''}$ spacing.

(35) Karl, N. Low Molecular Weight Organic Solids and Charge-Carrier Mobility in Organic Crystals. In *Organic Electronic Materials: Conjugated Polymers and Low Molecular Weight Organic Solids*; R. Farchioni, G. G., Ed.; Springer: New York, 2001; pp 215−239 and 283−326.

(36) Sze, S. M. *Physics of Semiconductor Devices*; John Wiley & Sons: New York, 2003.

(37) Knipp, D.; Street, R. A.; Volkel, A.; Ho, J. *J. Appl. Phys.* **2003**, *93*, 347−355.

(38) Knipp, D.; Street, R. A.; Volkel, A. R. *Appl. Phys. Lett.* **2003**, *82*, 3907−3909.

(39) Nelson, S. F.; Lin, Y. Y.; Gundlach, D. J.; Jackson, T. N. *Appl. Phys. Lett.* **1998**, *72*, 1854−1856.

(40) Pesavento, P. V.; Chesterfield, R. J.; Newman, C. R.; Frisbie, C. D. *J. Appl. Phys.* **2004**, *96*, 7312.

(41) Fritz, S. E.; Martin, S. M.; Frisbie, C. D.; Ward, M. D.; Toney, M. F. *J. Am. Chem. Soc.* **2004**, *126* (13), 4084−4085.