Design and Assembly of High-Aspect-Ratio Silica-Encapsulated Nanostructures for Nanoelectronics Applications

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Chapter 26
Design and Assembly of High-Aspect-Ratio Silica-Encapsulated Nanostructures for Nanoelectronics Applications

N.I. Kovtyukhova

Abstract This chapter summarizes our progress in design and assembly of new metal nanowire-based insulated interconnects and coaxially gated in-wire thin film transistors with the electrical characteristics closely approaching those of established large-scale planar thin film devices. Our approach relies on combining templated synthesis of nanostructures with wet successive adsorption techniques and electroplating. The strong advantages of this approach are (i) a possibility to easily incorporate various electronic materials into a single nanostructure, (ii) control of the device geometric parameters with sub-nanometer precision, and (iii) using low-energy-cost and environmentally friendly synthetic methods.

26.1 Introduction

A dramatic increase in research activity on nanoscale high-aspect-ratio inorganic structures has been motivated by their unique electronic, optical, catalytic, and mechanical properties determined by their shape, size, and, in many cases, single-crystal morphology. Among those, nanowires and nanotubes have received major attention as potential components of electronic circuits [1–5], photovoltaic cells [6–8], chemical and biological sensors [9, 10], battery anodes [11] and, very recently, nanomotors [12–14] and nanolocomotives [15, 16].

The chemical assembly of nanowires is now considered a potentially viable alternative to the conventional lithographic fabrication of nanoscale circuits, which is increasingly approaching physical and economic limits [1, 17, 18]. As high-aspect-ratio structures, nanowires and nanotubes appear to be ideal building blocks in chemically assembled electronic and optoelectronic nanotechnology. Their

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nanometer-size diameters and micron-size length allow for the fabrication of compact arrays of well-aligned parallel devices. Deposition of such an array on a lithographically pre-patterned substrate can be used to prepare planar ultradense electronic circuits composed of individually addressable device elements [19, 20]. Impressively, $\sim 10^{11}$ cross-point junctions can be fabricated on an area of 1 cm^2 [20]. Chemically grown arrays of vertically aligned parallel wires and tubes have been explored as 3D electron-harvesting and transport structures in solar cells [8], field emission displays [21], and multiple sensor arrays [9].

While most of this research has involved semiconductor nanowires and single-walled carbon nanotubes (SWNTs), functionalized metal nanowires have also been actively studied for this application [5, 20, 22–26]. Metal nanowires provide reliable control over physical dimensions, surface chemistry, and transport properties and can be easily prepared [27] and functionalized by low-temperature techniques [5, 22–26].

Our approach to electronically functional metal nanowires relies upon wet chemical assembly of established ultrathin film devices [6, 28] and their shaping into nanowire-based structures. This can be achieved by performing chemical and electrochemical synthesis inside the cylindrical pores of a template membrane. By exploiting surface chemistry of the metal wire and pore walls, the electroactive films can be deposited between two metal wire segments and/or around the wire body. The precise control over the film thickness is realized using successive adsorption techniques, such as layer-by-layer [23] or surface sol–gel deposition (SSG) [24, 25, 29, 30].

An important advantage of this strategy is a possibility to easily combine components with different electronic and chemical properties (such as metals, semiconductors, polymers, short SWNTs, and insulating oxides) in a single-wire structure. Multicomponent "all-in-wire" diodes [23, 26], transistors [25], photodetectors [31], and sensors [32] can be prepared in this way.

Additionally, the approach described here fulfills the requirements of future electronic applications particularly well because it (i) provides technologically simple preparation of a large number ($\sim 10^9$ per membrane) of relatively uniform nanowire devices with precise control over their geometric parameters and (ii) uses low-energy-cost and environmental friendly "green" synthetic methods.

Highly conductive metals offer some special advantages, particularly as low-resistance interconnects in high-speed circuits. A further reduction in RC (resistance–capacitance) and LC (inductance−capacitance) time constants for nanoscale circuits can be expected if low dielectric constant (low-k) materials can be introduced as insulating spacers between metallic nanowires [33]. For example, copper/low-k interconnect is currently a growing choice for high-performance chips [34]. Silicon dioxide is the relatively low-k dielectric material that is most widely used in CMOS integrated-circuit technology. Incorporation of SiO_2 into metal wire-based device structures requires new techniques for making ultrathin silica nanotubes of high quality with the thickness control at the sub-nanometer level.

This chapter summarizes our progress in design and assembly of ultrathin silica nanotubes, SiO_2-insulated metal nanowire interconnects, and coaxially gated in-wire thin film transistors with the electrical characteristics closely approaching

those of established large-scale planar thin film devices. We combine templated SSG synthesis of silica nanotubes on the pore walls of anodic aluminum oxide (AAO) membranes with electroplating of metal or composite metal–semiconductor−metal wire inside the tubes.

26.2 Template-Assisted Surface Sol–Gel Synthesis of SiO_2 Nanotubes

Replication of cylindrical pores of AAO membranes using deposition techniques, either vapor or liquid phase, developed for planar thin films has now widely been used to prepare oxide nanotubes of different compositions (see for recent review [8]). Conventional sol–gel methods, which involve immersing an AAO membrane in a precursor sol followed by gelation inside the pores, allow to adjust internal nanotube diameter by varying concentration and viscosity of the initial sol as well as the immersion times [35, 36]. However, by the beginning of this research, precise control over tube thickness and morphology, especially when the tube is only a few nanometers thick, has not been demonstrated yet.

More reliable control over the quality of planar thin films has been realized in layer-by-layer deposition methods, in which (i) preformed colloidal particles [37, 38] or (ii) molecular precursors [29, 30, 39] are successively adsorbed as a layer at a time onto the growing surface. Recently we demonstrated applicability of the first layer-by-layer technique to membrane substrates by preparing uniform and smooth free-standing semiconductor/polymer nanotubes and coated metal wires [23].

The second, SSG method, involves repeats of two-step deposition cycles, in which the adsorption of a molecular precursor and the hydrolysis (in the case of oxide film growth) steps are separated by a post-adsorption wash. The washing step desorbs weakly bound molecules that form additional layers [29]. Ideally, the SSG technique can limit each adsorption cycle to a single monolayer; however in practice, thicker layers have been found for planar oxide SSG films [29, 30]. Nevertheless, SSG allows very fine control over film thickness because a nanometer- or sub-nanometer-thick layer is grown in each two-step adsorption–hydrolysis cycle.

Here we describe growth of silica nanotubes on the pore walls of AAO membranes using the SSG technique. To understand the dynamics of tube growth, the process has been monitored by TEM and SiO_2 mass uptake measurements. The synthetic protocol is depicted schematically in Fig. 26.1, route 1 (for details see [24]). In the first step, $SiCl_4$ molecules are adsorbed on the hydrated surface of the alumina membrane. Subsequent washing with CCl_4 removes the unbound adsorbate molecules from the pores. In the second step, the adsorbed $SiCl_4$ is hydrolyzed to give SiO_2. Free-standing nanotubes were obtained by etching the alumina membranes in 50% H_2SO_4. Energy-dispersive X-ray (EDX) analysis of the product showed Si and O, with no detectable (< 0.5%) Cl or Al. Hence the conversion of $SiCl_4$ to silica is complete, and no aluminosilicate phase is present. This allows us to describe the chemical composition of the oxide as $(SiO_2)_x(SiOH)_y$.

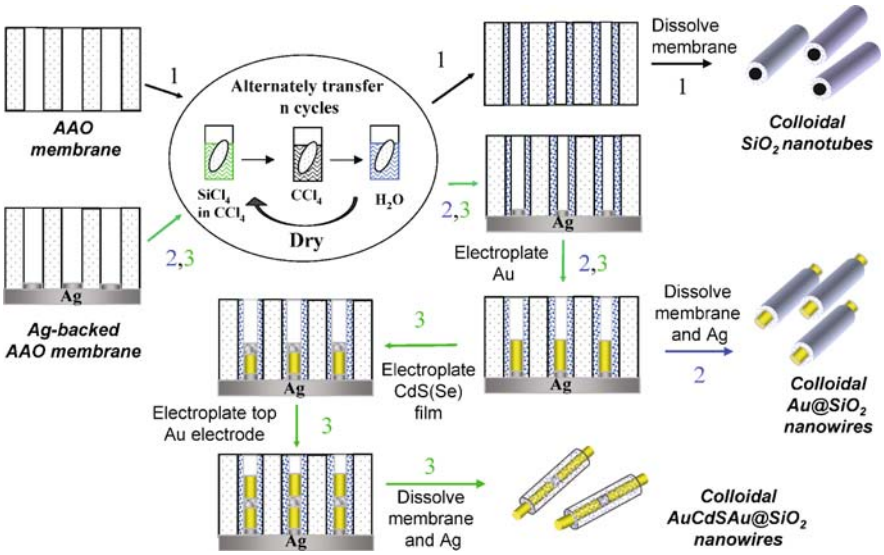

Fig. 26.1 Scheme of the template SSG synthesis of (*1*) SiO_2 nanotubes, (*2*) SiO_2-tube-encapsulated Au nanowires, and (*3*) coaxially gated in-wire thin film transistors. Commercial (Whatman Anodisc 25) and home-made AAO membranes can be used. Currently, AAO membranes with pore size in the range of 15–350 nm are available; however, scaling down to 15–50 nm pores will require longer SSG steps

TEM images (Fig. 26.2a, b) show robust SiO_2 nanotubes with smooth and uniform walls. Their shape clearly replicates the pore structure of AAO, including branches. Tubes 20–30 μm long can be found in optical micrographs (not shown) implying the growth of continuous tubules along the pore length. Figure 26.2a illustrates the remarkably high flexibility of these long silica nanotubes. A 100 nm diameter tube grown in five deposition cycles does not break even when bent at right angles. The external diameter of the tubes is determined by the pore diameter, and their internal diameter is adjustable by varying the number of deposition cycles and/or the concentration of $SiCl_4$. Nanotubes with external diameters ranging from 40 to 300 nm, and with wall thicknesses from 2 to 30 nm, were prepared.

The dependence of the nanotube wall thickness (which was estimated from TEM images of metal-filled nanotubes (Fig. 26.2c, d)) on the number of the deposition cycles is shown in Fig. 26.3a, trace 1. The graph is not linear: the amount of SiO_2 deposited per cycle increases gradually as the tubes are grown. For example, under the conditions shown in Fig. 26.3a, trace 1, the thickness change per cycle increases from 8.7 Å in the 4th–10th cycles to 15.3 Å in the 10th–20th cycles. Both values exceed the film thickness increase (~3 Å) expected if only one Si−O−H monolayer is added per cycle. The shape of this film thickness graph closely resembles that of the mass uptake of SiO_2 (Fig. 26.3a, trace 2). This correlation allows one to follow the process of nanotube growth by simply weighing the dry membrane after each SSG cycle.

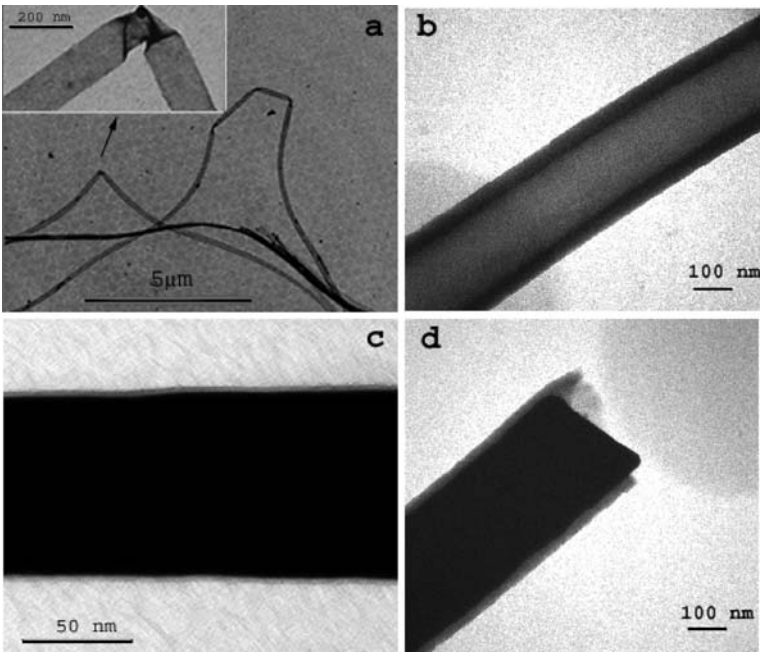

Fig. 26.2 TEM images of (**a, b**) SiO_2 nanotubes and (**c, d**) Au wires grown inside the SiO_2 nanotubes. (**a, c**) Five deposition cycles in 90 ± 20 nm diameter pores; (**b, d**) 20 deposition cycles in 280 ± 20 nm diameter pores. Reprinted with permission from [24]. Copyright 2003 Wiley-VCH Verlag GmbH & Co

The film growth at different $SiCl_4$ concentrations is shown in Fig. 26.3b. At any $SiCl_4$ concentration, a steep rise is observed in the first deposition cycle. After this, the film growth slows down significantly but the amount of SiO_2 deposited per cycle gradually increases. Ferguson and coworkers [38] attributed upward curvature in layer-by-layer growth of clay films to island nucleation and growth; however, this model is not consistent with the smooth morphology of SSG silica films seen in the TEM images.

Another possibility is that the upward curvature arises from occlusion of water in the growing film. Water is always present as a surface layer on hydrophilic surfaces under ambient conditions. The extent to which this surface-bound water will result in multilayer deposition depends on the amount of water present, the extent to which H_2O and CCl_4 molecules compete for interaction with $SiCl_4$, and the permeability of the deposited $[SiOCl_x(OH)_y]_n$ film to water, $SiCl_4$, and CCl_4. The coexistence of these three factors may cause the complex character of graphs shown in Fig. 26.3b, c. The fact that multiple layers of SiO_2 are grown in each cycle indicates that at high concentration, a multilayer of $SiCl_4$ molecules is present in the adsorption layer. In the subsequent washing step with CCl_4, all unreacted (unbound) $SiCl_4$ is removed. The following SSG step (immersion in water) completes hydrolysis of any remaining Si−Cl bonds and restores the water surface layer.

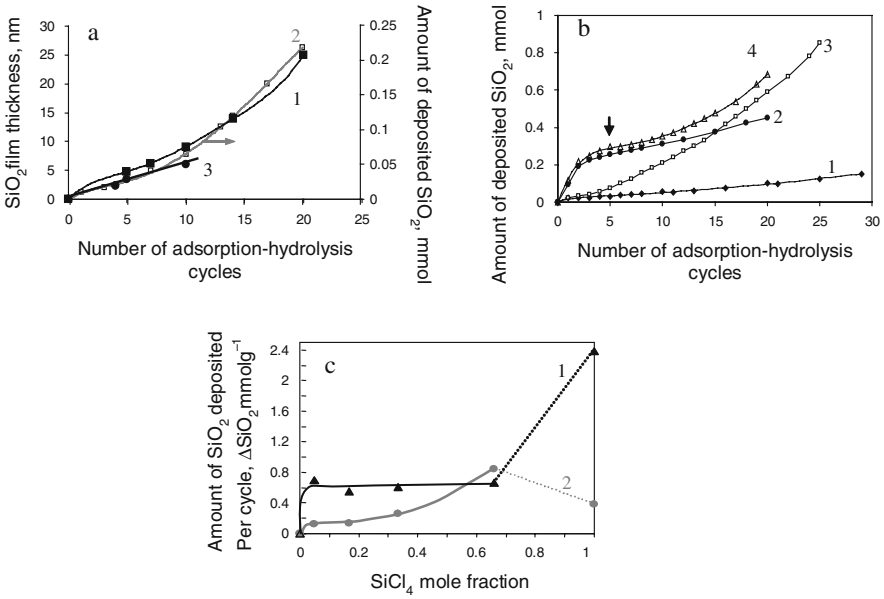

Fig. 26.3 **(a)** Plots of SiO_2 wall thickness (*1*, *3*) and amount of SiO_2deposited (*2*) from a 67 mol% solution of $SiCl_4$ versus the number of deposition cycles: pore diameter (*1*, *2*) 280 ± 20 nm and (*3*) 90 ± 20 nm. **(b)** Amount of SiO_2 deposited versus the number of deposition cycles for different concentrations of $SiCl_4$ in CCl_4: (*1*) 5 mol%; (*2*) 100 mol%; (*3*) 67 mol%; (*4*) 100% $SiCl_4$ was used in the first 5 cycles and 67% $SiCl_4$ was used in the next 15 cycles; *arrow* shows the point where the concentration was changed. Pore diameter 280 ± 20 nm. **(c)** Amount of SiO_2 deposited per cycle on (*1*) alumina and (*2*) silica-covered membrane surface versus $SiCl_4$ mole fraction. Pore diameter 280 ± 20 nm, bare membrane weight $0.033 \pm 2\%$, g. Reprinted with permission from [24]. Copyright 2003 Wiley-VCH Verlag GmbH & Co

We suggest that the amount of SiO_2 deposited in each SSG cycle is mainly determined by the amount of $SiCl_4$ adsorbed in the first step rather than by the hydrolysis step. In this case, a plot of SiO_2 amount deposited per cycle (ΔSiO_2) versus $SiCl_4$ mole fraction can be considered as a qualitative analogue of a $SiCl_4$ adsorption isotherm. Figure 26.3c, traces 1 and 2 shows two such plots taken (1) for the first deposition cycle and (2) as an average for the range of 5th−10th cycles, in which SiO_2 deposition is linear for all concentrations. The first isotherm (Fig. 26.3c, trace 1) characterizes $SiCl_4$ adsorption on the alumina surface while the second one (Fig. 26.3c, trace 2) is related to silica surface adsorption since, according to the TEM data, the pore walls are completely covered with SSG film after five cycles. The low concentration region of both plots is concave to the concentration axis, which is characteristic of strong interaction between surface and adsorbate [40], and is consistent with the chemical reaction of $SiCl_4$ with H_2O-covered alumina and silica surfaces. It is evident from the low concentration region of the plots that the $SiCl_4$ interaction with the alumina/H_2O surface is stronger.

Further flow of the adsorption isotherms for alumina and silica surfaces is different. On the silica/H_2O surface, the amount of SiO_2 deposited, as expected, increases gradually with the $SiCl_4$ mole fraction. However, on the alumina surface, the plot has a long plateau parallel to the concentration axis. We suggest that in the $SiCl_4$ mole fraction range of 0.05−0.67, fast formation of the $[SiOCl_x(OH)_y]_n$ layer at the alumina/H_2O//($SiCl_4 + CCl_4$) interface occurs, and this layer is dense enough to block further penetration of $SiCl_4$ through the film. An increase in adsorption on the alumina surface is observed when the $SiCl_4$ mole fraction equals 1. Apparently, in the absence of CCl_4 the hydrolysis reaction can continue until all water in the surface layer is consumed and replaced by the $[SiOCl_x(OH)_y]_n$ layer. Hence the amount of water available for hydrolysis of $SiCl_4$ determines its adsorption value. The fact that film growth is faster on the alumina pore walls (Fig. 26.3c, trace 1) than it is on several layers of the SSG film (Fig. 26.3c, trace 2) is consistent with the idea that the more polar alumina surface retains more water. Interestingly, in the plot of film grown on the silica/H_2O surface, a higher adsorption value is found at the $SiCl_4$ mole fraction of 0.67 than at that of 1 (Fig. 26.3c, trace 2).

Heat-treatment (100 °C, 3–13 h) of SiO_2-containing membranes dried at ambient temperature in Ar results in a weight loss of ∼ 4%, which can be ascribed to the removal of unbound water from the SiO_2 film. This indicates that the SiO_2 film is relatively porous, and pore fraction is estimated at ∼0.09 taking SiO_2 density at 2.17 g cm^{-3} [41]. This porosity is associated with relatively large pores and does not include micropores (if any) with radii approaching the thickness of an adsorbed water layer, because water in those pores can only be removed at higher temperatures. The porous structure of the SiO_2 film is consistent with the idea of occluded water assisting in multilayer film growth and is likely to be responsible for the gradual increase in the amount of SiO_2 deposited per cycle (Fig. 26.3a, b) rather than narrowing the pores during the SSG procedure. The tube growth inside the 90 nm wide pores is not found to be faster than that inside the 280 nm wide pores (Fig. 26.3a, traces 1, 3).

The same percent weight loss is observed for initial $SiCl_4$ concentrations of 5, 16, 33, and 100 mol%, while for 67 mol% $SiCl_4$ solution, the weight loss is 5.6% after 10th and 10% after 20th deposition cycle. Accordingly, estimated porosity is 0.126 for the SiO_2 film deposited in 10 cycles and it increases to 0.225 during the next 10 cycles. The porosity of the SiO_2 film measured under different growth conditions is consistent with the data shown in Fig. 26.3. In a 100% $SiCl_4$ solution the layer growth is actually slower than it is at 67 mol% $SiCl_4$ (Fig. 26.3b, traces 2, 3). The 100 mol% solution gives lower film porosity (0.09 after 5 deposition cycles), but upward curvature in film growth is found (Fig. 26.3b, trace 4) if the concentration is lowered to 67 mol%, which provides higher porosity (0.144 after 15 cycles). These facts suggest that, at relatively low CCl_4 concentration, thicker and poorer ordered $[SiOCl_x(OH)_y]_n$ layers, which may occlude both H_2O and CCl_4 molecules, are formed at the adsorption step of SSG cycles. Thus by an appropriate selection of synthesis conditions, one can control not only the thickness of nanotube walls, but also their porosity.

26.3 SiO_2-Insulated Metal Interconnects

While still in the membrane, the SiO_2-coated pores can be electrochemically filled with metal followed by membrane etching to give free-standing insulated wires (Fig. 26.1, route 2; for details on synthesis and electrical measurements see [24]).

Typical TEM images (Fig. 26.2c, d) show the gold wires inside uniformly thick and smooth silica tubes. The tube walls remain defect-free and no metal penetration of the walls is seen. The top ends of the wires are typically flat or convex, unlike nanowires grown in unmodified alumina membranes, which have cup-shaped ends. This cup-like shape has been explained as a consequence of the high surface tension of the alumina pore walls [23b]. The interaction of gold with the less polar silica pores is apparently weaker. The coulombic efficiency for plating Au and Ni wires is about 1.2 times higher (judging from wire lengths) in silica-modified pores than it is in unmodified anodic alumina.

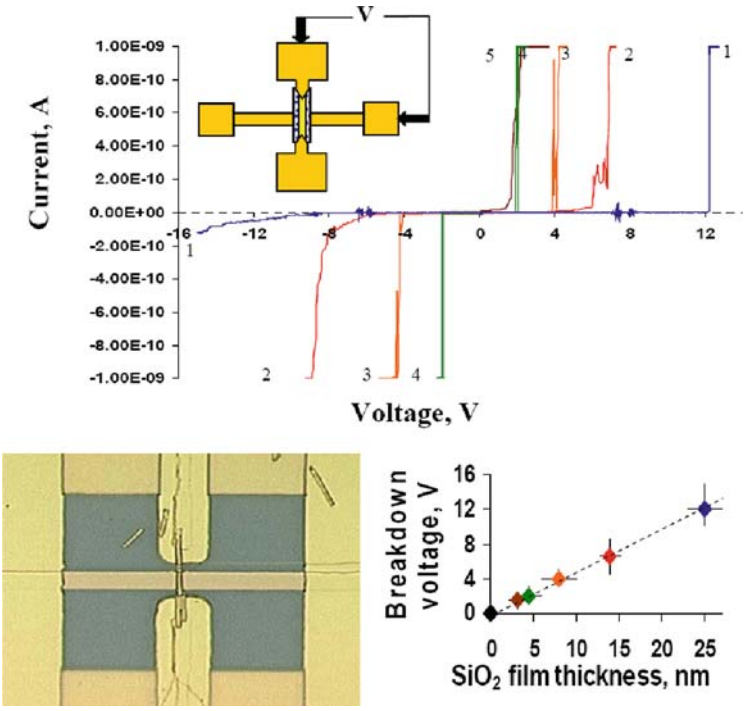

Fig. 26.4 *Top*: *I*–*V* characteristics of SiO_2-coated gold nanowires with different thickness of SiO_2 (nm): (*1*) 25, (*2*) 14, (*3*) 8, (*4*) 4.5, (*5*) 3.5. A scheme of a test structure for measuring the electrical properties is shown in the *inset*. *Bottom*: Optical micrograph of a test structure for measuring the electrical properties of SiO_2-coated gold nanowires (*left*). A plot of the breakdown voltage versus thickness (*right*). Reprinted with permission from [24]. Copyright 2003 Wiley-VCH Verlag GmbH & Co

When the silica-coated nanowires are released from the membrane, both ends are open, because the tube-shells break near the ends of the metal wire (Fig. 26.2d). This allows one to make electrical contact by evaporating metal onto the wire ends.

The $I-V$ characteristics of SSG SiO_2 films of different thicknesses (measured in Au@SiO_2/Au configuration) are shown in Fig. 26.4 (top). The curves show typical insulating behavior with breakdown voltages that increase linearly with film thickness (Fig. 26.4, bottom). The hard breakdown field is estimated at 4.8 MV cm^{-1}, which is only slightly less than the breakdown fields (10–15 MV cm^{-1}) of the SiO_2 dielectric used in CMOS integrated-circuit technology.

Because the SiO_2 tubes are porous, their dielectric constant is expected to be lower than that of dense silica ($\varepsilon = 3.8$ [10]). Porous silica is a promising dielectric material for nanoelectronics applications because of its relatively low dielectric constant [42]. Theoretical calculations predict a dielectric constant of 1.8–2.8 for a volume pore fraction of 0.4 and an almost linear decrease in ε with increasing porosity. In our experiments, it was difficult to measure the dielectric constant of the SiO_2 films precisely because of the uncertainty in the contact area in the Au@SiO_2/Au configuration. Nevertheless it is interesting to note that the synthesis offers some control over porosity, and that this will probably be reflected in the dielectric constant of the films.

26.4 Coaxially Gated In-Wire Thin Film Transistors

On the way toward realization of nano- and molecular-scale electronics, the development of strategies for promoting single devices to the level of integrated circuits is the key issue [17, 43–46]. In particular, for the realization of transistor circuits, each component transistor is required to give sufficient signal amplification and to be controlled by its own gate contact [17, 44–46]. Departing from this point, several approaches have been proposed to assembling logic circuits and nonvolatile memory from carbon nanotube [44] and semiconductor nanowire [45–47] building blocks. In the latter case, field-effect transistors (FETs) have been fabricated from cross-point nanowire junctions [45] or core-multishell nanowire structures [46], and the crossing nanowire or metal contact evaporated on the outer shell, respectively, have been used as the local gate contacts. The important advantage of the multishell-nanowire-based FETs lies in fact that they are by definition coaxially gated transistors, and in this implement a strategy of "wrap-around gate" projected for advancing conventional silicon transistors [1, 48, 49].

This chapter demonstrates the applicability of a "wrap-around gate" approach to nanoscale thin film transistors (TFTs). We describe the synthesis and characterization of coaxially gated in-wire TFTs. These devices consist of a cadmium chalcogenide thin film sandwiched between metal wire segments within a SiO_2 tube. The synthesis involves the above-described SSG deposition of SiO_2 tubes on the pore walls of an AAO membrane [24] and electroplating the composite nanowires within the tubes [31]. This approach is technologically simple and scalable with precise control over the diameter, segment lengths, and dielectric thickness. Two other

important advantages of the coaxially gated in-wire TFT structure are full encapsulation of the semiconductor segment, which prevents its oxidation, and possibility to use metal gate electrodes, which are compatible with a variety of gate dielectrics [1].

In-wire TFTs were prepared as shown in Fig. 26.1, route 3. First, the Ag-backed AAO membrane is subjected to deposition of SiO_2 nanotubes on the pore walls by repeating $SiCl_4$ adsorption–hydrolysis cycles [24]. The membrane is then used as the cathode in an electrochemical cell to electroplate 3–5 μm long Au segments inside the SiO_2 tubes. Semiconductor thin film segments are grown on the tip of the Au wire using electrochemically induced CdS film growth [50, 51] or cyclic voltametric CdSe deposition [31]. Top Au segments 3–5 μm long are electroplated onto the cadmium chalcogenide films. Finally, the Au/CdS(Se)/Au@$(SiO_2)_n$ (where n is the number of SSG cycles used for SiO_2–tube growth) nanowires are released by dissolving the Ag backing and AAO membrane. Metal/CdS/metal nanowires with different semiconductor segment lengths are prepared using 1 h and 15 min deposition times. In the latter case Ag clusters were chemically deposited prior to electrodeposition of the top metal segment in order to ensure good electrical contact. These devices are referred to as Au/CdS/Au@$(SiO_2)_{10}$ and Au/CdS/AgAu@$(SiO_2)_{14}$, respectively.

An optical micrograph and TEM images of the in-wire TFT structures are shown in Fig. 26.5a−c. The Au/CdS/Au junctions are clearly seen, and their thickness

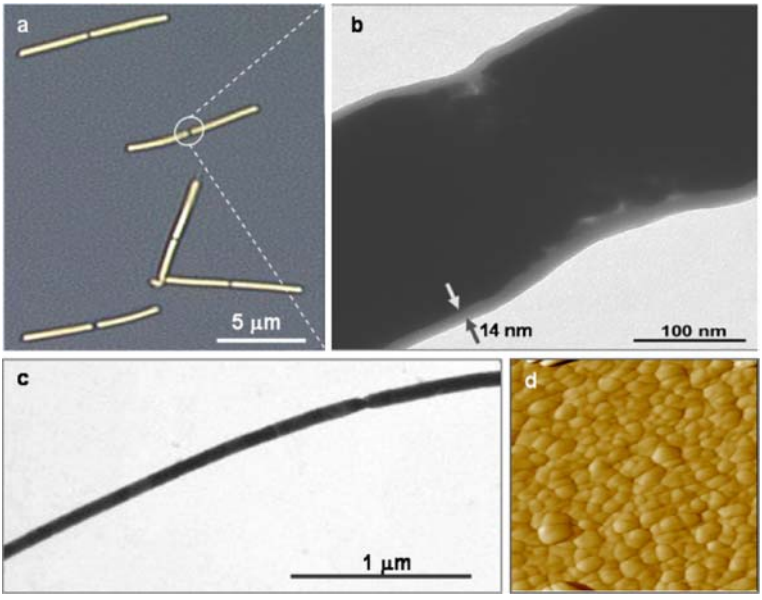

Fig. 26.5 Optical micrograph **(a)** and TEM images **(b, c)** of Au/CdS/Au@$(SiO_2)_{10}$ nanowires prepared in AAO membranes with pore size 280±20 nm (**a**, **b**) and 70±10 nm (**c**). (**d**) Tapping mode AFM image (585 × 585 nm, Z range 30.0°) of CdS film prepared on an Au-coated glass substrate using electrochemically induced deposition technique. Reprinted with permission from [25]. Copyright 2004 the American Chemical Society

can be roughly estimated at 100–200 nm for the wires prepared by using 1 h CdS deposition.

For the 15 min CdS deposition, TEM images show an approximate CdS film thickness at 30–50 nm. An AFM image of a 31 nm thick CdS film prepared the same way on a planar Au substrate shows densely packed 20–50 nm grains. An XRD pattern of the planar CdS film (not shown) shows one CdS-related peak at $2\Theta = 26.65^{o}$ ($d = 3.34$Å), the position of which corresponds to the (111) reflection of the cubic zinc blend structure ($d = 3.36$ Å) or the (002) reflection of the hexagonal wurzite structure ($d = 3.36$Å). However, the absence of other strong peaks from (100) and (101) planes of the hexagonal phase indicates that CdS crystallizes mainly in the cubic phase, in contrast to the hexagonal phase formed on ITO and SnO_2 substrates [50]. The average crystal size estimated from the X-ray line widths is 39.6 nm, which is consistent with the AFM data.

The thickness of the SiO_2 tubes that encapsulate the nanowires is uniform along the wire length and ranges from 12 to 14 nm for 10 SSG cycles (Fig. 26.5b) and from 16 to 18 nm for 14 SSG cycles. The flexibility of these shells allows them to precisely follow the shape of Au/CdS/Au junctions (Fig. 26.5b) thus enabling good adhesion of the gate dielectric to the semiconductor film.

The nanowires were aligned as shown in Fig. 26.6a for electrical measurements. $I_{DS}-V_{DS}$ characteristics of Au/CdS/Au@$(SiO_2)_{10}$ and Au/CdS/AgAu@$(SiO_2)_{14}$ devices are shown in Fig. 26.6b, c. At zero gate bias ($V_{GS} = 0$), turn-on potentials are -0.6 and -0.2 V, respectively, which is in reasonable agreement with the differences between the electron affinity of CdS (~4.5 eV) and the Au (~5.2 eV) and Ag (~4.7 eV) work functions, respectively. The Au/CdS/AgAu@$(SiO_2)_{14}$ devices show a zero gate bias DS resistivity 55 times lower than Au/CdS/Au@$(SiO_2)_{10}$, which may be attributed to better CdS/Ag electrical contact due to the formation of Ag−S bonds, and possibly to fewer grain boundaries in the thinner CdS film. However, the metal/semiconductor contacts of the in-wire TFTs are still much more resistive than those of planar TFTs [52, 53]. This implies a stronger effect of the contact resistance on the nanowire device properties. Therefore, all characteristics described below result from a field effect on both the CdS channel and Au(Ag)/CdS contacts.

The $I_{DS}-V_{DS}$ characteristics of both devices clearly show a field effect, which is more pronounced at negative drain voltage (Fig. 26.6b, c). At $V_{DS} = -2$ V, the Au/CdS/Au@$(SiO_2)_{10}$ devices have an ON/OFF current ratio of 10^3, a threshold voltage of 2.4 V, and a sub-threshold slope of 2.2 V per decade (Fig. 26.6d, gr. 1, 3). The Au/CdS/AgAu@$(SiO_2)_{14}$ devices show similar parameters at $V_{DS} = -0.2$ V and a gate sweep from 0 to 10 V. While the in-wire TFTs can operate at relatively low drain voltages, the above parameters are superior to those found with planar CdS [52] and nanocrystal-derived CdSe [53a]. TFTs in the gate voltage range from ±9 to10V. The lower V_T and a threefold decrease in the sub-threshold slope (S) relative to planar nanocrystal-derived CdSe TFTs (S 7−10 V per decade [53a]) may result from the thinner dielectric layer and coaxial gating. A similar tendency was predicted for planar double-gated versus conventional FETs [48].

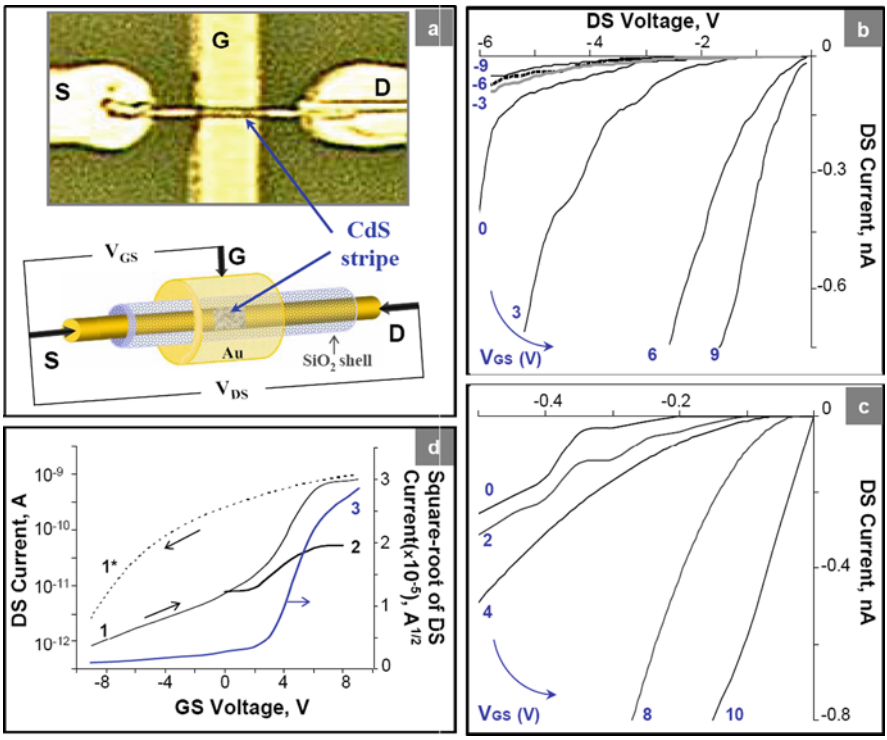

Fig. 26.6 **(a)** An optical micrograph and schematic presentation of the test structure and Au/CdS/Au@$(SiO_2)_{10}$ nanowire aligned for measuring the electrical properties. Letters *S*, *D*, and *G* indicate source, drain, and gate electrodes, respectively; (**b, c**) $I_{DS}-V_{DS}$ characteristics of in-wire TFTs for different values of gate voltage (V_{GS}): (**b**) Au/CdS/Au@$(SiO_2)_{10}$//Au (CdS deposition for 1 h); (**c**) Au/CdS/AgAu@$(SiO_2)_{14}$//Au (CdS deposition for 15 min). Gate leakage currents were in the range of 10^{-14}–10^{-12} A.; (**d**) $I_{DS}-V_{GS}$ characteristics of in-wire TFTs: Log I_{DS} (*1*, *1**) and $\sqrt{I_{DS}}$ (*3*) for Au/CdS/Au@$(SiO_2)_{10}$//Au at $V_{DS} = -2$ V for a gate sweep from −9 to 9 V (*1*) and vice versa (*1**); (*2*) Log I_{DS} for Au/CdSe/Au@$(SiO_2)_{14}$//Au at $V_{DS} = 5$ V for a gate sweep from 0 to 8 V. All measurements were performed in air at ambient temperature with a HP 4156B Precision Semiconductor Parameter Analyzer. Compliance current was set up at 1 nA. The TFTs were prepared using commercial AAO membranes with pore size 280 ± 20 nm. Reprinted with permission from [25]. Copyright 2004 the American Chemical Society

On the other hand, the channel mobility of the in-wire TFTs is approximately $5 \pm 2 \times 10^{-5}$ $cm^2\,V^{-1}s^{-1}$. This is 4–6 orders of magnitude lower than that found for TFTs with several micron long channels of planar nanocrystal-derived and vapor-deposited CdSe and CdS [13, 14]. To a certain extent, this decrease may be caused by the significant reduction of the channel length in the in-wire TFTs. The field-dependent mobility decrease is a predicted consequence of FET channel scaling [48, 54]. However, high Schottky contact resistance is most likely responsible for the low apparent mobility values. We believe that much higher mobility values can be achieved by further improving the metal/semiconductor interfaces and grain

structure of the semiconductor segment, as well as by using metal contacts with lower work function. Au/CdSe/Au@$(SiO_2)_{14}$ TFTs show poorer performance with an ON/OFF current ratio about 10 (Fig. 26.6d, gr. 2). This is consistent with observation by other groups [53] that planar CdSe TFTs fabricated without annealing exhibit very weak, if any, field effect.

Log $(I_{DS})-V_{GS}$ graphs with a gate sweep from -9 to 9 V and vice versa (Fig. 26.3d, gr. 1, 1*) show CCW hysteresis contrary to the CW one observed with planar CdSe TFTs [53]. The origin of the hysteresis is not currently understood but may be tentatively ascribed to trap states at the semiconductor/SiO_2 interface [53]. However, the chemical nature of the traps in our wet-assembled in-wire devices may differ from that in the thermally evaporated or annealed planar TFTs. Also a field effect on the Au/CdS contact properties may cause the CCW hysteresis. Oxidation of the planar TFTs [53a] is a less likely source of trap states in this case because the in-wire TFTs are encapsulated by SiO_2.

26.5 Conclusions

The surface sol–gel method is a simple way to prepare robust and flexible silica nanotubes. The thickness and porosity of the tubes can be precisely controlled by varying the composition of the precursor solution and the number of adsorption–hydrolysis cycles. The thickness of the SiO_2 layer deposited in each cycle, which always exceeds that of a monomolecular layer, can be explained assuming occlusion of water present as a surface layer. Free-standing SiO_2nanotubes with 2–30 nm walls, which are smooth and uniform along their length, were grown and characterized.

The SSG thin film deposition technique is well developed for other classes of materials, including metal oxides, chalcogenides, and phosphates. When performed in porous templates, as we have demonstrated here for SiO_2, the SSG method should offer a route to concentric multicomponent structures with well-controlled layer thickness and, presumably, tunable electrical and optical properties. The good control in film thickness that is obtained by SSG suggests that it should also be possible to precisely adjust the internal diameter of the AAO pores, and hence the diameter of nanowire replicas.

Electroplating metals inside the silica-coated pores of an AAO membrane is an easy route to nanoscale insulated metal interconnects of high quality. The hard breakdown field obtained for insulating SiO_2-nanotube coating on gold nanowires is only slightly lower than that of SiO_2 dielectric used in CMOS integrated circuits, and this is a surprising result given the fact that a wet chemical deposition method was used.

Coaxially gated in-wire thin film transistors can be made by using a combination of the templated SSG technique and electrochemical deposition of composite nanowires. The CdS-based TFTs can operate at drain voltages lower than 1 V and show better ON/OFF current ratio, threshold voltage, and sub-threshold slope than chemically similar planar TFTs. While the devices described here were not

optimized for performance, one might expect significant improvements by using strategies that have been developed or predicted for conventional FETs and TFTs [48, 52, 54]. The control of dimensions afforded by the template synthesis should make it possible to reduce the gate dielectric thickness, channel length, and diameter of the semiconductor body (see, e.g., Fig. 26.5c). The latter would extend the gate effect across the body region [48] and might also result in the formation of single-crystal semiconductor segments [51]. The SSG technique can be easily extended to other metal oxides that will allow substitution of higher *k* dielectrics, such as zirconium, titanium, and tantalum oxides for SiO_2 [29]. Finally, thermal annealing of the semiconductor segment prior to top electrode deposition is expected to improve the performance of the CdSe-based devices.

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