Nuclear Instruments and Methods in Physics Research A 629 (2011) 66–73

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Spark protection layers for CMOS pixel anode chips in MPGDs

Y. Bilevych [a], V.M. Blanco Carballo [a,b], M. Chefdeville [a,1], P. Colas [c], E. Delagnes [c], M. Fransen [a], H. van der Graaf [a,*], W.J.C. Koppert [a], J. Melai [b], C. Salm [b], J. Schmitz [b], J. Timmermans [a], N. Wyrsch [d]

[a] Nikhef, Science Park 105, 1098 XG Amsterdam, The Netherlands
[b] University of Twente/Mesa+Institute for Nanotechnology, Hogekamp 3214, 7500 AE Enschede, The Netherlands
[c] Irfu, CEA Saclay, F91191 Gif sur Yvette Cedex, France
[d] Ecole Polytechnique Fédérale de Lausanne (EPFL), Institute of Microengineering (IMT), Breguet 2, CH-2000 Neuchâtel, Switzerland

ARTICLE INFO

Article history:
Received 23 July 2010
Received in revised form
26 November 2010
Accepted 29 November 2010
Available online 8 December 2010

Keywords:
MPGD
Micromegas
Pixel readout
Amorphous silicon
Silicon nitride
Timepix
CMOS post-processing
Microsystems
Above IC
Radiation detectors
Discharges
Sparks

ABSTRACT

In this work we have investigated the functioning of high resistivity amorphous silicon and silicon-rich nitride layers as a protection against discharges in Micro-Patterned Gaseous Detectors (MPGDs). When the anode is protected by a high resistivity layer, discharge signals are limited in charge. A signal reduction is expected when the layers are too thick; simulations presented in this paper indicate that layers up to 10 μm thick can be applied without significantly degrading the detector performance. Layers of amorphous silicon and silicon-rich nitride have been deposited on top of Timepix and Medipix2 chips in GridPix detectors; with this, chips survive naturally occurring as well as intentionally produced discharges.

1. Introduction

A common problem associated with gas-filled proportional chambers is sparking. A spark or discharge is the development of a conductive and self-sustained plasma between two electrodes. Sparks are initiated by streamer formation [1].

Streamers are triggered in the presence of high electric fields when the space-charge distribution in the head and tail of the avalanche increases locally the electric field. In these conditions, photoelectrons are created outside the avalanche. These electrons contribute to the after pulsing avalanche and maintain the streamer expansion at the back side of the streamer. When the streamer connects the anode and cathode a spark may occur [2,3].

The physical origin of the discharges may depend on highly ionizing particles, high particle rate or other processes such as photon feedback, corona discharges or avalanche gain fluctuations [4]. All these mechanisms point to the same generally accepted physical picture—when the total charge density in an avalanche becomes higher than 10^7–10^8 electron–ion pairs (known as the Raether limit [5,6]) the avalanche may evolve into a discharge.

Normally the discharge is terminated when the spark current leads to a reduction in the electric field. The drop in the electric field leads to a local gain reduction. This self-quenching is observed in most gaseous detectors with the electrodes connected to the high voltage supply via a ~1 MΩ resistor. More details can be found in Ref. [6].

Due to the discharges, electrodes in the detector may get damaged (partially molten). Deposition can also occur. Discharge problems are more acute in Micro-Patterned Gaseous Detectors (MPGDs) than in classical wire chambers, as MPGDs have electrodes with smaller volume than those of wire chambers to dissipate the heat produced by a discharge. Fig. 1 top shows a pixel of a CMOS readout chip that has been perforated by a spark. Fig. 1 bottom shows a damaged grid after a discharge has occurred; a part of the aluminum mesh has been molten. Even if the electrodes are protected with a high melting point material other damage mechanisms remain. Sparks can cause an excess of charge dumped in the detector, which can destroy the readout electronics.

* Corresponding author. Tel.: +31 20 592 5092.
E-mail address: vdgraaf@nikhef.nl (H. van der Graaf).
[1] Now at LAPP, Chemin de Bellevue 9, BP 110 F-74941 Annecy-le-Vieux Cedex, France.

0168-9002/$ - see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2010.11.116

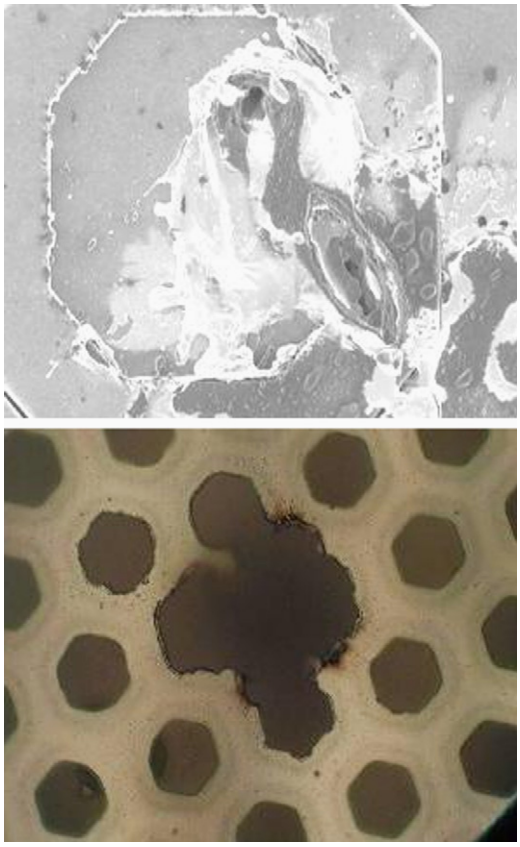

Fig. 1. SEM image of input pad of CMOS readout chip perforated by spark (top). Optical microscope image of aluminum grid molten by discharge (bottom).

To overcome the spark problem several groups have worked on solutions to reduce the spark probability [7,8] or limit the spark damage once the discharge appears [6,9–11].

Sparks can always be triggered by heavily ionizing particles so it is difficult to completely suppress them. It would be preferable to build a spark-proof detector. In Resistive Plate Chambers (RPCs) [12], with one or both electrodes made of a highly resistive material, this is the case. The instant drain of the charge deposited by the discharge is intrinsically blocked. The not drained-off charge creates a compensating electric field that produces a local drop in the applied field. This causes a self-quench of the discharge. The amount of charge involved in the discharge, limited by the total charge stored in the assembly of the participating electrodes, is then reduced [13].

It is attractive to pursue the combination of the protection given by RPCs with the high counting rate provided by MPGDs. This has been previously reported [14–16] but the materials and methods used cannot easily be employed for the post-processing of CMOS chips, which is our aim.

In this work a high resistivity layer, made of hydrogenated amorphous silicon (a-Si:H) or silicon-rich nitride (SiRN) has been used to cover Medipix2 [17] and Timepix [18] chips in GridPix detectors [19]. Besides quenching the spark, the a-Si:H or SiRN layer (named spark protection layer) prevents the evaporation of the thin metal input pads on the CMOS anode chip, due to the spark plasma, and reduces the charge entering the pixel circuitry.

2. Dimensioning spark protection layer

2.1. Quenching power of spark protection layer

The first requirement for the spark protection layer is to not affect the normal operation of the pixel chip, or to influence the normal (single electron initiated) avalanche charge signals. The resistance between adjacent pixel input pads should be sufficiently high—for modern pixel circuits this value should be higher than 100 MΩ. This sets a limit to the specific resistivity of the applied layer material and the layer thickness. The pixel input pad should be the only electrode in contact with the layer; if a (grounded) guard is surrounding the pads, then the resistance between the pixel pad and ground is reduced and therefore, the protection layer resistivity should be increased. CMOS pixel chips are usually covered by an isolating passivation layer leaving only the pixel pads and wire bonding pads uncovered.

Before any charge arrives to the protection layer, the top surface is at ground potential, assuming the pixel pad to be at ground potential too. The avalanche initiated by a primary electron after its drift towards a grid hole, has therefore a size and shape as it would have without the layer. In our case this avalanche has a width of $\sim$10 μm due to electron diffusion in the avalanche gap. Here we note that the width of the avalanche is small with respect to the pixel input pad (20 μm diameter). The avalanche will induce charge on all nearby electrodes (pixel input pads, all other exposed pixel circuitry, and the grid) due to electrostatic charge induction. The width of the charge distribution depends on the geometry of the electrodes, the thickness of the layer and relative permittivity ε_r of the layer material. The fraction of the total avalanche charge entering the pixel input pad is close to one if the charge spread, and therefore the layer thickness is small with respect to the diameter of the pixel input pad. If not, charge is lost in other exposed electrodes (in spite of being insulated) or adjacent pixel input pads. Details on the way the signal forms and spreads due to the effect of the layer are presented in Section 2.2.

It is useful to define the 'recovery' time constant of the potential at the surface of the layer. A column with cross-section O and a height equal to the layer thickness D has a resistance of $\rho D/O$. The virtual capacitance of this column equals $\varepsilon_0\varepsilon_r O/D$. The product of the column resistance and capacitance is a time constant $\tau=\varepsilon_0\varepsilon_r\rho$, which does not depend on the layer thickness. It can be associated with the recovery time of a potential charge on the layer surface. The avalanche charge causes a potential drop at the surface, causing a vertical current through the layer. As long as the recovery time constant is large with respect to the signal development time (ions crossing the avalanche gap), the electrostatic approximation of the signal development holds. Furthermore, the lateral spread of the charge signals over the pixels can be neglected if the inter-pixel time constant is large with respect to the recovery time constant of the layer.

The 'quenching power' of a protection layer is determined by the local reduction of the electric field due to the charge deposited during a discharge.

The cross-section diameter of a discharge is in the order of 1 mm, thus much larger than the avalanche gap ($\sim$50 μm). In these conditions the field reduction in the avalanche gap equals $Q_aD/(\varepsilon_0\varepsilon_rG)$, where Q_a equals the charge per unit of surface disposed onto the protection layer, D the layer thickness, ε_r the relative permittivity of the layer material, and G the thickness of the avalanche gap. Therefore, the quenching power P_q of a protection layer is defined as

$$P_q = D/(\varepsilon_r G) \tag{1}$$

This quenching power does not depend on the specific resistivity of the layer material. This tallies with the fact that the discharge development time ($\leq$2 ns) is very small with respect to the practical values of the recovery time constant.

In our GridPix detectors [19], a variation of 18 V in the potential difference between the grid and layer surface results in a factor 2 change in gain. The specific resistivity of the layer material should be low enough in order to limit the potential drop of the layer

surface, due to the vertical signal compensation current, to ~1 V, therefore not affecting the gain. Per pixel, the current equals the (single electron) pixel hit rate times the gain times the charge of the electron. For sLHC applications close to the beam pipe the specific resistivity of the material should therefore be as low as $10^9\ \Omega$ cm. The recovery time constant for such layers is in the order of 1 μs, still much larger than the discharge development time (≤ 2 ns). For usual applications it may be assumed that the discharge rate is very low with respect to the event rate.

For less high rate applications, materials with a specific resistivity in the range 10^9–$10^{13}\ \Omega$ cm can be applied, and the value is not critical.

2.2. Simulation of effect of resistive layer on signal

To estimate the impact of the resistive layer on the readout signal seen by the CMOS chip pre-amplifier, a simulation was carried out using the Spectre® simulator integrated in the analog artist framework electronic circuit simulation software [20].

As noted in the previous section, for a high resistivity layer having a dielectric constant value of 11 and a bulk resistivity of $10^{11}\ \Omega$ cm the capacitive transmission of the signal exceeds the ohmic transmission by 3 orders of magnitude for signals in the 50 MHz range and below, as those from ions in Micromegas [21]. The dielectric constant and resistivity values chosen for the simulated layer are typical values for the type of a-Si:H deposited on Timepix chips.

For the simulation purpose the detector was modeled as follows. A set of 5×5 pixels are connected to Timepix amplifiers. Each pixel is topped by a volume of a high resistivity layer, itself divided into $10 \times 10 \times 10$ volume elements. Each element is represented as a cube having a set of a resistance and capacitance in parallel connecting every two opposite faces of the cube. The gas volume over the pad is also divided into $10 \times 10 \times 10$ elements, each having a purely capacitive connection between every two opposite faces. Fig. 2 shows a schematic of the simulation model employed.

The capacitances and resistances are chosen to match the pad-to-grid mutual capacitance, for the gas part, and the bulk resistivity and surface capacitance for the protection layer part. Special care was taken for the edges and symmetry considerations were used to simplify the simulation.

The segmentation of each pixel in 10×10 elements allowed various coverages of the pixels by the collecting anode (full or cross shape in the middle, see Fig. 3).

For the simulation a test charge pulse is injected in the four central elements of the 10×10 pixel reticle. For three layer thicknesses (10, 15 and 20 μm) the fraction of the injected signal, collected at the pixel, is calculated in two cases, cross in the middle of the pixel (as for a real Timepix chip) and fully covered pixels. Results are summarized in Table 1.

For a cross shape pixel, the signal on the pixel is reduced by more than a factor of 2 for a layer thickness of 20 μm. Also, the signal is spread transversally over typically two and a half times the layer

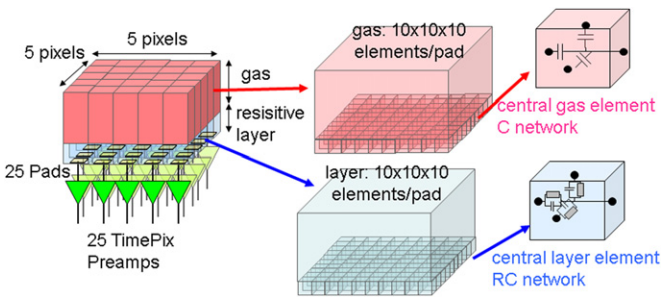

Fig. 2. Schematic image of simulation model. Gas layer is modeled as network of capacitances. High resistivity layer is modeled as RC network.

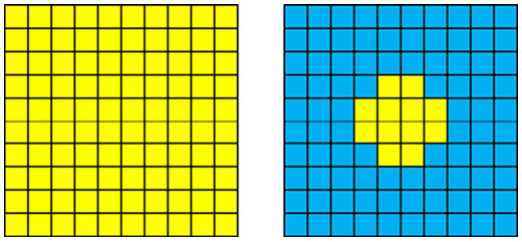

Fig. 3. The two different pixel structures employed for simulations. Left—"full" shape, pixel is completely covered by aluminum. Right—"cross" shape, central cross in pixel is aluminized.

Table 1
Fraction of injected signal collected at pixel for different protection layer thicknesses.

Thickness (μm)	Signal fraction (full shape)	Signal fraction (cross shape)
10	94%	76%
15	83%	57%
20	70%	44%

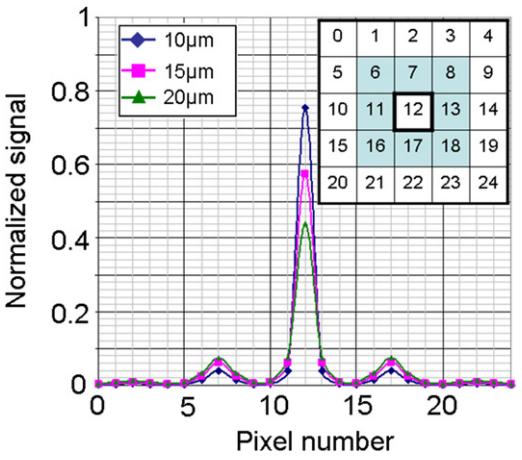

Fig. 4. Charge spread along a pixel matrix (top right part of figure) for different layer thicknesses after injection of charge pulse in the center of central pixel (number 12). Pixels have cross shape coverage.

thickness. For three different layer thicknesses (10, 15 and 20 μm) Fig. 4 shows how the charge, when injected in a central pixel, is spread around the neighboring pixels.

Simulations show that layers thicker than 15 μm would degrade significantly the performance of the detector by reducing its single electron detection efficiency and by spreading the charge over several neighboring pixels, resulting in a deteriorated two-electron separation. This calls for large signal pads, and a limitation of the simulated resistive layer thickness to less than 10 μm.

For high rate applications, where a resistivity as low as $10^9\ \Omega$ cm is needed, no change in the quenching properties of the layer is expected, as the quenching power (defined in Eq. (1)) depends on geometrical factors. For lower resistivity however, the inter-pixel noise will start to augment and also the charge spread will increase. This effect has been previously employed in detectors using pads covered with a highly resistive layer [22].

3. Deposition of highly resistive material layers

SiRN and a-Si:H layers were deposited on top of Timepix and Medipix2 chips. The two materials are well known in the

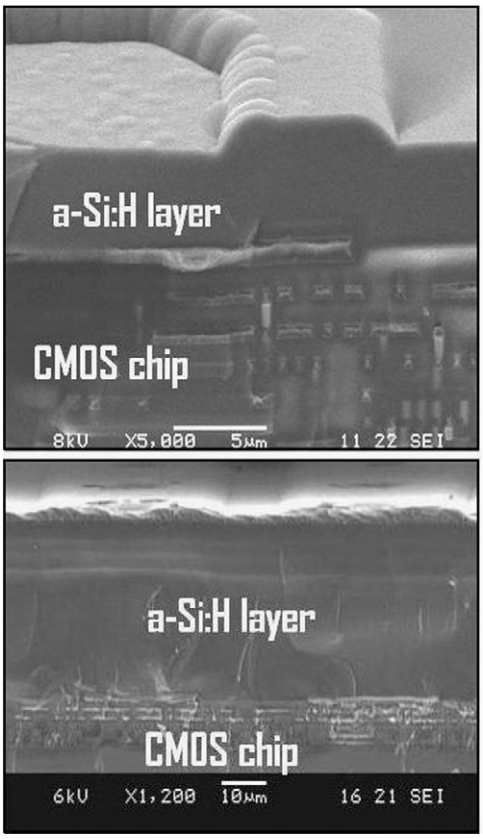

Fig. 5. Cross-section SEM picture of two Medipix2 chips covered with different thicknesses of a-Si:H: 3 μm (top) and 30 μm (bottom).

microelectronics industry and can be deposited in a CMOS compatible manner. Details about the deposition are given in the following sections.

3.1. Deposition of a-Si:H layers

Hydrogenated amorphous silicon (a-Si:H) is commonly used in MEMS[2] applications [23], photovoltaics [24] or thin film transistors [25]. The material is typically deposited at low temperature using PECVD,[3] which makes it compatible with many CMOS post-processing applications.

The deposition of the a-Si:H layers was performed at the Photovoltaics and Thin Film Electronics Laboratory of the EPFL-IMT, Neuchâtel, Switzerland. It is done using very high frequency PECVD (VHF PECVD) at 70 MHz. During deposition, the substrate reaches a maximum temperature of 200 °C. Plasmas at relatively low bias voltages are employed. Stress free layers are obtained. This process can thus be included in a wafer scale post-processing sequence on CMOS pixel wafers.

The process is optimized for intrinsic layer deposition at relatively high rates, as used for a-Si:H thick diode deposition [26]. A deposition rate of ~100 nm/min was obtained with a hydrogen dilution of silane ($[H_2]/[SiH_4]=0.35$). The specific resistivity of the deposited layer (as grown on glass substrate) is around 10^{11} Ω cm, weakly depending on the film thickness and substrate. Doping of the layers is possible to obtain lower resistivity. The a-Si:H layers can be patterned using dry etching in a SF_6/O_2 plasma.

[2] Micro electro mechanical systems.
[3] Plasma enhanced chemical vapor deposition.

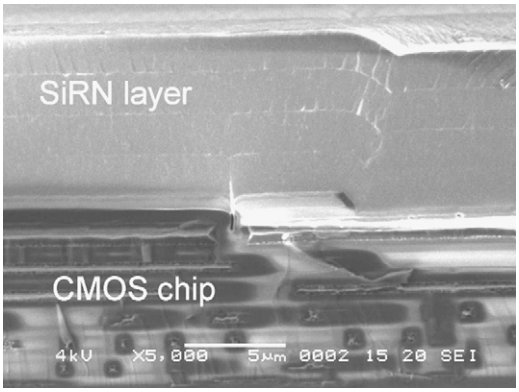

Fig. 6. Cross-section SEM picture of Timepix chip covered with 9 μm SiRN.

Several thicknesses of a-Si:H, ranging from 3 to 30 μm, have been deposited on top of Medipix2 and Timepix chips. Fig. 5 shows SEM[4] pictures of Medipix2 chips with different thicknesses of a-Si:H deposited on top.

3.2. Deposition of SiRN layers

Stoichiometric Si_3N_4 is regularly employed in the semiconductor industry as a passivation layer, interlayer or for isolation [27]. Non-stoichiometric silicon-rich Si_xN_y (SiRN) is also used in MEMS [28], and RF[5] applications [29] to obtain low stress layers. In both cases the material is typically deposited by low pressure chemical vapor deposition (LPCVD) at a temperature between 700 and 900 °C. Using this deposition technique a very good film quality is obtained.

Recently SiRN suspended structures fabricated by PECVD have been shown [30]. The process parameters can be controlled to produce low stress films. The PECVD technique allows depositing layers at lower temperature than LPCVD. Deposition can be done at temperatures well below 400 °C. This temperature is compatible with CMOS post-processing, and therefore PECVD was chosen to deposit SiRN onto the Timepix chips.

The SiRN deposition was done in the MESA+facilities of the University of Twente by PECVD at 13.56 MHz. Silane and ammonia react inside the chamber to form Si_xN_y at the wafer surface. The silicon content in the material, and therefore the resistivity, can be controlled by changing the silane-to-ammonia flow ratio. The specific resistivity of the deposited layer is around 10^{12} Ω cm, The temperature during deposition was 300 °C. A deposition rate of ~70 nm/min was achieved. A shadow mask was used to cover the wire bonding pads of the chips during deposition. The deposition was performed in steps of 30 min to minimize the time the chips remain continuously at high temperature. Fig. 6 shows a SEM picture of a Timepix chip, on top of which a 9 μm thick SiRN layer has been deposited in four steps. The stepwise process is seen back in the formation of an interfacial layer, which is probably an oxide formed after each deposition step.

4. Spark tests on dummy substrates

Before starting the spark tests on real CMOS chips, several experiments were performed on home built dummy substrates to

[4] Scanning electron microscope.
[5] Radio frequency.

assess the protection provided by the high resistivity materials. Various substrates can be fabricated at low cost in a fast manner.

4 in. silicon wafers containing thirteen 16×16 mm^2 aluminum anodes were fabricated. On each wafer, eleven anodes were covered with a 3 μm thick a-Si:H layer. The two remaining anodes were left uncovered for signal comparison purposes. Finally, the wafers were diced, obtaining individual anodes. Micromegas foils (35 μm hole diameter and 60 μm hole pitch) were placed on these anodes. Fig. 7 shows a diagram of the operating principle of a Micromegas detector.

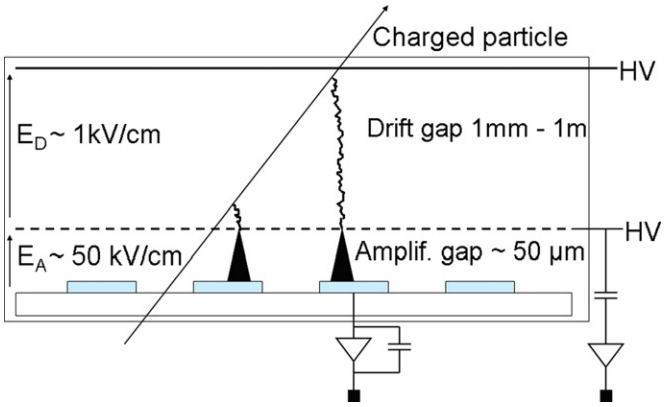

Fig. 7. Schematic representation of operating principle of Micromegas detector. Free electrons released in gas are swept by drift field and enter through Micromegas holes. Electrons are multiplied in amplification region and total charge is collected at pads.

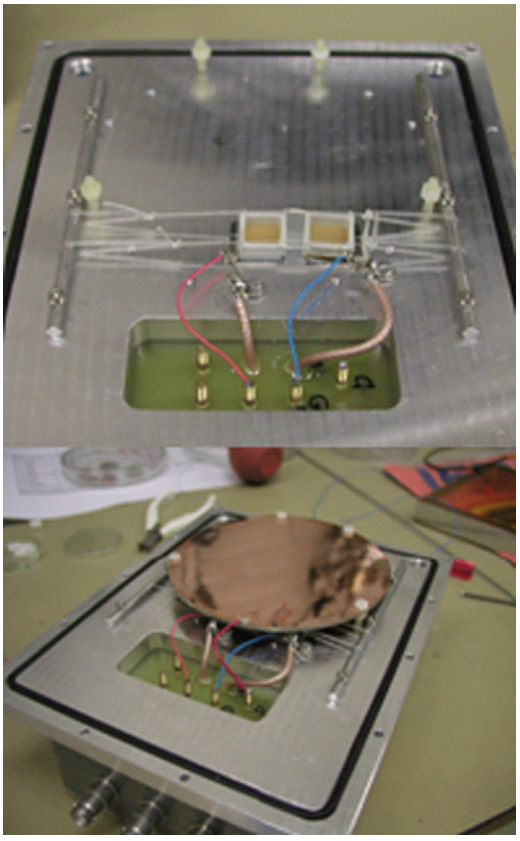

Fig. 8. Top—two devices with protected and non-protected anode covered with Micromegas and placed in measurement chamber. Bottom—measurement chamber after assembling cathode.

4.1. Measurement chamber

The assembled devices were placed inside the test chamber (see Fig. 8). This chamber consists of an aluminum base plate and a Kapton gas seal cover. One protected and one not-protected anode were placed in the test chamber both with a Micromegas grid on top. The devices were mounted onto an insulating frame. Two gas connections were made in the aluminum base plate. A cathode foil, mounted above the diced anodes, defined a 10 mm thick drift gap. A metal box under the gas chamber contains the high voltage and readout connectors.

4.2. Measurement setup

Discharges are fast processes with timescales in the order of nanoseconds. The measurement of signals that are generated in these processes requires careful design of the readout circuitry. The designed setup was physically small to reduce parasitic inductances and capacitances. All coaxial cables were terminated with their characteristic impedance and unavoidable parasitic LC circuits were dampened.

The input signals could be read out in two ways

- Anode readout—the charge signals correspond to the pixel input signals.
- Grid readout (see Fig. 9)—the signal induced by the movement of electrons and ions is read out from the grid.

For practical reasons the grid readout has been chosen. In this readout scheme a ground wire is directly connected to the anode, excluding any possibility of poor contacts (oxide on the aluminum housing and/or the silicon).

The discharge current is calculated as follows:

$$I_{dis} = -\frac{dU_{grid}}{dt} C_{grid} + I_{R_1} + I_{R_2} \tag{2}$$

At the timescales of discharges (about 10 ns), the differential part is dominant by more than one order of magnitude. Thus the discharge current expression can be simplified as

$$I_{dis} \approx -\frac{dU_{grid}}{dt} C_{grid} \tag{3}$$

An oscilloscope having a 50 Ω impedance is used to measure the voltage across R_3. Assuming U_C, the voltage over capacitor C, is constant during a discharge and $R_3 \| Z_{cable} \ll R_2$ further simplifies the expression for the discharge current to

$$I_{dis} \approx -C_{grid} \frac{dU_{measured}}{dt} \frac{R_2}{25} \tag{4}$$

4.3. Discharge measurements

For the measurement of induced discharges the chamber was flushed with He/iC$_4$H$_{10}$ (80/20). A container with ^{232}Th was placed

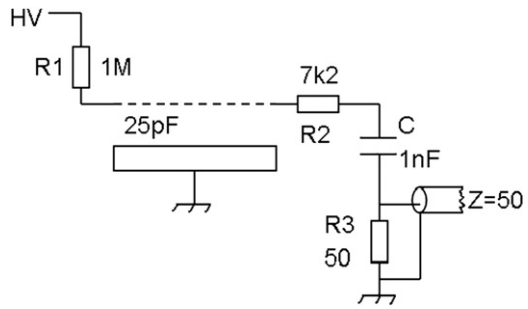

Fig. 9. Electrical equivalent of grid readout. Cathode is not displayed. Capacitance of grid is 25 pF.

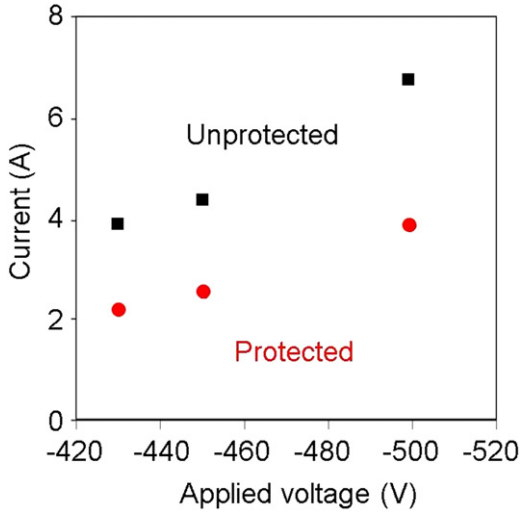

Fig. 10. Discharge peak current at different grid voltages for covered (dots) and uncovered (squares) anodes.

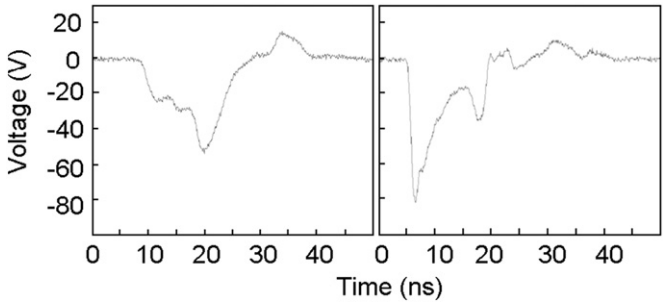

Fig. 11. Pulse amplitude of discharges on dummy substrates; discharge on covered anode (left) and on uncovered anode (right).

in the gas system upstream of the chamber [7]. ^{232}Th decays to ^{220}Rn, which decays through ^{216}Po to ^{212}Pb emitting two alpha particles of a few MeV separated by ~0.15 s. Spark signals can be recorded with the setup previously described. For these measurements a Tektronix TDS 7254 oscilloscope with an analog bandwidth of 2.5 GHz and a sample rate of 10 GS/s was used.

The discharge current was measured for different grid voltages. As shown in Fig. 10 the current in the protected anodes is lower than in the unprotected anodes.

A clear difference was found in the discharge process between covered and uncovered anodes. The discharge plot in the case of covered anodes has relatively smooth edges and slopes, while in the case of the uncovered anodes the discharge plot has a steep leading edge. This leads to higher transient currents in the case of uncovered detectors. Fig. 11 shows spark signals on covered and uncovered anodes at a grid voltage of −490 V. The shown signals are representative of hundreds of signals recorded in this manner.

Also, using protected anodes higher gains could be achieved before sparks appear than when using unprotected anodes. More details about the spark measurements performed with dummy substrates have been presented in Ref. [31].

5. Spark studies on CMOS chips

Layers of a-Si:H and SiRN with various thicknesses were deposited on CMOS chips. Sparks were intentionally produced to assess the protection provided by those layers. The protected CMOS chips were also operated in long term experiments under normal biasing conditions. Results are shown in the following sections.

5.1. a-Si:H protection layers on CMOS chips

Light gas mixtures are less prone to discharges than heavy gas mixtures [6,32]. This may be expected since the discharge probability is related to the amount of primary charge released in the conversion gap.

For this reason, a Timepix chip covered with a 3 μm thick a-Si:H layer and equipped with a Micromegas foil, was first operated in a He/iC$_4$H$_{10}$ (80/20) gas mixture. The gas gain was adjusted to approximately 3000 (at grid voltage of −400 V). During one month (720 h) cosmic ray events, ^{55}Fe conversions and tracks of electrons emitted by ^{90}Sr were recorded. After changing to an Ar/iC$_4$H$_{10}$ (80/20) gas mixture, the Timepix chip stopped functioning within two days of operation at a grid voltage of −420 V (gain~4000), presumably after a discharge causing a threshold DAC, integrated on the chip, to no longer function correctly. Visual inspection of the chip surface showed no damage, like evaporated aluminum, as was the case before in naked chips (see Fig. 1). This can be expected since the melting point of amorphous silicon (1147 °C) [33] is higher than that of aluminum (660 °C) [34]. Also the total mass of the protection layer to dissipate the heat produced by the spark is higher than the mass of the naked aluminum pixel pad. Apparently, the chip suffered internal damage due to a too large charge injected into one or more pixel input pads.

It was then decided to cover the chips with a thicker layer. This would quench the discharges in an earlier stage (see Section 2.2). In addition, all induced charge signals appearing at the pixel input pads are somewhat reduced due to the larger distance between the avalanche charge and the pixel input pad. Charge dilution, as a result of charge spread, is unavoidable if the thickness of the protection layer is of the order of the pixel input pad or greater.

Two Timepix chips were covered with an a-Si:H layer 20 μm thick. An integrated grid (InGrid) [19] was fabricated on top of one of the chips while the other one was covered with a Micromegas foil.

The chip equipped with the Micromegas foil was placed inside a chamber and flushed with Ar/iC$_4$H$_{10}$ (80/20). Normal data taking (including cosmic rays, ^{55}Fe and ^{90}Sr) took place during more than forty days. An approximate gain of 4000 was reached at a grid voltage of −420 V. After that, the chip was tested by provoking discharges. High density primary ionization events were obtained from induced alpha particles. Again the alpha particles were produced from the decay of ^{232}Th (see Section 4.3). In about 1% of the alpha events, the proportional signal develops into a discharge. The probability for this is clearly higher for alpha particles with a direction perpendicular to the chip. An example is shown in Fig. 12; where the alpha ionizes the gas, the discharge occurs, seen in the figure as a red circle. Some 150 pixels in the area receive a large coincident charge signal and are activated. As a result, the local values of supply voltage and threshold references are disturbed. Since these are common within pixel columns, many pixels above and below the discharge area are affected. Discharges do not harm the behavior of the chip—it keeps functioning correctly after the discharge tests.

The second chip having a 20 μm thick a-Si:H protection layer and equipped with an integrated grid was also tested in Ar/iC$_4$H$_{10}$ (80/20) obtaining similar results at a grid voltage of −420 V.

With a layer of 20 μm a-Si:H, the chips not only keep functioning, but discharges can actually be observed in detail. From these data we conclude that chips, protected with a 20 μm a-Si:H layer, are spark-proof for our typical working conditions.

Thinner layers of a-Si:H were also tested. A Timepix chip was covered with a 15 μm thick a-Si:H layer and an integrated grid was fabricated on top. Ar/iC$_4$H$_{10}$ (95/5) and Ar/iC$_4$H$_{10}$ (80/20) gas

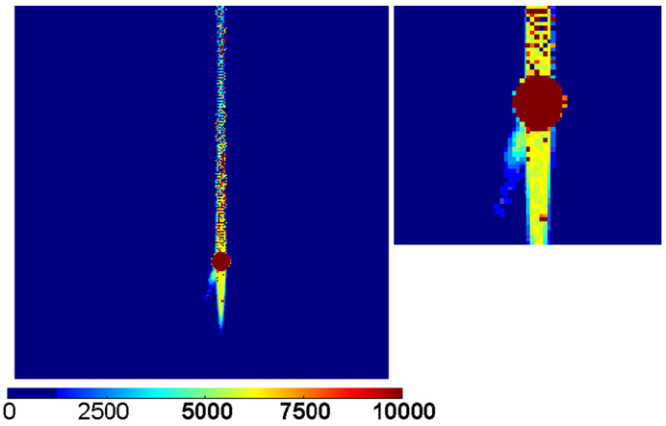

Fig. 12. Left—typical image of discharge event in Timepix chip protected with 20 μm a-Si:H. Color coding represents pulse height of input signal on pixel. Discharge is seen as red circle. Alpha particle triggering discharge is observed entering pixel matrix from bottom left side of discharge. Pixels activated in vertical line are due to disturbance of supply voltage and threshold references. The supply voltage is connected from bottom side in picture. Right—detail of spark event. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Table 2
Outcome of experiments carried out with several chips covered with different thicknesses of a-Si:H and equipped with Micromegas or InGrids.

Detector	Gas	Test	Failure time
3 μm Micromegas	He/iso (80/20)	~−400 V gain ~3000	>1 month
	Ar/iso (80/20)	~−420 V gain ~4000	2 days
20 μm Micromegas	Ar/iso (80/20)	Provoked sparks	>5 days
20 μm InGrid	Ar/iso (80/20)	~−420 V	>4 months
15 μm InGrid	Ar/iso (80/20)	~−420 V	>4 months
	Ar/iso (95/5)	~−350 V 95% efficiency	>4 months
	Xe/CO_2 (80/20)	−490 V gain ~3000	2 hours

mixtures were employed for the data taking. Measurements with the device were carried on for more than four months. Single electron detection efficiency higher than 95% was reached in Ar/iC_4H_{10} (95/5) at a grid voltage of ~−350 V. After changing to a Xe/CO_2 (80/20) gas mixture and a grid bias voltage of −490 V (gas gain~3000) the chip broke within 2 h of operation. Table 2 summarizes the experiments carried out with the various Timepix chips covered with different thicknesses of a-Si:H. For most of the detectors a specific failure time was not reached and the given value indicates that the detector was still operational after that time.

5.2. SiRN protection layers on CMOS chips

To assess the spark protection provided by the SiRN, tests were done with different chips having different protection layer thickness and working in different gas mixtures.

First a 13.2 μm thick SiRN layer was deposited on a Timepix chip. A Micromegas foil was framed over the chip and the detector was placed in a chamber that was flushed with Ar/iC_4H_{10} (80/20). Even with −520 V applied to the Micromegas foil (gas gain ~200000), the Timepix chip kept functioning normally. Sparks were observed in the chip pixel matrix. Cosmic ray tracks were recorded using this detector, confirming the normal operation of the device. This SiRN layer provides enough spark protection for the working point. Again, visual inspection of the chip showed no damage such as molten materials. It seems the heat produced by the spark is dissipated in the mass of the protection layer before reaching the melting point of silicon nitride (1900 °C [34]).

Table 3
Destruction voltage of three Timepix chips with different SiRN protection layer thickness after exposure to various working conditions.

Layer thickness (μm)	Gas mixture	Voltage
2.2	He/CO_2 (70/30)	−520 V
4.4	Ar/CF_4/iC_4H_{10} (95/3/2)	−360 V
6.6	Ar/iC_4H_{10} (80/20)	−430 V

Further tests were done with chips covered with thinner SiRN layers and an integrated grid assembled onto them. Table 3 summarizes at which grid voltage the various chips finally failed to operate properly due to spark damage. Absolute gas gain measurements were not performed for these devices. Single electron efficiency higher than 90% was reached for the Ar/iC_4H_{10} (80/20) gas mixture; for the other detectors it was not possible to reach such a high single electron efficiency.

- The detector having a 2.2 μm thick protection layer stopped functioning properly after ~1 hour operation in He/CO_2 (70/30) at −520 V. About −580 V would be needed for a good single electron detection efficiency.
- The detector having a 4.4 μm thick protection layer was operated in several gas mixtures and suffered many discharges probably because of a damaged grid. The detector was operated at −480 V in an Ar/CO_2 (70/30) gas mixture, and at −560 V in He/CO_2 (70/30), finally the chip stopped functioning properly when operated at −360 V in an Ar/CF_4/iC_4H_{10} (95/3/2) gas mixture after a total use time of a few weeks.
- The detector having a 6.6 μm thick protection layer was operated in an Ar/iC_4H_{10} (80/20) gas mixture at −430 V and stopped functioning after about one day of operation.

Various detectors in which the Timepix chip is covered with 8.8 μm thick SiRN are still operational after several months of operation. Recently few chips protected with 8.8 μm thick SiRN have stopped functioning due to spark damage. Pinholes were found in the SiRN layer, this could be the cause that stopped the chips from functioning. Clearly, the thinner SiRN layers do not provide enough spark protection for all working conditions.

When using a-Si:H, all the pixels involved in a spark event are in overflow. When using SiRN pixels are not in overflow. It is possible to distinguish different values in the spark event. The spark has a tube-like shape with a nearly flat top.

It has been shown that SiRN layers 8.8 μm thick, provide enough spark protection for our typical working point, whereas at least 15 μm or 20 μm thick a-Si:H layers are needed depending on the gas mixture employed, therefore the charge spread problem is more acute in the a-Si:H case. Via doping, the resistivity in the a-Si:H layer can be varied in a wide range. Doping of the SiRN layers has not been attempted and the actual resistivity range is more limited than for a-Si:H. For high rate applications both a-Si:H and SiRN are suitable, as far as the resistivity can be tuned to values in the order of 10^9 Ω cm.

6. Conclusions and future plans

By means of PECVD we have deposited layers of a-Si:H and SiRN on dummy substrates as well as on Timepix and Medipix2 chips. The process is CMOS compatible and the chips showed no degradation after the deposition of a maximum thickness of 20 μm a-Si:H or 13 μm SiRN. To avoid charge sharing between adjacent pixels, and degradation of the single electron efficiency, when using a-Si:H as a high resistivity material, the thickness should be limited to less than 10 μm.

The discharge process induced by alpha particles has been studied. The protection layer reduces the peak current that occurs during a discharge. The reduced energy of the discharges is below the level that would damage the protection layer by melting or evaporation.

An adequate layer thickness deposited on top of the Timepix and Medipix2 chips provides enough spark protection for our typical working point. In He/iC$_4$H$_{10}$ gas mixtures 3 μm a-Si:H provides enough protection to operate the device at more than 90% single electron detection efficiency. In Ar/iC$_4$H$_{10}$ gas mixtures 15 μm a-Si:H or 8.8 μm SiRN protects the chips against sparks, operating the detectors at more than 90% single electron detection efficiency. We must point out that some of the chips protected with SiRN have stopped functioning after a certain time, probably due to pinholes in the layer.

Using the detailed 2D and 3D spark information provided by GridPix detectors, an empirical model of the spark process is currently under development.

Detectors having two high resistivity electrodes, similar to RPCs, in which the grid is made out of a-Si:H, will be investigated. It is expected that this double protection will solve the problem that some chips still stopped functioning because of spark damage even with the SiRN layer.

Acknowledgements

This research is funded by the Dutch Foundation for Fundamental Research on Matter (FOM) and by the Dutch Technology Foundation STW through project TET 6630 "Plenty of room at the top". The authors would like to thank Sander M. Smits for mask design and Joop Rövekamp for the mechanical support.

References

[1] P. Fonte, V. Peskov, B.D. Ramsey, SLAC–ICFA Instrumentation Bulletin 15 Fall 1997, Available online at 〈http://www.slac.stanford.edu/pubs/icfa〉.
[2] R.T. Waters, in: J.M. Meek, J.D. Craggs (Eds.), Electrical Breakdown of Gases, Wiley and Sons, New York, 1978, pp. 385–582.
[3] W.J. Yi, P.F. Williams, J. Phys. D: Appl. Phys. 35 (3) (2002) 205.
[4] P. Fonte, Presentation at the 2nd RD51 Collaboration Meeting, Paris, 13–15 October 2008. 〈http://indico.cern.ch/materialDisplay.py?contribId=69\&sessionId=0\&mater〉.
[5] H. Raether, Electron Avalanches and Breakdown in Gases, Butterworth, London, 1964.
[6] J.P. Perroud, et al., Nucl. Instr. and Meth. A 488 (1–2) (2002) 162.
[7] S. Bachmann, et al., Nucl. Instr. and Meth. A 479 (2–3) (2002) 294.
[8] O. Baruth, et al., Nucl. Instr. and Meth. A 454 (1) (2000) 272.
[9] H.S. Cho, J. Kadyk, Nucl. Instr. and Meth. A 481 (1–3) (2002) 174.
[10] S. Keller, et al., Nucl. Instr. and Meth. A 419 (2–3) (1998) 382.
[11] F. Hartjes, et al., Nucl. Instr. and Meth. A 310 (1–2) (1991) 88.
[12] R. Santonico, R. Cardarelli, Nucl. Instr. and Meth. A 187 (2–3) (1981) 377.
[13] J. Crotty, et al., Nucl. Instr. and Meth. A 337 (2–3) (1994) 370.
[14] B. Boimska, et al., Nucl. Instr. and Meth. A 404 (1) (1998) 57.
[15] P. Fonte, et al., Nucl. Instr. and Meth. A 431 (1–2) (1999) 154.
[16] V. Peskov, et al., IEEE Trans. Nucl. Sci. NS54 (5) (2007) 1784.
[17] X. Llopart, M. Campbell, Nucl. Instr. and Meth. A 509 (1–3) (2003) 157.
[18] X. Llopart, et al., Nucl. Instr. and Meth. A 581 (1–2) (2007) 485; X. Llopart, et al., Nucl. Instr. and Meth. A 585 (1–2) (2008) 106.
[19] V.M. Blanco Carballo, et al., IEEE Electron Device Lett. 29 (6) (2008) 585.
[20] Spectre® Circuit Simulator Reference, Cadence Design Systems, Inc. (Cadence), 2655 Seely Avenue, San Jose, CA 95134, USA, 2003.
[21] Y. Giomataris, et al., Nucl. Instr. and Meth. A 376 (1) (1996) 29.
[22] M.S. Dixit, et al., Nucl. Instr. and Meth. A 518 (3) (2004) 721.
[23] C. Iliescu, B. Chen, J. Micromech. Microeng. 18 (1) (2008) 015024.
[24] M.D. Archer, R. Hill, Clean Electricity from Photovoltaics. Series on Photoconversion of Solar Energy, Imperial College Press, 2001 vol. 1.
[25] M.J. Madou, Fundamentals of Microfabrication: the Science of Miniaturization, CRC Press, Boca Raton, 2002.
[26] N. Wyrsch, et al., Proceedings of the MRS Symposium, vol. 869, 2005, p. 3.
[27] Stephen A. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, New York, 2001.
[28] S. Bouwstra, et al., Sens. Actuators A 21 (1–3) (1990) 332.
[29] L.J. Fernandez, et al., Electron. Lett. 41 (3) (2005) 124.
[30] K.J. Winchester, J.M. Dell, J. Micromech. Microeng. 11 (5) (2001) 589.
[31] A.A. Aarts, et al., IEEE 2006 Nuclear Science Symposium Conference Record 6 3865.
[32] J.P. Perroud, Nucl. Instr. and Meth. A 453 (1–2) (2000) 159.
[33] E.P. Donovan, et al., Appl. Phys. Lett. 42 (8) (1983) 698.
[34] David R. Lide, CRC Handbook of Chemistry and Physics.