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Analysis of Low Power and High Speed Phase Frequency Detectors for Phase Locked Loop Design

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Abstract

Phase Locked Loop (PLL) usual replicated problems are different requirements like small acquisition time, maximum locking range and minimum phase error variance. To meet these requirements various phase frequency detector (PFD) designs are proposed. The major trend in wireless transceivers is towards single-chip CMOS integration. But the increase of MOS devices on a single chip will consume more power. The PFD designs are targeted for specific applications. Conventional, PFDNG, Dynamic, PtPFD are evaluated and a design MUX based PFD using TGCMOS is suggested. All these designs are simulated using HSPICE with 180nm technology for 2.0V. Results show that PFDNG has consumed less power 0.079mW because of less transistors but shows high propagation delay. TGCMOSPFD shows highest energy efficiency among all the designs.

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Keywords: phase locked loop; phase frequency detector; power and speed;

1. Introduction

CMOS technology continues device scaling for high integration. However, as the feature size shrinks and chip designers attempt to reduce supply voltage to meet power targets in large multi-processors, parameter variations are becoming a severe problematic. Parameter variations can be broadly classified into device variations incurred due to imperfections in the manufacturing process and environmental variations and on-die temperature and supply voltage

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(VDD) fluctuations [1].

Nomenclature

VDD	Supply Voltage
CMOS	position of
CLK	clock
RST	reset

Modern CMOS nanometer technologies are very proficient, in terms of power consumption and speed, for the design of ICs; the power consumption could be negatively affected by current leakage only in large circuits. However, the performances of analog circuits are considerably degraded due to the small transistor gain, signal range, low supply voltage, and high variability of device parameters [2]. The significance of analog circuits using low supply voltage is extremely increasing in the recent past. The large component densities particularly in VLSI stress, lower power consumption. The low power consumption is a key issue in modern portable devices to increase the battery life, performance, the packaging density and circuit reliability.

Phase locked loops (PLLs) are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizer in communication systems for clock extraction and generation of a low phase noise local oscillator. The PLLs was first described in the early 1930s, where its application was in the synchronization of the horizontal and vertical scans of television. Later on with the development of integrated circuits, it found uses in many other applications. A PLL is a feedback control circuit, and is operated by trying to lock to the phase of a very accurate input through the use of its negative feedback path. A basic form of a PLL consists of four fundamental functional blocks namely:

1. Phase Frequency Detector (PFD) 2. Charge Pump (CP) 3. Voltage Controlled Oscillator (VCO)
4. Frequency Divider (FD)

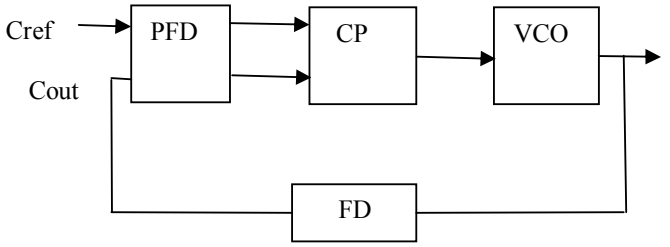


Fig 1. Block diagram of Phase Locked Loop

The organization of the paper is as follows: the functionality of the PFD and different types of the PFDs are discussed in section 2, NOR gate of PFD is designed by MUX using TGCMOS for low power and high speed explained in section 3, the discussion about the results is given in section 4 and shows output waveforms of the proposed PFD design. Finally, the conclusion of the paper is given is section 5.

2. Phase Frequency Detector

The phase frequency detector (PFD) acts as a comparator to compare signals Cout and Cref. This comparator is responsible for generating control signals (up and down), which commands the charge-pump (CP) circuit to charge or discharge current. The phase detector has two input signals Cref and Cout. Cout signal is the feedback signal, which is the output divider and Cref is coming from an input divider or crystal oscillator. Two conditions are realized at the input of PFD block: first Cref leads Cout i.e as Cref goes high, the output Up goes high. When the leading edge of Cout comes, Up goes to zero while Down does not show any change and remains low. Exactly

opposite mechanism happens in second case when Cout leads Cref . If both Cref and Cout are in same phase the outputs Up and Down are zero.

The UP and DOWN signals control the CP block in its charging and discharging process [3]. The states of the PFD as shown in fig 2 are represented by the logical output signals Up and Down and can be defined with:

- Up=0 and Down=1 then current is drawn from the loop.
- Up=0 and Down=0 then no change in current
- Up=1 and Down=0 then current is driven into loop filter

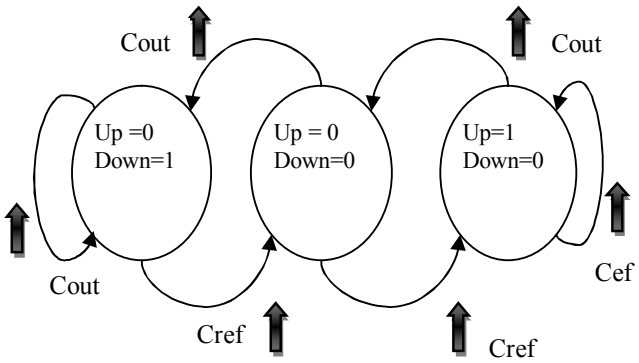


Fig 2. State Diagram of PFD

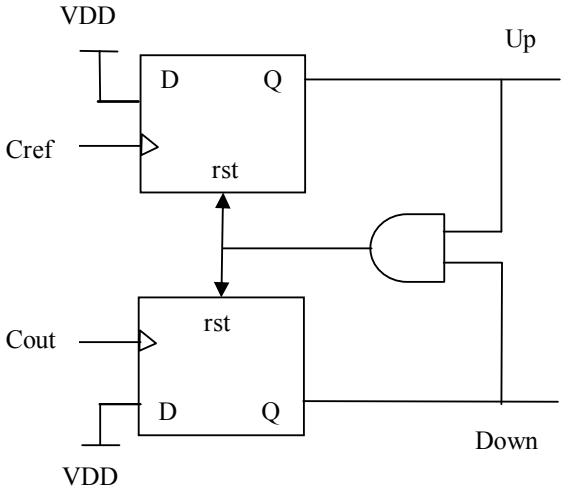


Fig 3. Conventional PFD

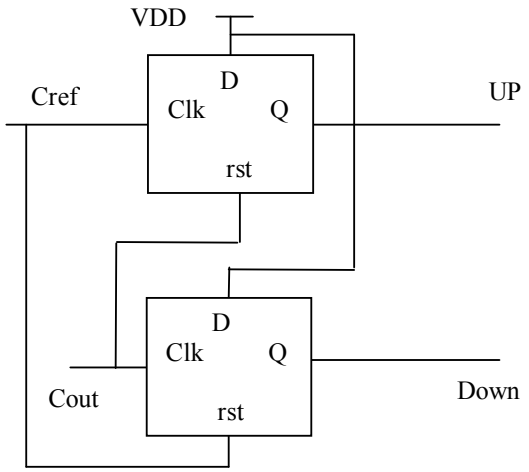


Fig 4. PFD with No Gate (PFDNG)

Fig 3. shows a detailed design for PFD with input/output terminals. A simple design of PFD consists of two D flip flops and AND gate. The D input of the flip-flops is connected to VDD and the input signals (Cref, Cout) are applied to the clock input. When the status of the clock changes to high, this flip-flop will charge and its output goes to high. The use of AND gate is to avoid both flip-flops to be high at the same time. The inputs of the AND gate are, the Up and DOWN signal from both flip-flops, and the output of the AND gate is connected to the reset input of the flip-flops. As soon as both outputs (UP, DOWN) are high the AND gate will generate a high signal that will reset both flip-flops avoiding the situation of both high at the same time [4-5].

Due to the AND reset path, the time desired to charge the AND gate and reset both flip-flops will be added to the reset delay time in the internal components of the flip flops and produce a large dead zone The change is to

remove the reset path and reduce the delay time that causing the dead zone problem. As shown in fig 4 PFD with No Gate (PFDNG) the D flip-flop schematic design had few changes from the Conventional PFD, these changes are allowed in getting rid of the reset path and applying the CLK signal directly to the RST input for each flip-flop to reset them momentarily both flip-flops have high output at the same time. The PFDNG functions exactly like Conventional PFD.

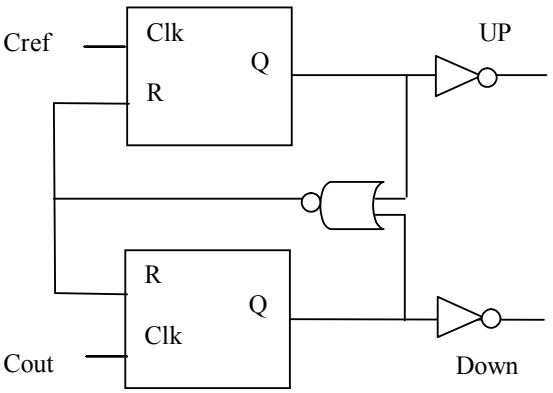


Fig 5. Dynamic PFD

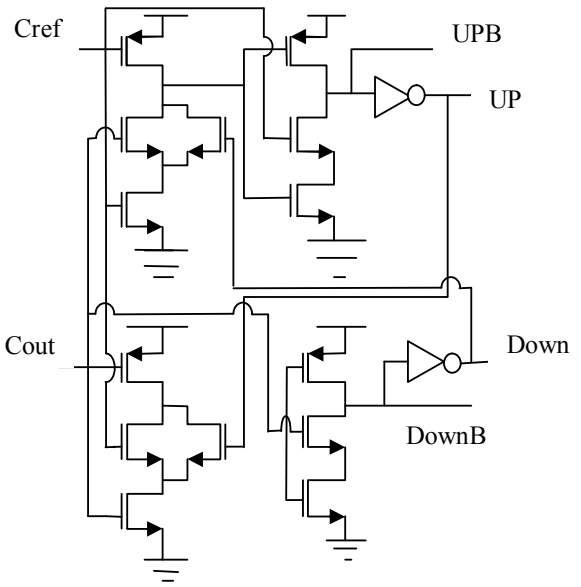


Fig 6. Pre Charged PFD (PtPFD)

The charge-pump PLL system has a Dynamic PFD and precharge type PFD (ptPFD) as shown in Fig 5 and Fig. 6 respectively. Dynamic PFD reduces the number of transistors compared to Conventional PFD. A sequential PFD has no limit to the error detection range, but has the limited range of operating frequency because of the long critical path delay throughout the signal path. To exceed its frequency limitation, a dynamic logic style PFD called ptPFD shown in Fig. 6 was proposed [6]. The conventional static logic circuitry of the sequential PFD was replaced by dynamic logic gates with inherently small parasitic capacitances, thus a high frequency operation is achieved. But the output signals of the ptPFD are influenced by the input signal duty ratio and its phase difference detection range is limited to π because of its simple structure without flip flops.

3. TGCMOS based MUX PFD

To overcome the power consumption in large circuits on a single processor, it is prominent to optimize the designs at the levels of gates and small blocks. In general MUX based designs will consume less power [7]. In the literature a novel low-power multiplexer-based 1-bit full adder is presented which consumes 23% less power than the most power efficient 10-transistor adders and is 64% speedier than the fastest of all other tested adders. As a consequence, we designed a NOR gate of the PFD using a MUX. The concentration is not only on the power consumption the speed of the design also focused. Then we have chosen Transmission Gate CMOS to design the MUX to meet the efficiency in power and speed.

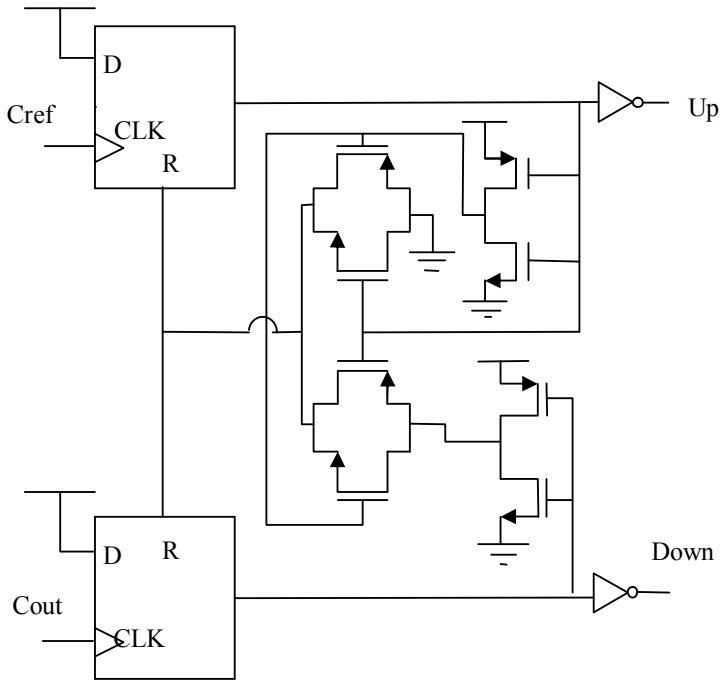


Fig 7. Dynamic PFD using TG CMOS

4. Results and Discussions

Different PFDs are simulated and verified the functionality using Tanner EDA tool. The power consumption and propagation delay of the designs are evaluated using HSPICE at 2.0V for 180nm technology. Among all the PFDs in terms of power consumption PFDNG has consumed less power 0.079mW because no gate was used in the design. Dynamic PFD has consumed high power, i.e. 0.781mW among the five designs as shown in Table 1.

Propagation delays of the PFD designs are calculated for each input and output of the designs. The worst case delays of the PFD are given in the Table 1. Dynamic TGCMOS PFD has shown high speed 2.1ps among the PFDs.

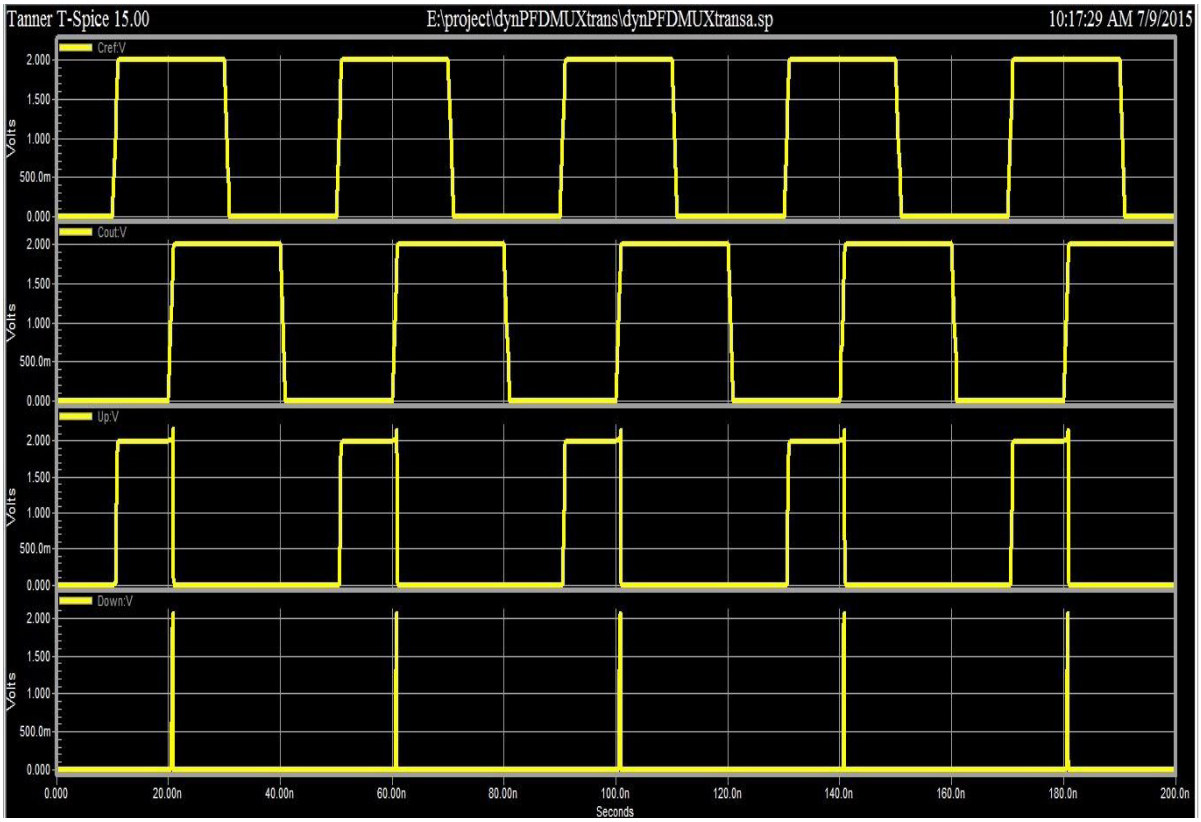
Power Delay Product (PDP) of the PFD designs are evaluated for energy efficiency of the designs. The proposed TGCMOS PFD shows energy efficiency among the rest of the design.

Table 1. Power and delay analysis of different PFDs

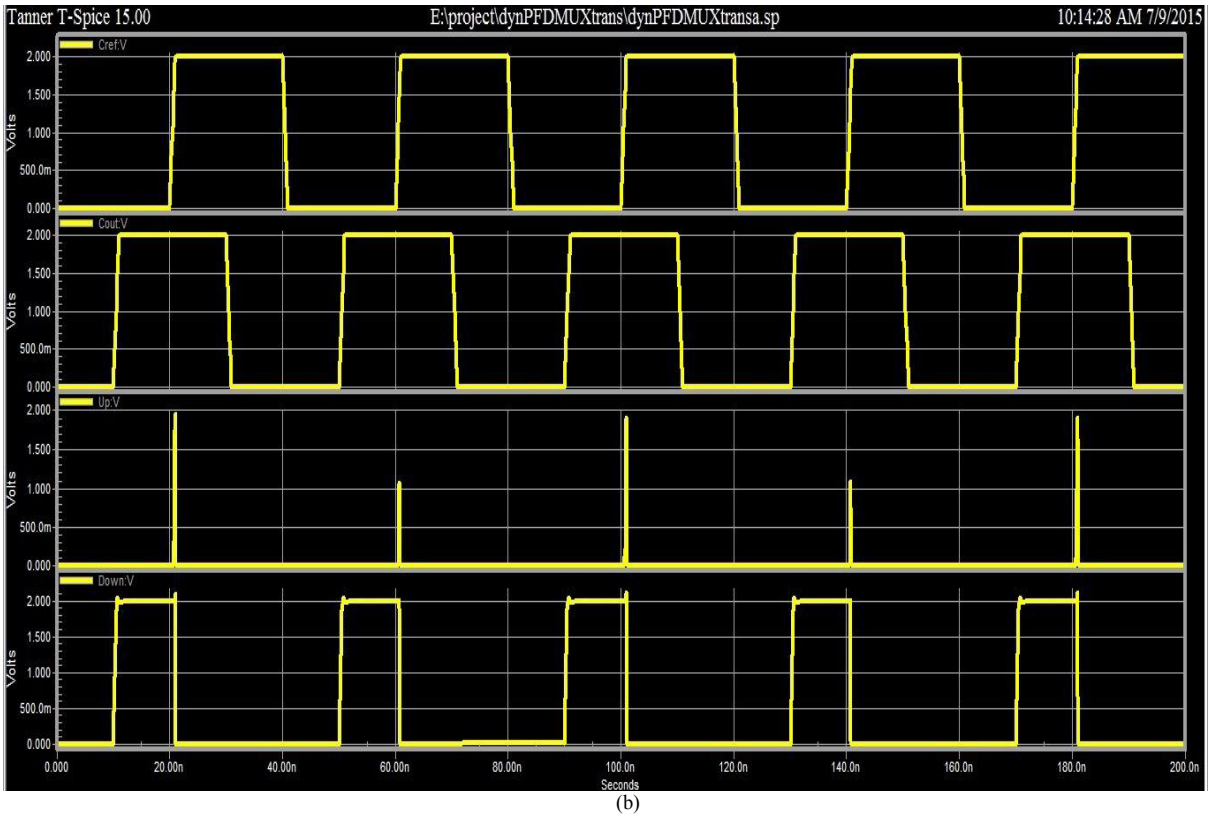
Different PFD designs	Power (mW)	Delay (ns)	PDP (10^{-12}) J	No. of MOS devices
Conventional	0.327	2.54	0.8305	22
PFDNG	0.079	20.53	1.6218	18
Dynamic	0.781	17.4	13.5894	20
PtPFD	0.113	2.49	0.2813	20
Dynamic TGCMOS	0.706	0.0021	0.00148	24

Though the MOS devices for TGCMOS PFD has 24 transistors it is the most efficient in terms of PDP.

The output waveforms of Dynamic TGCMOS PFD are as shown in fig 8. Two waveforms Cout and Cref arrive at the input pins with equal frequency, but unequal phases such that Cref leads Cout. As Cref goes high, output Up goes high. When the leading edge of Cout comes, Up goes to zero while Down does not show any change and remains low. Exactly the opposite thing happens when Cout leads Cref.



(a)



(b)

Fig. 8 (a). Cref leads Cout (b) Cout leads Cref

5. Conclusion

Phase Frequency Detector is the one of the vital block of the PLL design. PFD broadly affects the performance and power consumption of the PLL. To meet the low power and high speed PLL, different PFDs are evaluated for their performance and a PFD is proposed with these specifications using MUX with TGCMOS. TGCMOS MUX based PFD proved that the design is more energy efficient.

References

[1] J.S. Yuan, S. Chen, "Power amplifier resilient design for process and temperature variations using an on-chip PLL sensing signal,"Microelectronics Reliability 54 (2014) 167–171.

[2] Francisco Colodro, AntonioTorralba, "Frequency-to-digital conversion based on a sampled Phase-Locked Loop", Microelectronics Journal 44 (2013) 880–887.

[3] Hong-Yi Huang, Chun-ChiehWu, Ching-HsingLuo, "An MICS band frequency synthesizer using active inductor and auto-calibration scheme", Microelectronics Journal 43 (2012) 592–599.

[4] Dan H. Wolaver, "*Phase Locked Loop Circuit Design"*, Prentice Hall, Ch. 4, pp: 47-80.

[5] MhdZaher Al Sabbagh, B.S." 0.18µm Phase / Frequency Detector and Charge Pump Design for Digital Video Broadcasting For Handheld's Phase-Locked-Loop Systems," MS thesis, 2007.

[6] Youngshin Woo, Young Min Jang, and Man Young Sung, "A Novel Method For High- Performance Phase-Locked Loop," Journal of Circuits, Systems, and Computers, Vol. 13, No. 1 (2004) 53- 63.

[7] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer-Based Low-Power Full Adder", IEEE Transactions on Circuits and Systems—II: Express Briefs, Vol. 51, No. 7, July 2004, pp: 345-348.