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Effect of doping profiles on $Si/CoSi_2$ permeable base transistors

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Abstract. Permeable base transistors (PBT) with buried epitaxial $CoSi_2$ Gates have been fabricated by local high-dose cobalt ion-implantation, with subsequent rapid thermal annealing and homoepitaxial overgrowth by low-pressure vapor phase epitaxy. Transistors obtained by Co ion-implantations into low-doped n-type Si (100) as well as Si(111) show typical output characteristics with triode-like and pentode-like regions, depending on doping concentration and applied gate voltage. Pinch-off was observed at zero and at low negative gate voltages, respectively. Breakdown drain–source voltage exceeds 20 V for devices with 0.7 μm gate spacings and finger widths. A transconductance of 80 mS/mm has been obtained with PBTs on a low resistivity substrate, wherein the $CoSi_2$ gate was implanted into an epitaxial Si layer.

Keywords. PBT, permeable base transistor, Si PBT, Si(111) PBT, Si(100) PBT, silicon low-pressure vapor phase epitaxy, LPVPE, high dose ion-implantation, cobalt ion-implantation, cobaltdisilicide, cobaltsilicide, $CoSi_2$ $Si/CoSi_2/Si$ heterostructure.

1. Introduction

Because of their conceptual simplicity permeable base transistors (PBT) have been proposed for high-speed digital circuits [1] as well as for high-frequency, high-voltage amplifiers [2] and oscillators [3]. The PBT had been suggested by Lindmayer [4] in 1964, but not until 1979 it had been fabricated with an embedded tungsten grid in GaAs by Bozler et al. [5]. The first overgrown version in Si was built by Ishibashi et al. [6] in 1984, using heteroepitaxy of Si and $CoSi_2$. Until now these overgrown PBTs have reached transconductances g_m per gate finger length z of 50 mS/mm [7, 8], whereas the so-called etched-groove PBTs exhibit 155 mS/mm [9] and a transit frequency of 26 GHz [10]. This work describes the improved results of an overgrown $Si/CoSi_2/Si$ PBT version, obtained by mesotaxy [11], which has been first

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presented by the authors in 1990 [12]. In fabricating a PBT, mesotaxy, meaning the formation of an epitaxial silicide layer inside of a monocrystalline semiconductor by high-dose ion implantation and subsequent annealing, overcome two basic problems, namely, the lateral patterning and the heteroepitaxial overgrowth of the silicide. In addition, this process allows the fabrication of planar $Si/CoSi_2/Si$ heterostructures in Si(111) as well as in MOS-device compatible Si(100), which has not been achieved by any other growth technique so far.

2. Technology of the PBT

For our initial investigations we used n-type Si(100) and Si(111) wafers with doping concentrations of $5 \times 10^{15}\,cm^{-3}$ and $1 \times 10^{17}\,cm^{-3}$. Thermally oxidized wafers with 500–800 nm thick SiO_2 layers were patterned by optical lithography and reactive ion etching (RIE). The subsequent implantations were performed at energies of 100 keV and 200 keV with various doses in the range of $1.15–3.0 \cdot 10^{17}\,cm^{-2}$ at temperatures of 350°C to 400°C. In contrast to previous work [12], the oxide mask was not removed prior to annealing, because the buffered HF attacks the $CoSi_2$ precipitates, and thus the silicide stripes, which were formed during rapid thermal annealing (RTA), were often disintegrated or disconnected. An additional deposited SiO_2 cap layer protected the silicon surface from pin-hole formation during RTA at 750°C for 30 s and 1150°C for 10 s [13]. Depending on implantation dose and energy the $CoSi_2$ precipitates coalesce and form 40–60 nm thick epitaxial silicide layers, defining the gate length l_g of the PBTs. The SiO_2 was removed by wet chemical etching and the heterostructure was overgrown by low-pressure vapor phase epitaxy (LPVPE) at 800°C and 0.1 torr in a cold-wall reactor. The samples were cleaned ex situ by sulfuric acid with hydrogen peroxide and ammonium hydroxide with hydrogen peroxide and in situ by an annealing step at 800°C and 10^{-6} torr for 10 min. Figure 1 shows a cross-sectional transmission electron microscopy (TEM) picture of a buried silicide finger after epitaxial Si overgrowth, oriented parallel to a ⟨110⟩ direction. In Si(111) the edges of the fingers have an angle of about 70.7° (Fig. 2(a)), which indicate that the vertical border is parallel to a (111) plane. In Si (100) the edges are also aligned to the energetically favoured (111) planes, as proven by the 45° angle of the $CoSi_2$ edge in Fig. 2(b). The silicide embedded in both Si(100) and Si(111) have abrupt interfaces and the $CoSi_2$ layers are well integrated.

Underetching at the edges of the oxide stripes by chemical reaction of $CoSi_2$ with buffered HF, as shown in a previous work [8], and shadow and scattering effects in addition to high aspect ratios are disadvantageous for fabricating submicron PBTs with SiO_2 masks. So, a multilayer structure of SiO_2(50 nm)/W(230 nm)/Cr(50 nm) was successfully tested as implantation mask. Due to the larger stopping-power of Co in W, this mask can be made thinner than the pure SiO_2 mask. The thin oxide layer between Si and W prevents silicidation at the Si surface. Chromium serves as RIE mask for tungsten and oxide etching with

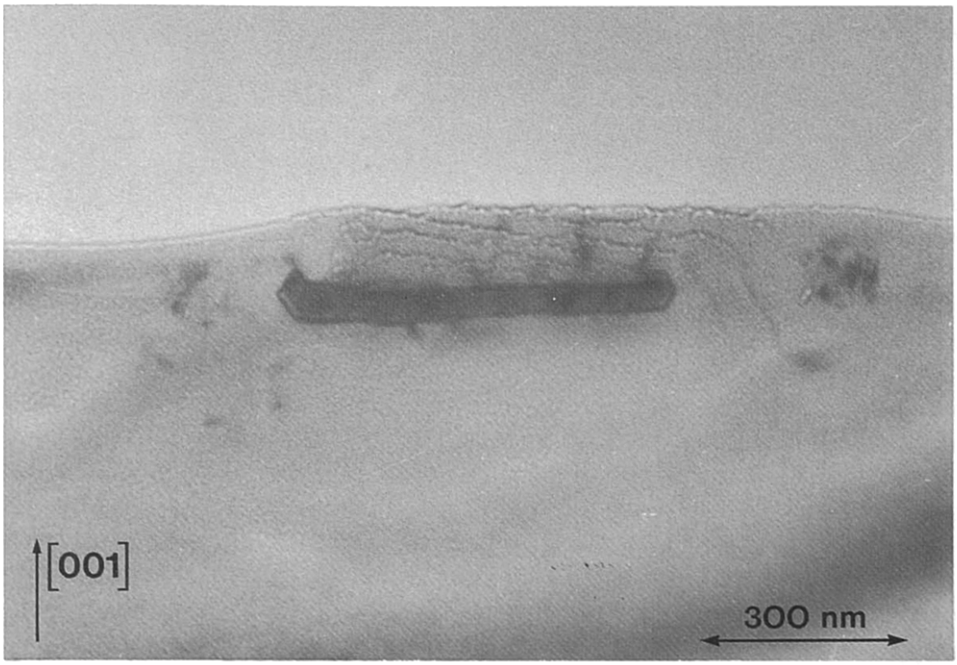

Fig. 1. Cross-sectional TEM micrograph of a 1 μm width buried $CoSi_2$ finger in Si(100) after epitaxial overgrowth (implantation dose: 1.15×10^{17} cm^{-2}, energy : 100 keV, $l_g = 40$ nm).

SF_6/CHF_3 and CHF_3, respectively. During Co implantation the complete chromium mask is sputtered away and the tungsten can be removed by wet chemical etching in a NH_4OH/H_2O_2 solution. Only a short etch in buffered HF is necessary to remove the thin oxide layer after the RTA process. A second litography step for metallization (Ti/Pt/Au) of the source contact followed. In order to fabricate the gate contacts the silicon was mesa etched by RIE using the top metallization as the mask. Then the drain contacts (Cr/AuSb/Cr) were evaporated. After this step DC measurements can be made obtained on the PBTs and the Schottky diodes. For high-frequency (HF) measurements the wafers were covered by a 1.2 μm thick polyimide layer serving as isolation and for the reduction of the gate capacitance of the needed additional contacts (Cr/Au). In order to connect the gate, source and drain contacts the polyimid layer was locally etched off by an oxygen plasma and a lift-off process defined the final structure for applying a HF probe-station.

3. PBT characterization

This work is focused on PBT operation, but to meet this goal, good Schottky diodes with high barrier heights, low leakage currents, high breakdown voltages and ideality factor near unity are important. The Schottky barrier heights (SBH) of buried $CoSi_2$ in Si obtained by ion-implantation is not known from literature, therefore we tried to determine them using current–

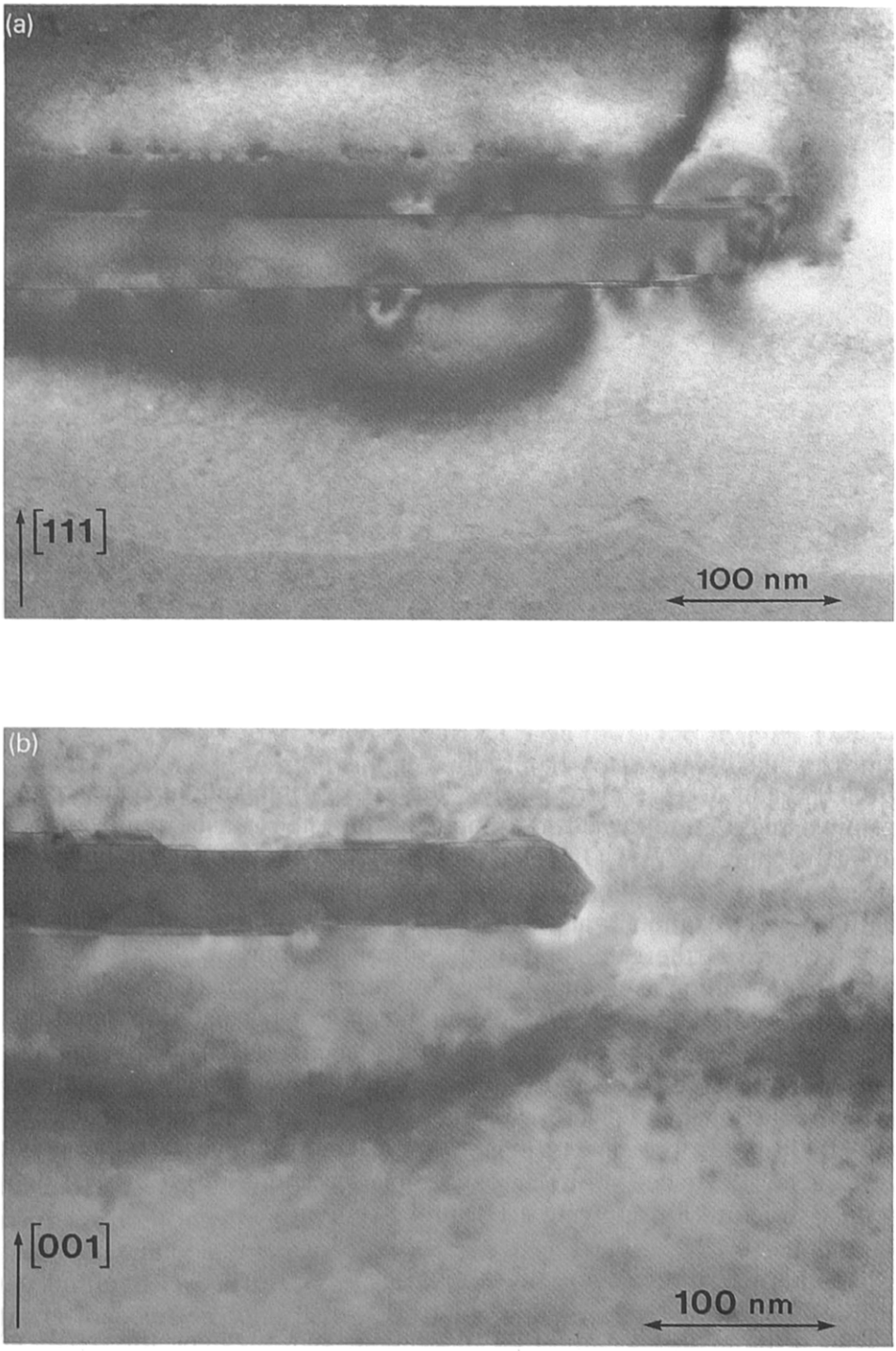

Fig. 2. Cross-sectional TEM, showing the edge performance of the silicide in (a) Si(111) and (b) Si(100) with the same fabrication parameters as Fig. 1.

voltage, capacitance–voltage and current–temperature measurements. Diodes with areas of 400 μm^2 to 250,000 μm^2 and various ideality factors in the range of 1.03–1.6 revealed values of 0.63–0.71 eV for the upper and 0.78 ± 0.03 eV for the lower $CoSi_2$/Si(100) interface diodes, whereas there exists nearly no difference in SBH (0.78 ± 0.03 eV) between the "up" and "down" Si(111) diodes, obtained by 200 keV implantations. For lower implantation energies and doses the SBH of the upper Si(111) diodes also decreases. Until now these phenomena have not been completely understood.

Nevertheless, PBTs on Si(100) and Si(111), fabricated by ion beam synthesis, revealed good electrical properties. Si(111) PBTs with a grid periodicity of 3 μm (1.5 μm gate finger width w and gate spacings b, respectively) exhibit a transconductance of 45 mS for a device with 3 mm gate finger length, demonstrating the homogeneity of the silicon silicide vertical interfaces. In addition, high breakdown voltages (Fig. 3) were obtained with Si(100) PBTs having a grid periodicity of 1.4 μm ($w = b$). As seen in the same figure for drain–source voltages less than 1.5 V this device operates as normally-off PBT. It is remarkable that pinch-off can be reached up to $V_{DS} = 18$ V and a low negative gate voltage of −2 V. These transistors with gate length of only 40 nm on low-doped substrates show, instead of the current saturation effect, typical triode-like behaviour corresponding with an undesired high output conductance g_D, which is a consequence of the punch-through effect in low-doped substrates. The high g_D in connection with high drain and source resistances reduces considerably the external transconductance [14]. So, it is not astonishing that the measured transconductance per total gate finger length of 19.5 mS/mm, as can be seen in Fig. 3(b), is approximately three times smaller than the

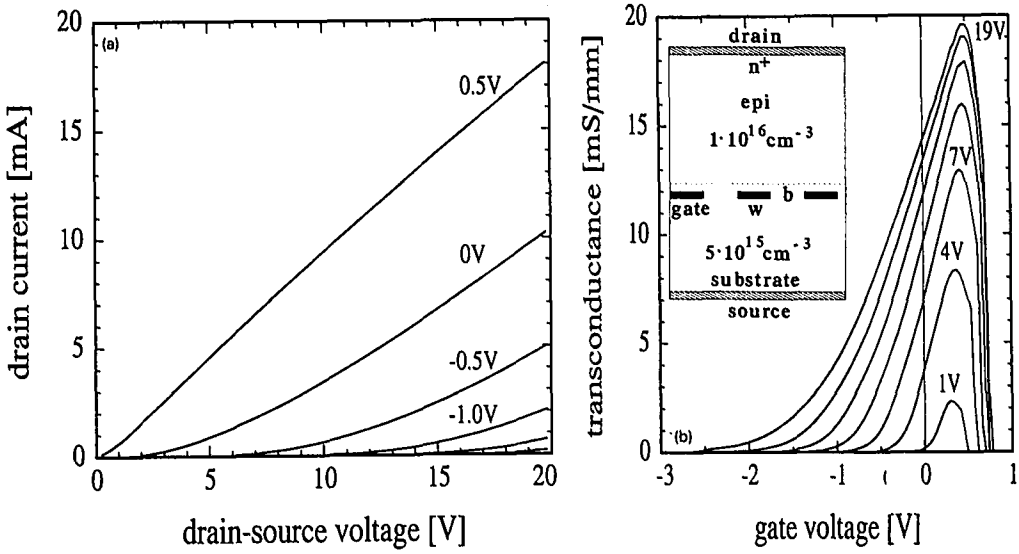

Fig. 3. PBT, measured in common-source circuit, with $l_g = 40$ nm, $b = w = 0.7$ μm and $z = 0.9$ mm: (a) output characteristics with gate voltage as parameter; (b) transconductance per gate finger length with drain–source voltage as parameter and as inset the doping profile.

theoretical value, estimated by the saturated velocity model [15]. In order to reduce parasitic resistances and g_D, PBTs were produced on low-resistivity (4 mΩ cm) Si(100) substrates by performing the ion implantation into a 420 nm overgrown epitaxial layer with a doping concentration of 4×10^{16} cm^{-3}. Figure 4 shows the output characteristics, the measured transcoductance g_m and the average doping profile of such a transistor, having a z of 300 μm. The maximum g_m in Fig. 4(b) exceeds 50 mS/mm and reaches 85% of its theoretical limit. Due to the relative low doping concentration (8×10^{15} cm^{-3}) of the 800 nm thick second epitaxial layer pinch-off was available despite the relatively large 1.0 μm gate spacings. To get a further increase in transconductance a sample with the doping profile shown in Fig. 5(b) was grown. The above described second epitaxy was substituted by a 3×10^{16} cm^{-3} doped layer and indeed, the transconductance increases to values of 80 mS/mm (Fig. 5(b)), but due to the bad combination of doping concentration and 1 μm gate spacings no pinch-off has been available (Fig. 5(a)). Figures 3(a), 4(a) and 5(a) demonstrate the influence of doping concentration on PBT output characteristics: with increasing doping concentration the drain current saturation increases, if one neglects the additional ohmic current of the noncontrollable part of the current channel between the gate fingers in the third device (Fig. 5). The distances between the output characteristics for various gate voltages become more equidistant for increasing doping concentration, as aspected. These tendencies agree well with the computer simulations in [3] for non-constant doping profiles. From the first high-frequency S-parameter measurements at non-optimized 2 μm grid periodicity PBTs a f_t of 1.6 GHz was observed for a device with a reduced transconductance of 13 mS/mm.

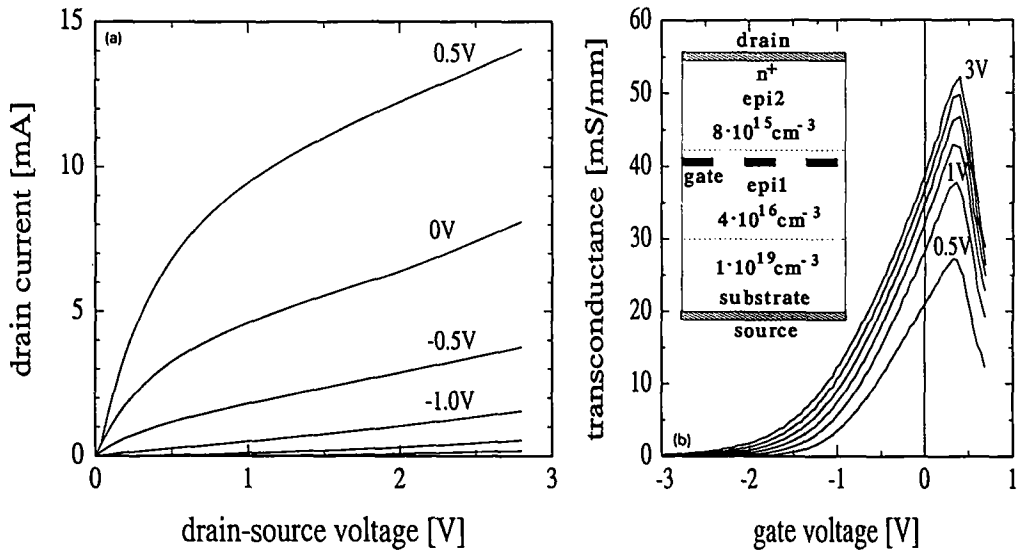

Fig. 4. PBT, measured in common-source circuit, with $l_g = 40$ nm, $b = 1$ μm, $w = 2$ μm and $z = 0.3$ mm: (a) output characteristics with gate voltage as parameter; (b) transconductance per gate finger length with drain–source voltage as parameter and as inset the doping profile.

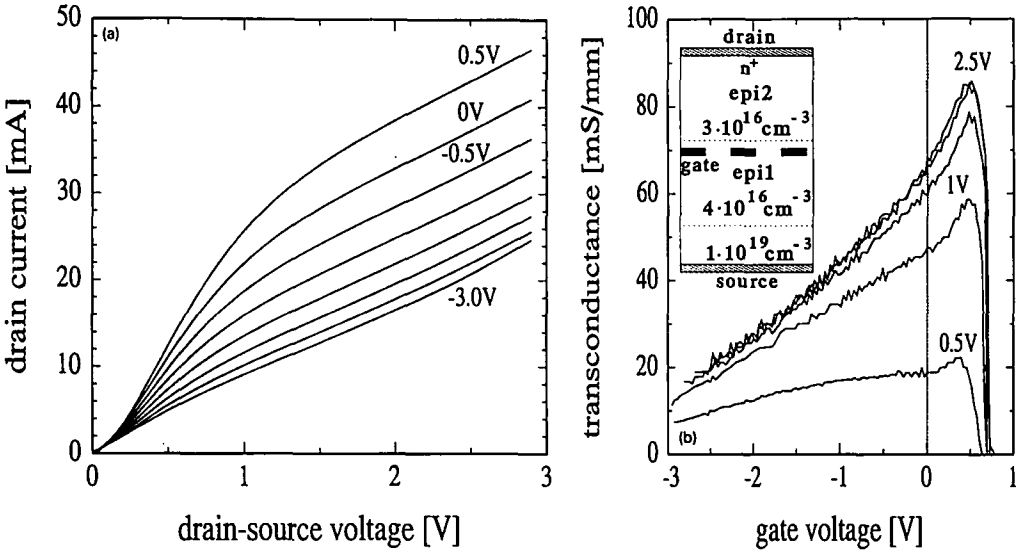

Fig. 5. PBT, measured in common-source circuit, with $l_g = 40$ nm, $b = w = 1$ μm and $z = 0.15$ mm: (a) output charactereistics with gate voltage as parameter; (b) transconductance per gate finger length with drain–source voltage as parameter and as inset the doping profile.

4. Conclusion

The successful fabrication of PBTs by ion beam synthesis of buried, epitaxial $CoSi_2$ in Si(100) as well as Si(111) has been demonstrated. The metallic silicide grid inside the monocrystalline silicon was obtained by local high-dose cobalt ion-implantation and using only homoepitaxial overgrowth. Breakdown voltage greater than 20 V indicate the possibility of high-voltage applications for PBTs. For Si(100) PBTs with 1 μm gate spacings a transconductance of 50 mS/mm and pinch-off was observed. In addition, the measured maximum g_m of 80 mS/mm is the highest published value for overgrown Si PBTs, until now. Scaling down the lateral patterning in combination with optimizing the doping profile should lead to further increase of the transconductance and improved high frequency performance.

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References

[1] C.O. Bozler and G.D. Alley, The permeable base transistor and its application to logic circuits, *Proc. IEEE* **70**(1) (1982) 46–52.

[2] G.D. Alley, High-voltage two-dimensional simulations of permeable base transistors, *IEEE Trans. Electron Devices* **ED-30** (1983) 52–60.
[3] D.D. Rathman, Optimization of the doping profile in Si permeable base transistors for high-frequency, high-voltage operation, *IEEE Trans. Electron Devices* **37**(9) (1990) 2090–2098.
[4] J. Lindmayer, The metal gate transistor, *Proc. IEEE* **52** (1964) 1751.
[5] C.O. Bozler, Fabrication and microwave performance of the permeable base transistor, *Int. Tech. Dig.* **25** (1979) 384–387.
[6] K. Ishibashi and S. Furukawa, A Si permeable base transistor by metal/semiconductor hetero-epitaxy, *Int. Electror Devices Meeting*, 1984, pp. 868–870.
[7] N. Nakamura, T. Oshima and K. Nakagawaand M. Miyao. Fabrication of $Si/CoSi_2/Si$ permeable base transistor using self-aligned and two step molecular beam epitaxy, Extended abstracts of the *21st Conf. on Solid State Devices and Materials*, Tokyo, 1989, pp 85–88.
[8] A. Schüppen, S. Mantl, L. Vescan, S. Woiwod, R. Jebasinski and H. Lüth, Permeable base transistors with ion-implanted $CoSi_2$ gate, *Mater. Sci. Eng.* **B12** (1992) 157–160.
[9] A. Gruhle and H. Beneking, Silicon etched-groove permeable base transistors with 90-nm finger width, *IEEE Electron Device Lett.* **11**(4) (1990) 165–166.
[10] A. Gruhle, P.A. Badoz, F. Chevalier, A. Halimaoui, F. LAlanne, M. Mousi, J.L. Regolini, G. Vincent and D. Bensahel, Silicon etched-groove permeable base transistor fabrication with cutoff frequencies (f_T, f_{max}) above 25 GHz, in: M. Ilegems and M. Dutoit (eds.), *Solid State Device Research 91*, (Proc. 21th Eur. Solid State Device and Research Conf.— ESSDERC '91, MONTREUX, Switzerland, September 1991), Elsevier, Amsterdam, 1991, pp. 27–30; *Microelectron. Eng.* **15** (1991) 27–30.
[11] A.E. White, K.T. Short, R.C. Dynes, J.P. Garno and J.M. Gibson. "Mesotaxy: single-crystal growth of buried $CoSi_2$ layers, *Appl. Phys. Lett.* **50** (2) (1987) 95–97.
[12] A. Schüppen, S. Mantl, L. Vescan and H. Lüth, A permeable base transistor on Si(100) with implanted $CoSi_2$ Gate, *Proc. 20th Eur. Solid State Device and Research Conf.— ESSDERC '90*, 1990, pp. 45–48.
[13] K. Radermacher, S. Mantl, K. Kohlhof, and W. Jäger. Temperature and energy dependence of ion-beam synthesis of epitaxial $Si/CoSi_2/Si$ heterostructures, *J. Appl. Phys.* **68**(6) (1990) 3001–3008.
[14] H. von Känel, J. Henz, M. Ospelt, and A. Gruhle, The permeable base transistor, *Phys. Scr.* **T35** (1991) 287–292.
[15] S.M. Sze. Physics of semiconductor devices. John Wiley and Sons, New York, NY, 1981.