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An automatic phase error compensating multiphase LC oscillator: analysis and design

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Abstract In this work a self phase error compensating multiphase LC oscillator is proposed. Mismatches in LC tanks are considered as the main source of phase errors. Considering this, an analytical approach is proposed to find a relationship between phase errors and their corresponding coupling factors as a necessary condition for phase error cancellation then a self compensating circuit is proposed accordingly. The compensation circuit first detects the phase errors then employs them in a current tuner to change each stage coupling factor to reduce phase errors. The building blocks of the proposed circuit are investigated and the transistor level implementation of each one is presented afterwards. The theoretical results are evaluated and confirmed through simulations using ADS software in 0.18 μm CMOS technology. Simulation results show that not only phase errors are reduced with respect to the previous methods but also this procedure does not impose any further power consumption and phase noise to the circuit.

Keywords Multiphase LC oscillators · Phase errors · Fabrication mismatches · Coupling factors · Wireless communications

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1 Introduction

The problem of generating sinusoidal waveforms with accurate phase difference has drawn a lot of attentions lately because of their key role in applications such as image-reject, zero-IF and low-IF receivers [1–3]. So implementing multiphase oscillators as the key building blocks in many wireless communication systems is of important concern [4]. Furthermore, the need for multiphase clocks in frequency multipliers based on edge combination [5], frequency synthesizers and fractional-N dividers [6] is inevitable. Also in receivers downconverting high frequency signals using signals at much lower frequency than them is possible by multiphase oscillators [7, 8]. Moreover, multiphase oscillators can be also employed in high speed samplers and clock and data recovery circuits, either [9].

Several methods have been proposed to implement multiphase oscillators. One common way is using ring oscillators [10–14] but they have the disadvantage of poor phase noise characteristics [10, 11]. Frequency dividers which work at N times of the desired frequency [15] are another approach to generate multiphase outputs but they have the difficulty of high frequency signal production. Another method to create multiphase outputs lies on the possibility of coupling several LC tanks by transistors [16]. Because of the filtering characteristics of the LC tanks, phase noise in the mentioned structure is improved considerably [17] so it can be a good choice for multiphase generation.

The applications of multiphase oscillator usually need accurate phase differences among the outputs. For example, phase inaccuracies can limit the ability of eliminating image frequencies [18] in the image rejection receivers. Therefore, compensating methods should be devised in order to reduce them [6, 19]. Studies show that fabrication

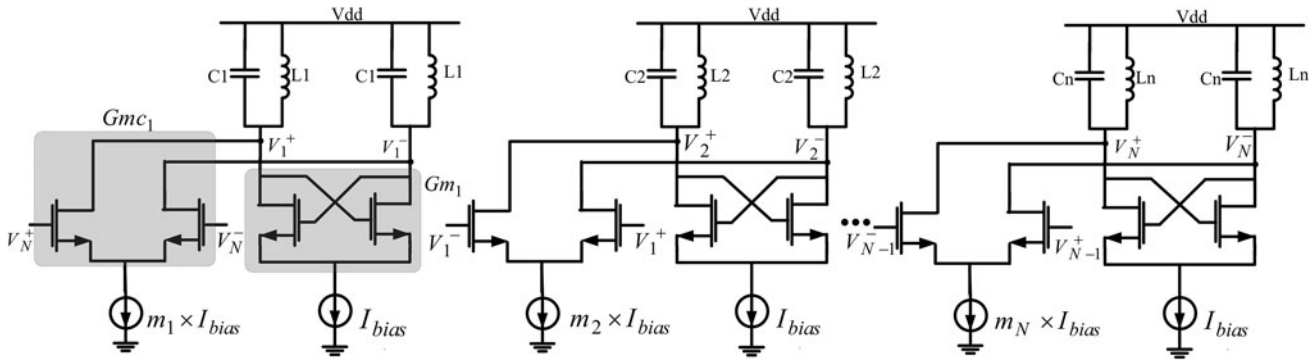


Fig. 1 Multiphase LC oscillator [16]

mismatches among the elements of LC tanks can be the major factor for phase error [16]. References [20–22] investigate and estimate phase and amplitude errors in a quadrature oscillator. In [23] a new method is presented for reducing quadrature phase and amplitude errors considering different coupling factor for each stage. Despite of previous works like [20] the traditional tradeoff between phase error and phase noise is cancelled in [23]. Reference [24] used the mentioned method to design a phase and amplitude tunable quadrature oscillator. Because of the complexity of the equations, same procedure as [24] cannot be employed for multiphase oscillators with more than 2 stages. Reference [16] analyzed phase errors in an N-stage multiphase LC oscillator and proposed some methods to reduce them but using these methods increases both the power consumption and phase noise of the circuit. In this work we extract a novel method (circuit) to automatically reduce phase errors while phase noise performance of the circuit is improved. The key parameter here is to change the coupling factors in each stage with respect to its corresponding phase error. Also the compensation circuit consumes no additional power.

The rest of the paper is organized as follows: in Sect. 2 multiphase LC oscillators are briefly described and essential equations for approaching to the proposed method are extracted. In Sect. 3, needed blocks for implementing the self compensating circuit is introduced. In Sects. 4 and 5 power consumption and phase noise of the circuit is investigated and in Sect. 6 simulation results are presented and at last in Sect. 7 the most important results of this work are summarized.

2 Proposed method

The schematic of a multiphase LC oscillator is shown in Fig. 1.

As shown in Fig. 1, the first stage composed of two networks. G_{m_1} network is basically in charge of creating a negative resistance to compensate the losses caused by parasitic resistances of inductor and capacitor of each stage. By adding G_{mc_1} network, signal can go through other stages and create different output phases. Note that the same structured networks exist in each stage. m_1,m_2,…,m_n are tail currents ratios of Gmc_n and Gm_n networks in each stage and they are called coupling factors. When there are no mismatches, for having no phase and amplitude errors, coupling factors should be chosen equally to symmetrize the circuit. Considering this and the Barkhausen criteria for oscillation [25], the phase difference between two successive stages can be found as (1).

$$\Delta\theta = \frac{\pi}{N}, \tag{1}$$

where $\Delta\theta$ is the phase difference between two successive stages and N is the number of stages.

Considering the first stage phase equal to zero (reference phase), every stage phase can be expressed by (2).

$$\theta_n = (n-1)\frac{\pi}{N}, \tag{2}$$

where θ_n is the phase of nth stage.

Note that (1) and (2) are not true in the presence of fabrication mismatches. Here, first an analytical approach is described and using it a simple equation is extracted for reducing phase errors (difference between the output phase found by (2) and the real one) then a self compensating circuit is proposed to implement the mentioned equation.

We assume the selectivity of the tanks high enough so the output voltages can be considered sinusoidal with very good approximation [20], and can be expressed in phasor form. Therefore for every stage, (3) can be written.

$$V_{o_n}^{\pm} = -Z_{nRLC}(j\omega) \times I_n^{\pm}, \tag{3}$$

where $V_{o_n}^{\pm}$ is the output voltage phasor and $I_n^{\pm}$ is the current phasor passing through each tank and Z_{nRLC} is the LC tank impedance of the nth stage and can be found by (4).

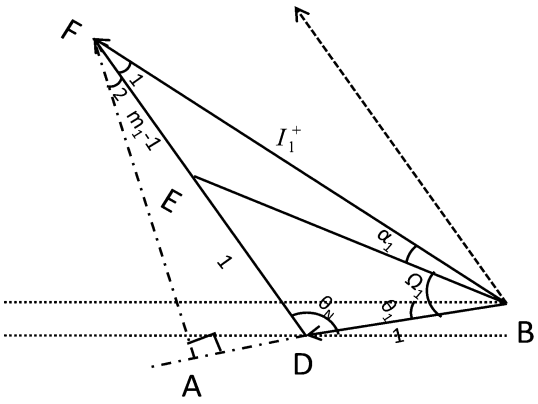


Fig. 2 Phasor diagram of I_1^+

$$Z_{nRLC}(j\omega) = \frac{1}{\frac{1}{R_{pn}} + j\left(\omega C_n - \frac{1}{\omega L_n}\right)}, \tag{4}$$

where ω is the oscillation frequency, L_n and C_n are the nth stage inductor and capacitor values respectively and R_{pn} is the equal parallel resistance of the tank which results of L_n and C_n parasitic resistances.

The phasor form for output voltages is as (5).

$$V_{o_n}^+ = A_n \angle \theta_n, \tag{5}$$

where A_n is the output voltage amplitude. (The equations will be extracted using $V_{o_n}^+$ but the same sayings are true for $V_{o_n}^-$).

In this steady state oscillation, transistors operate in the large signal regime and behave much like switches so the injected current into each tank assumed to be square wave [23]. The harmonic of current involved in oscillation can be found using (6) and (7).

$$I_1^+ = \frac{2}{\pi} I_{\text{bias}}[(1\angle\pi + \theta_1) + (m_1 \angle \theta_N)], \tag{6}$$

$$I_n^+ = \frac{2}{\pi} I_{\text{bias}}[(1\angle\pi + \theta_n) + (m_n \angle \pi + \theta_{n-1})] \quad 1 < n \le N, \tag{7}$$

where I_{bias} is the Gm_n network tail current (see Fig. 1).

In order to find a way to reduce phase errors, first we need to apply the phase condition for (3). For this purpose the phase of (6) and (7) should be found.

Figure 2 shows the phasor diagram of I_1^+ (the term $(2/\pi)I_{\text{bias}}$ is neglected because it has no effect on the current phase. Note that the phasor diagram for I_n^+ yields to the same results).

According to Fig. 2, the phase of I_1^+ can be found using (8).

$$\angle I_1^+ = \pi + \theta_1 - (\alpha_1 + \Omega_1), \tag{8}$$

where Ω_1 can be found immediately by (9).

$$\Omega_1 = \frac{\pi - (\theta_N - \theta_1)}{2}. \tag{9}$$

Considering the fact $\theta_N - \theta_1 \approx \pi - \frac{\pi}{N}$, for finding α_1, (10) can be written.

$$\sin\alpha_1 = \frac{(m_1 - 1)}{\sqrt{1^2 + 1^2 + 2\cos(\pi - \frac{\pi}{N})}} \frac{\tan(F_1)}{\sqrt{1 + \tan^2(F_1)}}. \tag{10}$$

Equation (11) can be written using Fig. 2.

$$\tan(F_1 + F_2) = \frac{\overline{AD} + 1}{\overline{Af}} = \frac{1 + m_1 \cos\frac{\pi}{N}}{m_1 \sin\frac{\pi}{N}}. \tag{11}$$

Using (11) and considering the fact $F_2 \approx \frac{\pi}{2} - \frac{\pi}{N}$, we can write (12).

$$\tan(F_1) = \frac{\sin\left(\frac{\pi}{N}\right)}{m_1 + \cos\left(\frac{\pi}{N}\right)}. \tag{12}$$

Using (10) and (12) will lead us to (13).

$$\sin\alpha_1 = \frac{(m_1 - 1)\cos\left(\frac{\pi}{2N}\right)}{\sqrt{m_1^2 + 2m_1\cos\left(\frac{\pi}{N}\right) + 1}} \tag{13}$$

For small values of α_1, (13) is reduced to (14).

$$\alpha_1 = \frac{(m_1 - 1)\cos\left(\frac{\pi}{2N}\right)}{\sqrt{m_1^2 + 2m_1\cos\left(\frac{\pi}{N}\right) + 1}} \tag{14}$$

Note that using the same approach for other stages will lead to the same equation and the general rule can be extracted for calculating α_n as (15).

$$\alpha_n = \frac{(m_n - 1)\cos\left(\frac{\pi}{2N}\right)}{\sqrt{m_n^2 + 2m_n\cos\left(\frac{\pi}{N}\right) + 1}} \tag{15}$$

In fact α_n is a parameter that relates the current phase to the coupling factor of each stage and by changing coupling factors one can control the phase of current injected to each tank.

Therefore, by using (8) and (9), the Phase of I_1^+ can be found as (16).

$$\angle I_1^+ = \frac{\pi}{2} + \frac{\theta_1}{2} + \frac{\theta_N}{2} - \alpha_1 \tag{16}$$

By using the same approach we can find the phase of I_n^+ using (17).

$$\angle I_n^+ = \pi + \frac{\theta_{n-1}}{2} + \frac{\theta_n}{2} - \alpha_n \quad 1 < n \le N \tag{17}$$

Applying the phase condition for (3) will lead us to (18) and (19).

$$\varphi_1 - \alpha_1 = \frac{\pi - (\theta_N - \theta_1)}{2}, \tag{18}$$

$$\varphi_n - \alpha_n = \frac{\theta_n - \theta_{n-1}}{2} \quad 1 < n \leq N, \tag{19}$$

where φ_n is the LC tank phase and can be found by (20).

$$\varphi_n = \tan^{-1}\left[\frac{R_{pn}(1 - L_n C_n \omega^2)}{L_n \omega}\right]. \tag{20}$$

Using (1) and considering the fabrication mismatches, the phase difference between two successive stages can be modeled as (21) and (22).

$$\pi - (\theta_N - \theta_1) = \frac{\pi}{N} + \psi_{e_1}, \tag{21}$$

$$\theta_n - \theta_{n-1} = \frac{\pi}{N} + \psi_{e_n} \; 1 < n \leq N, \tag{22}$$

where ψ_{e_1} is the phase error between Nth and first stage and $\psi_{e_n} (n \neq 1)$ is the phase error between $(n-1)$th and nth stage.

Clearly for satisfying Barkhausen criteria (23) must be fulfilled.

$$\sum_{n=1}^{N} \psi_{e_n} = 0 \tag{23}$$

Replacing (21) and (22) in (18) and (19) respectively results to (24).

$$\varphi_n - \alpha_n = \frac{\pi}{2N} + \frac{\psi_{e_n}}{2} \tag{24}$$

Equation (24) expresses a relationship among the phase of nth stage LC tank, the phase of the current passing through it and the phase error of nth stage. As shown in (15), the value of α_n can be tuned by changing the coupling factor of the corresponding stage. So according to (24) changing α_n would change ψ_{e_n}. Clearly for having a phase error less oscillator we should have (25).

$$\varphi_n - \alpha_n' = \frac{\pi}{2N}, \tag{25}$$

where α_n' is the new α_n that reduces the phase error.

Replacing (25) in (24) will lead us to (26).

$$\alpha_n' = \alpha_n + \frac{\psi_{e_n}}{2} \tag{26}$$

In extracting (26) from (24) and (25), φ_n considered to be constant. In fact according to (20) the value of φ_n depends on the tank elements (which remain constant) and the oscillation frequency. The oscillation frequency can be found using (27) [16].

$$\omega = \sqrt{\omega_{res}^2 + \left(\frac{\omega_{res}}{2Q}\frac{m\sin(\Delta\theta)}{1 + m\cos(\Delta\theta)}\right)^2} - \frac{\omega_{res}}{2Q}\frac{m\sin(\Delta\theta)}{1 + m\cos(\Delta\theta)}, \tag{27}$$

where ω_{res} is the LC tank resonance frequency, Q is the tanks' quality factors and $m = m_1 = \ldots = m_n$ (coupling factors which considered equal for all stages). Note that (27) is extracted considering a symmetric circuit without any mismatches. According to (27) the oscillation frequency changes by changing the coupling factors but because of the small nature of phase errors, a small change in α_n (and therefore m_n) is needed to reduce them so the frequency deviation is small and can be neglected (this will be confirmed through simulation) so φ_n can be considered constant.

Using (26), one can compensate phase errors resulting from circuit elements mismatches. For this purpose first phase error between two successive stages should be measured and added to α_n to find α_n'. Then α_n' should be translated to m_n'(the corresponding value for α_n' according to (15)) and change the tail current of the Gmc_n network. The block diagram of an N stage self compensating oscillator is shown in Fig. 3. Note that ψ_{e_n} is defined between $n-1$ and nth stage so by correcting one stage phase the phase difference between two stages is corrected.

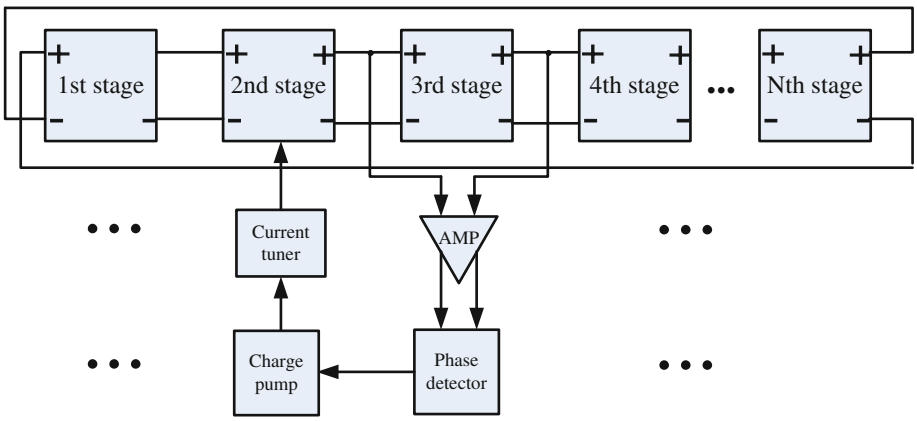


Fig. 3 The self compensating oscillator block diagram

3 Circuit level implementation of the compensating circuit

As shown in Fig. 3, first the sinusoidal output voltages of two successive stages are converted to square ones using amplifiers so they can be fed to phase detectors. Then the phase detector produces an output square voltage proportional to the phase error between the corresponding stages, after that the charge pump and current tuner blocks adjust the Gmc_n network tail current so that the phase error is compensated. In the following section we describe the transistor level design of each block in Fig. 3.

3.1 Amplifier

The amplifier circuit converts the sinusoidal voltages into square ones enabling the detector circuit to detect the phase difference between two successive stages. The mentioned circuit is shown in Fig. 4.

For having larger bandwidth, the output swing of the amplifier is increased using large tail current (I_b) instead of large resistors ($R_{1,2}$). Doing so will increase the power consumption of the circuit but in this work we employed a method to hold the power consumption unchanged. This method is explained more in Sect. 3.4.

3.2 Phase detector

Phase detector, PD, generates a square waveform with a duty cycle proportional to the phase difference between its inputs. Schematic of the used phase detector is shown in Fig. 5 [26].

Also, like the amplifier circuit the output swing is increased by using large tail current instead of a large resistor because larger bandwidth is desired. Note that as will be explained in Sect. 3.4 the tail current increase does not impose a power penalty to the circuit.

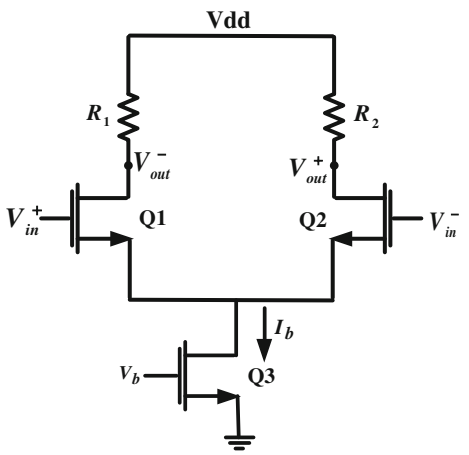


Fig. 4 The amplifier circuit

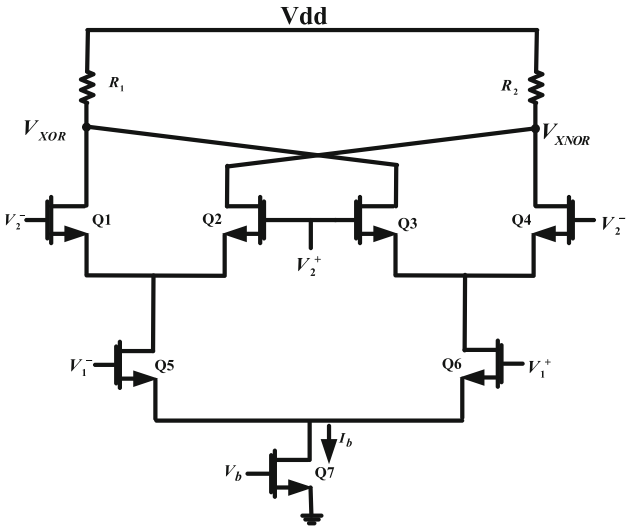


Fig. 5 The phase detector circuit

3.3 Charge pump

The charge pump circuit creates a DC signal (V_{tun}) proportional to the phase difference of phase detector's input waveforms. Figure 6 shows the schematic of the charge pump circuit.

As shown in Fig. 6, V_{XNOR} from phase detector is fed to the input of charge pump circuit. When V_{XNOR} is high then the capacitor C_p is discharged through Q3 and when it is low, C_p is charged through Q4. According to (1) phase difference between two successive stages should be equal to $\frac{\pi}{N}$ which results the duty cycle of V_{XNOR} to be equal to $(N-1)/N$. Therefore when there are no mismatches in order to hold V_{tun} constant I_p must be $(N-1)$ times greater than I_N.

3.3.1 Dynamic of the charge pump

Figure 7 shows the transient behavior of charge pump circuit in presence of a phase error occurring in t = 0.

A linear estimation is used to measure the voltage change resulting from phase error.

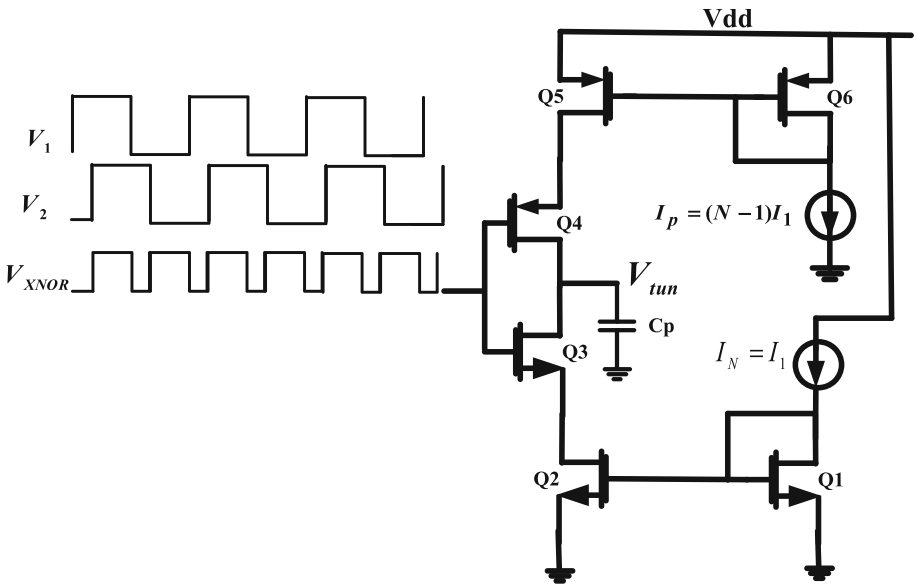
As it is clear in Fig. 7 the slope of voltage is equal to tan(α) in a period of V_{XNOR} waveform. Equations (28) and (29) can be written considering Figs. 6 and 7.

$$V_{\text{rise}} = (N-1)\frac{I_1}{C_p}t_{\text{rise}}, \tag{28}$$

$$V_{\text{fall}} = \frac{I_1}{C_p}t_{\text{fall}}, \tag{29}$$

where V_{rise} and $V_{\text{fall}}$are the amount of increase and decrease in the V_{tun} in a period of V_{XNOR} respectively and t_{rise}, t_{fall}

Fig. 6 The charge pump circuit



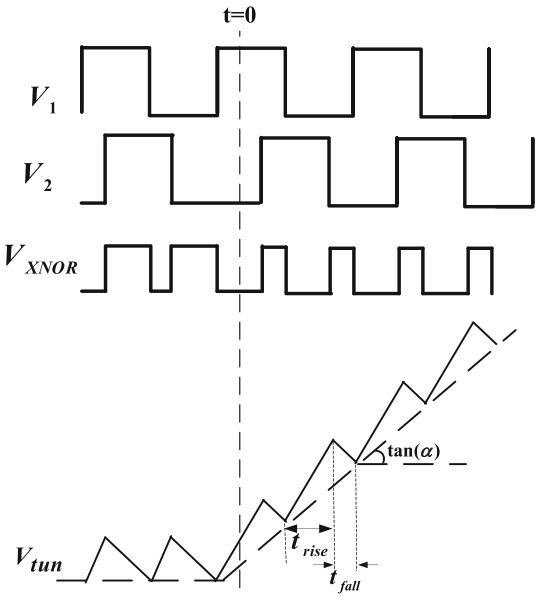


Fig. 7 Transient behavior of charge pump circuit in the presence of phase error

are the rise and fall time (see Fig. 7). Also, I_1 and C_p are introduced in Fig. 6. Equations (30), (31) and (32) can immediately be found considering Fig. 7.

$$t_{\text{rise}} + t_{\text{fall}} = T_{\text{XNOR}}, \tag{30}$$

$$t_{\text{rise}} = \frac{T_{\text{XNOR}}\Delta\varphi}{\pi}, \tag{31}$$

$$t_{\text{fall}} = \frac{T_{\text{XNOR}}(\pi - \Delta\varphi)}{\pi}, \tag{32}$$

where T_{XNOR} is the period of V_{XNOR} and it is equal to half the period of the oscillator output and $\Delta\varphi$ is the phase difference between two successive stages. Using (28)–(32) will lead us to (33) and (34).

$$V_{\text{rise}} = \frac{I_1}{C_p}\frac{T_{\text{XNOR}}}{\pi}(N-1)\Delta\varphi, \tag{33}$$

$$V_{\text{fall}} = \frac{I_1}{C_p}\frac{T_{\text{XNOR}}}{\pi}(\pi - \Delta\varphi) \tag{34}$$

The slope of voltage increase in the capacitor C_p can be found as (35) using (33) and (34).

$$tg(a) = \frac{V_{\text{rise}} - V_{\text{fall}}}{T_{\text{XNOR}}} = \frac{I_1}{C_p}\frac{N}{\pi}\psi_{e_n} \tag{35}$$

So considering (35), the change in C_p voltage can be found as (36).

$$\Delta V_{\text{tun}}(t) = \frac{I_1}{C_p}\frac{N}{\pi}\psi_{e_n}(t) \tag{36}$$

where $\Delta V_{\text{tun}}(t)$ is the change in V_{tun} because of the phase error. (See Fig. 6).

3.4 Current tuner

In Sect. 3.3.1 we found $\Delta V_{\text{tun}}(t)$ as a function of ψ_{e_n}. To build a phase compensating circuit $\Delta V_{\text{tun}}(t)$ should be used to change the value of α_n to reach to α_n' (see Eqn. (26)). Therefore $\Delta V_{\text{tun}}(t)$ should be equal to the variation of $\alpha_n(\alpha_n' - \alpha_n)$. Using (26) and (36) leads us to (37).

$$\frac{I_1}{C_p}\frac{N}{\pi}t = \frac{1}{2} \tag{37}$$

For (37) to be true, t (which stands for time) should be tuned. Therefore the charge pump circuit in Fig. 6 should be modified to Fig. 8.

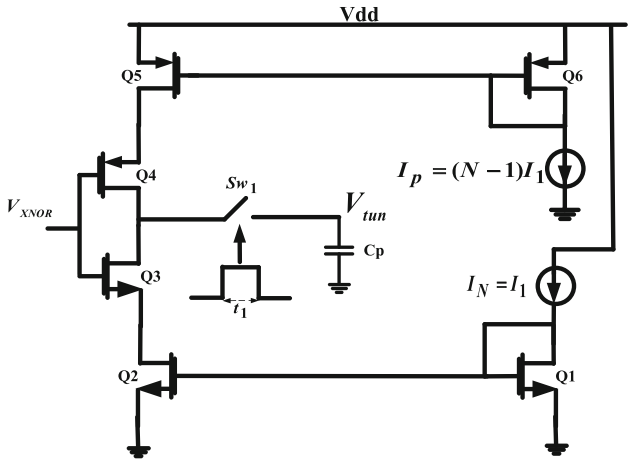


Fig. 8 The modified structure of Fig. 6

In Fig. 8 the Switch SW_1 is ON only for the limited time interval of t_1 to satisfy (37). Using this method also reduces the power consumption of the circuit. Because after t_1, SW_1 must switch off, other compensation circuits such as amplifiers and phase detectors can be disabled as well as the charge pumps so in the steady state none of them impose any further power consumption to the circuit. Therefore as it mentioned in Sects. 3.2 and 3.3 tail currents can be increased for increasing output swing of amplifiers and phase detectors without being concerned about the increase of circuit power consumption.

In order to design the current tuner we need to extract an equation for m_n with respect to α_n using (15). Limiting the case for 3, 4 and 5 stage oscillators shows that considering a second order estimation for (15) yields to equations with 99.9 % accuracy, the following equations can be extracted for these oscillators.

$$m_n = 1.715\alpha_n^2 + 2.089\alpha_n + 1.005 \text{ 3 stage oscillator}, \quad (38)$$

$$m_n = 1.001\alpha_n^2 + 1.614\alpha_n + 1.005 \text{ 4 stage oscillator}, \quad (39)$$

$$m_n = 0.945\alpha_n^2 + 1.566\alpha_n + 1.005 \text{ 5 stage oscillator}, \quad (40)$$

These estimations are made considering m_n to change only from 0.4 to 1.6 which is enough for phase error correction because of the small nature of phase errors.

The general form of (38)–(40) is as (41).

$$m_n = A\alpha_n^2 + \mathrm{B}\alpha_n + \mathrm{C} \quad (41)$$

where A, B and C are the constants defined in (38)–(40). The proposed circuit to convert α_n into m_n and create the Gmc_n network tail current for each stage is shown in Fig. 9.

According to Fig. 9, (42) can easily be derived.

$$m_n \times i_{bias} = kV_{C_p}^2(t) + 2k\left(V_{C_p}(0) - V_{th}\right)V_{C_p}(t) + k\left(V_{C_p}(0) - V_{th}\right)^2 + i_{Q_2} \quad (42)$$

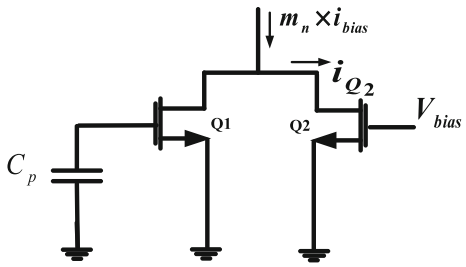


Fig. 9 The proposed circuit to convert α_n into m_n

where $V_{C_p}(0)$ is the initial voltage of C_p, $V_{C_p}(t)$ is the voltage variations of C_p resulting from the compensation circuit, V_{th} is the threshold voltage of Q1, i_{Q_2} is the bias current of Q2 and K is defined as (43).

$$k = \frac{1}{2}\mu_n Cox\frac{w}{l} \quad (43)$$

where μ_n is the electron mobility, Cox is the gate oxide capacitance per unit area and $\frac{w}{l}$ is the aspect ratio of Q1.

Therefore by equalizing (41) and (42) and considering i_{bias} equal to 1 mA, the needed parameters to design circuit of Fig. 9 according to (38)–(40) can be derived. The term i_{bias} as a constant value is added to the left side of (42) to attain consistent units in both sides.

4 Power consumption

As mentioned previously, because the phase compensation circuits (amplifiers/phase detectors/…) need only operate during a limited time interval, they are disabled and consume no power in steady state. Therefore, the only parameter which changes after compensation is Gmc_n network tail current. Using (26) and (41), (44) and (45) can be written.

$$i_n = A\alpha_n^2 + B\alpha_n + C \quad (44)$$

$$i_n' = A\left(\alpha_n'\right)^2 + B\alpha_n' + C = A\left(\alpha_n + \frac{\psi_{e_n}}{2}\right)^2 + B\left(\alpha_n + \frac{\psi_{e_n}}{2}\right) + C \quad (45)$$

where i_n and i_n' are the Gmc_n tail currents before and after compensation, respectively. Subtracting (44) from (45) will lead us to (46).

$$\Delta i_n = \frac{A}{4}\left(\psi_{e_n}\right)^2 + \left(A\alpha_n + \frac{B}{2}\right)\psi_{e_n} \quad (46)$$

where Δi_n is the current difference of Gmc_n before and after compensation.

Because of the small nature of phase errors and the value of A being approximately equal to 1 (see (38)–(40))

the first term of (46) can be neglected. Therefore the overall change of Gmc_n network currents can be found using (47).

$$\text{Total current change} = \sum_{n=1}^{N} \Delta i_n = \left(A\alpha_n + \frac{B}{2}\right) \sum_{n=1}^{N} \psi_{e_n} \tag{47}$$

Using (23) in (47) will result into the total current change of zero so after compensation, power consumption of the circuit remains unchanged.

5 Phase noise analysis

As explained before, in the steady state mode the compensating circuits (amplifiers, phase detectors, charge pumps) are disabled so they cannot have any contribution in the phase noise. Therefore we can predict phase noise of oscillator outputs will not change considerably. In fact the only changes in oscillator after compensation is the change of Gmc_n network tail current which is not much because of the small nature of phase errors and cannot change phase noise considerably. (This will be confirmed through simulation in Sect. 6).

6 Simulation results

To evaluate the proposed structure a 3, 4 and 5 stage oscillator is designed using 0.18 µm technology in ADS software. (As mentioned in the introduction, quadrature phase tuning is investigated in [24] and here we pay attention to the oscillators with more than 2 stages). The simulation is performed considering different mismatches in a range from 1 to 10 % between the inductor of the first stage and other stages but the same results can be extracted considering the same percent mismatches for capacitors.

Table 1 shows the values for different elements of the oscillator and proposed compensating circuits.

Figures 10, 11 and 12 show the simulation results for 3,4 and 5 stage oscillators in 1–10 % mismatch range, respectively and compare the proposed method with what references [16, 20] proposed to reduce the phase errors (increase of coupling factors). As shown, the proposed method has a better effect in reducing phase errors. Although because of the approximations made to achieve (15) and (26), the compensation circuit has a limited ability to reduce phase errors but according to Fig. 10, 11 and 12 it yields to better results compared to previous methods and has no tradeoffs with power consumption and phase noise performance of the oscillator.

Table 2 shows the different values for oscillation frequency versus coupling factors. As it can be seen the oscillation frequency does not change much so the assumption made in Sect. 2 to consider φ_n constant for achieving (26) is accurate.

Furthermore, despite the proposed method, increasing coupling factors will result in the increase of power

Table 1 Different element values for circuit implementation

Parameter	Value	Unit
Inductance (L_n) of LC tank	8	nH
Capacitance (C_n) of LC tank	0.5	pF
Quality factor (Q) of LC tank	4	–
(W/L) for oscillator transistors	10/0.18	µm/µm
(W/L) for amplifier transistors	10/0.18	µm/µm
(W/L) for phase detector (XOR) transistors	2/0.18	µm/µm
Tail currents (I_{bias}) of oscillator	1	mA
Coupling factors before compensation	1	–
Bias current of amplifiers	2.5	mA
Bias current of phase detectors (XOR)	1.25	mA
Bias current (I_1) of the charge pump circuits	0.16	mA
Capacitor (C_p) of the charge pump circuits	0.01	nF

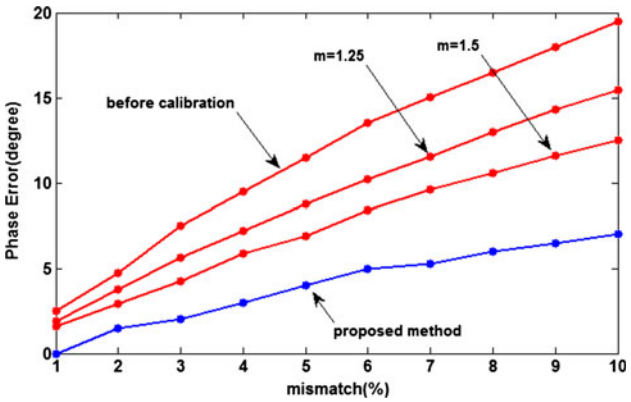


Fig. 10 ψ_{e_1} versus different values of mismatches in a 3 stage oscillator

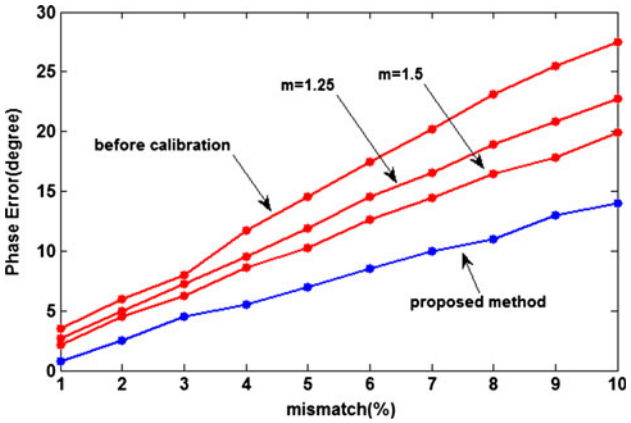


Fig. 11 ψ_{e_1} versus different values of mismatches in a 4 stage oscillator

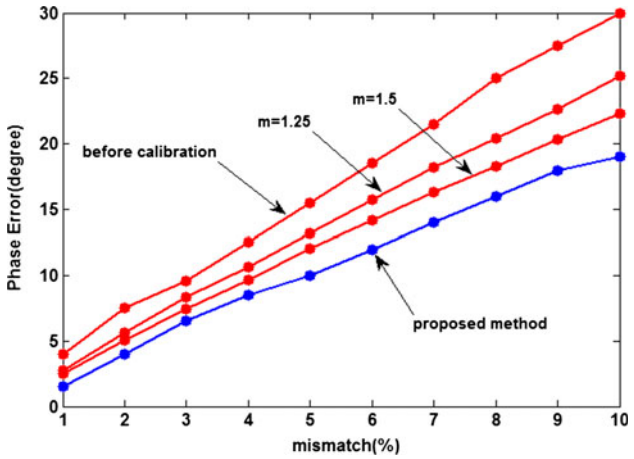


Fig. 12 ψ_{e_1} versus different values of mismatches in a 5 stage oscillator

Table 2 Oscillation frequency values versus different coupling factors

m_n	0.4 (GHz)	0.7 (GHz)	1 (GHz)	1.3 (GHz)	1.6 (GHz)
3 Stages	2.5	2.53	2.57	2.61	2.64
4 Stages	2.47	2.50	2.52	2.53	2.54
5 Stages	2.45	2.47	2.48	2.49	2.5

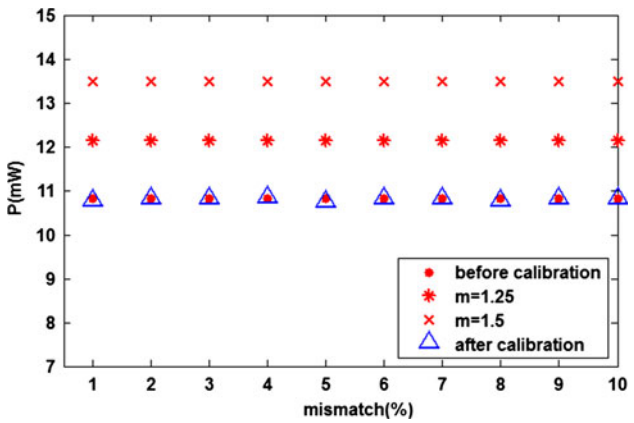


Fig. 13 Circuit power consumption versus different values of mismatches in a 3 stage oscillator

consumption. The power consumption simulation results for the mentioned oscillators are shown in Figs. 13, 14 and 15.

It is mentioned in Sect. 5 that the proposed method would not change phase noise significantly. The simulation results for phase noise in 3, 4 and 5 stage oscillators are shown in Figs. 16, 17 and 18 for 100 kHz frequency offset, respectively. It can be seen that the phase noise resulting from the proposed method is improved compared to the other compensation methods. These results were predictable because according to [16] by increasing coupling

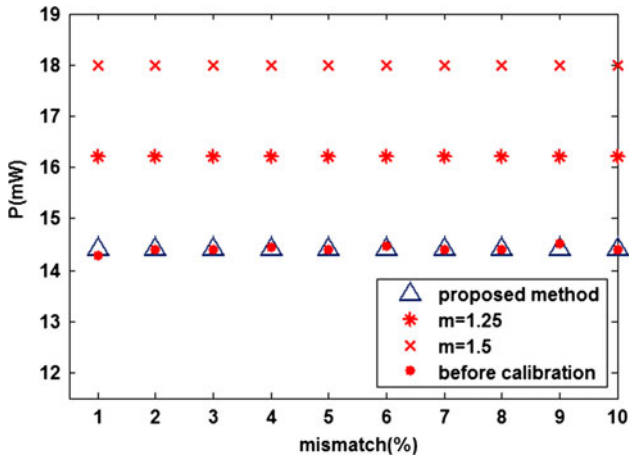


Fig. 14 Circuit power consumption versus different values of mismatches in a 4 stage oscillator

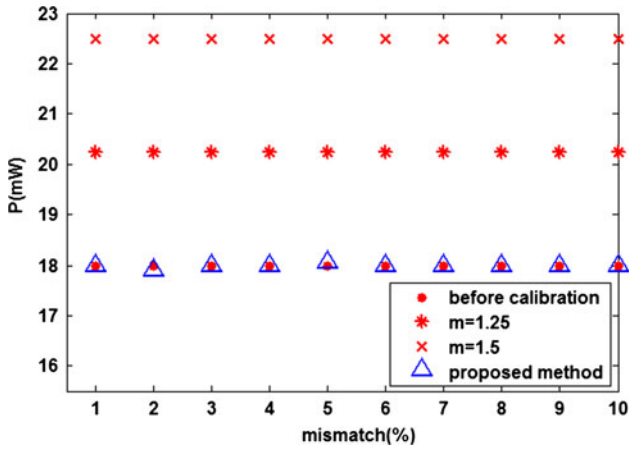


Fig. 15 Circuit power consumption versus different values of mismatches in a 5 stage oscillator

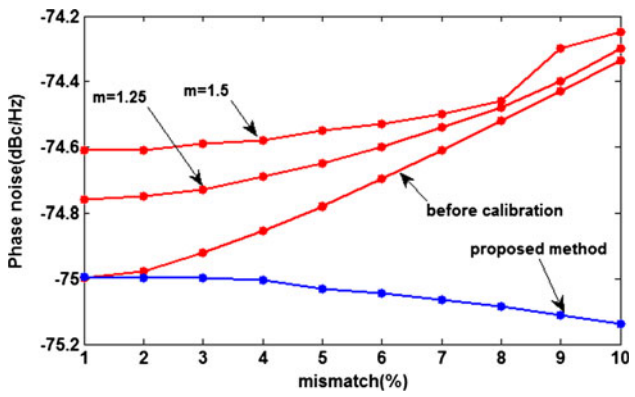


Fig. 16 Phase noise versus different values of mismatches in a 3 stage oscillator at 100 kHz frequency offset

factors, phase noise will increase but in this work the proposed method will not impose any further phase noise to the oscillator. So, the traditional tradeoff between phase noise and phase error in multiphase oscillators is cancelled.

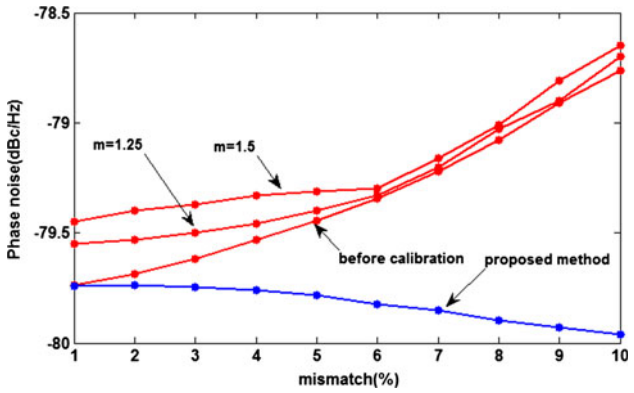


Fig. 17 Phase noise versus different values of mismatches in a 4 stage oscillator at 100 kHz frequency offset

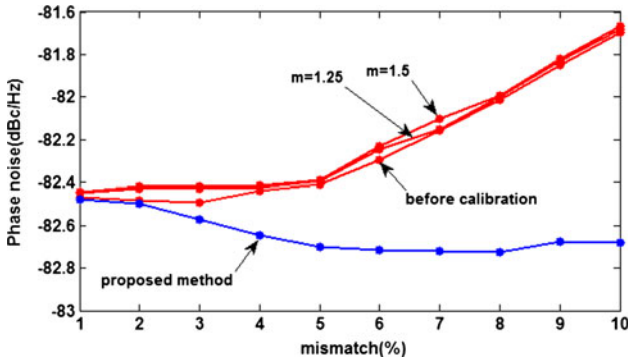


Fig. 18 Phase noise versus different values of mismatches in a 5 stage oscillator at 100 kHz frequency offset

7 Conclusion

In this work we present a novel method to reduce phase errors for N-stage multiphase LC oscillators considering different fabrication mismatches for inductors and capacitors of the LC tanks. (Which considered as the main sources of phase deviations.) The mentioned method is automatic and reduces the phase errors independent of their values and it is completely compatible with the unpredictable nature of fabrication mismatches. Moreover, the proposed method will not change the power consumption of the circuits and the output phase noises are even improved slightly. Therefore, the traditional tradeoff between phase noise and phase error is cancelled in this work.

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