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# Feasibility study of 25 V SiGe RF-power transistors for cellular base station output amplifiers

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**Abstract**

For 2+ GHz-bandwidth applications, the commonly used bipolar Si RF-power transistors in the output amplifiers in cellular base stations for mobile communications are pushed to the limit of performance. The objective of this work was to study the feasibility of using SiGe/Si grown on pre-processed Si wafers for power-HBTs operating at 25 V for improved performance. The large size HBT devices ($2 \times 0.1$ mm$^2$) were processed using an existing 100 mm poly-Si emitter RF power BJT technology with Au metallization and some necessary modified steps for SiGe implementation. The base layers with designed Ge and B profiles were deposited either by MBE or CVD. The devices showed very high $BV_{cbo}$ ($>80$ V) with very low leakage currents. The current gain was very stable over a wide $I_C$ range, and weakly influenced by the environmental temperature. At 2 GHz, the CW output power of 20 W (at 25 V) was obtained with an efficiency of 68% in class AB operation. The long-term temperature stability was excellent. SiGe RF power-HBTs could be operated at full output power for an extended time without any external temperature bias compensation, which is virtually impossible with conventional Si-BJTs. 

*Keywords:* Bipolar transistor; Power amplifier; Heterojunction; Epitaxy; SiGe; Si

## 1. Introduction

Si RF-power bipolar transistors (BJT) are commonly used in the output amplifiers in cellular base stations for mobile communications. Using a 25 V supply voltage, such devices can deliver typically 5–60 W output power. For 2+ GHz-bandwidth applications, the bipolar Si RF-BJTs are pushed to the limit of performance. The devices are operated in the gain fall-off region close to $f_T$, where power, gain and efficiency deteriorate rapidly as the operating frequency is further increased. With the continuing development of mobile and wireless communications, there is a need for improved semiconductor devices for the new system.

Heterojunction bipolar transistors (HBT) using a thin and heavily doped SiGe layer as the base have shown better frequency performance than conventional Si BJTs. SiGe-devices have thus received much attention for various high-frequency mobile and wireless applications. Low-voltage SiGe-based RF-ICs have been made commercially available, but very few studies on RF power applications have been published. Nevertheless, some positive results were reported for SiGe-power-HBTs operated in the bandwidth range of 1–6 GHz. In 1996, Schüppen et al. [1] demonstrated SiGe low-voltage power HBTs with >70% PAE at 900 MHz and 45% PAE at 2 GHz. For high-power high-voltage SiGe-HBTs, the first small-signal characterization was published in 1995 by Hobart et al. [2]. In 1996, 230 W pulsed SiGe-HBTs operating at 2.8 GHz for military radar applications was reported [3]. In 1997, M/A-COM reported a 5–10 V 6 GHz device for radar applications, which was also characterized at 1.88 GHz for direct comparison with existing technologies for base station power transistors [4].

The objective of this work was to study the feasibility using SiGe/Si heterostructures pseudomorphically grown on pre-processed Si wafers for SiGe-power-HBTs for 25 V RF-base station type of applications. The main challenge is whether strained SiGe layer materials grown by MBE or CVD could have high enough quality for the RF power applications and the long-term stability under stress of a high electric field.

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Another study presented in this communication is the temperature dependence of the current gain, $\beta$, for SiGe-base transistors. For a normal Si-BJT, the temperature derivative of $\beta$ has a large positive value, which causes problems with the device stability at high current levels. With a proper design of the n-Si/p-SiGe emitter–base (e–b) heterojunction, the $\beta$ increase of a SiGe-HBT at high temperature can be much smaller, or even with a negative temperature coefficient, which thus decreases the need for emitter ballasting and improves the gain [5].

## 2. Device design and processing

### *2.1. Summary of the process flow*

The devices in this study were manufactured using an existing 0.8 μm poly-Si emitter RF power BJT (25 V operation) technology with Au metallization. The baseline flow was extended with several additional steps for SiGe implementation.

$n^+$-Si(100) wafers with an n-type ($5–6\times10^{15}$ cm$^{-3}$) 6.5 μm thick CVD epi-layer on top were used as the substrate. Processing started by forming a poly-buffered fully recessed oxidation isolation for defining the active device area. The LOCOS oxidation was carried out in two steps. Approximate 1.8 μm of field oxide was first grown, followed by a low-dose B implantation in the device regions close to the LOCOS edge for achieving a junction termination to improve the breakdown voltage of the base–collector (b–c) junction. A second oxidation was subsequently made to increase the total field oxide thickness to 2.8 μm. Thereafter, diffused resistors for ballasting were formed by implanting B into resistor areas.

An epitaxial Si/SiGe/Si base was deposited either by molecular beam epitaxy (MBE) or chemical vapor deposition (CVD), in the batch of eight wafers for each run, with desired layer parameters as will be shown in Section 2.2. The samples grown by a Balzers UMS-630 Si MBE apparatus [6] had very good layer uniformity with minimum parameter tuning for achieving desired device performance. CVD growth [7] was carried out using an ASM Epsilon 2000 reactor. The CVD method has a quite small process window, and thus requires careful tuning and analysis of parameters when new profiles are to be implemented. This CVD system is aimed for commercial production, but for the limited deposition in this work it was not a crucial factor.

After SiGe deposition, processing continued with dry-etching removal of deposited Si and SiGe on field areas. Thereafter, a double layer stack of 25 nm oxide and 110 nm silicon nitride was deposited by low-temperature CVD on top of the structure. In this layer, small stripe windows (0.8 μm wide, spaced 1.4 μm apart), which are vias for emitter and base contacts to the base layer, were opened by dry etching. A 250 nm poly-Si was deposited, patterned and dry-etched for forming emitter and base contact fingers (1.3 μm wide, 0.9 μm separation). Using two different resist masks, every second poly-Si finger was implanted with a high dose of As or B. The whole structure was then covered with a TEOS/nitride cap, and annealed in an RTP equipment at 975 °C for 45 s, to activate and drive-in the dopants in the emitter and base contacts.

The nitride was then removed. A 50 nm of TEOS was deposited, patterned and opened by dry etching for forming contact holes on top of the emitter and base poly-Si fingers. The metallization consisted of a thin layer of PtSi for low-contact resistance, a sputtered TiW layer as a barrier, and $\sim 1$ μm of Au produced by electroplating [8].

The fabrication process finished with passivation using plasma-CVD nitride, and a 30 min heat treatment at 425 °C at forming gas ambient for alloying the metal/semiconductor contacts. Before evaluation in RF-power packages, the wafers were thinned to 110–115 μm using back grinding, in order to reduce the thermal resistance of the device, and a thin layer of Au was deposited by sputtering on the backside. A schematic presentation of the cross-section and an SEM overview of the processed HBT are depicted in Fig. 1(a) and (b).

### *2.2. Design of base profiles*

To study the profile influence on the current gain of the RF-power transistor, devices with three different base profiles were designed and manufactured.

Profile #1 consisted of a laterally shifted double box profile, as shown in Fig. 2(a) (the emitter will be formed to the left, and the collector is to the right). Starting with a 10 nm buffer layer on top of the collector, 10 nm undoped $Si_{0.88}Ge_{0.12}$, 20 nm $Si_{0.88}Ge_{0.12}$ containing a B concentration of $5\times10^{18}$ cm$^{-3}$, 20 nm B-doped Si ($N_B = 5\times10^{18}$ cm$^{-3}$), and finally an undoped 15–40 nm Si layer on top of the structure were grown.

The profile is designed so that the b–c junction will occur in the SiGe layer, which improves the Early voltage. The e–b junction is outside the SiGe-profile, thus the $\beta$-increase from the HBT is also small (only 2–3 times). The thicknesses of the top i-Si and i-SiGe layers are given by the outdiffusion of B and Ge from the base layer. We tried to estimate the exact layer thicknesses using simulation tools, but were not confident about the results, since the quality of the diffusion models are not good for this kind of structure. The layer thicknesses must therefore be tuned experimentally.

Profile #2 aims at improving the high-frequency performance by grading the Ge content in the base,

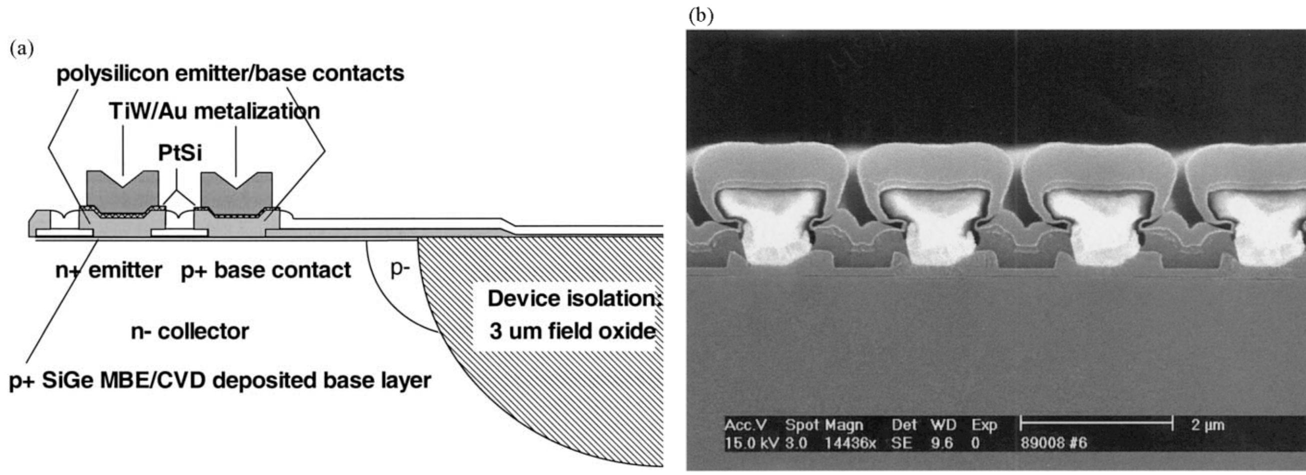


Fig. 1. (a) Schematic cross sectional drawing, showing part of repeated e–b structure (left) and device isolation (right); and (b) SEM micrograph of the processed SiGe RF power HBT, showing repeated e–b structure only.

from 5% Ge concentration close to the emitter to 15% close to the collector. The trapezoidal SiGe layer is uniformly doped by $5 \times 10^{18}$ cm$^{-3}$ of B.

Profile #3 is a modification of profile #1, where the Ge profile over the b–c junction has been extended 10 nm beyond the B-doped base layer towards the emitter, in order to provide a significant amount of Ge at the e–b junction, and thus further change the temperature characteristics of the transistor.

## 3. Results and discussion

In order to obtain a large current handling capability, multiple finger design for emitters and base-contacts was chosen. The largest device contains $570 \times 0.9$ µm pairs of fingers. The b–c junction is nominally over an area of $2 \times 0.1$ mm$^2$, which thus demands very high quality growth of the p-SiGe layer by MBE or CVD. A hard breakdown at $\sim 80$ V with very low leakage current was obtained for nearly all tested device samples for the reverse biased b–c junction with an open emitter configuration, $BV_{cbo}$, which corresponds well with the expected avalanche breakdown voltage governed by the doping concentration at the under-lying CVD epi-layer ($\sim 6 \times 10^{15}$ cm$^{-3}$). This is an indication for a good quality of epilayer growth, i.e. no dislocations were generated at the substrate–epi-layer interface and in the SiGe layer during the thermal processing steps.

Typical $I$–$V$ characteristics measured with the common-emitter configuration are shown in Fig. 3(a) for an MBE grown SiGe-HBT with a trapezoidal Ge profile (profile #2, $x = 0.05$–$0.15$). The measured breakdown voltage with an open base circuit, $BV_{ceo}$, is $> 25$ V. The transistor reveals very good saturation behavior, and the derived Early voltage is $\geq 270$ V. Fig. 3(b) shows the Gummel plot of the same HBT. The collector current, $I_C$, exhibits an almost ideal behavior over a large $V_{be}$ range, and the derived ideality factor is 1.02. The base current increase is however influenced by the bias, where $n = 1.9$ for $V_{be} \leq 0.6$ V and $n = 1.1$ in the range of 0.6 V $< V_{be} \leq 0.7$ V. Although the increase of both $I_b$ and $I_c$ is getting slow for $V_{be} > 0.7$ V due to effects of large current injection and series resistance, the current gain was nearly constant over a wide $I_C$ range.

Similar DC characteristics were obtained from CVD grown SiGe-HBTs. The analysis showed that the active B doping concentration in these HBTs was likely a

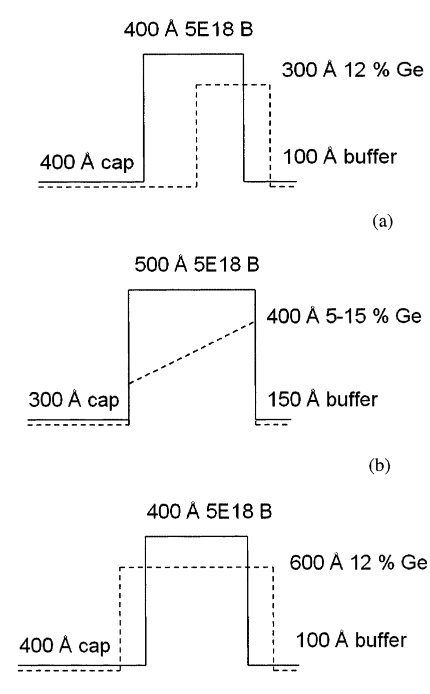


Fig. 2. Three different base profile designs.

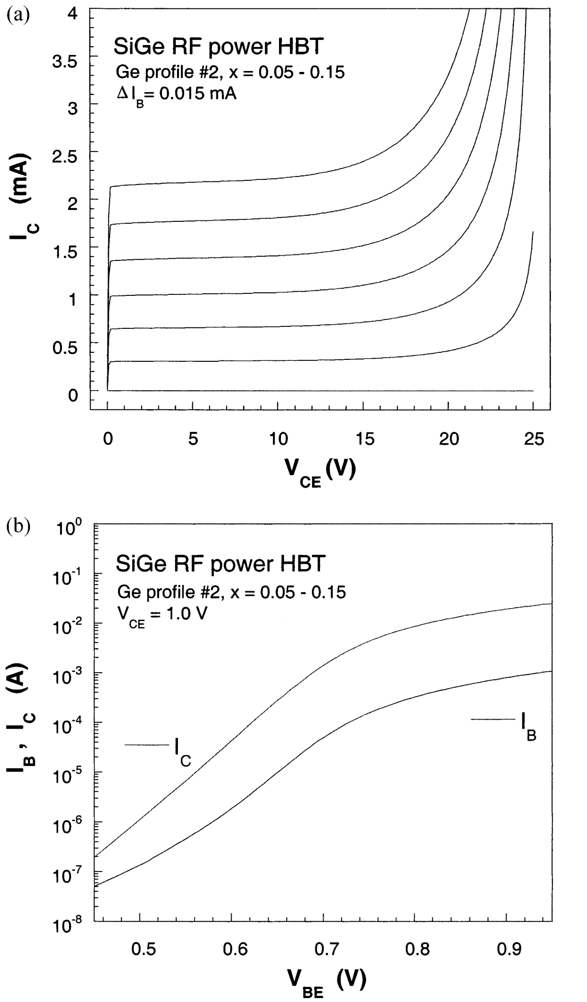


Fig. 3. (a) $I$–$V$ characteristics; and (b) the Gummel plot of an MBE grown SiGe RF power HBT with the common-emitter configuration.

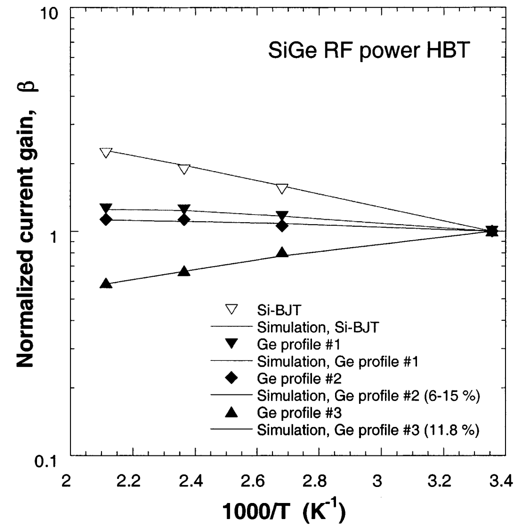


Fig. 4. Current gain values of the SiGe-power-HBT, normalized to one measured at room temperature, are plotted as a function of the operation temperature. For a comparison, data for a conventional Si RF power transistor are also shown.

factor of two lower than the desired value, which in turn resulted in a higher $\beta$ value but a lower Early voltage ( $\sim$ 72 V). The results of DC evaluations for all processed large area transistors with three different base profile designs are summarized in Table 1. Most of the measured breakdown voltages were following the specification, indicating a good control of the epi-growth and that no problem was introduced by the manufacturing steps. For a comparison, results for a Si RF power BJT fabricated using the base-line flow with implanted base are also depicted in the table.

The temperature dependence of the $\beta$ value for HBTs with three different designed base profiles was carefully studied. The measurements were performed at the temperature of 27, 100, 150, and 200 °C, respectively, with e–b sweeping voltage from 0.7 to 1.1 V on medium sized test transistors, and the low current $\beta$ was extracted. The results are summarized in Fig. 4. For the reference Si-BJT, there is a strong increase of $\beta$ when increasing the operation temperature. In contrast, the SiGe-HBTs showed very good thermal properties. The $\beta$ value of the processed devices with profile # 1 and # 2 was weakly influenced by the environmental temperature up to 200 °C, the highest temperature tested, which is essentially demanded for power amplification. Furthermore, the SiGe HBT with a box-like Ge profile (profile # 3) demonstrated a negative temperature coefficient, i.e. $\beta$ decreased as the temperature was increased. This is an expected result, since the valence band offset at the e–b junction interface contributes to the gain with a factor that decreases with increasing temperature.

In order to get some insight of the device thermal properties, device simulations using the ISE TCAD simulator were carried out. Dopant re-distribution through the emitter was computed using conventional

Table 1
Measured DC properties of the processed transistors with different base designs

| Profile # | Growth | $BV_{cbo}$ (V) | $BV_{ceo}$ (V) | $BV_{ebo}$ (V) | $\beta$ |
|---|---|---|---|---|---|
| 1 | CVD/MBE | 80 | 25 | 4–5 | 60–70 |
| 2 | MBE | 80 | 25 | 1–2 | 20–30 |
| 3 | CVD | 78 | 20 | 4–5 | 200–300 |
| Si ref | Implanted | 88 | 22 | 4–5 | 60–70 |

diffusion data without further correction. A very good agreement was obtained for the MBE grown HBT with a trapezoidal Ge profile (profile #2) when using almost all design parameters except a minor adjustment of the Ge content (using $x = 0.06–0.15$ instead). For CVD grown HBTs with the base profiles #1 and #3, a reduced B doping concentration $2.4 \times 10^{18}$ cm$^{-3}$ was set for the simulation. The Ge content was thereafter used as an adjustable parameter for the best fitting to the experimental data. The simulation results are plotted in Fig. 4.

RF measurements were performed on some packed devices with good DC-characteristics. At 2 GHz, the CW output power of 20 W (25 V supply voltage) was obtained with an efficiency of 68% in class AB operation, which is a significant improvement compared with the efficiency value (typically 50%) obtained from a conventional Si RF bipolar device. It deserves to be pointed out that the long-term temperature stability was excellent. SiGe RF power-HBTs could be operated at full output power for an extended time without any external temperature bias compensation, which is virtually impossible with conventional Si-base devices.

## 4. Summary

It has been demonstrated that the strained SiGe layer materials are suitable for RF power applications. The device structure and industrial usable processing technology have been developed during the work. The processed SiGe-HBTs showed expected DC characteristics and RF output power, and excellent power efficiency and thermal stability, which are useful for power module applications in mobile and wireless communication systems in the 2+ GHz bandwidth range.

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