Photoelectrochemical Hydrogen Evolution Using Si Microwire Arrays

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Supporting Information

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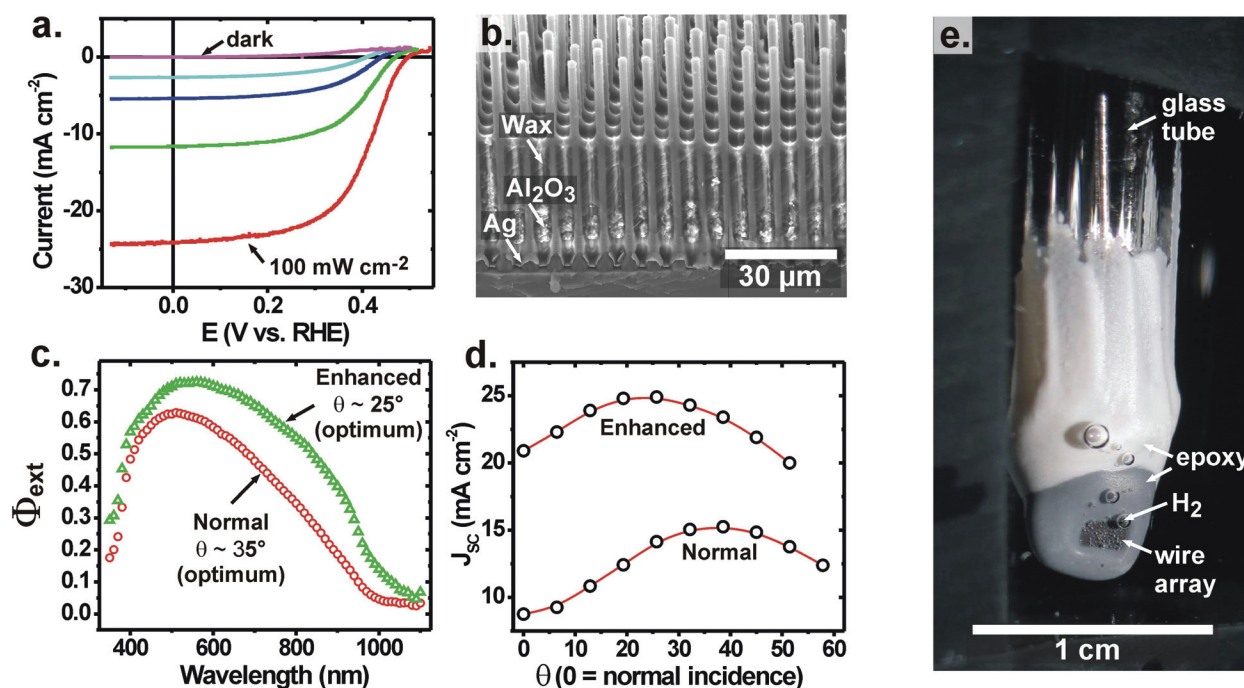
Supplementary Figures

Figure S1. Panel (a) shows the *J-E* data collected for the electrode fabricated with 'enhanced' absorption due to light-trapping elements, in 0.5 M aq. H_2SO_4 under ELH-type W-halogen solar simulation. Panel (b) shows a cross-sectional SEM image of the same sample. Panel (c) compares the spectral response collected for the sample with light-trapping elements ('enhanced') versus the spectral response for the normal sample. The red response in the 'enhanced' cell is significantly improved. Panel (d) shows the increased J_{sc} with reduced angle dependence, for the enhanced sample compared to the normal sample. Panel (e) shows a digital photograph of a normal Pt/n⁺p-Si wire-array electrode evolving hydrogen under ~ 1 sun illumination. Small bubbles can be seen nucleating on the wire-array surface. The larger bubbles are stuck on the epoxy, and are the result of the coalescence of many small bubbles.
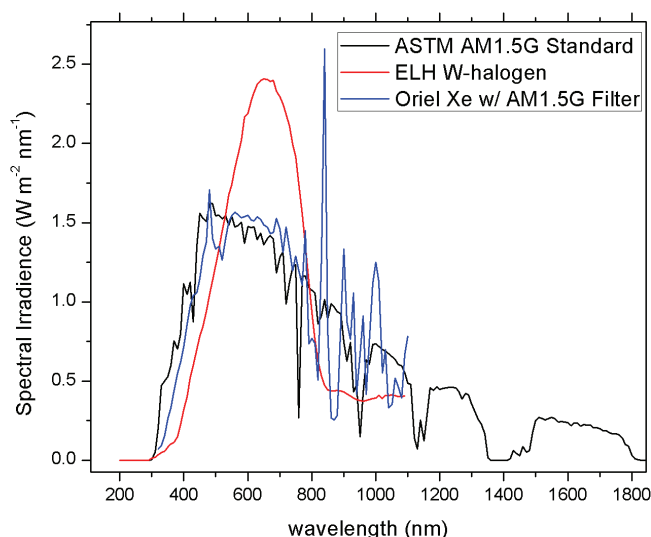
Figure S2. Spectral irradiance of solar simulator lamps compared to the ASTM AM1.5G (global tilt) reference spectra.

Materials and Methods

Wire-array growth. Si microwire arrays were grown using a process similar to that described previously.[1, 2] Boron-doped p$^+$-Si (111) wafers, having a resistivity of < 0.001 Ω·cm (Silicon Quest International), were used as growth substrates. The wafers were coated with 450 nm of thermal oxide that had been patterned with 4-μm-diameter circular holes arranged on a square lattice with a 7 μm pitch. The holes were defined in the oxide by photolithographic exposure and development of a photoresist layer (Microchem S1813), followed by a buffered HF(aq) (BHF) etch (Transene Inc.). The holes were then filled with 600 nm of Cu (ESPI metals, 6N) via thermal evaporation onto the patterned photoresist, followed by liftoff. Patterned substrates approximately 1.5 cm × 1.5 cm in dimension were then annealed in a tube furnace for 20 min at 1000 °C under H_2 flowing at a rate of 500 sccm. Wire growth was initiated by flowing $SiCl_4$ (Strem, 99.9999+%), BCl_3 (Matheson, 0.25% in H_2), and H_2 (Matheson, research grade) at rates of 10, 1.0, and 500 sccm, respectively, for 30 min. After growth, the tube was purged with N_2 at 200 sccm and was allowed cool to ~ 650 °C over the course of ~30 min. The resulting wires were typically between 40-60 μm in length and ~2.8 μm in diameter. These growth conditions have been shown to yield p-Si wires with active doping concentrations of ~ 10^{17} cm^{-3}.[1, 3]

Diffusion of the radial n$^+$ emitter. The Cu catalyst was removed from the as-grown wire arrays by etching in 10 % aq. HF for 10 s, 6:1:1 by volume H_2O:H_2O_2 (30 % in H_2O):conc. aq. HCl at 75 °C for 15 min, 10% aq. HF for 10 s, and 20 wt % aq. KOH at 20 °C for 60 s. A conformal SiO_2 diffusion-barrier that was ~ 200 nm in thickness was grown via dry thermal oxidation for 2 h at 1100 °C under a pure O_2 ambient. The wire-array samples were then coated with a solution that contained 4.4 g hexamethycyclotrisiloxane (Sigma-Aldrich), 1 g polydimethylsiloxane PDMS (Sylgard 184, Dow Corning), and 0.10 g of PDMS curing agent in 5 ml of dicholoromethane. These samples were then spun at 1000 RPM for 30 s and cured at 150 °C for 30 min to produce a 10–20 μm thick PDMS layer selectively at the base of the wire array.[6] After a ~ 2 s etch in a 1:1 mixture of 1.0 M tetrabutylammonium fluoride in tetrahydrofuran (Sigma-Aldrich) and dimethylformamide (referred to as 'PDMS etch') and a H_2O rinse, these partially in-filled arrays were immersed for 5 min in BHF to remove the exposed diffusion-barrier oxide. The PDMS was then completely removed by etching for 30 min in PDMS etch, which was followed by a 10 min piranha etch (3:1 aq. conc. H_2SO_4:H_2O_2) to remove residual organic contamination. After 5 s in 10 % aq. HF, thermal P diffusion was performed using solid-source CeP_5O_{14} wafers (Saint-Gobain, PH-900 PDS) at 850 °C for 15 min under an N_2 ambient, to yield a radial n$^+$ emitter region in the regions of the wires unprotected by the thermal oxide. A SEM image of these wires (after a 10 s etch in BHF to removed the thin dopant oxide) is shown in Figure 4d. Based on spreading-resistance measurements on planar control wafers, we estimate the dopant concentration in the n$^+$ layer at ~10^{19} cm^{-3} with a junction depth of ~ 200 nm.

The wire array chip was then heated to 150 °C on a hot plate, and mounting wax (Quickstick 135, South Bay Tech.) was melted into the array. Excess wax was removed from the array by applying gentle, even pressure with the flat surface of a glass cover slip to a tissue (KimWipe) that was draped over the sample on the hotplate. The mounting wax was then etched in an O_2 plasma (400 W, 300 mTorr) until ~ 10 - 20 μm of the wire tips were exposed (~60 min) as shown in Figure 3d.

Fabrication of planar n$^+$p-Si. The process for pn-junction fabrication was adapted from Fahrenbruch and Bube.[4] Boron-doped p-type (100)-oriented Si wafers (Silicon Inc.) with a resistivity of ~ 0.7 Ω cm were unpacked in a clean-room and cleaved into chips ~ 3 cm x 3 cm.

These chips were cleaned for 15 min in 6:1:1 by volume $H_2O:H_2O_2$ (30 % in H_2O):conc. aq. NH_3OH at 75 °C (RCA 1) followed by 15 min in 6:1:1 by volume $H_2O:H_2O_2$ (30 % in H_2O):conc. aq. HCl at 75 °C (RCA 2). The chips were then etched for 30 s in BHF, rinsed in H_2O, and dried.

These clean p-Si chips were then stacked in-between solid source CeP_5O_{14} diffusion wafers (Saint-Gobain, PH-900 PDS) and heated at 850 °C for 15 min under an N_2 ambient in a tube furnace. The n^+p-Si wafers were then etched for 30 s in BHF to remove the dopant oxide. 500 – 1000 nm of Al was then thermally evaporated onto the unpolished back surface of the wafers. The wafers were annealed for 10 min at 800 °C to drive the evaporated Al through the backside n^+ layer to make ohmic contacts. The edges of the chips were cleaved off and discarded, to eliminate shunts from the backside Al ohmic contact around the edge to the diffused n^+ emitter.

Electrode fabrication. Four types of electrodes were fabricated, consisting of p-Si planar, p-Si wire-array, n^+p-Si planar, and n^+p-Si wire-array samples. In each case, the Si samples were cleaved into square ~ 0.5 cm × 0.5 cm pieces. Ohmic contact to the p-Si wire-array, p-Si planar, and n^+p-Si wire-array chips were made by rubbing Ga-In eutectic on the back side of the chip. For the n^+p-Si samples, the annealed Al back-contact served as an ohmic contact. Electrical connections were made to the samples by attachment of coiled tin-copper wire using conductive silver paint. The wire arrays were then sealed, using Hysol 1C epoxy, at the end of glass tubing through which the wire had been directed such that the surface-normal direction to the chip was perpendicular to the glass tube. A second type of epoxy (Hysol 9460) was used to define the active area of the electrode (~0.02 to 0.1 cm^2), because Hysol 1C was found to wick in-between the Si microwires on the face of the electrode.

Prior to Pt deposition and photoelectrochemical measurements, the p-Si wire-arrays samples (but not the others) were etched as follows: 10 s 10 % aq. HF, 30 min 30 wt. % aq. $FeCl_3$, 10 s 10 % aq. HF, 1 min 20 wt. % aq. KOH, and 10 s 10 % aq. HF. After each step, the wires were rinsed with 18.3 MΩ cm resistivity H_2O, and dried under a stream of N_2 (g). This etching sequence removed the copper catalyst, the outer ~50 nm of Si, and the native oxide, leaving a clean surface for Pt deposition.

Platinum deposition. Pt deposition on the p-Si electrodes was accomplished via a galvanic displacement reaction whereby Si is oxidized (and then etched by HF) and Pt is reduced onto the

electrode surface.[5] The planar samples were immersed for 3-4 ~2.5 min intervals in an aq. solution that contained 0.5 M HF and 1 mM K_2PtCl_6. The electrode was tested after each deposition interval (see below). The electrode performance typically increased after every deposition cycle up to the 3rd or 4th cycle, after which additional deposition of Pt did not improve the performance. Slightly improved performance could be achieved by sonicating the electrode to remove excess Pt and then re-platinizing for an additional 2.5 min. The data shown in Figure 1a are representative of the best performance that was achieved using this procedure.

The wire-array samples were similarly immersed in the platinization solution for 2.5 min intervals, with the optimum time around 7.5 min. Depositions for longer times were attempted, but led to lower photocurrents and hence worse performance.

For the n^+p-Si samples, Pt was deposited by electron beam evaporation at a base pressure of $\sim 6 \times 10^{-6}$ torr onto the completed epoxy-sealed electrodes as the final step before testing. The thickness of Pt was monitored by a quartz crystal microbalance. 1 nm of Pt was deposited on the planar electrodes. For the wire arrays, 1.5 nm was deposited, and the wires were tilted along one axis during deposition to improve the sidewall coverage of the exposed wire tips.

Photoelectrochemical characterization. All photoelectrochemical measurements were performed in a flat-sided Pyrex glass electrochemical cell. The solution was stirred rapidly to minimize bubble nucleation on the electrode and to reduce the associated variation of the measured *J-E* data. The measurements were performed using a three-electrode configuration with a saturated calomel reference electrode (SCE) and Pt-coil counter electrode, each separated from the main compartment by a medium porosity glass frit. After data collection, the data were shifted on the potential axis such that the potential of the reversible hydrogen electrode (RHE) was zero, but no other corrections were performed (i.e. the data were not iR corrected or corrected for any other extrinsic losses). For all measurements reported herein, research-grade H_2 was continuously bubbled through the solution in order to maintain a fixed Nernst potential for the H^+/H_2 redox couple and to remove dissolved oxygen.

The Pt/p-Si electrodes were tested in 0.5 M aq. K_2SO_4 adjusted to pH ~ 2 using H_2SO_4. To remove detrimental dissolved metal impurities from these standard-grade lab reagents, the electrolyte solution was pre-electrolyzed for > 12 h with ~3 V applied across two large carbon-cloth electrodes under stirring. The electrodes were tested at pH ~ 2, because this pH appeared to

be a good compromise between, (1) the reduced Pt activity and Si stability at higher pH's and, (2) reduced V_{oc} values at lower pH's. Platinized p-Si wire-array electrodes with the base masked off with SiO_2 (in an identical fashion to the n^+p-Si electrodes), did not show performance significantly different than p-Si wire-array electrodes without the SiO_2 mask.

The Pt/n^+p-Si electrodes were tested in ultrapure 0.5 M H_2SO_4 (Aristar Ultra) in 18.2 MΩ resistivity water. The lower pH was selected due to the higher activity of the Pt catalyst in acidic media.

During measurements, the cell was illuminated using either a 300 W tungsten-halogen ELH lamp (OSRAM) or a Newport Oriel Xe lamp with an AM1.5G filter set. The light intensity was calibrated using a Si photodiode to produce a photocurrent equivalent to that obtained under 100 mW cm^{-2} of AM1.5 illumination at the working electrode. The spectral irradiance curves for both lamps are given in Figure S2.

The quality factor (n) for the electrodes was extracted by a linear fit of the dependence of the photovoltage (V_{oc}) on the logarithm of the light-intensity (and hence photocurrent, J_{ph}). The analytical expression for the photovoltage is given by the ideal diode equation solved for zero net current:

$$V_{oc} = (nk_BT/q)\ ln\ (J_{ph}/\gamma J_s), \tag{1}$$

where n is the diode quality factor, k_B (m^2 kg s^{-2} K^{-1}) is Boltzmann's constant, T (in K) is the temperature, q (C) is the charge on an electron, J_{ph} (A m^{-2}) is the photocurrent density, J_s is the saturation current density (related to recombination pathways), and γ is the ratio of the actual junction area to the geometric surface area of the electrode (i.e. the roughness factor).[1]

Angle-resolved photocurrent measurements. The short-circuit ($E = 0$ vs. RHE) photocurrent was measured under broad-area 100 mW cm^{-2} of ELH-type illumination while the electrode was rotated along one axis. Normal incidence was taken to be the angle at which the photocurrent was minimized.

Spectral response. Spectral response measurements were made using illumination from a 75 W Xe lamp that was passed through an Oriel monochromator (0.5 mm slits), chopped at ~13 Hz, and focused to a beam spot that was adjusted in size to slightly under-fill the electrode area. A

calibrated Si diode (UDT UV-050) was used as a standard for the sample channel. Another Si photodiode was used to measure a beam-split portion of the illumination and hence serve as a continuous calibration of the output intensity. A potentiostat (Gamry Series G 300) was used to hold the potential of the Si working electrode at short circuit ($E = 0$ vs. RHE) and to record the sample current. The chopped components of the signals were measured with independent lock-in detection of the sample channel (potentiostat analog output) and of the calibration channel.

Fabrication of electrodes with light-trapping features. Electrodes were also fabricated with light trapping features that included: (1) an a-SiN$_x$:H antireflective coating (which also serves to enhance carrier collection from the non-pn-junction portion of the wire initially protected with SiO$_2$)[6], (2) a Ag back reflector, and (3) Al$_2$O$_3$ light-scattering particles (Figure S1e). We have recently shown that these elements enhance the optical absorption[7] and hence the efficiency of solid-state wire-array photovoltaics.[8] After pn-junction fabrication, the wire arrays were etched for 5 min in BHF, to completely remove the remaining oxide diffusion barrier. The wires were then cleaned for 15 min in 6:1:1 by volume H$_2$O:H$_2$O$_2$ (30 % in H$_2$O):conc. aq. HCl at 75 °C and 30 s in BHF, prior to deposition of an a-SiN$_x$:H layer (~ 140 nm thick at the wire tip and ~ 60 nm thick at the wire base) using plasma-enhanced chemical vapor deposition, as described previously.[7]

1-μm planar-equivalent thickness of Ag was then deposited in successive 500-nm-thick thermal evaporations at two different shallow angles ($\pm$ ~5°) while the sample was slowly rotated. The array was then infilled with ~5 μm of PDMS using a process similar to the one described above. This PDMS etch barrier allowed the Ag at the wire tips and sidewalls to be selectively removed by etching for 6.5 min in 8:1:1 methanol: conc. aq. NH$_4$OH: 30 wt.% aq. H$_2$O$_2$.

Al$_2$O$_3$ light-scattering particles with an 80-nm nominal diameter (South Bay Technology) were then added to the wire array. The wire-array was placed face-up in a flat-bottomed glass centrifuge tube and ~ 3 ml of an ethanolic dispersion of the particles (~0.3 mg/ml) was added. Centrifugation (~3000 RPM) for 5 min was used to drive the particles to the base of the wire-array. The array was then infilled with wax and processed similarly to the devices without the added light trapping features. Prior to Pt deposition the a-SiN$_x$:H layer at the exposed tips of the wires was removed with a ~2 min BHF etch.

Supplementary References

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