

High-Mobility Graphene Nanoribbons Prepared Using Polystyrene Dip-Pen Nanolithography

Yun-Sok Shin,[†] Jong Yeog Son,^{*,†} Moon-Ho Jo,[†] Young-Han Shin,^{*,§} and Hyun Myung Jang[†]

[†]Department of Materials Science and Engineering and Division of Advanced Materials Science, Pohang University of Science and Technology, Pohang 790-784, Korea

[‡]Department of Applied Physics, College of Applied Science, Kyung Hee University, Suwon 446-701, Korea

[§]Departments of Physics and Chemistry and EHSRC, University of Ulsan, Ulsan 680-749, Korea

 Supporting Information

ABSTRACT: Graphene nanoribbons (GNRs) are fabricated by dip-pen nanolithography and polystyrene etching techniques on a SrTiO₃/Nb-doped SrTiO₃ substrate. A GNR field-effect transistor (FET) shows bipolar FET behavior with a high mobility and low operation voltage at room temperature because of the atomically flat surface and the large dielectric constant of the insulating SrTiO₃ layer, respectively.

Graphene nanoribbons (GNRs, where graphene is a monolayer of graphite) have attracted much attention recently because of their novel electronic and spin-involved properties.^{1–7} In particular, a GNR with a narrow width and atomically smooth edges is a promising candidate as a field-effect transistor (FET) with fast switching speed and high carrier mobility for next-generation electronics.^{8–13}

The fabrication of GNRs has been demonstrated using various techniques such as lithographic patterning,^{5,6,14} chemical,^{15–18} sonochemical,^{2,19} unzipping nanotube,¹³ cyclodehydrogenation,²⁰ local thermal reduction,²¹ electrochemical reduction,²² and organic wire mask²³ methods. Jiao et al. recently demonstrated high-quality GNR FETs on a SiO₂/p-doped Si substrate with a mobility up to 1500 cm²/(V·s).¹³ Nevertheless, the surface roughness and low dielectric constant (low-*k*) of SiO₂ may limit the quality of GNR FETs in terms of high mobility and low bias operation of a back gate, respectively. Therefore, insulating materials with both an ultraflat surface and high-*k* are required for high-quality GNR FETs.

Dip-pen nanolithography (DPN) is a powerful technique to fabricate nanostructures such as nanowires and nanodots with precise control of their position and size.^{24–27} The combination of DPN and etching techniques with polystyrene (PS) can provide a new method to fabricate GNRs in a controlled way (top-down approach). In this Communication, we demonstrate a scalable, high-quality GNR FET fabricated on a SrTiO₃/Nb-doped SrTiO₃ substrate using a PS DPN method.

GNRs were deposited by a mechanical exfoliation method on epitaxial SrTiO₃ thin films deposited by pulsed laser deposition techniques using a commercially available 1-in.-diameter SrTiO₃ target. Five-nanometer-thick SrTiO₃ thin films were evaporated on conducting Nb-doped SrTiO₃ substrates (Nb doping level of

1 wt % and resistivity of 0.001 Ω·cm) by pulsed laser beams at a base pressure of about 10^{−7} Torr. The temperature of the samples and oxygen partial pressure were maintained at 800 °C and 0.1 mTorr, respectively. To prepare an atomically flat surface of the Nb-doped SrTiO₃ substrates, the SrTiO₃ substrates were etched in a dilute HF solution and annealed at 1000 °C for 1 h.

Figure 1 shows a schematic of the sequential PS DPN processes used for the fabrication of the GNRs. PS nanorods were deposited by a DPN method onto an exfoliated graphene sheet on a SrTiO₃/Nb-doped SrTiO₃ substrate (Figure 1a). A Si₃N₄ DPN tip with a radius of less than 10 nm and a PS toluene solution were used. The speed of the DPN tip was 50–300 nm/s, and the widths of the corresponding PS nanorods were 150 to 30 nm (see Supporting Information). The PS nanorods were dried and annealed in a vacuum oven for 90 min at 40 °C and for 30 min at 120 °C, respectively. Note that the glass transition temperature of the PS nanorods is about 100 °C. Figure 1b shows the process of exposure to oxygen plasma to remove the graphene sheet except for the GNR pattern covered with PS nanorods. The power and exposure time of the oxygen plasma were 80 W and 30 s, respectively, at an operation pressure of 10 mTorr. As the PS structures are more resistant to oxygen plasma than the graphene sheet, only PS nanorods and the GNR below remained on the substrate after oxygen plasma exposure (Figure 1c). Finally, all of the PS nanorods were removed by successive serial sonication processes using acetone, ethanol, and distilled water. Thereby, only GNRs were formed on the substrate (Figure 1d).

Figure 2a shows an atomic force microscopy (AFM) image of a graphene sheet on a SrTiO₃ substrate where the lateral stripes indicate the roughness of the surface of the SrTiO₃ substrate (a surface roughness of 0.2 nm). The graphene sheet (light milky color), whose edge is underlined by a dotted line, covers the upper part of the image window. The graphene sheet was confirmed to be single-layered using Raman spectroscopy, as shown in Figure 2b, where the only Raman shift peak was observed at about 2700 cm^{−1}. Multilayer graphene sheets show not only a main peak but also satellite peaks in the Raman shift peak area. Figure 2c,d shows AFM images of PS nanorods (white), which had widths down to 30 nm, made by the DPN method on the graphene sheet and GNRs (light milky color) with widths down to 25 nm covered by the PS nanorods, respectively. Using the etching processes described above

Received: September 19, 2010

Published: March 28, 2011

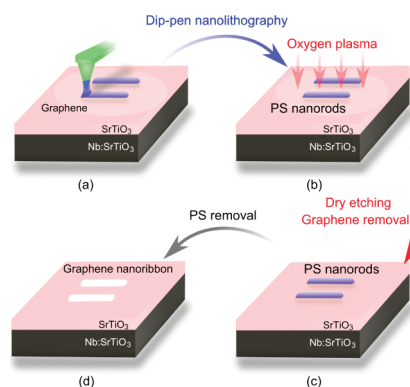


Figure 1. Schematic of the polystyrene (PS) dip-pen nanolithography (DPN) method. (a) A DPN tip writes PS nanorods onto a graphene sheet on a SrTiO₃/Nb-doped SrTiO₃ substrate. (b) Oxygen plasma etches the graphene sheet with the PS nanorods on the substrate. (c) Only PS nanorods remain on the substrate. (d) Graphene nanoribbons are formed after removing the PS nanorods.

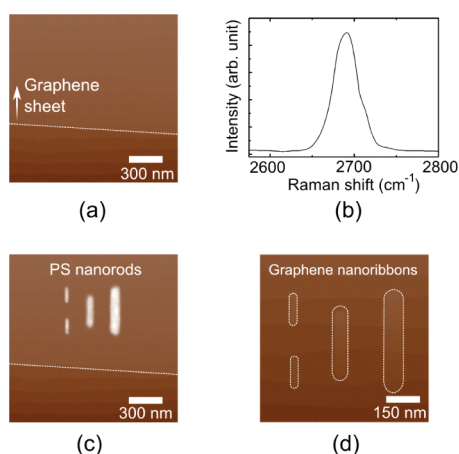


Figure 2. (a) Atomic force microscopy (AFM) image of the graphene sheet on the SrTiO₃ substrate. (b) Raman spectroscopy of the graphene sheet in (a). (c) AFM image of the graphene sheet with the PS nanorods. (d) AFM image of various graphene nanoribbons on the substrate. The white dotted lines indicate the graphene boundary.

with oxygen plasma and chemicals, the GNRs were well formed according to the designed PS pattern.

A FET with a GNR channel was formed on a SrTiO₃/Nb-doped SrTiO₃ substrate with vertical (sample A) and parallel (sample B) orientations with respect to terrace edges using the DPN method (Figure 3a,b), where the conducting Nb-doped SrTiO₃ substrate was used as a back gate. A source (drain) electrode consisting of a Pb nanodot and a Au nanowire were made by DPN processes. For ohmic contact between the GNR and the Au nanowire as the source (drain), a Pb nanodot was predeposited at the left (right) end of the GNR using the DPN method with a PbCl₂ solution, solidified in a vacuum oven at 40 °C for 60 min, and annealed at 200 °C for 30 min. Two Au nanowires over the Pb nanodots were formed using the DPN method with a AuCl₄ solution, solidified in a vacuum oven at 40 °C for 60 min, and annealed at 250 °C for 30 min. Figure 3c,d shows AFM images of a GNR labeled with sample A without and with the corresponding source and drain, respectively. In Figure 3d, the larger dot of the source (drain) connected with the left (right) end of the GNR indicates a Pb/Au dot.

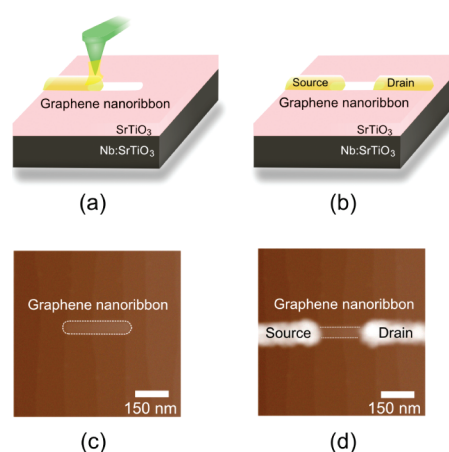


Figure 3. A graphene nanoribbon (GNR) field effect transistor (FET). (a) A DPN tip deposits a Au electrode as a source. (b) Schematic of the GNR FET composed of a GNR channel, an adjacent source and drain, and a back gate (Nb-doped SrTiO₃ substrate) after the DPN processes. AFM images of (c) only a GNR and (d) the GNR FET labeled with sample A. The white dotted lines indicate the graphene boundary.

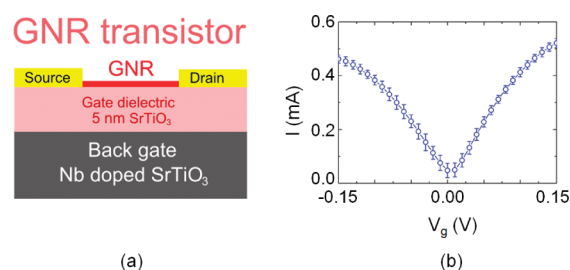


Figure 4. (a) Schematic side view of a FET composed of a GNR channel, source and drain electrodes, and a back gate where the dielectric constant (calculated from the capacitance of the SrTiO₃ layer) of the 5 nm thick insulating SrTiO₃ layer is 170. Note that the dielectric constant of SiO₂ is 3.9. Figure 4b shows bipolar FET characteristics of the current I in sample A as a function of the applied gate voltage V_g , where the conduction carrier is an electron (hole) for a positive (negative) V_g .

Figure 4a shows a schematic side view of a FET composed of a GNR channel, source and drain electrodes, and a back gate where the dielectric constant (calculated from the capacitance of the SrTiO₃ layer) of the 5 nm thick insulating SrTiO₃ layer is 170. Note that the dielectric constant of SiO₂ is 3.9. Figure 4b shows bipolar FET characteristics of the current I in sample A as a function of the applied gate voltage V_g , where the conduction carrier is an electron (hole) for a positive (negative) V_g .

Hereafter, we estimate an average mobility $\mu_{n(h)}$ in the GNR channel, where $n(h)$ indicates an electron (hole). The average mobility of $\mu_{n(h)}$ is about 3150 (−2740) cm²/(V·s) at 300 K. We used the formula²⁸ $\mu_{n(h)} = (g_{n(h)}L)/(WV_{sd}C_g)$ to estimate the mobility, where $g_{n(h)} (= \Delta I/\Delta V_g = 0.47$ (0.41) mA/0.15 V) = 3.13 (2.76) mA/V, $L = 150$ nm, $W = 50$ nm, $V_{sd} = 0.1$ V, and C_g are the average conductance with respect to V_g , the channel length of the GNR, the width of the GNR, the applied voltage between the source and drain, and the capacitance per unit area between the GNR and the back gate, respectively. Note that the maximum mobility $\mu_{n(h)}$ in the GNR channel is about 4900 (−4000) cm²/(V·s) at 300 K, where $g_{n(h)}$ in the above formula²⁸ is replaced by the differential conductance $g_m (= dI/dV_g)$, which is derived from numerical derivative).

In conclusion, we fabricated a graphene nanoribbon field effect transistor on a SrTiO₃/Nb-doped SrTiO₃ substrate by combining dip-pen nanolithography and polystyrene etching techniques. The GNR FET demonstrated bipolar FET behavior with a high mobility and low operating voltage due to the ultraflat surface and large dielectric constant of the insulating SrTiO₃ layer, respectively. We want to emphasize that the combination of the DPN and polystyrene etching techniques makes it possible to fabricate the scalable, high-quality GNR FET arrays.

■ ASSOCIATED CONTENT

S Supporting Information. S1, nanorod width as a function of the dip-pen speed; S2, cross section of the SrTiO₃ surface; S3, cross section of the GNR; S4, current–voltage characteristics for various gate voltages; S5, complete refs 18, 20, and 21; S6, FET performance of sample B. This material is available free of charge via the Internet at <http://pubs.acs.org>.

■ AUTHOR INFORMATION

Corresponding Author

jyson@khu.ac.kr; yhshin.at.uou@gmail.com

■ ACKNOWLEDGMENT

This work has been supported by the Brain Korea 21 project 2010 and World Class University (WCU) program by the Ministry of Education, Science and Technology (Project No. R31-2008-000-10059-0). Y.-H.S. acknowledges financial support by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2010-0028128). M.-H. Jo acknowledges financial support by Priority Research Centers Program through the NRF funded by the MEST (2009-0094037) and Basic Science Research Program through the NRF funded by the MEST (2010-0017853).

■ REFERENCES

- (1) Geim, A. K.; Novoselov, K. S. *Nat. Mater.* **2007**, *6*, 183.
- (2) Li, X. L.; Wang, X.; Zhang, L.; Lee, S.; Dai, H. *Science* **2008**, *319*, 1229.
- (3) Wang, X.; Ouyang, Y.; Li, X. L.; Wang, H.; Guo, J.; Dai, H. *Phys. Rev. Lett.* **2008**, *100*, 206803.
- (4) Wang, X.; Li, X. L.; Yoon, Y.; Weber, P. K.; Wang, H.; Guo, J.; Dai, H. *Science* **2009**, *324*, 768.
- (5) Zhen, Z. H.; Lin, Y. M.; Rooks, M. J.; Avouris, P. *Physica E* **2007**, *40*, 228.
- (6) Han, M. Y.; Ozyilmaz, B.; Zhang, Y.; Kim, P. *Phys. Rev. Lett.* **2007**, *98*, 206805.
- (7) Cresti, A.; Nemec, N.; Biel, B.; Niebler, G.; Triozon, F.; Cuniberti, G.; Roche, S. *Nano Res.* **2008**, *1*, 361.
- (8) Son, Y.-W.; Cohen, M. L.; Louie, S. G. *Phys. Rev. Lett.* **2006**, *97*, 216803.
- (9) Barone, V.; Hod, O.; Scuseria, G. E. *Nano Lett.* **2006**, *6*, 2748.
- (10) Areshkin, D. A.; Gunlycke, D.; White, C. T. *Nano Lett.* **2007**, *7*, 204.
- (11) Liang, G.; Neophytou, N.; Nikonov, D. E.; Lundstrom, M. S. *IEEE Trans. Electron Devices* **2007**, *54*, 677.
- (12) Nakada, K.; Fujita, M.; Dresselhaus, G.; Dresselhaus, M. S. *Phys. Rev. B* **1996**, *54*, 17954.
- (13) Jiao, L.; Wang, X.; Diankov, G.; Wang, H.; Dai, H. *Nat. Nanotech.* **2010**, *5*, 321.
- (14) Tapasztó, L.; Dobrik, G.; Lambin, P.; Biro, L. P. *Nat. Nanotech.* **2008**, *3*, 397.
- (15) Datta, S. S.; Strachan, D. R.; Khamis, S. M.; Johnson, A. T. C. *Nano Lett.* **2008**, *8*, 1912.
- (16) Ci, L.; Xu, Z.; Wang, L.; Gao, W.; Ding, F.; Kelly, K. F.; Yakobson, B. I.; Ajayan, P. M. *Nano Res.* **2008**, *1*, 116.
- (17) Campos, L. C.; Manfrinato, V. R.; Sanchez-Yamagishi, J. D.; Kong, J.; Jarillo-Herrero, P. *Nano Lett.* **2009**, *9*, 2600.
- (18) Campos-Delgado, J.; et al. *Nano Lett.* **2008**, *8*, 2773.
- (19) Wu, Z.-S.; Ren, W.; Gao, L.; Liu, B.; Zhao, J.; Cheng, H.-M. *Nano Res.* **2010**, *3*, 16.
- (20) Cai, J.; et al. *Nature* **2010**, *466*, 470.
- (21) Wei, Z.; et al. *Science* **2010**, *328*, 1373.
- (22) Mativetsky, J. M.; Treossi, E.; Orgiu, E.; Melucci, M.; Veronese, G. P.; Samori, P.; Palermo, V. *J. Am. Chem. Soc.* **2010**, *132*, 14130.
- (23) Jarvholm, J.; Srinivasarao, M.; Tolbert, L. M. *J. Am. Chem. Soc.* **2009**, *131*, 398.
- (24) Demers, L. M.; Ginger, D. S.; Park, S.-J.; Li, Z.; Chung, S.-W.; Mirkin, C. A. *Science* **2002**, *296*, 1836.
- (25) Basnar, B.; Weizmann, Y.; Cheglakov, Z.; Willner, I. *Adv. Mater.* **2006**, *18*, 713.
- (26) Basnar, B.; Willner, I. *Small* **2009**, *5*, 28.
- (27) Son, J. Y.; Shin, Y.-H.; Ryu, S.; Kim, H.; Jang, H. M. *J. Am. Chem. Soc.* **2009**, *131*, 14676.
- (28) *Semiconductor material and device characterization*; Schroder, D. K., Ed.; Wiley: New York, 2006; p 500.