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Low-Temperature Solution-Processed Amorphous Indium Tin Oxide Field-Effect Transistors

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Because of their excellent mobilities, large band gaps, broad transparency windows, and mechanical stress tolerance, amorphous metal oxide semiconductors (AOSs) are attractive materials for the fabrication of transparent/flexible thin-film transistors (TFTs).[1] Such TFTs may be useful in improving the aspect ratio of conventional displays, in invisible circuitry, and in bendable devices.[1] AOS films are typically grown using vacuum techniques such as sputtering, ion-assisted deposition, pulsed laser deposition, and chemical vapor deposition.[2−5] Combinatorial approaches have enabled the discovery of new compositions with high field-effect carrier mobilities (μ) and low carrier doping (n). The latter must be controlled/suppressed to achieve large TFT on-to-off current ratios (I_{on}/I_{off}).[5] For instance, optimized In−Zn−Ga−O[2] and In−Zn−O[3] TFTs with SiO_2 gate dielectrics exhibit impressive performance (μ up to 80 and 100 $cm^2\ V^{-1}\ s^{-1}$, respectively) when deposited at 25 °C. Other interesting AOSs investigated for TFT applications include Zn−Sn−O[4] and In−Sn−O.[5] However, controlling exact stoichiometries for property reproducibility in such multicomponent systems is challenging.[6] Furthermore, vacuum-based processes are typically expensive and, unfortunately, incompatible with high-throughput printing.[1]

Solution-processed AOS film fabrication would be advantageous because of process simplicity, chemical composition/stoichiometry control, and compatibility with printing processes. Recently, solution-processed metal oxide films such as In_2O_3,[7a] ZnO,[7b−f] Zn−Sn−O,[8] In−Ga−O,[9] and In−Zn−O[9c] have been integrated into different TFT architectures exhibiting mobilities from 0.1 to ∼40 $cm^2\ V^{-1}\ s^{-1}$. However, for high performance, these films must be annealed at high temperatures (T_a = 400−700 °C) that are incompatible with inexpensive plastic substrates. In this communication, we report the growth of solution-processed amorphous In−Sn−O (ITO) films for TFT fabrication at temperatures <250 °C. By control of the precursor solution In^{3+}/Sn^{4+} ratio and the T_a value, performance characteristics of $\mu > 2\ cm^2\ V^{-1}\ s^{-1}$ and $I_{on}/I_{off} > 10^4$ have been achieved for TFTs using SiO_2 as the gate dielectric. Furthermore, we demonstrate that hybrid integration of solution-processed ITO semiconductor films with a solution-processed nanoscopic, high-k self-assembled nanodielectric (SAND)[10] affords $\mu \approx 10-20\ cm^2\ V^{-1}\ s^{-1}$ with excellent I_{on}/I_{off} ratios.

Figure 1A shows the bottom-gate−top-contact TFT architecture employed in this study. Devices were fabricated on heavily doped Si substrates (gate) coated with either thermally grown SiO_2 (300 nm, $C_i \approx 11\ nF/cm^2$) or SAND [16.5 nm, $C_i \approx 280\ nF/cm^2$; see Figure S1 in the Supporting Information (SI) for the structure] as the gate dielectric layer. On these substrates, the ITO films were deposited by spin-coating of precursor solutions consisting of the metal chlorides in 2-methoxyethanol with added ethanolamine. This procedure was repeated twice to achieve ∼30 nm thick films (see Figure S2). Next, the semiconductor films were annealed at progressively higher temperatures (T_a = 200−250 °C). Finally, Al source and drain electrodes (∼50 nm thick) were vapor-deposited through a shadow mask to define the TFT channel length (L = 100 μm) and width (W = 500, 1000, 2000, 5000 μm). Experimental details are described in the SI.

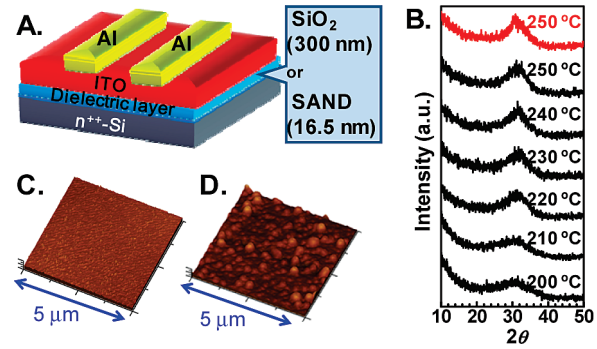

Figure 1. (A) Schematic of the TFT structure with the gate dielectrics employed in this study. (B) GIAXRD patterns of ITO films deposited on (black lines) Si/SiO_2 and (red line) Si/SAND substrates (precursor solution $[In^{3+}]/[In^{3+} + Sn^{4+}]$ molar ratio = 0.7) and annealed at the indicated temperatures. (C, D) AFM images of ITO films on (C) Si/SiO_2 and (D) Si/SAND substrates annealed at T_a = 250 °C.

The ITO film microstructure and morphology on Si/SiO_2 and Si/SAND substrates were investigated by grazing incidence angle X-ray diffraction (GIAXRD) and tapping-mode atomic force microscopy (AFM). Figure 1B shows XRD patterns of ITO films ($[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.7$; see below) annealed at different temperatures, which demonstrate that these films are essentially amorphous, independent of T_a and the gate dielectric material. Grazing-incidence-angle XRD data further support the amorphous nature of these compositions (Figure S3). The AFM images in Figures 1AC,D and Figure S4 reveal that these ITO films are compact, dense, uniform, and fairly smooth, with rms roughnesses of ∼0.5 and 6 nm (for 25 μm^2 areas) on Si/SiO_2 and Si/SAND, respectively, which are comparable to those for the corresponding substrates. We believe that these film morphologies are the result of: (1) the good quality of the underlying dielectric, (2) the intrinsic efficacy of the spin-coating technique for depositing smooth oxide films, and (3) the amorphous nature of these films. All of the present ITO films are colorless and highly optically transparent (band gap ≈ 3.65 eV; Figure S5), exhibiting an average transparency of ∼90% in the visible region (Figure S5) for films fabricated on glass. Therefore, these semiconductor films are suitable for the fabrication of transparent n-channel TFTs.

Figures 2A,B shows typical transfer and output plots for TFTs fabricated on Si/SiO_2 as the gate dielectric from ITO films having an optimized $[In^{3+}]/[In^{3+} + Sn^{4+}]$ molar ratio of 0.7 (T_a = 250 °C). These TFTs exhibit excellent response, with crisp saturation characteristics and larger I_{on}/I_{off} ratios than ITO TFTs fabricated from the vapor phase.[5] In addition to reproducibility issues, multicomponent metal oxide films of specific stoichiometries are difficult to fabricate, since each composition requires the use of different targets or expensive multitarget setups.[11]

For solution-processed metal oxide films, it is convenient and inexpensive to prepare precursor solutions with desired compositions simply by dissolving different ratios of metal sources and base in the appropriate solvent. Consequently, we investigated ITO films fabricated from precursor

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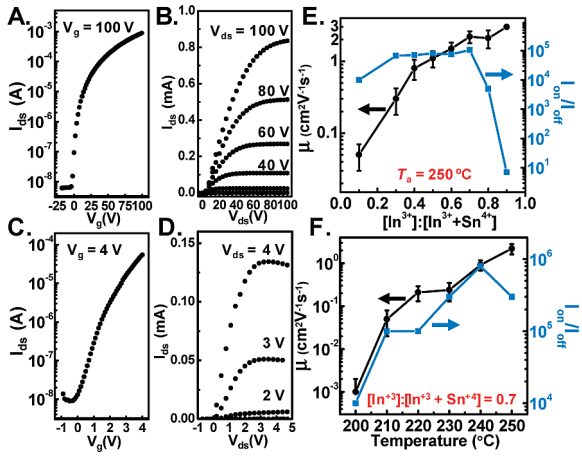

Figure 2. (A, C) Transfer and (B, D) output plots for ITO-based TFTs ($[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.7$, $T_a = 250$ °C) having the following structures: (A, B) Si/SiO_2 (300 nm)/In_2O_3 (30 nm)/Al (50 nm), $L = 100$ μm, $W = 1000$ μm; (C, D) Si/SAND (16.5 nm)/In_2O_3 (30 nm)/Al (50 nm), $L = 100$ μm, $W = 500$ μm. (E) Saturation μ and I_{on}/I_{off} plots as functions of $[In^{3+}]/[In^{3+} + Sn^{4+}]$ for ITO−SiO_2 TFTs in which the ITO film was annealed at 250 °C before Al deposition. It should be noted that the μ value for $[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.9$ is not accurate because of the large doping level (see Figure S6). (F) Saturation μ and I_{on}/I_{off} plots as functions of T_a for ITO−SiO_2 TFTs with $[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.7$ in which the ITO films were annealed at the indicated temperatures before Al contact deposition. In (E) and (F), $L = 100$ μm and $W = 1000$ μm.

solutions having various $[In^{3+}]/[In^{3+} + Sn^{4+}]$ ratios. Figure 2E shows the TFT response parameters as a function of the $[In^{3+}]/[In^{3+} + Sn^{4+}]$ ratio for ITO−SiO_2-based devices. From these data it is clear that when the indium content is increased, the electron mobility in saturation increases from 0.05 ± 0.02 ($[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.1$) to 2.21 ± 0.41 cm^2 V^{-1} s^{-1} ($[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.7$) with an excellent I_{on}/I_{off} of ~10^5 (Figure S6). TFTs based on even higher In^{3+} contents ($[In^{3+}]/[In^{3+} + Sn^{4+}] =$ 0.8−0.90) exhibit similar mobilities but with progressively deteriorating I_{on}/I_{off} (from 10^5 to 10; see Figure S6). This occurs because the film composition is approaching that of conducting ITO.[2] Because of the sharp turn-on, linear regime mobilities are comparable (±10%) to the saturation mobilities. Furthermore, these TFTs exhibit low/negligible $I_{SD}-V_{SD}$ hysteresis and, for $[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.7$, minimal V_T shift upon multiple scans (Figures S7 and S8). The dependence of the mobility on the channel width (from 500 to 5000 μm) is also small (Figure S8). The good charge transport achieved at lower T_a's for amorphous ITO (250 °C vs, e.g., 400 °C for In_2O_3-based TFTs[7a]) is the result of the lower conversion temperatures needed for conversion of mixed-metal hydroxide lattices to oxide, relative to those in single-element systems.[12]

For the optimum metal composition ($[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.7$), we also investigated the effect of annealing the ITO films at temperatures below 250 °C. Figure 2F shows plots of μ and I_{on}/I_{off} versus T_a, which demonstrate that when T_a decreases from 250 to 200 °C, the mobility decreases from ~2.2 to ~0.03 cm^2 V^{-1} s^{-1} because of incomplete ITO lattice formation.[12] However, our data demonstrate that for these AOS films, annealing at T_a's as low as 220 °C affords TFTs with respectable mobilities (>0.2 cm^2 V^{-1} s^{-1}) and $I_{on}/I_{off} \sim 10^5$ (Figure S9).

Finally, we explored the fabrication of ITO films on SAND nanodielectrics. Figures 2C,D and Figure S10 show the transfer and output plots for ITO/SAND-based devices ($[In^{3+}]/[In^{3+} + Sn^{4+}] = 0.7$; $T_a = 250$ °C; $L = 100$ μm; $W = 500$, 1000 μm). These unoptimized TFTs operate at very low voltages and exhibit field-effect mobilities larger than those of the SiO_2-based TFTs (10−20 cm^2 V^{-1} s^{-1}), which is not surprising considering the lower interface trap density of SAND versus SiO_2 dielectrics.[13] The high performance of these AOS ITO TFTs is compatible with large drain currents at low power, fast charge/discharge capacitive loads, and high operating speeds, which suggests a wide range of applications. These results demonstrate that hybrid integration of a solution-processed AOS provides TFTs with performance unobtainable via conventional approaches.

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Supporting Information Available: Experimental details for ITO film and TFT fabrication. This material is available free of charge via the Internet at http://pubs.acs.org.

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