Energy & Environmental Science

PAPER

View Article Online
View Journal

Cite this: DOI: 10.1039/c5ee02484f

Conductance and capacitance of bilayer protective oxides for silicon water splitting anodes†

A. G. Scheuermann,[a] K. W. Kemp,[a] K. Tang,[a] D. Q. Lu,[a] P. F. Satterthwaite,[a] T. Ito,[ab] C. E. D. Chidsey[c] and P. C. McIntyre*[a]

Received 12th August 2015,
Accepted 9th November 2015

DOI: 10.1039/c5ee02484f

www.rsc.org/ees

State-of-the-art silicon water splitting photoelectrochemical cells employ oxide protection layers that exhibit electrical conductance in between that of dielectric insulators and electronic conductors, optimizing both built-in field and conductivity. The SiO_2-like layer interposed between a deposited protective oxide film and its Si substrate plays a key role as a tunnel oxide that can dominate the total device impedance. In this report, we investigate the effects of changes in interfacial SiO_2 resistance and capacitance in the oxide bilayer through both solid state leakage current and capacitance–voltage measurements and through electrochemical methods applied to water splitting cells. Modelling is performed to describe both types of data in a simple and intuitive way, allowing for insights to be developed into the connections among both the dielectric (charge storage) and conductive (charge transport) properties of bilayer protective oxides and their effects on oxygen evolution performance. Finally, atomic layer deposited (ALD) Al_2O_3 is studied as an insulator layer with conductivity intermediate between that of tunnel oxide SiO_2 and the more conductive ALD-TiO_2, to further generalize this understanding.

Broader context

The development of efficient and stable water-splitting cells is a key step in the long term goal of artificial photosynthesis. Although much progress has been made in developing wind, solar, and other alternative energy sources, only 1/3 of global carbon emissions comes from electricity generation. The majority of the remaining emissions arises from human transportation and the production, transportation, and consumption of goods. As such, using artificial photosynthesis to cleanly generate both solar fuels and solar chemicals presents another key component to achieving a sustainable energy economy. Insulator-protection layers, particularly atomic layer deposited TiO_2, have been shown to be capable of stabilizing a variety of highly efficient light absorbers for these processes, among them, silicon, the most common solar cell material. The overall utility of such schemes derives from the stable power output that can be achieved from a cell. Maximizing that power in turn involves simultaneous optimization of conductivity, interfacial carrier recombination, built-in field, and overall stability. Such optimization often requires state-of-the-art protection layers for semiconductor photoelectrochemical devices to exhibit properties intermediate between dielectric insulators and conductive oxides. This report seeks to elucidate the relationship between capacitive charge storage and conductive charge transport across the interface between silicon and catalyst that includes tunnel oxide SiO_2 and an atomic layer deposited oxide surface coating. Understanding this relationship can help advance state-of-the-art artificial photosynthesis technology.

1. Introduction

Photoelectrolysis systems are of interest for the on-site production of clean chemicals and fuels, both as end-use products and as an integrated energy storage solution for mitigating the intermittency of solar radiation. One persistent challenge in this field is the difficulty of simultaneously achieving high photovoltaic efficiency and chemical stability of semiconductor photoelectrodes during water oxidation under wide-ranging pH conditions. Wide band gap semiconducting metal oxides are frequently stable under water oxidation conditions but have inherent photocurrent limitations, prompting the need for novel structures and materials capable of delivering high performance combined with stability. There are several classes of junction types now popular in the literature to address these problems: Type 0 photoelectrochemical cells (PECs) where the junction is formed directly between a semiconductor layer and the

[a] Department of Materials Science and Engineering, Stanford University, Stanford, CA, USA. E-mail: pcm1@stanford.edu
[b] Tokyo Electron Ltd, Technology Development Center, 650, Hosaka-cho Mitsuzawa, Nirasaki, Yamanashi 407-0192, Japan
[c] Department of Chemistry, Stanford University, Stanford, CA, USA

† Electronic supplementary information (ESI) available. See DOI: 10.1039/c5ee02484f

electrolyte; Type I metal–insulator–semiconductor cells (MIS) where a Schottky junction is formed between a metallic catalyst and a semiconductor substrate, in most cases necessarily with an insulator interlayer in between; and Type II buried junction cells where a pn homo- or hetero-junction is formed in the semiconductor substrate so that oxide layers and/or catalyst layers above are in series with the solar junction. The Type II buried junction cell is similar in some ways to a separate photovoltaic system and electrolysis system except that the wire length is on the nanometer scale—incorporating the oxide layers and catalyst directly—as opposed to any additional wire that may be used to separate a photovoltaic system placed further from the electrolyte. Additionally, such integration may relax the need for as conductive and maximally transparent conductive oxide layers as is required in stand-alone PV cells. The junction type defines both the advantages and disadvantages inherent in each system, as described previously.[1] For each cell architecture, one must also consider the efficiency of a single junction vs multiple junctions, where the single junction device can only achieve a maximum theoretical solar-to-hydrogen (STH) efficiency of 11.2%. A tandem device, on the other hand, with two materials of bandgap 1.23 and 1.84 eV, could achieve 22.8% STH efficiency, above the current US Department of Energy (DOE) goal.[2] All of these ideal-bandgap materials will likely need some form of protection to ensure high efficiency over years of operation. Thus, future advances need to consider the materials selection and junction type as well as schemes to make realistic and stable tandem structures.

In 2011, Chen and Prange *et al.*[3] demonstrated that atomic layer deposition (ALD) of a thin and chemically-protective TiO_2 layer can avoid oxidation of the surface of a silicon photoanode during long-duration oxygen evolution. This initial work showed that it was possible to decouple efficient light absorption by the silicon anode from the oxygen evolution reaction (OER) occurring on the surface of a water oxidation catalyst layer by the presence of an interposed ALD-TiO_2 layer. This conformal and pinhole-free oxide layer was found to be dense enough to block the solution from oxidizing the underlying semiconductor (greatly increasing its stability), but conductive enough to allow efficient hole transport between an n-type silicon substrate and an iridium OER catalyst.[3,4] Temperature dependent conductance measurements were also performed. Ultrathin TiO_2 films of 2 nm in thickness exhibited nearly temperature independent conductivity suggesting quantum tunnelling as the mechanism of charge transfer. Thicker films showed a temperature dependence suggesting bulk limited conduction of some form. In 2013, Scheuermann *et al.*[5] showed that ALD-TiO_2 could be used with a variety of other catalyst materials as well as thinner catalyst layers to produce efficient devices with similar stability while using smaller amounts of more Earth-abundant metals. It was found that effective hole conduction was possible across thicker ALD-TiO_2 layers with a relatively minor increase in resistance compared to the large expected increase of effective resistance from a quantum tunnel barrier. The small additional overpotential for water oxidation arising from this resistance varied linearly with thickness and was found to be approximately 21 mV per nm of ALD-TiO_2. Importantly, this study showed that tunnelling was not the sole conduction mechanism as the ALD-TiO_2 thickness was increased. The resistance was controlled by bulk conduction of electronic carriers through states in the TiO_2 band-gap between the catalyst and anode. In 2014, Hu *et al.*[6,7] deposited ALD-TiO_2 with a similar recipe to that used in previous work[3–5] and utilized a thick nickel catalyst, producing even more conductive TiO_2. This reduced the overpotential penalty for increasing TiO_2 thickness approximately to zero; the TiO_2 reported by Hu *et al.* was conductive enough to act as a degenerate semiconductor instead of an insulator, and was still found to provide over 100 hours of stability for water splitting on silicon anodes. A limitation imposed by using a degenerate semiconductor TiO_2 protection layer is, however, formation of a semiconductor–insulator–semiconductor (SIS) junction of nSi–SiO_x–TiO_2, as opposed to an MIS junction in which a high work function OER catalyst metal sets the Fermi level at equilibrium. As illustrated by McDowell in recent work,[8] the nSi–SiO_x–TiO_2 junction can be formed from a wide variety of TiO_2 deposition methods, but it achieves photovoltages of only 150 to 350 mV in most cases. This is insufficient for a viable bottom cell in a tandem water splitting device, even with a perfect fill factor. For somewhat lower effective doping of the TiO_2, there remains an inherent defect-induced reduction of efficiency for MIS solar cells.[9] For this reason, dielectric oxides—with low effective doping—have an advantage in attaining high built-in voltage. Recent observations indicate, however, that there is a serious photovoltage reduction as a function of the thickness of insulating protective oxide layers on nSi MIS photoanodes.[1] This thickness dependence is the result of the need to a maintain high minority carrier concentration by photogeneration adjacent to a semiconductor/oxide interface where recombination can occur. Photocurrent transport across these MIS structures can be described using a simple capacitor model where a large hole concentration at the semiconductor/oxide interface is required to sustain a certain leakage current through the device. It has been further shown that buried p^+n junctions, rather than MIS Schottky structures, can avoid this photovoltage reduction in dielectric oxide protected photoanodes, achieving photovoltages up to 630 mV.[1]

While there have been an increasing number of reports in the literature on metal oxide protection layers,[1,3–8,10–13] and on metal (catalyst) protection of unstable semiconductors[14,15] (based on earlier work of dark water splitting electrolysis using stable catalyst electrodes[16,17]), a direct study of the role of the oxide interlayer that necessarily forms between a silicon substrate and such coatings has not, to our knowledge, been performed. In this report, we first describe the effects of plasma slot-plane-antenna (SPA) growth of nanoscale layered SiO_2 of controlled thickness in Si/SiO_2/metal anodes. We show that a direct tunnelling model well describes conduction through the SiO_2 in these anodes. We then study the SiO_2 interlayer in a photoanode with a protective ALD-TiO_2 surface coating. This work reveals the point at which a key transition occurs from protective oxide structures that are conductive and predominantly transport charge to those that are capacitive and predominantly store charge. Quantifying this

transition identifies the range of thicknesses that can achieve optimized protected silicon photoanodes. Theoretical simulations predict both the conductive and capacitive behaviour of bilayer oxide photoanode junctions. In particular, capacitance data measured in the presence of large leakage current densities are analyzed to provide better understanding of interface properties that must be controlled when manipulating the SiO_2 interlayer. Finally, we have prepared matching sets of anodes with an Al_2O_3/SiO_2 bilayer as an analogue to the TiO_2/SiO_2 stack, to further generalize the understanding of interlayer oxide materials properties on water splitting performance.

2. Results and discussion

2.1 Interlayer SiO_2 effects in MIS anodes

2.1.1 Slot-plane-antenna (SPA) SiO_2 growth and characterization. Prime grade Si(100) wafers were prepared using a three-part clean to remove organics, trace metal ions, and finally the silicon dioxide layer, leaving an HF-last surface for plasma oxide growth (see Methods). The slot plane antenna (SPA) method, which was developed by Tokyo Electron Limited based on the earlier work of Ohmi *et al.* on Radial Line Slot Antenna (RLSA), is then utilized.[18] SPA uses radical oxidation that can achieve ultrathin oxide layers on silicon with a low density of interface traps (D_{it}) and thickness reproducibility equal to or better than thermal oxidation, and at significantly lower temperatures. It can achieve 0.7 to 1.0% thickness non-uniformity for films of 1.5 to 10 nm with D_{it} values $<10^{10}$ eV^{-1} cm^{-2} at temperatures as low as 400 °C.[19] A 2.45 GHz microwave is introduced from the top of the apparatus and distributed across the slot plane antenna (schematic in ESI,† S1). As the microwaves are emitted downward they generate a uniform, high density plasma below the dielectric shower plate with a diameter exceeding 30 cm, capable of uniformly covering large wafers. Inert gases and oxygen are emitted through nozzles around the gas ring and the substrate is heated resistively to temperatures between 400 °C and 500 °C for radical oxidation of ultrathin layers. For these experiments, the deposition temperature was set to 500 °C, for an actual substrate temperature of approximately 400 °C and was allowed to equilibrate while argon was purged through the chamber at 100 sccm. Then the argon flow rate was increased to 1500 sccm and oxygen gas was introduced at 400 sccm for 10 seconds. Finally the argon flow was set to 1200 sccm and oxygen held at 40 sccm for 25 seconds at a process pressure of 5 Torr. The microwave power was set to 3000 W and held for the duration of the growth time (Table 1). After the microwave power is shut off, argon is allowed to flow for an additional 3 seconds to conclude the process. This process was optimized for the thinnest possible oxides; decreasing the process time to 3–5 seconds results in final oxide thickness of ~15 Å as measured by ellipsometry, the approximate minimum for this method. By extending the run length, oxide films of >100 Å thickness can be grown.

The SiO_2 thickness was measured using a Woollam ellipsometer calibrated by cross-sectional transmission electron microscopy (TEM) analysis. Oxide thickness is a particularly important parameter in determining the film's utility for electrochemical applications, given the exponential decrease of the transmission coefficient for quantum tunnelling with SiO_2 film thickness. As can be seen in Table 1, the film growth rate decreases with increasing time. Besides uncontrolled oxidation of the semiconductor surface during oxygen evolution on the anode, another source of premature failure for MIS photoelectrochemical cells is deterioration or delamination of the catalyst. Delamination can be a serious problem for relatively noble metals, such as many OER catalysts, on oxide surfaces. In order to determine whether delamination of metal overlayers on SiO_2 had occurred before water splitting, atomic force microscopy was performed on the sample surface before and after forming gas anneal and before and after catalyst metal deposition. Immediately after SPA-SiO_2 growth, the root mean square (rms) surface roughness was measured to be 0.276 nm for a 5 μm × 5 μm area. After an anneal in forming gas (95% N_2/5% H_2) at 450 °C the surface roughness remained ~0.3 nm. Surface roughness after e-beam deposition of iridium remained similar at 0.301 nm. After a forming gas anneal at 450 °C on the iridium coated surface, the rms roughness decreased slightly to 0.263 nm (ESI,† S2). XPS analysis confirmed that the surface composition and bonding is similar before and after the forming gas anneal and that iridium is still present on the surface, allowing electrochemical characterization of Ir/SiO_2/Si anodes to be performed. Fig. 1 shows the cyclic voltammetry data for a 2 nm Ir/~1.5 nm SPA-SiO_2/p^+Si anode in the dark compared to data from an equivalent structure prepared using a p^+Si substrate out of the wafer box, with the vendor-supplied chemical SiO_2 surface layer in place. Both cyclic voltammetry data performed during ferri/ferrocyanide redox (top pane) and during water oxidation in basic and neutral solution (bottom pane) produced nearly identical results for the two oxide structures. This may result from two factors: 1 – the chemical and physical properties of the two SiO_2 films are nearly identical or 2 – the resistive contributions of the SiO_2 layer in these structures are insignificant to overall device performance, thus masking any differences that may exist. To gain a better understanding of the ideal performance of the SiO_2 interlayer, a series of electrochemical anodes was fabricated using the conditions shown in Table 1.

Table 1 Ellipsometer thickness data for a series of SPA-SiO_2 runs on (100) silicon

Process time (seconds)	Mean film thickness (nm)
5	1.46
15	1.72
30	1.88
60	2.11
90	2.24
120	2.34
1800	5.38
7200	11.5

2.1.2 Resistance modelling of empirical and theoretical results. Anodes with varying SPA-SiO_2 thickness were fabricated and measured in ferri/ferrocyanide solution to determine the

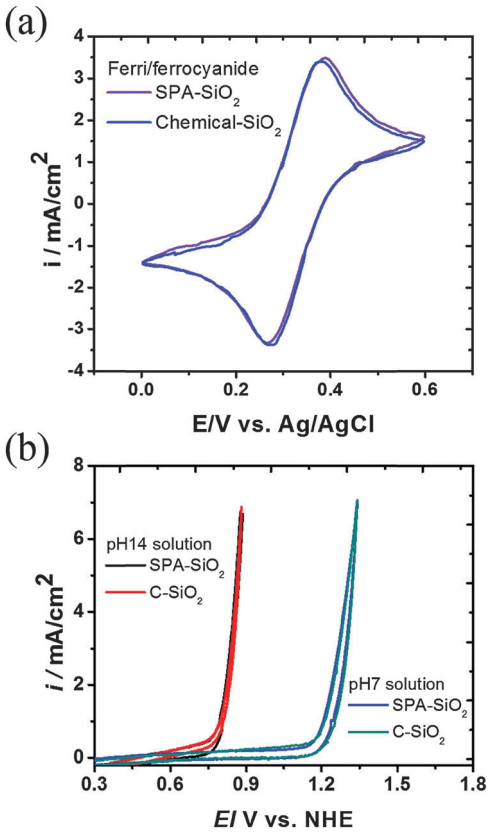

Fig. 1 Electrochemical comparison of 2 nm Ir/ ~1.5 nm SiO_2/p^+Si anodes in the dark using slot plane antenna (SPA) and vendor chemical (C) SiO_2 showing the similar performance obtained from both. (a) First sweep cyclic voltammogram in 10 mM ferri/ferrocyanide in 1 M KCl. (b) Water oxidation in base, 1 M NaOH (pH = 14), and 1 M sodium phosphate buffer (pH = 7). In both cases the scan rate was 100 mV s^{-1}, the surface area was 0.196 cm^2, and an Ag/AgCl sat. KCl reference electrode was used.

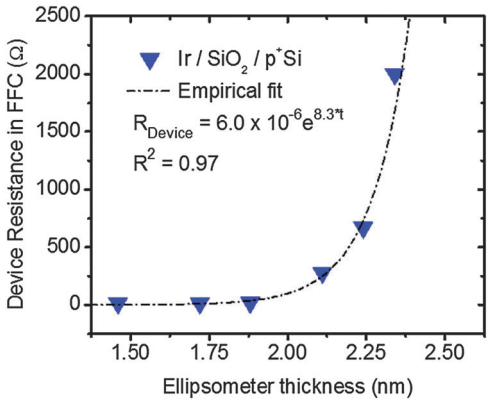

Fig. 2 Ir/SiO_2/p^+Si device resistance from the experimental ferri/ferrocyanide cyclic voltammograms as a function of SPA-SiO_2 thickness as measured by ellipsometry. The device resistance increases exponentially with high correlation becoming significant above ~2.0 nm in SiO_2 thickness.

equivalent total resistance of the interposed insulating SiO_2 layer between the silicon and metal catalyst. This resistance is extracted by first measuring the cyclic voltammogram using the reversible redox couple (such as in Fig. 1, top panel). Then the curves are fit to a theoretically determined profile using EC-lab software V10.21 based on Butler–Volmer kinetics and mass transport limitations of the electrolyte. The fitting procedure was described in detail previously.[5] A standard set of parameters are used, representative of the materials' properties, and only a series resistance term is altered to fit each subsequent curve (also see ESI,† S3). Fig. 2 presents the modelled device resistance of six Ir/SiO_2/p^+Si anodes that displayed at least short-term stability afforded by the metal catalyst layer (at least 3 voltammetry sweeps unchanged, cyclic voltammetry profiles in ESI,† S4) to ensure accuracy of the measurements. This data series is fit to a simple exponential function of the SiO_2 thickness t with high correlation, showing the exponentially increasing resistance to charge transfer with increasing interlayer thickness. For less than 2 nm of oxide thickness, the device is conductive and relatively insensitive to changes in thickness. Greater than 2 nm, the absolute resistance of the anode is extremely sensitive to SiO_2 thickness. Anodes fabricated with 5.4 and 11.5 nm SiO_2 layers both exhibited no significant conductivity over the range of voltages tested (−4 to 4 V). These data support the results shown in Fig. 1, indicating that anodes with SiO_2 layer thicknesses <1.5 nm are likely to exhibit similar resistance, and indicate the sharp transition from a conductive oxide structure to a capacitive, charge-storing structure that occurs for ~2 nm SiO_2 thickness in metal/SiO_2/silicon junctions. The thickness of both oxides shown in Fig. 1 can also be extracted from capacitance–voltage analysis. This procedure gave a thickness of the vendor-supplied oxide of 1.30 nm, and 1.32 nm for the SPA-SiO_2.

In a further test of whether this empirically determined exponential thickness scaling is consistent with direct tunnelling conduction, Sentaurus TCAD software by Synopsys Inc. was utilized to fit the data with a hole tunneling model as shown in Fig. 3. Values used for the model are described in the methods section and the hole effective mass is varied to fit the data.[20] The modelling was performed for both the ellipsometrically-determined thickness and the electrically-determined thickness to present the range of applicable hole effective masses. The horizontal thickness uncertainty in ellipsometry is determined by measuring 15 points across each sample piece and presenting the range. The electrically-determined thickness is measured by fitting cyclic voltammetry data and the error is the uncertainty of the fitting model. The vertical resistance uncertainty for both graphs is due to the resolution of the electrochemical series resistance model. The fitted hole effective masses are consistent with previous literature reports that typically show the hole effective mass in SiO_2 ranging from 0.3 to 0.5 on Si substrates.[21–24] Some reports have calculated lower masses in the 0.23–0.37 range.[25] The hole effective masses fit here fall in the center range of previously-reported masses and the overall trend produces a strong fit to data both suggesting that the SPA-SiO_2 behaves as a tunnel oxide in the Ir/SiO_2/Si stack.

2.2 Interlayer SiO_2 effects in the TiO_2/SiO_2 bilayer

2.2.1 Electrochemical characterization of the TiO_2/SiO_2 stack. With an understanding of conduction through the SPA-SiO_2,

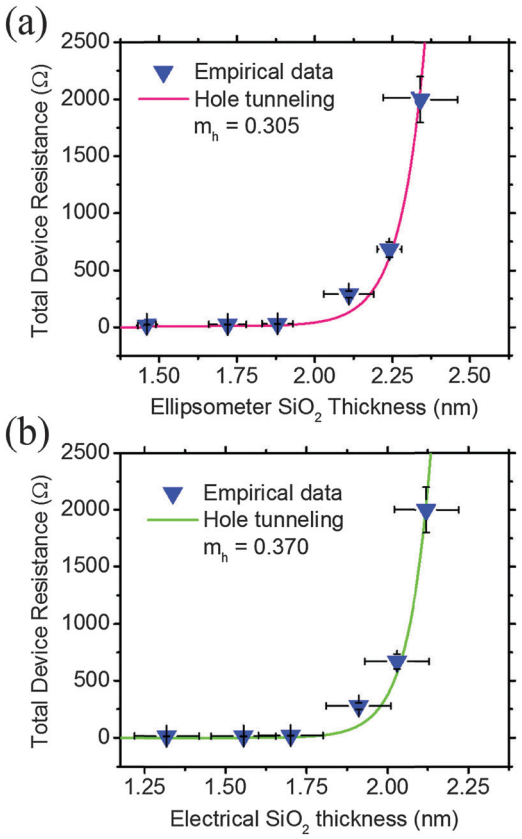

Fig. 3 Sentaurus modelling of hole tunnelling current is performed and a series resistance value is extracted from the *IV* around the zero gate voltage point for each thickness (an analogous procedure to the modelling of the empirical data). Hole effective masses of 0.305 and 0.370 for the ellipsometric thickness and electrical thickness, respectively, produce a good fit of the theoretical tunnelling resistance to the empirically determined resistance from cyclic voltammetry.

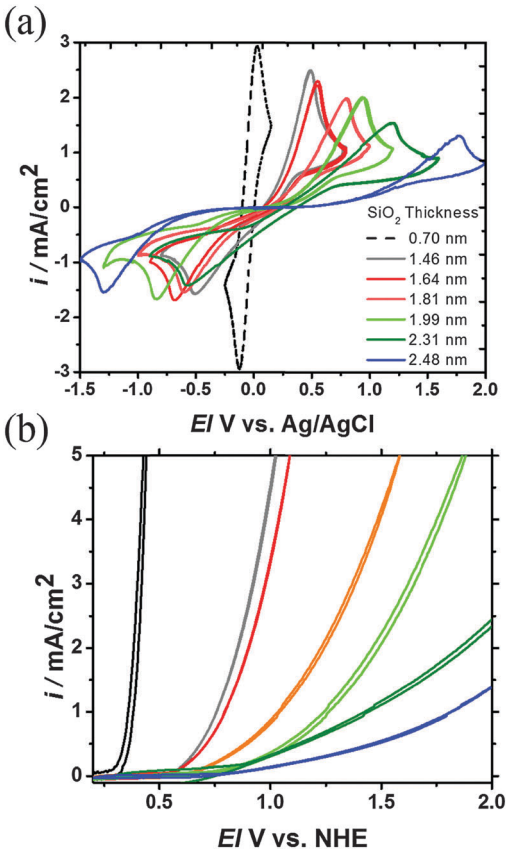

Fig. 4 Ir/1.5 nm ALD-TiO_2/'*x*' nm SiO_2/nSi under 1 Sun of AM 1.5G illumination for (a) 10 mM ferri/ferrocyanide and (b) 1 M NaOH basic solution for water oxidation. The thinnest SiO_2 layer is achieved by the oxygen scavenging method. All others are achieved with slot-plane-antenna (SPA) plasma oxidation.

the interlayer was next studied in the anode structure of interest. ALD-TiO_2 thin films of 1.5 nm are deposited on top of the SPA-SiO_2 films and measured electrochemically in the as-deposited state and by solid-state measurements in both the as-deposited state and after a 450 °C forming gas anneal. Both as-deposited and post-annealed TiO_2 thin films are amorphous. Data obtained by TEM, Raman, XRD, and XPS analysis of the films are shown in ESI,† S5–S8. Fig. 4 shows the ferri/ferrocyanide cyclic voltammograms and water oxidation measurements in 1 M NaOH basic solution of as-deposited Ir/1.5 nm TiO_2/'*x*' nm SiO_2/nSi photoanodes under 1 Sun AM 1.5G illumination. As can be seen in both cases, the decrease in performance with increasing SiO_2 thickness is severe.

In order to extend the probed range to thinner SiO_2 layers, an oxygen scavenging method was used to thin an already-formed SiO_2 interlayer.[26,27] In this method, a titanium metal layer is deposited on top of the stack to scavenge oxygen from the interlayer SiO_2 through the interposed ALD-TiO_2 layer at elevated temperature. The residual silicon atoms have been shown to epitaxially regrow on the Si(100) substrate surface. The Ti metal coating with dissolved oxygen is then etched away preferentially in aqueous HF solution, leaving the protection layer intact, and the thickness of the residual SiO_2 measured by ellipsometry and XPS. In this case, a thickness of ~0.7 nm is measured after the procedure (Fig. 4). A separate, full study of this method for thinning the interlayer SiO_x in ALD-TiO_2 protected anodes is ongoing.

2.2.2 Resistance modelling. Fig. 5 shows the total device resistance, extracted from the electrochemical data as before, and compared against the predictions of hole tunnelling. Interestingly, addition of ALD-TiO_2 to the MIS stack causes the resistance to increase at lower SiO_2 thickness compared to the case when no TiO_2 is present. Conduction through the device seems, therefore, to involve a complex relationship between the two oxides in the bilayer, as opposed to a simple additive resistance. Because the tunnelling current through the SiO_2 layer is a function of the density of states of the material on either side, the density of trap states available for bulk, hole-conduction through the TiO_2 may affect the overall device resistance in two ways: by setting the TiO_2 bulk resistance and by mediating the tunnelling resistance through the SiO_2 layer. Fig. 5 presents the measured data bound by two limiting cases. In green, Sentaurus software was used to model the case where the 1.5 nm TiO_2 layer exhibits negligible bulk conductivity and, therefore, behaves as a tunnel oxide with hole effective mass of 0.23.[28,29] In the other

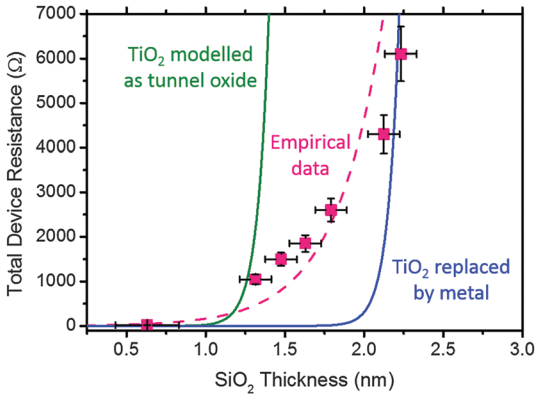

Fig. 5 Ir/1.5 nm TiO_2/'x' nm SiO_2/nSi device resistance (pink) from ferri/ferrocyanide cyclic voltammograms as measured in 1 Sun of AM 1.5G illumination. The green and blue curves show the two theoretically-predicted limiting cases of the protecting TiO_2 acting as a tunnel oxide (green) and removing it completely and tunnelling directly into the metal as in Fig. 3 (blue). Data are plotted *versus* the electrically determined SiO_2 thickness and the pink dashed line shows the best fit exponential curve to the empirical data.

bounding case, the TiO_2 is replaced by a metal, providing a large density of states for hole tunnelling (blue). The actual data (pink), falls in between the two.

The results in Fig. 4 and 5 show that, for moderately conductive TiO_2 in the bilayer, even very thin SiO_2 layers (1 to 1.5 nm) contribute non-negligible resistance and that a large resistance penalty is incurred for even one monolayer of additional SiO_2 growth. The high conductance obtained for the oxygen-scavanged device with an even thinner SiO_2 interlayer suggests that new methods of controlling the SiO_2 film thickness may provide a reliable route to low resistance water splitting cells even with insulating protection layers. These data also provide an additional insight into the contributions of bulk conduction of electronic carriers through the TiO_2. In previous work, we reported on the linear overpotential scaling of Ir/TiO_2/SiO_2/p^+Si anodes in the dark with changing TiO_2 thickness, relating this to a bulk-limited conduction mechanism.[5] A reasonable question is whether changes in the interfacial SiO_2 thickness during ALD-TiO_2 deposition might account for this added resistance, instead of the resistance of the TiO_2 film. Fig. 4 and 5 demonstrate the expected nonlinearity of the resistance scaling trend with increasing SiO_2 and that monolayer-level changes in SiO_2 thickness can change the anode resistance by several hundreds of Ohms at a time. Thus it is impossible to recreate the linear overpotential scaling in ref. 5 by changing the underlying SiO_2 thickness alone.

2.2.3 Capacitance characterization of the TiO_2/SiO_2 stack. Quantifying the transition point from a relatively conductive to a capacitive bilayer oxide stack in terms of the total device resistance is helpful for analysis of photoelectrochemical devices because (1) a series resistance in any solar cell decreases the steepness of the *I–V* curve, thus reducing the fill factor and the maximum efficiency; and (2) a capacitive oxide inserted inside the junction (as in a MIS Schottky junction structure) has been shown to require hole accumulation to mediate leakage, lowering the photovoltage achieved at a given current.[1] Measuring the photoanode electrical resistance from cyclic voltammetry convolves these two effects, requiring the careful use of p^+Si reference structures to separate the series resistance of the oxide bilayer from the photovoltage. Also, such electrochemical measurements do not directly probe the semiconductor/oxide interface quality. Because state-of-the-art protection layers for photoelectrochemical devices sit at the transition between leaky and capacitive oxides, it is helpful to supplement electrochemical data with solid state capacitance–voltage (*CV*) characterization, which is a standard method for studying MIS capacitors and transistors. However, the high leakage currents exhibited by MIS electrodes for water splitting cells lead to non-idealities in *CV* analysis that must be understood to properly interpret the data. ESI,† S9 reviews ideal capacitance–voltage behavior in relation to the non-ideal behavior discussed in the following paragraph of this article.

Solid-state leakage- and capacitance–voltage analyses were carried out as detailed in the methods section on a set of eight photoanodes as a function of interlayer SiO_2 thickness with the structure Ir/1.5 nm ALD-TiO_2/'x' nm SPA-SiO_2/nSi (Fig. 6(a)). The solid-state leakage currents in Fig. 6(b) show increases between 3 to 4 orders of magnitude for a 1 nm decrease in SiO_2 thickness. This increasing leakage current takes the capacitance voltage curves from near-ideal behavior at high frequencies into a regime where the *CV* behaviour is highly non-ideal. Fig. 6(c) shows the multi-frequency capacitance–voltage data for the photoanode structure with 1.46 nm of SiO_2 – the lower end of the range studied – and Fig. 6(d) shows the *CV* resulting from the device structure with 1.99 nm of SiO_2 – above which thickness the device resistance is found to rapidly increase in electrochemical measurements (Fig. 3). The device with 1.46 nm of SiO_2 exhibits high leakage current density causing the *CV* curves to shoot upward, especially in accumulation, where electrons tunnel from the n-type silicon conduction band, through the interlayer oxide, and into the gate electrode. When adding only half a nanometer of thickness to the SiO_2 interlayer oxide, the leakage current density is reduced dramatically and charge storage across the oxide layers can be effectively measured at all frequencies, as indicated in Fig. 6(d) by the saturated capacitance at higher voltage in accumulation. The inversion capacitance also shows saturated behaviour for thicker oxide layers. Ideally, however, inversion is not observed at higher frequencies at all because the minority carrier generation cannot follow the AC signal, as discussed in ESI,† S9. Inversion observed at these higher frequencies (1 MHz to 1 kHz) has been correlated to a persistent inversion layer at the nSi surface surrounding the patterned Ir electrodes used in these solid state measurements. Holes in this inversion layer can be swept under the electrodes during capacitance–voltage measurements. This so-called "peripheral inversion" has been reported on elsewhere.[30]

Electrochemical measurements reported in this article used anode samples that had a thin and continuous coating of metal catalyst, so that this peripheral inversion does not affect PEC device performance. However, electrical contact by such an inversion layer to partial catalyst layers, either to lower the utilization

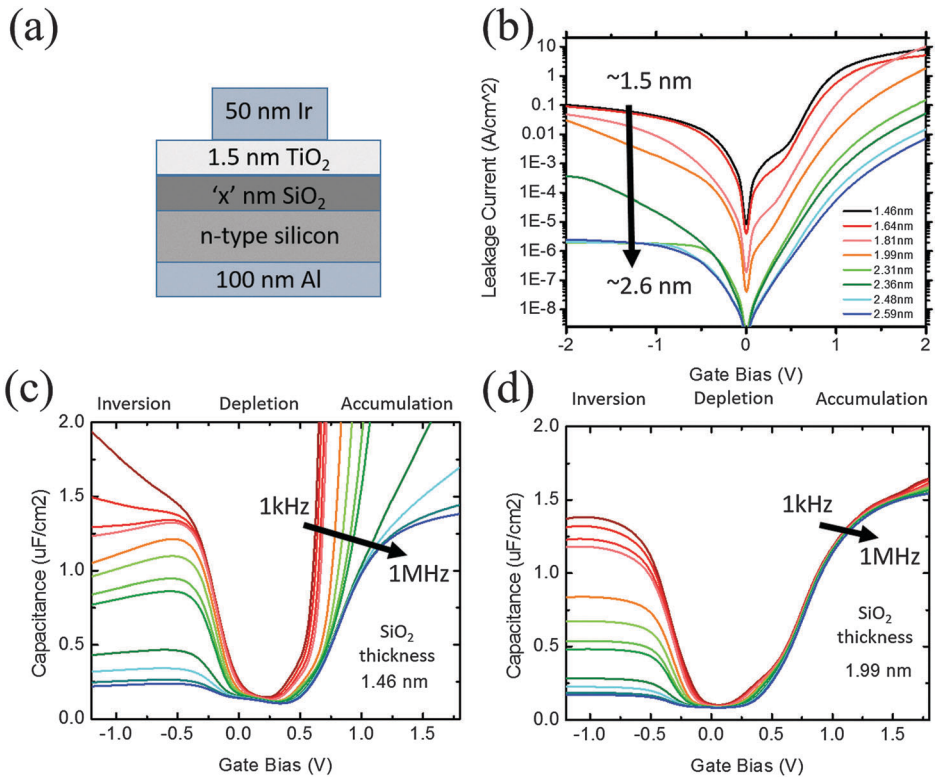

Fig. 6 (a) The device stack of Ir/1.5 nm TiO_2/'x' nm SPA-SiO_2/nSi was studied at 8 different thicknesses systematically changing the SiO_2 thickness. All data shown here are measured in the dark and after a 450 °C forming gas anneal. (b) Leakage current analysis of the anode series showing exponentially decreasing leakage at a given voltage as a function of thickness. (c) Capacitance–voltage analysis of the device with 1.46 nm of SiO_2 showing large non-idealities where the curves shoot upward especially at low frequency in accumulation. The *CV* traces from red to blue are taken at 1 kHz to 1 MHz respectively with 50 mV AC amplitude and the DC gate bias is swept from negative (inversion) to positive (accumulation) values. (d) *CV* of 1.99 nm SiO_2 device showing more ideal behaviour due to diminished leakage from the tunnel oxide SiO_2.

of rare metals or to achieve better light management, may be useful for MIS water splitting cells as it is for MIS solar cells.[31–35] Therefore, analysis of peripheral inversion and the transition between leaky and capacitive behaviour may be important for further optimization of MIS water splitting photoelectrodes.

2.2.4 Capacitance modelling. Models have been described in previous literature to quantify the influence of high leakage currents on capacitance–voltage curves in Si MOS structures.[36,37] However, they were developed with small corrections in mind, where leakage was an undesirable side effect as opposed to one of the main features of the measurement. Recently, we have developed a model capable of delineating the effects of series resistance, and tunneling leakage current on non-ideal capacitance–voltage curves.[38] Fig. 7(a) shows a simplified equivalent circuit diagram where G_{ox} is a conductance parallel to the oxide capacitance C_{ox} representing leakage current through the oxide, C_s is the semiconductor capacitance, and G_0 is a shunt conductance representing filamentary or shorting-type conduction that forms an Ohmic, as opposed to a Schottky, contact to the substrate. Any possible conductance directly to the back contact from surface conduction around the sample (*e.g.* if the ALD protection layer is highly conductive) or from cleaving would also contribute to G_0. This model for high gate leakage current densities is used to analyze non-ideal capacitance voltage data from these insulator-protected water-splitting cells. As shown in Fig. 7(b) (and ESI,† S12), the model accomplishes an almost perfect simulation of the experimental data at all voltages and frequencies measured. Further, the capacitance fit is achieved without the need to change G_0, indicating that the non-idealities of the *CV* curve are very well described purely by an increasing leakage current, G_{ox}, shifting any charge stored from the oxide to the semiconductor. The fitting of G_0 and G_{ox} are thus independent of each other, indicating that the fitting result is unique and physical. ESI,† S13 further shows that these non-ideal capacitance–voltage curves are insensitive to changes in measurement parameters such as the integration time and DC scan rate. This makes capacitance–voltage analysis a viable characterization technique for relatively conductive insulator-protected devices as well as the classical low-leakage dielectrics used in commercial MIS semiconductor electronics. ESI,† S14 shows the extracted G_{ox} necessary to make these capacitance fits, and the G_0 required to simulate the parallel conductance data.

Fig. 7(c) shows the experimental data and simulations for the accumulation capacitance for devices with various SiO_2 thickness as a function of frequency. For thin oxides, by decreasing the measurement frequency, the capacitance transitions from measuring the oxide to measuring only the capacitance associated with the silicon substrate adjacent to the

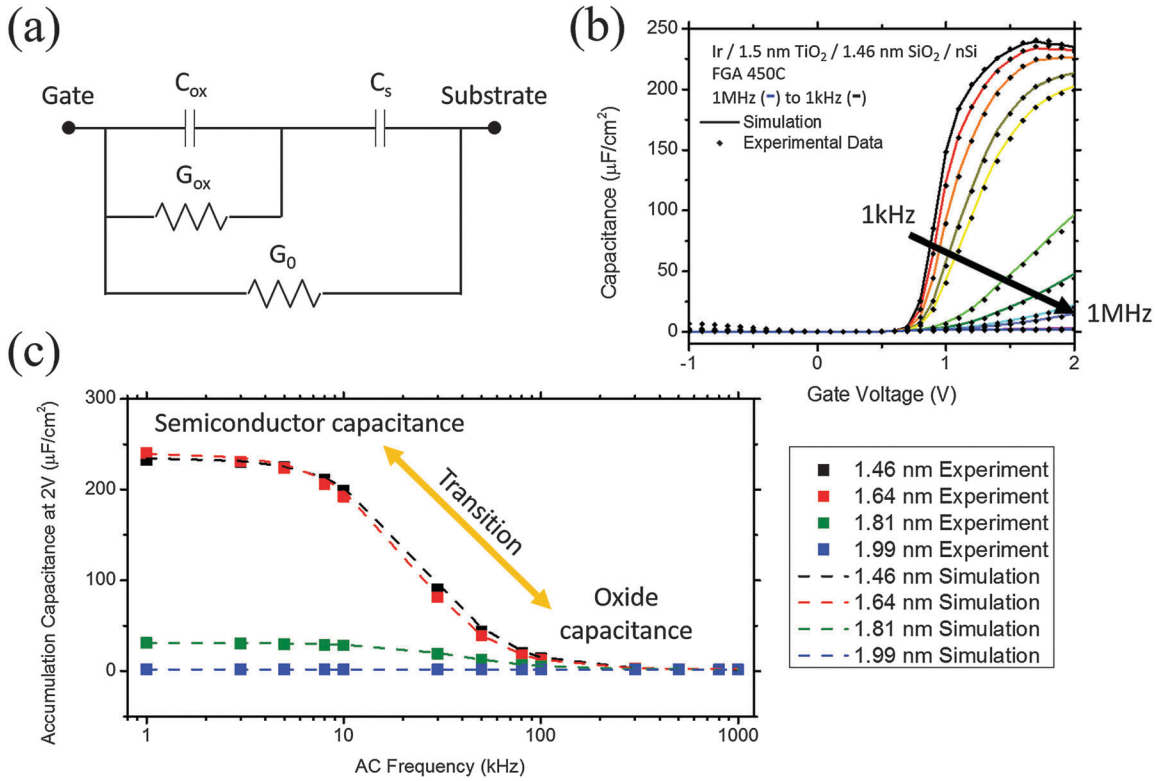

Fig. 7 (a) The simple equivalent circuit diagram used, modelling the oxide leakage as G_{ox} in parallel with the oxide capacitance C_{ox} and a shunt G_0. (b) This model can simulate capacitance–voltage non-idealities using an oxide leakage conductance G_{ox} (where G_0 is only necessary to fit the conductance non-idealities). (c) Alignment between experimental data and simulation for the capacitance transition. At low frequency, thin films do not store any charge in the oxide, so the measurement probes the capacitance of the Si substrate. At high frequency, and eventually at all frequencies for $\geq$2 nm SiO_2 thickness, the oxide capacitance can be probed, giving values in the range of 1–2 μF cm^{-2} (as seen in Fig. 6).

interface, indicating that the bilayer oxide presents little barrier to charge leakage between the metal and semiconductor. As the thickness of the SiO_2 tunnel oxide is increased, the frequency dependence decreases until with $\geq$2 nm of SiO_2, the device acts as a near-ideal MIS capacitor at all measurement frequencies. These data show a transition from, essentially, completely leaky devices from the capacitance perspective to near-ideal capacitance voltage behavior occurring over the range of 1.5 to 2.0 nm of SiO_2 thickness. Referring back to Fig. 3–5 shows that these two characterization schemes, one of measuring charge conductance and one of measuring charge stored, describe the transition over the same physical thickness range.

2.3 Generalizing: ALD-Al_2O_3 as an intermediate system

Aluminum oxide is a common dielectric material with far ranging applications, including use as a gas and water barrier. Previous studies have shown that thin films of alumina are effective at blocking water vapor from oxidizing underlying calcium substrates, allowing for the precise determination of the water vapor transmission rate (WVTR) through these coatings.[39,40] Alumina coatings can also protect potentially unstable substrates under water oxidation and reduction conditions, but only at near-neutral pH, as indicated by the relevant Pourbaix diagram.[41] This is unlike TiO_2, which is stable across the whole range of pH values.

The Al_2O_3/SiO_2 bilayer exhibits more voltage-symmetric leakage conduction than does the TiO_2/SiO_2 bilayer, as discussed in ESI,† S15. Consistent with its greater band gap and barriers to both hole and electron conduction, ALD-alumina MIS structures on silicon typically have much lower leakage current densities than do structures with TiO_2. Because Al_2O_3 is expected to exhibit intermediate electrical behaviour between that of SiO_2 and TiO_2, and exhibits potential at moderate pH as a protective layer against oxidative corrosion, it is a good system to further generalize the relationships studied here in resistance scaling of photoelectrochemical devices. Fig. 8 shows the results of the solid state leakage current measurements and the series resistance as extracted from ferri/ferrocyanide redox cyclic voltammetry. In Fig. 8(c), the thickness scaling trend of p^+Si anode device resistance for each oxide system is compared, showing the intermediate nature of alumina.

Our recent report[1] showed the utility of a buried p^+n junction as compared to a Type I nSi Schottky junction cell to minimize photovoltage losses arising from the need to maintain high photogenerated hole concentrations at the oxide/silicon interface. In the case of Ir/TiO_2/SiO_2/Si photoanodes, this strategy increased the photovoltage from negative apparent photovoltage to 550 to over 600 mV across the thickness range including a maximum of 630 mV.[1] Here we fabricate an equivalent set on p^+Si, nSi, and p^+nSi substrates with the Al_2O_3/SiO_2 bilayer oxide.

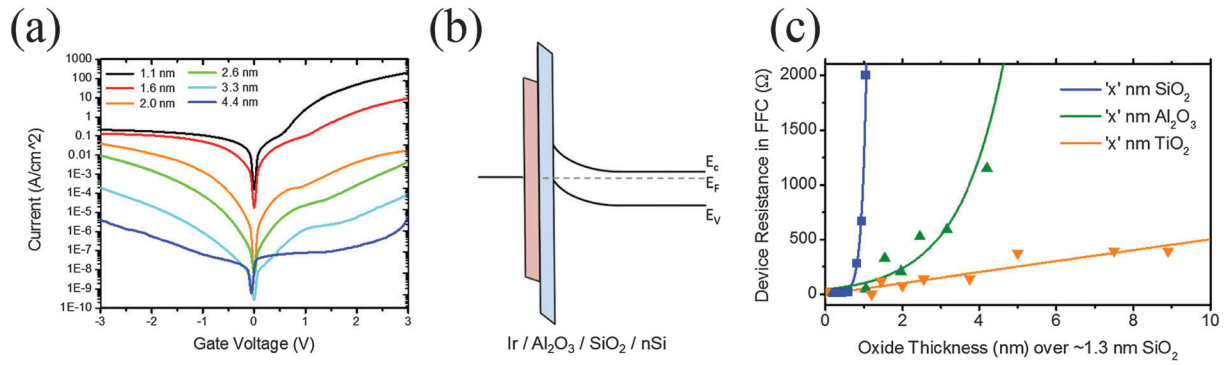

Fig. 8 (a) Leakage current density (measured in the dark) *versus* voltage of Ir/'*x*' nm ALD-Al_2O_3/1.3 nm SPA-SiO_2/nSi anodes. (b) Ir/Al_2O_3/SiO_2/nSi band diagram showing symmetric band alignment about the Si band edges, similar to SiO_2 and unlike TiO_2. (c) Resistance scaling from ferri/ferrocyanide cyclic voltammetry for the Ir/'*x*' nm '*X*' oxide/1.3 nm SiO_2/p^+Si structure measured in the dark to directly compare conductivity of the SiO_2, Al_2O_3, and TiO_2 thickness scaling over a 1.3 nm SiO_2/Si substrate. The alumina exhibits an intermediate thickness scaling of resistance compared to that of SiO_2 (tunnel oxide) and TiO_2 (bulk-limited Ohmic resistance).

Each anode is analyzed with the reversible redox couple ferri/ferrocyanide and under water oxidation conditions as before (ESI,† S16–S18). The total resistance extracted from the ferri/ferrocyanide electrochemistry is shown in Fig. 9(a) and exhibits exponential scaling with thickness, although as shown in Fig. 8(c), the characteristic is less steep than for SiO_2. Similar to TiO_2/SiO_2 bilayers, the nSi extracted series resistance and water splitting overpotential both scale more rapidly with alumina thickness in Al_2O_3/SiO_2 than do the p^+Si values. The photovoltage is defined as the difference between the photoanode overpotential and the p^+Si overpotential for water splitting, at a characteristic photocurrent of 1 mA cm^{-2}. The oxide series resistance loss should be the same in the p^+Si, nSi, and p^+nSi cases; therefore, any difference in thickness scaling of the overpotential required to support this current density when comparing dark electrolysis on p^+Si to the photoelectrolysis with the other anodes is indicative of the photovoltage loss described previously. Here, the p^+n junction eliminates more than half of this loss, achieving photovoltages at 1 mA cm^{-2} as high as 570 mV for the Al_2O_3/SiO_2 bilayer compared with the 490 mV maximum for the nSi case. For thicker insulator layers, the benefit of the p^+n layer is even more pronounced, as previously observed for TiO_2/SiO_2 bilayers.[1] These findings further indicate the advantage of decoupling capacitive oxides from the semiconductor junction by utilizing the buried p^+n configuration. The fact that the loss is not completely removed by the p^+ surface region, however, indicates the importance of satisfying all of the protected photoanode design principles described previously, including the need to limit the overall insulator resistance to reasonable values while ensuring a high quality interface.[1] The contributions of a relatively ideal tunnel oxide such as SiO_2 or the non-ideal resistive oxide Al_2O_3 can dominate the overall impedance of the device even at small oxide thicknesses. Sentaurus software was also used to compare the alumina data to the predictions of a quantum tunneling model, showing that satisfactory fits were not possible with literature-reported hole effective masses (ESI,† S19).

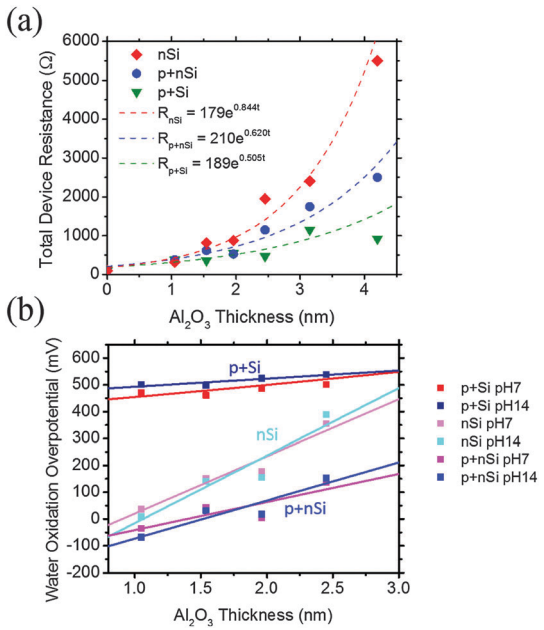

Fig. 9 (a) Total resistance from ferri/ferrocyanide electrochemistry for Ir/'*x*' nm ALD-Al_2O_3/1.3 nm chemical SiO_2/Si devices for nSi (red) and p^+nSi (blue) 1 Sun AM 1.5, and p^+Si (green) dark. As seen in the TiO_2/SiO_2 system, nSi exhibits a photovoltage loss compared to p^+Si, here shown as a greater series resistance per nanometer of oxide. The p^+nSi eliminates more than half of the loss. (b) Water oxidation overpotential at 1 mA cm^{-2} for nSi exhibits a greater loss per nanometer than for p^+Si, meaning a photovoltage loss. The p^+nSi device has higher photovoltage at every Al_2O_3 thickness, but does not recover all of the loss. The photovoltage at 1 mA cm^{-2} is 570 mV for p^+nSi junctions compared to 490 mV for the nSi MIS Schottky junction with ~1 nm of Al_2O_3.

3. Conclusions

The resistive and capacitive contributions of the SiO_2, SiO_2/TiO_2, and Al_2O_3/TiO_2 insulator systems applied to silicon anodes for photoelectrochemical water oxidation have been investigated. By using slot-plane-antenna (SPA) plasma oxidation and atomic layer deposition (ALD), anodes can be fabricated with monolayer

precision of the insulator interlayer thickness, representing the smallest window of data acquisition currently possible. The SiO_2 is found to behave as a tunnel oxide, matching theoretical simulations well with a hole tunneling effective mass of 0.37. When studied in the Ir/SiO_2/Si anode structure, this means that SiO_2 thicknesses less than 2 nm achieve maximum conductance in an electrochemical device. In the Ir/1.5 nm TiO_2/SiO_2/Si bilayer structure, the TiO_2 also contributes to the capacitance and the SiO_2 contributes non-negligible resistance at thicknesses as low as 1 nm.

The density of conduction states in the TiO_2 affects tunneling across the SiO_2, meaning that the two must be considered together to optimize such photoanodes. This work shows that, regardless of the conductivity of the protection layer, the thickness of the SiO_2 interlayer should be less than 2 nm to avoid substantial resistive losses across anode structure. Because relatively insulating protection layers ensure a high MIS built-in field and minimal non-radiative recombination, this influence of the SiO_2 interlayer can be especially significant. This work suggests that SiO_2 interlayers less than 1 nm in thickness could provide greatly improved performance of insulator-protected photoanodes if such layers can be synthesized reproducibly and with high interface quality.

In an effort to explore other insulator systems beyond TiO_2 and to better understand the extent of these findings, ALD-Al_2O_3 was studied on silicon anodes. Al_2O_3 coated structures exhibited intermediate conductance, not as high as the ALD-TiO_2, but also not behaving as a tunnel oxide such as SiO_2. These experiments suggest that it may be possible to exploit leakage pathways in a larger group of insulators, expanding the scope of possible protection layer materials. The photovoltage of Al_2O_3 coated devices was also studied and the characteristic insulator thickness-dependent photovoltage loss described recently for TiO_2/SiO_2 bilayers and SiO_2 interlayers was also observed. Consistent with that recent report,[1] a p^+n junction located 450 nm below the oxide/silicon interface was capable of reducing photovoltage loss. The best photovoltage achieved for a Ir/Al_2O_3/SiO_2/Si device with $\sim$1 nm of protective Al_2O_3 increased from 490 mV (for nSi MIS Schottky junctions) to 570 mV when a buried p^+n junction was used.

4 Methods and materials

4.1 Silicon substrates

Heavily boron-doped (100) p-type silicon wafers (ρ = 0.001–0.002 Ω cm, thickness 505–545 μm) were used as conductive silicon substrates to study water oxidation in the dark. Moderately phosphorous-doped (100) n-type silicon wafers (ρ = 0.14–0.24 Ω cm, thickness 450 μm) were used for Type I MIS Schottky junction photoanodes. Buried junction devices were made with n-type silicon wafers and were subjected to a standard clean using a Semitool Spray Acid: first the wafers are subjected to ozone and DI water, then NH_4OH (2000 : 1) is added to help remove particles and organics, and lastly ozone, DI water, and HF (1150 : 1) are used to etch the chemical oxide and regenerate the surface oxide also removing any metallic species. The implant is performed with a 4×10^{15} cm^2 dose of boron at 15 keV. Following the implantation, the samples were annealed at 950 °C for 40 minutes leaving a junction depth of approximately 0.8 microns.

4.2 Wafer clean and slot-plane antenna (SPA) oxidation

Before SiO_2 growth, prime grade Si(100) wafers were prepared using a three part clean: 10 minutes at 50 °C in 5 : 1 : 1 H_2O : H_2O_2 : NH_4OH to remove trace organics, 10 minutes at 50 °C in 5 : 1 : 1 H_2O : H_2O_2 : HCl to remove trace metal ions, and then 30 seconds in 2% HF to remove the silicon dioxide layer. Lastly the substrates were spun dry leaving a hydrogen passivated silicon surface for plasma oxide growth. Measurement of apparent SiO_2 thickness *via* ellipsometry before the plasma growth of oxide gives a value of approximately 7 Å. The SiO_2 layer is regrown with precise thickness control using the slot plane antenna (SPA) plasma method. A 2.45 GHz microwave is used to generate a uniform high density plasma below the dielectric shower plate with a diameter exceeding 30 cm, capable of uniformly covering large wafers. The deposition temperature was set to 500 °C for an actual substrate temperature of approximately 400 °C and allowed to equilibrate while argon was purged through the chamber at 100 sccm. Then the argon flow rate was increased to 1500 sccm and oxygen gas was introduced at 400 sccm for 10 seconds. Finally the argon flow was set to 1200 sccm and oxygen held at 40 sccm for 25 seconds at a process pressure of 5 Torr. The microwave power was set to 3000 W and held for the duration of the growth time. After the microwave power is shut off, argon is allowed to flow for an additional 3 seconds to conclude the process. This process was optimized for the thinnest possible oxides; decreasing the process time to 3 to 5 seconds results in depositions around 15 Å in thickness, the approximate minimum for this method. By extending the run length, films of over 100 Å can be grown but they require increasingly long deposition times. More details can be found in previously published work.[30]

4.3 Atomic layer deposition (ALD) of TiO_2

Titanium dioxide layers were deposited in a custom home-built ALD chamber with tetrakis(dimethylamido)titanium (TDMAT) as the metal precursor and water as the oxidant. The bubbler is kept at 70 °C and a gradient is maintained between the bubbler and chamber reaching 120 °C at the inlet. The substrate temperature was approximately 170 °C for all deposition in accordance with the ALD window reported previously, the TDMAT was pulse time was 0.7 s and the H_2O pulse time was 0.5 s.[17] The purge pressure was approximately 600 mTorr. These depositions had stable growth rates of $\sim$0.6 Å per cycle over the thickness ranges studied. Details of our ALD system and process have been published separately.[41]

4.4 Atomic layer deposition (ALD) of Al_2O_3

Aluminium oxide layers were deposited in the same custom home-built ALD chamber with trimethylaluminium (TMA) as the metal precursor and water as the oxidant. The precursors

are delivered by a system built by Masafumi Kitano of Fujikin incorporated, which uses nitrogen as a push gas to deliver TMA to the main chamber. The substrate temperature was approximately 270 °C, the equilibrium purge pressure was ~600 mTorr, and the resultant growth rate varied between 0.72 and 0.75 Å per cycle over the thickness range studied.

4.5 Deposition of catalyst and back-contact

Iridium metal catalysts and platinum and aluminium back-contact metals were deposited by electron beam evaporation. The surface catalyst was a blanket 2 nm layer of iridium for all water splitting cells. MOS capacitors for solid-state analysis had 50 nm of Ir to allow for effective probing of the metal gate. All p^+-Si samples had a back-side contact of 20 nm of e-beam Pt deposited and n-Si samples had an e-beam deposited 100 nm Al backside contact to provide an Ohmic contact.

4.6 Aqueous solution preparation

As in previous work, aqueous solutions of pH 0, 7, and 14 were prepared to study performance across the pH range. Solutions were 1 M H_2SO_4, 1 M NaH_2PO_4/Na_2HPO_4 buffer, and 1 M NaOH respectively. All solutions were prepared with MilliQ water and checked against both a bench top glass pH electrode and the reversible hydrogen potential using Pt electrodes. Solution resistance values of the solutions in the electrochemical cell used in this work were 4.3 Ω, 40.0 Ω, and 11.2 Ω for the pH 0, 7, 14 solutions, and were measured by electrochemical impedance spectroscopy. All water oxidation overpotential numerical results are corrected by subtracting the product of the measured current and the series resistance from the applied voltage: $E_{corr} = E_{applied} - iR_{series}$. The plotted water oxidation curves are the raw data, not corrected.

4.7 Ferri/ferrocyanide preparation

The reversible redox couple ferri/ferrocyanide was prepared to study electronic carrier transport in these anodes. Potassium ferricyanide and potassium ferrocyanide trihydrate were used to make a 1 : 1 solution containing 10 mM of each species with 1 M potassium chloride. MilliQ water was used for these solutions.

4.8 Cyclic voltammetry

Electrochemical measurements were carried out using a glass frit isolated Ag/AgCl/saturated KCl reference electrode and a platinum wire counter electrode, as detailed by Chen *et al.*[3] The active area of 0.196 cm^2 was defined by a bored Teflon cone pressed down onto the nano-layered anode. All ferri/ferrocyanide *CV*'s were measured at a scan rate of 100 mV s^{-1} in a static solution. A peristaltic pump was used during water oxidation to circulate the solution at 1 mL s^{-1}; water oxidation current *vs.* potential data were also collected at a scan rate of 100 mV s^{-1}.

4.9 MIS capacitor fabrication

MIS capacitors were fabricated using stencil lithography. Various gate metals were deposited through a shadow mask defining circular capacitors of diameters ranging from 100 to 250 μm and thicknesses of 50 nm on n-Si.

4.10 Solid-state leakage (*IV*) and capacitance (*CV*) analysis

Solid-state *IV* measurements were taken with an Agilent 4155C Semiconductor Parameter Analyzer and *CV* measurements were taken with a Hewlett Packard 4284A precision LCR. In *CV*, the complex reactance was measured taking the real component as the conductance *G* and the imaginary as the capacitance *C*. All measurements were taken at room temperature. *IV* scans are measured from zero applied voltage to positive and then from zero applied voltage to negative substrate voltage respectively. *CV* measurements are performed with the high potential on the substrate and the low on the gate and then plotted against gate voltage. The LCR meter can measure between 20 Hz and 1 MHz. The AC measurement frequencies used in each measurement in this study are 1, 3, 5, 8, 10, 30, 50, 80, 100, 300, 500, 800 kHz, and 1 MHz. The DC bias is swept at approximately 215 mV s^{-1} from the inversion to accumulation regime with a 0.1 V bias step, no delay, an averaging rate of 4, medium integration time, and a 50 mV AC bias. The LCR meeting has three integration times, short, medium, and long that correspond to 30, 65, and 200 ms respectively. The medium time is used throughout except in ESI,† S13. Measurements are performed in the dark with the sample on copper tape on an insulating glass slide on a vacuum chuck. An air suspended table is used to minimize noise due to series resistance fluctuations. The back contact is probed by contacting the copper tape with a Micromanipulator type 7H hard tip probe made of beryllium and copper for minimum series resistance. The gate metal is contacted with a Micromanipulator type 7S spring loaded tip made of tungsten which has high compliance such that the tip does not scratch through the 50 nm metal.

4.11 Cyclic voltammetry modelling for equivalent resistance

The cyclic voltammograms obtained in ferri/ferrocyanide were fit to theoretically determined profiles using EC-lab software V10.21. The maximally conductive anode *CV*'s were first fit (less than 2 nm SiO_2 in the metal/SiO_2/Si case) assuming no uncompensated series resistance, a surface area of 0.196 cm^2, ferricyanide and ferrocyanide concentrations of 10 mM, a scan rate of 100 mV s^{-1}, room temperature, and the charge transfer coefficient $\alpha = 0.50$. The best fits were obtained with $E_0 \approx 0.3$ *vs.* Ag/AgCl/sat. KCl electrode, $k_0 = 0.01$ cm s^{-1}, $D_O = 8.5 \times 10^{-6}$ cm^2 s^{-1}, and $D_R = 3.5 \times 10^{-6}$ cm^2 s^{-1} (S3). Similar values were used in our past analysis and compared favorably to literature values for this sort of analysis.[5] The voltammogram of all other anodes in this study in ferri/ferrocyanide were then fit with the same parameters, only varying the uncompensated series resistance.

4.12 Sentaurus modelling

Theoretical resistance of oxide stacks was modelled using Synopsys Sentaurus TCAD (Version I-2013.12-SP1). Accurate simulation of the experimental resistance data for SiO_2 on p^+ crystalline silicon was accomplished by varying the hole

tunnelling mass in SiO_2. Band offsets were determine by the Anderson rule based on the electron affinities and bandgap energies of the materials. Default material properties, found within the software databases, were used for both silicon and SiO_2. A summary of these material properties is given in ESI,† S20. An Iridium workfunction of 5.3 eV was assumed based on the range of reported values (5.0–5.7 eV) in literature.[42] For dielectric stacks involving TiO_2 a bandgap of 3.2 eV,[43] an electron affinity of 4.2 eV,[44] and a dielectric constant of 32[45] were assumed. The TiO_2 was assumed to have moderate n-type doping of 1×10^{17} cm^{-3}. When treating TiO_2 as a tunnelling oxide a hole effective mass of $0.23m_0$[28,29] was used based on previous reports. For Al_2O_3 we used a bandgap of 6.1 eV[46,47] and an electron affinity of 1.95 eV[47] with a dielectric constant of ~ 8.[48] Resistance was calculated from a linear fit of the simulated I–V characteristics between 0 and 100 mV. This voltage regime was used to be consistent with the cyclic voltammetry determination of resistance. Using the effective electrical oxide thickness determined from capacitance–voltage measurements a hole effective mass of $0.375m_0$ was established.

4.13 Capacitance high leakage modelling

The capacitance voltage breakdown modelling is performed by a self-coded GUI program in MATLAB R2013a. Among the three parameters in the equivalent circuit, C_{ox} is assumed to be constant while C_s and G_{ox} vary with applied gate voltage (V_g). C_{ox} is approximated by the measured high frequency capacitance at strong accumulation region (f = 1 MHz, V_g = 2 V), where C_s can be removed from the equivalent circuit since $C_s \gg C_{ox}$ and $\omega \cdot C_s \gg G_{ox}$. The extraction of C_s and G_{ox} is achieved by manually changing these two values to fit the calculated frequency dispersion of capacitance (C–ω curve) with the experimental dispersion at each V_g point. This modelling is valid all the way in the accumulation region to the flat band voltage point, beyond which capacitance response due to interface traps (D_{it}) starts to affect the fitting.

Author contributions

A. S. prepared all samples and performed all experiments for this study with the aid of undergraduates D. Lu on metal/SiO_2/Si samples and P. Satterthwaite for oxygen scavenging. K. Kemp performed all Sentaurus modelling for hole quantum tunnelling. K. T. with support from A. S. developed the capacitance–voltage breakdown model and analysed the experimental data. T. I. performed the SPA-SiO_2 plasma oxidation. A. S., C. E. D. C. and P. C. M. designed the experiments. All authors helped in the preparation of the manuscript.

Conflicts of interest

The authors declare no competing financial interests.

Acknowledgements

We thank T. Carver for metal e-beam evaporation and the SNF for upkeep of the slot-plane-antenna (SPA) capability as well as Tokyo Electron Ltd who financially backed a new magnetron for the system partway through the project. A. S. would also like to thank R. Long and O. Hendricks from the McIntyre and Chidsey groups for their support and insights throughout this work. We also thank L. Zhang and M. Kitano for their help in building and maintaining the ALD chambers. C. Hitzman, A. Vailionis, A. Meng, and O. Hendricks are acknowledged for assistance with Raman, XRD, TEM, and XPS characterization respectively. Our collaborators at Tyndall National Institute Paul Hurley, Martyn Pemble, Ian Povey, and Adrian Walsh are acknowledged for providing the p+n wafers used in this study. This work was partially supported by the Stanford Global Climate and Energy Project and National Science Foundation program CBET-1336844. A. S. graciously acknowledges financial support from a Stanford Graduate Fellowship and a National Science Foundation Graduate Fellowship. The Tyndall silicon fabrication facility is acknowledged for the p^+/n silicon junctions used in this study.

Notes and references

1 A. G. Scheuermann, J. P. Lawrence, K. W. Kemp, T. Ito, A. Walsh, C. E. D. Chidsey, P. K. Hurley and P. C. McIntyre, *Nat. Mater.*, 2015, DOI: 10.1038/nmat4451.
2 B. A. Pinaud, J. D. Benck, L. C. Seitz, A. J. Forman, Z. Chen, T. G. Deutsch, B. D. James, K. N. Baum, G. N. Baum, S. Ardo, H. Wang, E. Miller and T. Jaramillo, *Energy Environ. Sci.*, 2013, **6**, 1983.
3 Y. W. Chen, J. D. Prange, S. Duhnen, Y. Park, M. Gunji, C. E. D. Chidsey and P. C. McIntyre, *Nat. Mater.*, 2011, **10**, 539.
4 A. G. Scheuermann, J. P. Lawrence, M. Gunji, C. E. D. Chidsey and P. C. McIntyre, *ECS Trans.*, 2013, **58**(10), 75.
5 A. G. Scheuermann, J. D. Prange, M. Gunji, C. E. D. Chidsey and P. C. McIntyre, *Energy Environ. Sci.*, 2013, **6**, 2487.
6 S. Hu, M. R. Shaner, J. A. Beardslee, M. Lichterman, B. S. Brunschwig and N. S. Lewis, *Science*, 2014, **344**, 1005.
7 K. Sivula, *ChemCatChem*, 2014, **6**, 2796.
8 M.T. McDowell, M. Lichterman, R. Liu, A. Carim, B. Brunschwig, N. Lewis, Symposium J Spring MRS Meeting, San Francisco, CA, April 9, 2015.
9 M. A. Green, *Appl. Phys. Lett.*, 1978, **33**, 178–180.
10 B. Mei, A. A. Permyakova, R. Frydendal, D. Bae, T. Pedersen, P. Malacrida, O. Hansen, I. E. L. Stephens, P. C. K. Vesborg, B. Seger and I. Chorkendorff, *J. Phys. Chem. Lett.*, 2014, **5**, 3456.
11 M. F. Lichterman, A. I. Carim, M. T. McDowell, S. Hu, H. B. Gray, B. S. Brunschwig and N. S. Lewis, *Energy Environ. Sci.*, 2014, **7**, 3334–3337.
12 M. T. McDowell, M. F. Lichterman, J. M. Spurgeon, S. Hu. I.D. Sharp, B. S. Brunschwig and N. S. Lewis, *J. Phys. Chem. C*, 2014, **118**, 19618–19624.
13 B. Mei, T. Pederson, P. Malacrida, D. Bae, R. Frydendal, O. Hansen, P. C. K. Vesborg, B. Seger and I. Chorkendorff, *J. Phys. Chem. C*, 2015, **119**, 15019–15027.

14 M. J. Kenney, M. Gong, Y. Li, J. Z. Wu, J. Feng, M. Lanza and H. Dai, *Science*, 2013, **342**, 836.
15 B. Mei, B. Seger, T. Pedersen, M. Malizia, O. Hansen, I. Chorkendorff and P. C. K. Vesborg, *J. Phys. Chem. Lett.*, 2014, **5**, 1948–1952.
16 D. Corrigan, *J. Electrochem. Soc.*, 1987, **134**, 377.
17 E. L. Miller and R. E. Rocheleau, *J. Electrochem. Soc.*, 1997, **144**, 3072.
18 K. Sekine, Y. Saito, M. Hirayama and T. Ohmi, *J. Vac. Sci. Technol., A*, 1999, **17**, 3129.
19 T. Sugawara, S. Matsuyama, M. Sasaki, T. Nakanishi, S. Murakawa, J. Katsuki, S. Ozaki, Y. Tada, T. Ohta and N. Yamamoto, *Jpn. J. Appl. Phys.*, 2005, **44**, 1232.
20 Effective mass is a concept used in physics to match the observed behaviour of a particle to Netwonian second law behaviour to simplify solutions to the Schrödinger equation. The value reported is a pre-factor to the free electron mass, m_0, and is typically specific to the process studied, such as band transport or tunnelling. The tunnelling effective mass is determined by measuring direct tunnelling behaviour, fitting the data to a direct tunnelling model, and extracting the pre-factor that achieves the ideal fit. For WKB tunnelling, experimental tunnelling current in MOS structures is used in particular.[49,50] An analogous procedure is carried out in this work and the best-fit pre-factor for SPA-SiO_2 in the photo-electrochemical cell falls in the middle of literature reported values, particularly when computing it with SiO_2 thickness values obtained from capacitance voltage analysis.
21 R. K. Chanana, K. McDonald, M. D. Ventra, S. T. Pantelides and L. C. Feldman, *Appl. Phys. Lett.*, 2000, **77**, 2560.
22 R. K. Chanana, *Appl. Phys. Lett.*, 2011, **109**, 104508.
23 M. I. Vexler, S. E. Tyaginox and A. F. Shulekin, *J. Phys.: Condens. Matter*, 2005, **17**, 8057–8068.
24 Y. T. Hous, M. F. Li, Y. Jin and W. H. Lai, *J. Appl. Phys.*, 2002, **91**, 258.
25 R. Waters and B. Van Zeghbroeck, *Appl. Phys. Lett.*, 1998, **73**, 3692.
26 H. Kim, P. C. McIntyre, C. O. Chui, K. C. Saraswat and S. Stemmer, *J. Appl. Phys.*, 2004, **96**, 3467.
27 K.-I. Seo, D.-I. Lee, P. Pianetta, H. Kim, K. C. Saraswat and P. C. McIntyre, *Appl. Phys. Lett.*, 2006, **89**, 142912.
28 J. Racko, M. Mikolasek, L. Harmatha, J. Breza, B. Hudec, K. Froehlich, J. Aarik, A. Tarre, R. Granz-ner and F. Schweirz, *J. Vac. Sci. Technol., B*, 2011, **29**(1), 01AC08.
29 J. Racko, M. Mikolasek, R. Granzner, J. Breza, D. Donoval, A. Grmanova, L. Harmatha, F. Schwierz and K. Froehlich, *Cent. Eur. J. Phys.*, 2011, **9**(1), 230.
30 É. O'Connor, *et al.*, Observation of peripheral charge induced low frequency capacitance-voltage behaviour in metal-oxide-semiconductor capacitors on Si and GaAs substrates, *J. Appl. Phys.*, 2012, **111**, 124104.
31 R. B. Godrey and M. A. Green, *Appl. Phys. Lett.*, 1979, **34**(11), 790.
32 M. A. Green, *Semicond. Sci. Technol.*, 1993, **8**, 1.
33 R. Singh, M. A. Green and K. Rajkanan, *Sol. Cells*, 1981, **3**, 95–148.
34 M. A. Green and A. W. Blakers, *Sol. Cells*, 1983, **8**, 3–16.
35 M. Grauvogl and R. Hezel, *Prog. Photovoltaics*, 1998, **6**, 15–24.
36 K. J. Yang and C. Hu, *IEEE Trans. Electron Devices*, 1999, **46**(7), 1500–1501.
37 C.-H. Choi, Y. Wu, J.-S. Goo, Z. Yu and R. W. Dutton, *IEEE Electron Device Lett.*, 2000, **47**(10), 1843–1850.
38 K. Tang, A. Scheuermann, L. Zhang and P. McIntyre, unpublished work.
39 H. Klumbies, P. Schmidt, M. Haehnel, A. Singh, U. Schroeder, C. Richter, T. Mikolajick, C. Hossbach, M. Albert, J. W. Bartha, K. Leo and L. Mueller-Meskamp, *Org. Electron.*, 2015, **17**, 138–143.
40 T. Hirvikorpi, M. Vähä-Nissi, T. Mustonen, E. Iiskola and M. Karppinen, *Thin Solid Films*, 2010, **518**, 2654–2658.
41 N. L. Nukiman, *et al.*, *Durability and corrosion of aluminium and its alloys: overview, property space, techniques and developments*, INTECH Open Access Publisher, 2012.
42 *CRC Handbook of Chemistry and Physics*, ed. W. M. Haynes, T. J. Bruno and D. R. Lide, 95th edn, 2014, pp. 12–124.
43 N. Fuke, *et al.*, *Sol. Energy Mater. Sol. Cells*, 2009, **93**, 720–724.
44 A. G. Pattantyus-Abraham, *et al.*, *ACS Nano*, 2010, **4**, 3374–3380.
45 S. Swaminathan and P. C. McIntyre, *Electrochem. Solid-State Lett.*, 2010, **13**, G79–G82.
46 C. O. Chui, H. Kim, P. C. McIntyre and K. C. Saraswat, *IEEE Electron Device Lett.*, 2004, **25**, 274–276.
47 V. V. Afanas'ev, *Adv. Condens. Matter Phys.*, 2014, **2014**, 1–30.
48 M. Friedemann, M. Woszczyna, A. Müller, S. Wundrack, T. Diziomba, T. Weimann and F. J. Ahlers, *Sci. Technol. Adv. Mater.*, 2012, **13**, 025007.
49 Y. T. Hou, M. F. Li, Y. Jin and Y. W. H. Lai, *J. Appl. Phys.*, 2002, **91**, 258–264.
50 M. I. Vexler, S. E. Tyaginov and A. F. Shulekin, *J. Phys.: Condens. Matter*, 2005, **17**, 8057.