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AIP ADVANCES **2**, 041403 (2012)

A doping-free approach to carbon nanotube electronics and optoelectronics

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The electronic properties of conventional semiconductor are usually controlled by doping, which introduces carriers into the semiconductor but also distortion and scattering centers to the otherwise perfect lattice, leading to increased scattering and power consumption that becomes the limiting factors for the ultimate performance of the next generation electronic devices. Among new materials that have been considered as potential replacing channel materials for silicon, carbon nanotubes (CNTs) have been extensively studied and shown to have all the remarkable electronic properties that an ideal electronic material should have, but controlled doping in CNTs has been proved to be challenging. In this article we will review a doping-free approach for constructing nanoelectronic and optoelectronic devices and integrated circuits. This technique relies on a unique property of CNTs, i.e. high quality ohmic contacts can be made to both the conduction band and valence band of a semiconducting CNT. High performance nanoelectronic and optoelectronic devices have been fabricated using CNTs with this method and performance approach to that of quantum limit. In principle high performance electronic devices and optoelectronic devices can be integrated on the same carbon nanotube with the same footing, and this opens new possibilities for electronics beyond the Moore law in the future. *Copyright 2012 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported license.*[http://dx.doi.org/10.1063/1.4773222]

I. INTRODUCTION

The technique of doping lies at the very heart of semiconductor industry. Doping provides high degree of control on the electronic properties of semiconductors, but at the same time distorts the lattice of otherwise perfect lattice of the semiconductor so as to increase scattering and power dissipation, and reduce the speed of the device. While not desirable, these drawbacks associated with doping are still tolerable for devices of relative large size. But as the device size is scaled down to several nanometers, the random and statistic nature of dopants in the device results in uncontrollable fluctuations in device per formation, and ultimately sets an upper limit to the performance of the devices and integrated circuits.

After more than four decades of rapid developments of the Si-based metal-on-semiconductor (MOS) technology, in 2005, the International Technology Roadmap of Semiconductor (ITRS) committee announced that the Si-based CMOS will reach its absolute performance limits by around 2020.[1,2] Recognizing that it may be timely to accelerate development of the most promising technologies for well-defined new information processing devices, the ITRS committee requested in 2008 the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) working groups to recommend one or two of the most promising technologies for detailed roadmaping and accelerated development. To response, the ERD/ERM working groups conducted a study to evaluate several "Beyond CMOS candidate information processing technologies," followed by near-consensus

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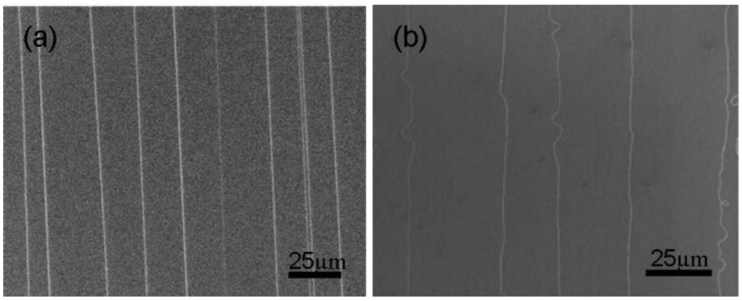

FIG. 1. SEM images showing SWCNT arrays grown on silicon wafers using (a) Cu and (b) Fe-based catalysts. Reprinted with permission from R. L. Cui *et al.*, J. Phys. Chem. C **114**, 15547 (2010). Copyright 2010, American Chemical Society.

selection of one or two technology entries having high potential for enabling a paradigm shifting information processing technology. The single candidate selected was "Carbon-based Nanoelectronics" to include carbon nanotubes (CNT)[3] and graphene[4] for additional resources and detailed road mapping for ITRS as promising technologies targeting commercial demonstration in the 5–10 year horizon. In 2009 the ITRS supported the ERD/ERM Working Group's choice of carbon-based nanoelectronics for additional focused roadmapping and accelerated development.[2]

Both carbon nanotube and graphene have extremely high intrinsic carrier mobility, atomically well-defined surfaces, and miniaturized dimensions.[5] Unlike CNT, an intrinsic graphene does not have a well defined bang gap which prevents the graphene from being used as field-effect transistors (FETs) directly in high performance digital integrated circuits.[6] In principle a graphene nanoribbon (GNR) can be fabricated with an energy gap that is inversely proportional to the width of the ribbon.[7] But unfortunately, the opening of the band gap is usually accompanied by a rapidly decreasing carrier mobility, making the graphene-FET less suitable for high-performance digital applications.[8]

The superb electronic properties of CNTs make the CNT-based nanoelectronic devices superior in many ways to Si-based devices.[9] On the device level, CNT FETs are shown to be about five times faster than Si devices with the same gate length, but consumes only a few percent power when compared with that based on Si.[9,10] On the circuit level, it was recently demonstrated that a pass-transistor-logic (PTL), which is similar but different from CMOS, can be used in CNT based circuits.[11–13] In CMOS, signals are applied only to the gates of FETs. But in PTL signals can be inputted either on gates or sources of FETs, making the PTL based circuits more efficient. For example, a full adder circuit requires totally 28 FETs to implement in CMOS, but only 6 FETs are enough in PTL style,[11] making CNT one of the most promising channel materials for the nanoelectronics beyond 2020.

II. CHEMICAL VAPOR DEPOSITION GROWTH OF SINGLE-WALLED CARBON NANOTUBE

Among the various forms of CNTs, the horizontally aligned ultralong parallel arrays of single-walled CNTs (SWCNTs) directly grown on substrates are most suitable for fabricating high performance nanoelectronic and optoelectronic devices, for this type of samples suffer minimum damage to the structure leading to the highest performance among all CNT-based devices.[14–16] While Fe-based catalysts are widely used to grow SWCNT arrays,[15] the very high activity for Fe catalyzing the decomposition of carbon stocks often brings about the formation of multi-walled CNTs (MWCNT) and amorphous carbon. In addition, too much carbon feeding can even make the catalyst inactive and stop the tube growth.[17] In this aspect, Cu presents particular advantage. This is because Cu has the proper activity catalyzing the decomposition of carbon stocks and a lower solubility of carbon than that of Fe. This makes Cu a superior catalyst for growing SWCNT arrays of high quality (Fig. 1) and more suitable for FETs.[14,17]

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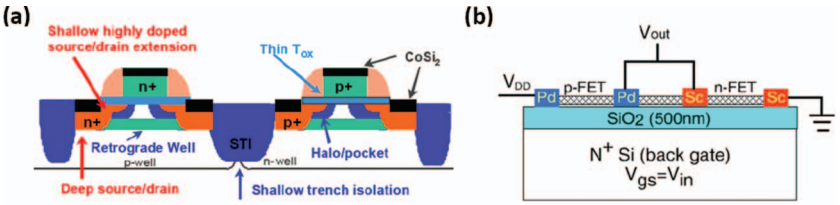

FIG. 2. Schematic diagrams showing the structure of (a) Si-based and (b) CNT-based CMOS inverters.

III. DOPING-FREE FABRICATION AND PERFORMANCE OF CNT FETs

As discussed in the preceding section, in CNT-based FETs, the channel materials are made via chemical rather than top-down fabrication method. In principle this provides a big advantage in fabricating small dimension devices than the conventional micro fabrication approach, since the dimension of the channel is defined basically by chemical means, *i.e.* interactions, instead of lithography masks. Therefore the fabrication of the nanosize channel of the CNT-based device is much cheaper, more reliable and chemically more stable than that of the Si-based device, and demands less sophisticated equipments for fabrication and packaging.

While various device structures have been explored in the past five decades since the discovery of the first transistor,[18] the Si-based FET has became the most important device and CMOS technology and the mainstream technology which accounts for more than 90% of the devices in today's integrated circuits (ICs). CMOS technology is based on the complementary use of n-type and p-type FETs, and the main reasons for the dominance of CMOS technology in ICs are its excellent error immunity and low energy consumption.[19]

The simplest CMOS circuit is an inverter (Fig. 2) which is the most fundamental logic gate that performs a Boolean operation on a single input variable. While the fabrication of a typical standard twin-well Si CMOS inverter involves totally 32 steps, including 10 lithography, 6 etching, 8 ion implantation and 8 film growth steps, the fabrication of a CNT-based CMOS inverter involves only 17 steps without any complicated ion implantation or other doping steps.[20] The significant reduction in the fabrication steps is largely due to the doping-free and isolation-free process developed for CNT-based CMOS process, which we will discuss in some details in the following section.

In a conventional CMOS circuit (Fig. 2(a)), the electronic property of the semiconductor channel and the polarity of the FET are defined by the nature of doping in the channel and well. A semiconductor can be either n- or p-type, depending on the type of majority carriers provided by the dopants in the semiconductor being electron or hole. Similarly, a FET can be n- or p-type depending on the majority carriers in its on state being electrons or holes. But unlike the Si-based CMOS, in a short channel (ballistic or quasi-ballistic) CNT FET, carriers are not mainly provided by dopants in the channel (here CNT). Instead they are provided directly from the metal electrodes and controlled by the gate as depicted in Fig. 3.

The unique atomic and electronic structures of a semiconducting CNT allow the n-type ohmic contact be made to its conductance band by suitable low work function metal such as Sc[21] or Y,[22] and p-type ohmic contact to be made to the valence band by high work function metal, such as Pd.[23] Carefully low temperature experiments have been carried out and shown that these n- and p-type contacts may inject carriers without barrier into the semiconducting CNTs with moderate diameter between 1.5–3.0 nm, and the linear ohmic feature in the corresponding I-V characteristic persists down to extremely low temperature, e.g. at least 4.3K (Fig. 4), allowing almost perfect conductance approaching to theoretical limit of $4G_0$,[21,23] with $G_0=e^2/h$ being the quantum conductance. High performance n- and p-type CNT FETs can thus being made readily without doping on CNTs with performance approaching the theoretical limit.

Taking the Sc-contacted back-gate CNT FET as an example. Figure 4 shows the main characteristics of an almost perfect n-type CNT FET. The excellent performance of the Sc-contacted n-type CNT FETs results from several favorable features, in particular the excellent wetting with the CNT (Fig. 4(a)), suitable work function of 3.3 eV to align with the conductance band of the CNT,

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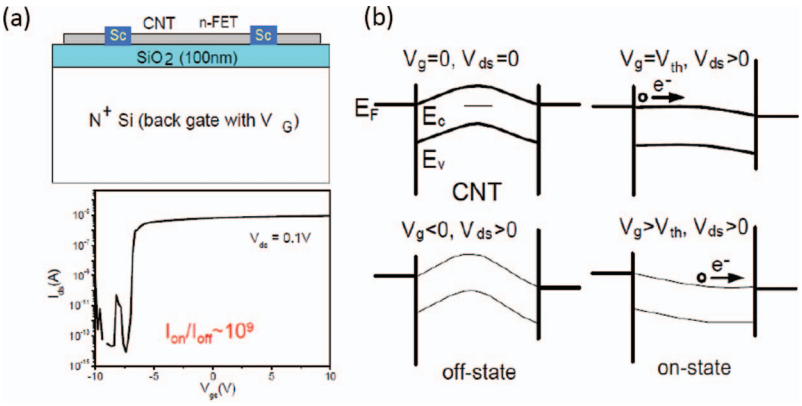

FIG. 3. Schematical diagram depicting (a) the structure of a back-gate CNT FET and its transfer characteristic, and (b) n-type operation.

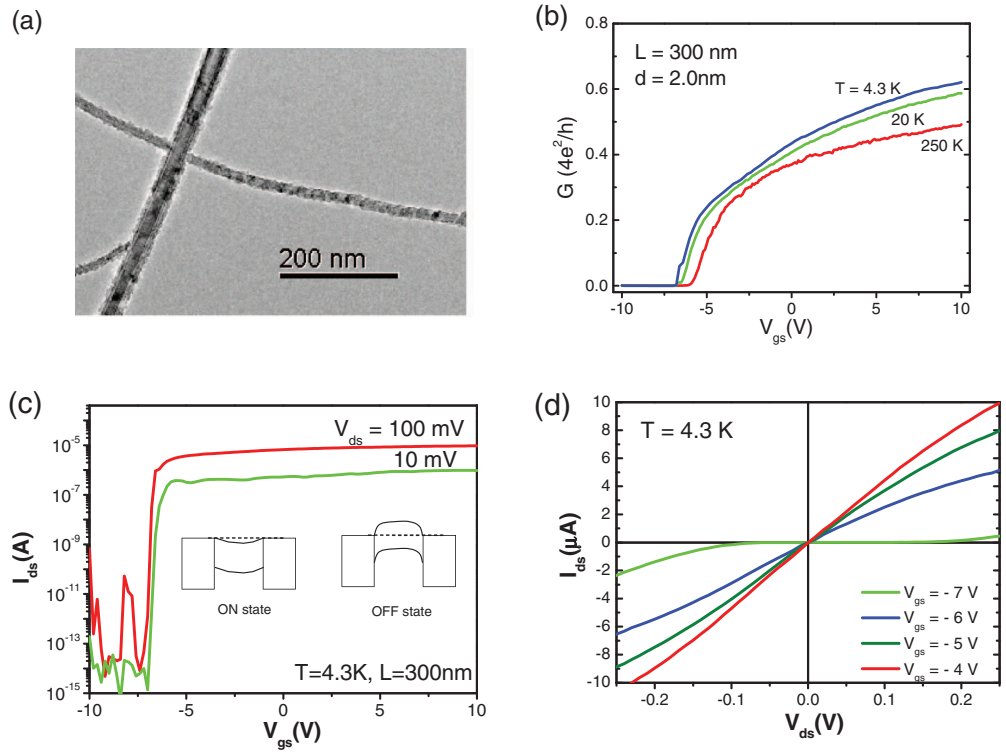

FIG. 4. Back-gated CNT based n-type CNT FET. (a) TEM image showing uniformly Sc-coated CNTs of various diameters. (b) Low bias channel conductance G vs gate voltage V_{gs} for a SWCNT with a diameter d = 2.0 nm and a length L = 300 nm. (c) Transfer characteristics of the same device as in (b) at different bias and at 4.3 K. Inset, schematic ON and OFF state band diagrams for a device with zero Schottky barriers for electron injection into the conduction band of the CNT. (d) $I_{ds} - V_{ds}$ curves for different V_{gs} at 4.3 K. Reprinted with permission from Z. Y. Zhang *et al.*, Nano Lett. **7**, 3603 (2007). Copyright 2007, American Chemical Society.

and suitable interaction with CNT which is not too strong to distort the perfect sp^2 arrangement of carbon atoms of the CNT and not too weak to allow efficient electrons injection into the CNT channel efficiently.

The field-transfer characteristics of the device (Fig. 4(b)) show clearly that the device is an n-type FET exhibiting on state at large gate voltage V_{gs}(~10 V) and a near ballistic on state conductance $G_{on} = 0.49\ G_0$ at 250 K. The on state conductance increases with decreasing temperature and reaches $G_{on} = 0.62\ G_0$ at 4.3 K. The metallic-like temperature dependence of the on state conductance and

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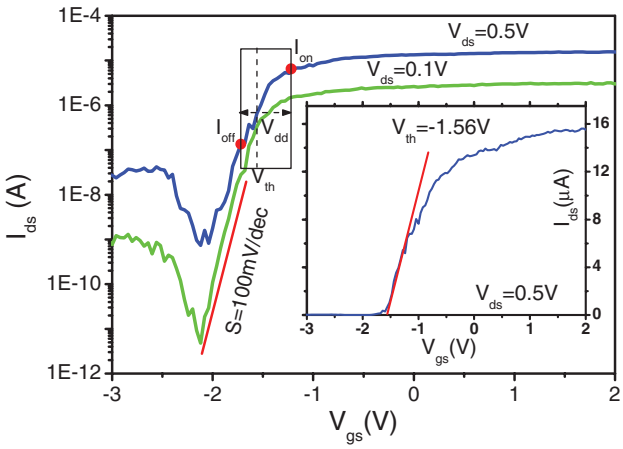

FIG. 5. Electric characteristic and relevant quantities that are used for defining gate-delay and energy-delay products. Inset, linear scale plot of I_{ds} versus V_{gs} measured at $V_{ds} = 0.5$ V in which the threshold voltage, $V_{th} = -1.56$V, was extracted using the standard peak transconductance method. The pane area defines the 0.5 V gate voltage window. Reprinted with permission from Z. Y. Zhang *et al.*, Appl. Phys. Lett. **92**, 133117 (2008). Copyright 2008, American Institute of Physics.

the almost perfect linear I_{ds}-V_{ds} characteristics down to 4.3 K suggest that the majority carriers in the channel are injected from the metal electrode instead from thermal excitations of extrinsic dopants which decreases with decreasing temperature. The perfect linear output characteristics at small bias (Fig. 4(d)) demonstrate amply that the contacts between the source/drain electrode and the CNT are ohmic and effectively barrier free even at 4.3K. At low temperature (4.3 K, Fig. 4(c)) the I_{on}/I_{off} ratio exceeds 10^9 at V_{ds}=0.1 V.

To make a fair quantitative comparison between nanoelectronic devices fabricated using different methods and materials, Intel device department suggested to benchmark CNT and other nanoelectronic devices against state-of-the-art Si FETs using several universal benchmark metrics,[9] and among those metrics the intrinsic gate-delay $\tau = CV/I$ and energy-delay product $CV/I \cdot CV^2$ are particularly important, with C being the gate capacitance, V=V_{dd} the supplied voltage of operation, and I the on-state current. The intrinsic gate delay τ represents the fundamental RC delay of the device, providing therefore an indicator to the frequency limit for the transistor operation. The energy-delay product, on the other hand, represents the switching energy of the device and is a fundamental parameter for logic applications. These metrics are shown to be relatively insensitive to gate dielectric and device geometry and are therefore good metrics for comparing different types of devices.

The on-state current I is defined under an operation voltage V as shown in Fig. 5 for a typical top-gate n-type CNT FET.[9] Both the intrinsic gate-delay and energy-delay products are calculated for devices with channel length L=440 nm, 220 nm[10] and 120 nm[24] and compared directly with that of previous reported n-type CNT FETs and Si based n-MOSFETs[9] for gate-delay (Fig. 6(a)) and energy-delay product (Fig. 6(b)). These figures clearly show that the performance of the Sc contacted n-type CNT FETs exceeds the performance of all earlier n-type CNT FETs and also state-of the-art Si n-MOSFETs. In particular, the CNT FET with a channel length of 120 nm has a gate-delay which is of the same order of magnitude as that of the current 32 nm technology node of Si-MOS FET, and an energy-delay product as that of the next 22 nm generation (Fig. 6). The significant improvement of the gate-delay and energy-delay products of CNT FETs over the silicon counterparts is mainly due to the quasi-ballistic nature of transport and the very high Fermi velocity in CNT FETs.

IV. TEMPERATURE PERFORMANCE OF CNT FETs: POTENTIAL FOR LOW AND HIGH TEMPERATURE ELECTRONICS

Unlike the conventional Si-based CMOS, the polarity of CNT FETs can be defined by controlling the injection of carriers to the CNT channel through suitable metal contacts. High-performance CNT

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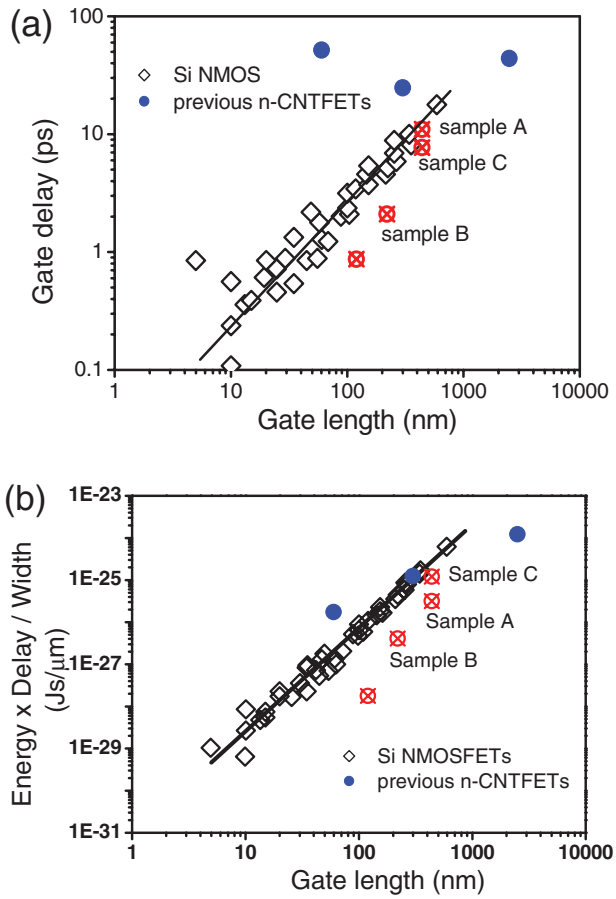

FIG. 6. Performance comparison between CNT-based FETs and Si-based FETs. (a) Gate delay vs gate length and (b) energy-delay product per device width vs gate length for n-type CNT FETs. Reprinted with permission from Z. Y. Zhang *et al.*, Appl. Phys. Lett. **92**, 133117 (2008). Copyright 2008, American Institute of Physics.

FETs can thus been made via a doping-free process. As a result of the absence of dopant in the device, CNT FETs are particularly suitable for low- and high-temperature electronics applications.[25]

It is well known that silicon-based CMOS devices can work normally at temperature range from −55 °C to 120 °C. At very low temperature, performance of the devices may be significantly degraded as a result of dopant freeze-out, leading to increased parasitic series resistance, kink phenomena and transient effects.[26,27] At high temperature, performance degradation may also occur due to such dopants related effects as p-n junction leakage and diffusion.[28,29] However, the dopants-related performance degradation at extreme temperature environment can be avoided in CNT FET devices and circuits since CNT devices can be fabricated with a doping-free process, providing a significant benefit for CNT devices when working at low- and high temperature.

We first consider the high-temperature performance of Pd-contacted top-gate p-type CNT FETs. The electronic properties of the devices were measured above room temperature (RT) in air. The transfer and output characteristics of a typical CNT FET with a channel length of about 2 μm are compared at two typical temperatures, i.e. at RT and 523 K (250 °C), as shown in Figs. 7(a), 7(c), and 7(d). The transfer characteristics of the device (Fig. 7(a)) show clearly that at RT, the on-state current saturates at about 24 μA and off-state current is as low as 3 pA yielding a current on/off ratio of more than 10^6. When the temperature is raised up to 250°C, the FET still shows typical p-type field-effect characteristics but with degraded performance. In particular the current on/off ratio drops to 10^3 which results largely from the slight decrease of the on-state current and a drastic increase of the off-state current. The decrease in the on-state current (from 24 μA to about 11 μA)

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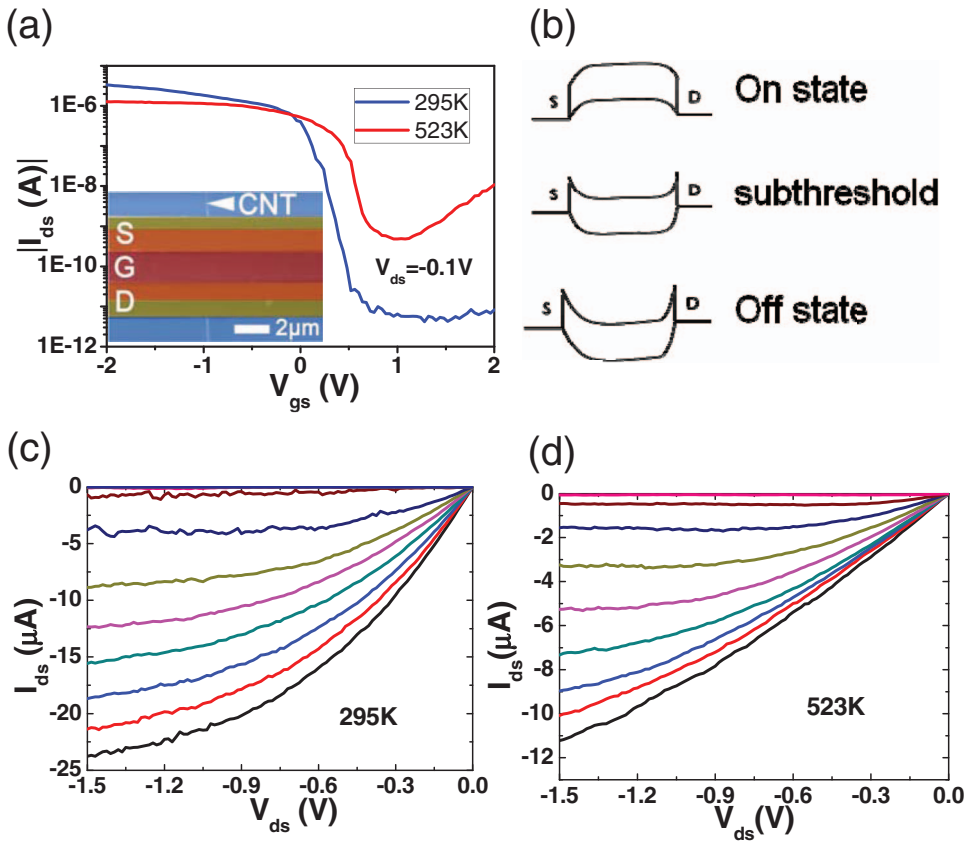

FIG. 7. Room temperature and high temperature performance of a typical CNT FET. (a) Transfer characteristics of a 2 μm CNT FET measured at room temperature (295 K) and 523 K. The inset is a top-view SEM image of this device. (b) Schematic energy band diagram for CNT FET at different states. Output characteristics of the CNT FET for V_{gs} varies from −2 V to 0.4 V with a step of 0.3 V from bottom to top at (c) room temperature and (d) 523 K. Reprinted with permission from T. Pei *et al.*, Adv. Func. Mater. **21**, 1843 (2011). Copyright 2011, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

results mainly from the increased phonon scattering at higher temperature.[30] On the other hand the off state current increases tremendously for more than three orders of magnitude since it is governed by thermal activation of the carriers across the potential barrier and is exponentially dependent on temperature (Fig. 7(b)).

For conventional MOS devices, the well-designed dopant distribution may be changed at high temperature, since the dopants may diffuse and redistribute resulting in permanent damage to the Si MOS circuits when operating at high-temperature.[28,29] However, this damage mechanism is absent in the CNT devices fabricated via doping-free process in which no dopant is intentionally introduced and the operation of the devices is not dependent on dopant concentration and distribution.

We now consider the very low temperature behavior of CNT FETs. Low temperature operation is considered as a promising way to improve the performance of silicon CMOS circuits. But there are some disadvantages associated with Si-based MOS devices when operating at temperature lower than liquid nitrogen due to dopant freeze-out and related degradation of ohmic contacts and kink effect.[27] On the other hand CNT FETs fabricated via doping-free process are free of these effects simply because the operation of the CNT FETs is not dependent on dopants.

The electronic properties of a typical top-gated CNT FET were measured at RT and liquid helium temperature (4.3 K) respectively and shown in Fig. 8. At 4.3 K, the device shows a much lower off-state current than that at RT and a much smaller subthreshold slope of 30 mV/dec than the corresponding values of 100 mV/dec at RT. Moreover, the on/off current ratio increases enormously from 10^5 at RT up to 10^9 at 4.3 K. Compared with corresponding Si MOS devices, CNT FETs have

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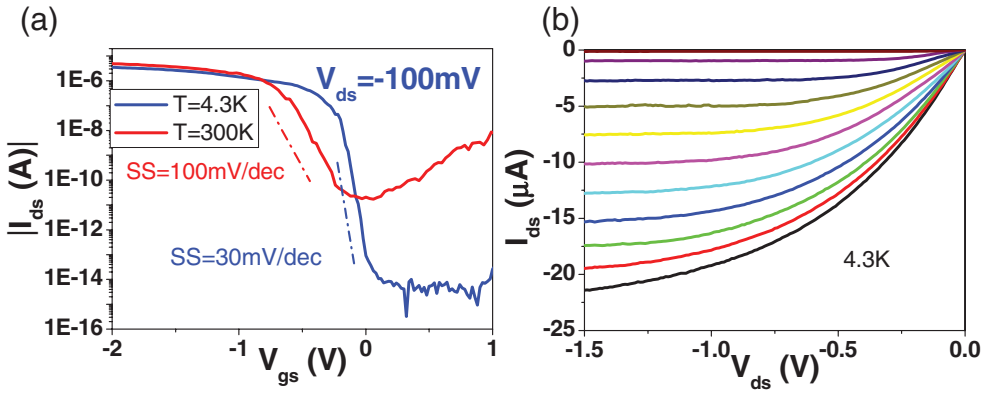

FIG. 8. Low temperature performance of a CNT FET. (a) Transfer characteristics of a 0.8 μm CNT FET measured at 300 K and 4.3 K. The on/off current ratio increases from 10^5 to 10^9, while the subthreshold swing decreases from 100 mV/dec to 30 mV/dec from RT to 4.3 K. (b) Output characteristics of the CNT FET measured at 4.3 K, with the gate voltage being varied from -2 V to 1 V with a step of 0.3 V from bottom to top. Reprinted with permission from T. Pei *et al.*, Adv. Func. Mater. **21**, 1843 (2011). Copyright 2011, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

the following advantages when working at very low temperature. First, the I-V characteristic at low bias (Fig. 8(b)) is linear and there are no oscillations due to Coulomb blockage occurring in the transfer curves (Fig. 8(a)), indicating a perfect ohmic contact between the CNT and source/drain contacts. It is also clear that there are no kink phenomena in the output characteristic even at 4.3 K, showing that the CNT FETs are free of the negative effect due to dopant freeze-out at low temperature. CNT FETs can therefore operate at very low temperature down to 4.3 K with improved performance and without being affected by the negative effects which are associated with dopants.

V. DOPING-FREE FABRICATION AND PERFORMANCE OF CNT BASED OPTOELECTRONIC DEVICES

We now consider the possible application of CNT in optoelectronics. Since semiconducting SWCNTs are one-dimensional and direct band gap materials with superb electric and optical properties, they are promising candidates for future integrated nano-electronic and optoelectronic devices.[31] Almost perfect films of vertically aligned semiconducting SWCNTs can be grown. These CNT films have an extremely low index of refraction and therefore ultralow reflectance yielding almost perfect absorption close to 100% of the incident visible light.[32] Semiconducting CNTs also have several unique features that are important for photovoltaic (PV) applications, these include extremely large room temperature mobility,[33,34] tunable diameter and thus band structure to match the solar spectrum,[5] and can be ohmic contacted for either barrier-free electron injection with Sc[21] or Y[22] or barrier-free hole injection with Pd.[23] The use of CNTs represents a typical approach to reduce both cost and size and to improve efficiency in PV applications.

A. CNT based p-n junction and diode characteristics

In a typical photodetector or PV device, a build-in field is essential for efficient separation of photon excited electron-hole pairs and for observing photovoltaic effects.[35] In CNT diodes, such a build-in field is usually provided by forming a p-n junction via either chemical doping[36] or electrostatic doping via split gates.[36–39] A Schottky barrier (SB) formed between a metal electrode, e.g. Ti, and a semiconducting SWCNT can also provide the required field for separating electrons and holes. But the formation of the SB reduces the maximum achievable photovoltage.[40] Here we consider a CNT diode[41] which is formed by contacting a semiconducting SWCNT asymmetrically with Pd on the one end and Sc or Y on the other end (Fig. 9(a)). Since neither SB nor sharp p-n junction exist in the diode, in principle a maximum photovoltage which is ultimately determined

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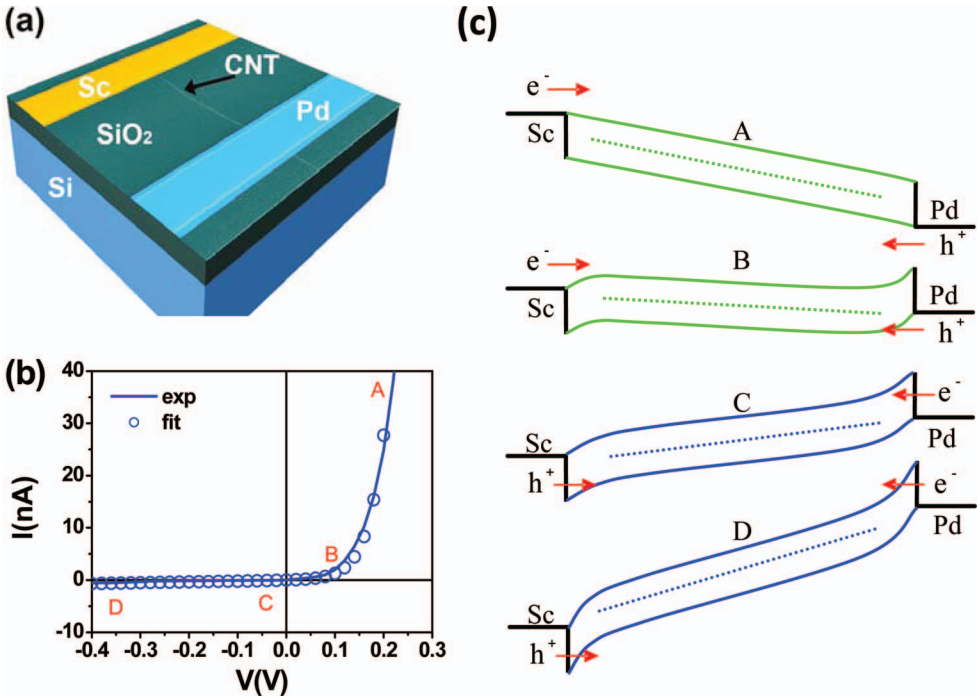

FIG. 9. Structure and I-V characteristic of a CNT diode. (a) Depicted structure and superimposed SEM image showing an asymmetrically contacted CNT diode. In the device, the diameter of the SWCNT channel is about 1.5 nm, which is laid on a 500nm SiO_2 and contacted by Sc and Pd electrodes. The inter electrodes distance is about 800nm. (b) Room-temperature I–V characteristic of the CNT device, showing a typical rectifying diode characteristic. (c) Energy band diagrams corresponding to the four points A, B, C, and D of (b), respectively.

by the band-gap of the CNT may be obtained for a given semiconducting SWCNT with this device geometry.

The asymmetrically contacted semiconducting SWCNT exhibits a typical diode rectifying I-V characteristic (Fig. 9(b)). When a large forward bias is applied (schematic A of Fig. 9(c)), both electrons and holes may be injected into the CNT channel without barrier, leading to a large current with contributions from both electrons and holes, i.e. the diode acts as a barrier-free bipolar diode (BFBD). At zero or small bias, e.g. as shown in schematic B of Fig. 9(c), the current is significantly reduced and limited by thermionic electrons and holes emission over a potential barrier of the order of the band gap of the CNT E_g. For small reverse bias (schematic C of Fig. 9(c)), the dark current is first dominated by thermionic current over the potential barrier $\sim E_g$ near Pd (Sc) contact for electrons (holes). At larger reverse bias, the barrier for the carrier injection is thinned and tunneling current starts to dominate (schematic D of Fig. 9(c)).

For a high quality diode, we may model the I-V characteristic of the diode in dark using the diode equation[35]

$$I_{dark} = I_s\{\exp[e(V - I_{dark}R_s)/nkT] - 1\}, \quad (1)$$

where V is the bias, I_s is the reverse saturation current, R_s is the effective series resistance, e is the electron charge, k is the Boltzmann constant, T is the temperature, and n denotes the ideality factor of the diode. The experimental data (blue curves in Fig. 9(b)) can be fitted perfectly well using equation (1), yielding $I_s = 20pA$, $n = 1.17$, and $R_s = 3.05 \times 10^5\Omega$.

B. CNT based photodetector

The asymmetrically contacted CNT diode discussed in the preceding section responses to infrared light and may thus been used as an infrared photodetector.[42] When the diode is illuminated

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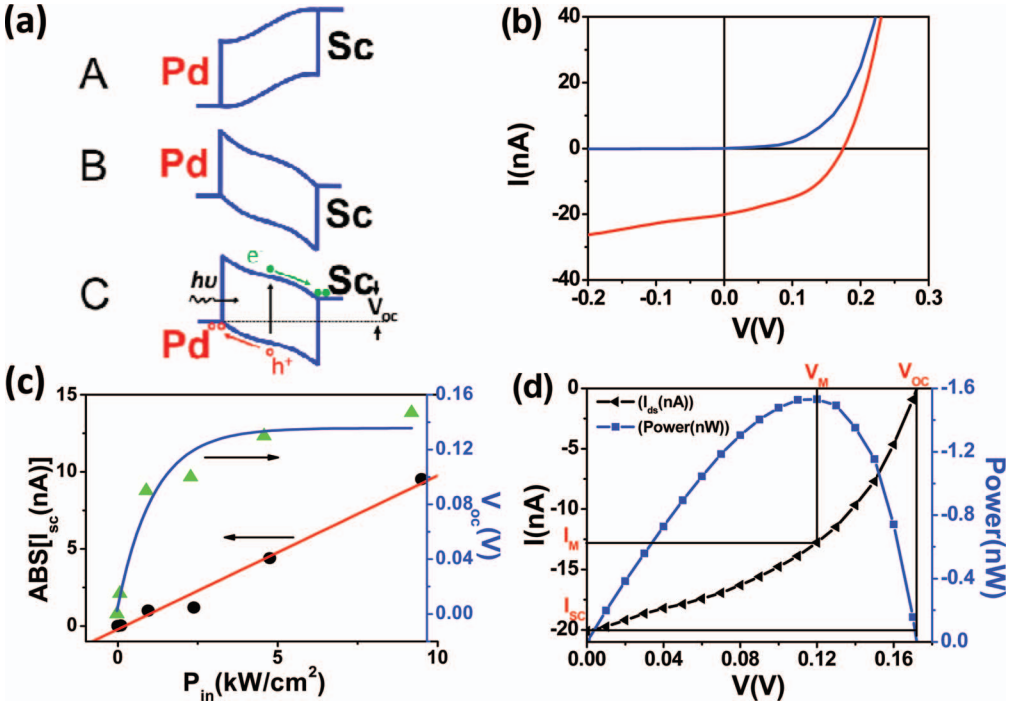

FIG. 10. (a) Schematic diagrams corresponding to large forward bias (panel A), zero or small bias (panel B) and under illumination (panel C). (b) Experimental and fitted (blue) dark I-V characteristic and that under illumination (red) measured from a device with a channel length of 1.0 μm and light intensity of 90 kW/cm^2. In (c) are V_{oc} (blue) and I_{sc} (black) as functions of incident light power, and in (d) I-V (black) and output power (blue) characteristics, illustrating the key parameters related to the performance of the device: $I_M = 12.8$ nA, $V_M = 0.11$ V, $V_{oc} = 0.17$ V, $I_{sc} = 19.8$ nA, and FF = 0.42.

by a laser beam with $\lambda = 785$ nm, light creates electron-hole pairs in the CNT which are then separated by the built-in electric field in the diode yielding a photovoltage V_{oc} (Fig. 10(a)) in an open circuit and photocurrent I_{sc} in a short circuit. Under low illumination condition, the total current in the channel is determined by the balance between the diffusion or dark current I_{dark} and the light generated current I_{sc}, and to a good approximation the total current is given by

$$I(V) = I_{dark} - I_{sc} = I_s\{\exp[e(V - I_{dark}R_s)/nkT] - 1\} - I_{sc}, \tag{2}$$

which to a rough approximation is an illumination dependent shift of the dark current as illustrated in Fig. 10(b) (red solid curve).

For low incident light intensity, the light generated current I_{sc} increases with increasing incident flux. If the incident flux b_0 is increased by a factor P_{in}, I_{sc} will increase by the same factor, i.e. $I_{sc}(P_{in}b_0) = P_{in}I_{sc}(b_0)$, and this is amply demonstrated in Fig. 10(c) (red curve). When the circuit is open, the total current is zero

$$I(V_{oc}) = 0 \approx I_s[\exp(eV_{oc}/nkT) - 1] - I_{sc}. \tag{3}$$

Using equation (3) we then have for the open circuit voltage

$$V_{oc}(P_{in}) = (nkT/e)\ln[P_{in}I_{sc}(b_0)/I_s + 1]. \tag{4}$$

At very low incident power, $V_{oc(P_{in})}$ increases rapidly with increasing P_{in}, but it saturates at a value about *0.15 V* (Fig. 10(c), blue curve) for large incident flux.

The key performance metric for a solar cell is the power conversion efficiency which is defined as

$$\eta = (I_M \cdot V_M)/P_{in} = (FF \cdot I_{sc} \cdot V_{oc})/P_{in}, \tag{5}$$

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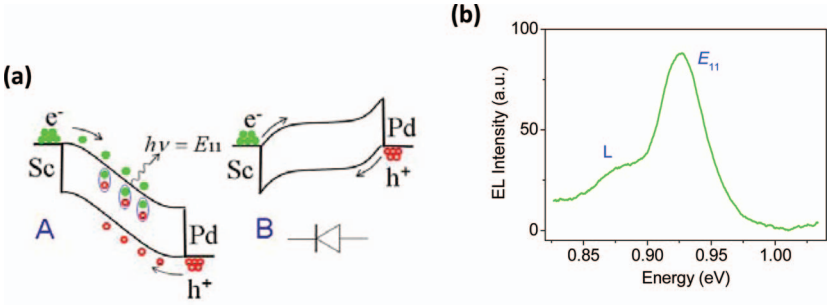

FIG. 11. Structure and characteristics of a CNT light emitting diode. (a) Scheme A, the diode is forward biased, Scheme B the diode is zero or slightly reversed biased. (b) Electroluminescence spectrum of the diode when operated at large forward bias with a large diode current I = 7.5 μA. Reprinted with permission from S. Wang *et al.*, Nano Lett. **11**, 23 (2011). Copyright 2011, American Chemical Society.

where I_M and V_M describe the bias point at which the power generation ($P = I_M \cdot V_M$) reaches a maximum, and FF is the fill factor. Using $I_{sc} = 19.8\ nA$, $V_{oc} = 0.17\ V$, $P_{in} = 90$ kW/cm^2, and FF = 0.42 (Fig. 10(d)), we obtain $\eta \sim 0.11\%$ for the device shown in Fig. 10(d) with a device channel length L $\approx 1.0\ \mu$m. While both the FF and the power conversion efficiency values look very low when compared with that of a Si-based solar cell,[35] they are of the same order of magnitude as that obtained from an almost perfect CNT diode[43] fabricated via electrostatic doping on a suspended CNT, but the latter has a smaller I_{sc}. The low value of η achieved for CNT is largely due to the fact that the diameter of the CNT and thus the absorption cross-section is extremely small for a single CNT based diode, and the small value of FF is largely due to the large series resistance which is ultimately limited by the quantum contact resistance R_0. Both η and FF may in principle be increased by connecting more semiconducting SWCNTs in parallel in a CNT based PV module.

C. CNT based light emitting diode

High efficient light emitting diode (LED) has been one of the top priority targets for the development of carbon based optoelectronics. While extensive investigations have been carried out on CNT based diodes,[36,37] only few investigations on the characteristics of CNT based LED have been reported.[38–40] The most successful CNT based light emitters are those FET based emitters.[44,45] A CNT FET can be either ambipolar type, where at large bias and under suitable gate voltage, electrons and holes can be injected simultaneously into the CNT channel and recombine to yield electroluminescence (EL),[44] or the FET can be unipolar where only one type of carriers (e.g. holes for a p-type FET) are injected into the CNT.[45] At large bias strong electric field may be generated around local defects to induce impact excitations or ionizations, generating electron-hole pairs and subsequently giving rise to EL.[45] However, these devices rely on the use of large bias and at least three independent electrodes to bias the diode, to generate electron rich (n-) and/or hole rich (p-) regions, and this increases the complexity in the design and fabrication of integrated nanoelectronic and optoelectronic circuits.

High performance CNT based LED may also be constructed based on the diode structure discussed in the preceding sessions.[46] As shown in Fig. 11(a), at large bias electrons are injected without barrier from Sc contact into the conduction band and holes are injected into the valence band from Pd electrode. When these injected electrons radiatively combine with injected holes in the CNT channel, photons are emitted. The emitted photon energy distribution or EL spectrum (Fig. 11(b)) shows a clear emission peak at 0.925 eV which may well be fitted using a Gaussian to yield a peak with a full-width at half maximum (FWHM) of about 40 meV.

The integrated EL intensity shows an excellent linear relationship with current (Fig. 12(a)). The device exhibits a current threshold at about 5μA for obvious light emission, and this large current threshold signifies the difficulty in fabricating CNT based LEDs. This is because an efficient CNT LED requires roughly an equal amount of electrons and holes being injected into the CNT channel, and at the same time few defects are present in the channel where non-radiative recombination of

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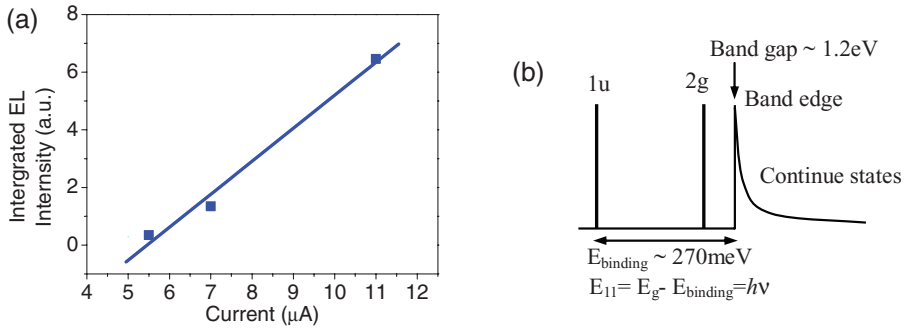

FIG. 12. (a) Integrated infrared emission intensity as a function of current. (b) Schematic representation of electronic states associated with a (12,4) semiconducting SWCNT with d = 1.14 nm. The states below the band edge are bound excitonic states. Reprinted with permission from S. Wang *et al.*, Nano Lett. **11**, 23 (2011). Copyright 2011, American Chemical Society.

the injected electrons and holes occur. Conventional strategy for fabricating a LED is to form a p-n junction via chemical doping. But this procedure introduces additional non-radiative sites in the channel and is therefore highly undesirable since these sites will further reduce the very limited radiative recombination rate in a SWCNT (less than 10^{-4}/per electron-hole pair). On the other hand, any symmetrically contacted CNT device will inevitably introduce a significant Schottky barrier either for electrons (in the case of p-contact, e.g. Pd) or holes (in the case of n-contact, e.g. Sc or Y) injection from the contacts, and the best choice that one can make is to use a contact, e.g. Ti,[44] that forms Schottky barrier with both the conduction and valence bands of the CNT with equal height (~E_g/2), making it highly unlikely to allow for a current that is substantially higher than the threshold current at low or moderately large bias. A large gate voltage may be utilized to reduce the thickness of the Schottky barrier, and thus to increase the current and improve the radiative intensity of the device.[44]

The relationship between exciton states energies and band gap energy (E_g) of the CNT used in Fig. 11 is depicted Fig. 12(b). The observed emission peak of Fig. 12(b) at 0.925eV may be identified as that resulting from the excitonic E_{1u} state of a (12, 4) SWCNT with a diameter of 1.14 nm,[47] and the peak energy corresponds to $E_{11}=E_g-E_{binding}$, with $E_{binding}$ being the exciton binding energy. Earlier photoluminescence (PL) and optical resonance experiments shown that for a CNT with d ~ 1.14 nm and E_{1u} ~ 0.925 eV, the CNT can be assigned an index (12, 4) and a binding energy ~270 meV.[47] Figure 12(b) shows clearly that the E_{11} emission peak is of a FWHM of about 40 meV, and this corresponds to the energy state E_{1u} that is located below the band edge with a FWHM which is much less than that of the excitonic binding energy ~ 270 meV. The emission peak observed here at E_{11} = 0.925 eV agrees very well with that observed in PL experiment ~ 0.925 eV.[47] The weaker EL peak (marked as L in Fig. 12(b)) is very similar to that observed by Mueller *et al.*,[39] and may be attributed to have resulted from weakly localized excitons which might be associated with defects of CNT or trapping charges near dielectric surfaces.

VI. DISCUSSIONS AND CONCLUSIONS

Since the CNT was first experimentally verified by Iijima[48] and first CNT-based FET was developed in 1998,[49] significant progress has been made in improving the performance and exploring potential applications of CNT-based devices. While it is now well established that semiconducting SWCNTs based FETs outperform that based on Si with the same channel length in several most important device metrics, including the gate delay (a measure of the potential switching speed)[9,10] and energy-delay product (a measure of the energy to perform a function), the full advantages in the circuit level[11] remain to be explored and demand more detailed investigations.

While doping plays a crucial role in determining the electronic properties and device polarity in Si-based CMOS processes, for short-channel CNT devices the polarity of the devices can be controlled by choosing suitable contact materials.[21,23] In particular, it is found that Sc and Y can

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provide barrier-free injection of electrons into the conduction band of a semiconducting CNT,[21,22] while Pd can provide barrier-free injection of holes into the valence band of the CNT[23] with moderate diameter between 1.5–3.0 nm. This doping-free approach not only reduces the fabrication steps and thus cost significantly, but also offers huge advantages in the performance of so fabricated nanoscale devices. This doping-free approach eliminates all failure mechanisms and inhomogeneity associated with the presence of dopants in the devices, in particular noise due to the fluctuations in dopant distribution, carrier frozen out at low temperature and device degradation due to dopants diffusion at high temperature. The use of CNT as the channel material and doping-free fabrication process thus allows the working temperature of CNT based devices be extended down to extremely low temperature of at least 4.3K with improved performance and high temperature of up to 300C with accepted on/off current ratio.[25] While this remarkable temperature performance largely extends the areas of applications of CNT based nanoelectronic devices, it also suggests the feasibility of three-dimensional (3D) integration of CNT-based devices where temperature is the key issue. These features form a solid foundation for potential large scale integration of CNT-based nanoscale devices and applications of these devices in low- and high-temperature electronics.

The symmetric band structure of CNT near the Fermi level also suggests promising optoelectronic applications of CNT based devices. While symmetric n- (Sc or Y) and p-type (Pd) contacts may be used for building high performance CNT FETs, asymmetric contact pair, e.g. Sc and Pd, may be utilized to establish build-in field similar to that present in a conventional p-n junction and to construct CNT diode with a near to perfect ideality factor.[41] Both LED[46] and photodetector[42] have been built based on this doping-free approach, which provides a perfect platform for directly integrating nanoelectronic and optoelectronic devices, via simply putting symmetric and asymmetric n- and p-contact pairs on top of CNTs.

Unlike other semiconducting nanostructures, e.g. semiconducting nanowires, a good quality SWCNT has a perfect structure without any intrinsic dangling bonds, and therefore does not interact strongly with normal substrates or mechanical support. CNTs may therefore be grown on and transferred between any substrates or mechanical support with designed properties, thus allowing flexible electronic devices be made on flexible substrate but with much better performance than that based on organic molecules[50] and be integrated into complex system with both low- and high-κ materials, which is idea for 3D architecture. Another very important property of CNT which distinguishes nanostructured sp^2 carbon from all other nanostructures is its large mean free path. With carefully prepared CNT devices, the room temperature mean free path may exceeds tens microns which may well cover a circuit of moderate complexity. CNTs thus provide potential building blocks for constructing room temperature quantum devices and even for quantum circuits at moderately low temperature where all component devices are well within the coherence width of the electron wave.

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