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Threshold voltage control of Pt-Ti-O gate Si-metal-insulator semiconductor field-effect transistors hydrogen gas sensors by using oxygen invasion into Ti layers

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Although the threshold voltages (Vth) of the as-processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs under same channel ion dose conditions show a large variation such as 0.846 V among several wafers, the air-annealing and succeeding hydrogen post-annealing procedure for the FETs hydrogen gas sensors leads to excellent uniform Vth distributions and large sensing amplitude ΔVg. The oxygen invasion process through Pt grain boundaries to amorphous Ti layers at 400 °C air-annealing for two hours is not a simple dopant diffusion process but super-heavily oxygen-doped process partly to grow nano-crystalline TiOx. The oxygen-invaded Ti layers change to a kind of new materials; novel mixing layers of nano-crystalline TiOx and super-heavily oxygen-doped amorphous Ti formed on SiO_2/Si substrates. The Ti mixing layers change from metals to semiconductors or insulators. As the Ti layers are so thin like 5 nm, the total amount of oxygen invaded into Ti layers will be saturated and stabilized. From the device operation point of view, it is crucial to control the Vth precisely that the Ti novel mixing layers are thin and fully depleted. This is supported by the fact that the Vth change before and after air-annealing procedures can be well explained by the difference of vacuum work function between Pt and Ti. © *2011 American Institute of Physics*. [doi:10.1063/1.3645028]

I. INTRODUCTION

Recently much attention has been paid to hydrogen gas sensors because renewable energy systems, such as solar or hydrogen energy, require reliable hydrogen safety monitoring sensor systems that can withstand harsh open-air environments. As one of the possible candidates for such applications, we have proposed a novel platinum-titanium-oxygen (Pt-Ti-O)-gate Si-metal-insulator semiconductor field-effect transistors (MISFETs) hydrogen gas sensor.[1–3] The Pt-Ti-O gate Si-MISFETs hydrogen gas sensors are typically fabricated by annealing Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs in air at 400 °C for two hours. Our sensors consist of unique gate structures composed of Ti and oxygen accumulated regions around Pt grains on top of a novel mixing layer of nanocrystalline TiOx and superheavily oxygen-doped amorphous Ti formed on SiO_2/Si substrates. The Pt-Ti-O gate Si-MISFETs hydrogen gas sensors after hydrogen annealing procedure show excellent sensor characteristics, in which the sensing amplitude ΔVg, defined by the magnitude of threshold voltage Vth shifts under the hydrogen exposure, can be well fitted by a linear function of the logarithm of hydrogen concentration C(ppm) between 100 ppm and 1% of air-diluted H_2 concentrations,

$$\Delta Vg(V) = 0.355 \mathrm{Log}\, C(\mathrm{ppm}) - 0.610, \qquad (1)$$

where Log C(ppm) denotes the common logarithm of C(ppm).[2] As the standard definition of the sensitivity derived from the derivative of ΔVg (V) versus C(ppm) leads to concentration dependent sensitivity, we have introduced alterative constant sensitivity per decade. In our papers, the gradient 0.355 V represents the sensitivity of the fabricated FET sensors, which is about ten-times larger than the value of 355 mV/decade at 115 °C compared with hitherto developed Pt-gate Si-MOSFETs hydrogen gas sensors or the expected value of 38.5 mV/decade from Nernst equation.[4] The sensing range seems to be suitable for most hydrogen safety monitoring sensor systems. Furthermore the long intrinsic lifetime more than 10 years has been reported from preliminary accelerated temperature and/or humidity aging tests about the Pt-Ti-O gate Si-MISFETs hydrogen gas sensor chips.[3,5] The Pt-Ti-O gate structures are determined with the help of transmission electron microscope (TEM), X-ray diffraction, Auger analysis, and TEM energy dispersive X-ray spectroscopy (EDX) analysis before and after air annealing.[1–3]

One of the most novel features about device operations of Pt-Ti-O gate Si-MISFETs hydrogen gas sensors is a way of controlling the threshold voltage Vth by using oxygen invasion into titanium layers from open air through thin platinum layers. It shows us a serious question about the controllability of Vth because precise control of Vth of Si-MOSFETs will be impossible even if by using the most prevailed dopant diffusion process by gaseous sources such as AsH_3 instead of ion implantation[6] and/or the annealing temperature of 400 °C is too low as the oxidation temperature of Ti layers. In fact, some of the preliminary experimental results showed that threshold voltages of as processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs were scattered among wafers under the same dose conditions of ion implantation. Sensing amplitudes were scattered so much over the wafers including the samples without any hydrogen responses.[2,7]

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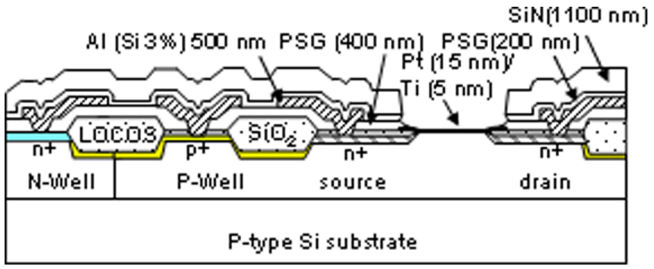

FIG. 1. (Color online) A schematic cross-section diagrams of fabricated sensor FETs.

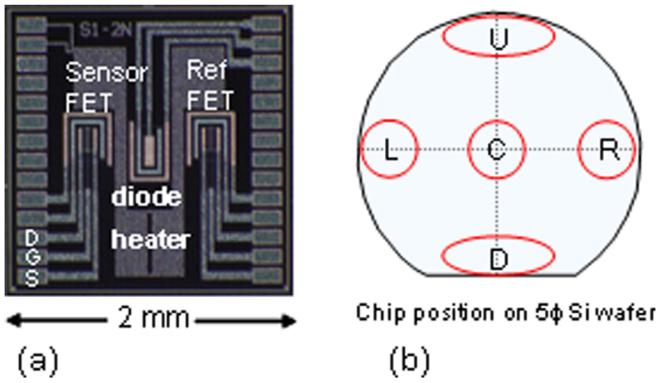

FIG. 2. (Color online) (a) A photograph of fabricated sensor chip and (b) five representative chip positions (U,C,D,L,R) in 5-ϕ wafer for device characterization.

In this study, we would like to investigate the control mechanism of Vth for the developed Pt-Ti-O gate Si-MISFETs hydrogen gas sensors and clarify how the oxygen invasion into the Ti layer through Pt grain boundaries affect device characteristics.

II. EXPERIMENTAL

A. Fabrication process

As the fabrication process for sensor chips was already reported in detail,[2] concise explanation is given with the help of a schematic cross-section diagram in Fig. 1. One of the fabricated sensor chips is shown in Fig. 2(a) as a photograph. The size of the sensor chips is 2×2 mm^2. The representative measured five chip positions (U, C, D, L, R) on the 5-inch Si wafer are shown in Fig. 2(b). The sensor chips are composed of a sensor FET, a reference FET, a PN junction diode as a thermometer, and an Al wiring heater. The sensor chips were fabricated using 0.8-μm CMOS-compatible 5-inch lines in which Pt/Ti-gate metal fabrication was enabled. The silicon substrate was a p-type boron-doped 10.5 Ωcm resistivity with (100) orientation inclined at off angle of 4 degrees toward [010] direction. The gate oxide SiO_2 was 18 nm thick and formed using the wet oxidation process. The Pt/Ti-gate metal layers were deposited using the electron beam (EB) evaporation method. The gate areas were patterned using the lift-off technique. We have prepared various Pt/Ti-gate Si-MOSFETs with different thicknesses of Pt layer and Ti layer. All the sensor wafers evaluated in this study are listed in Table I. The standard thickness of gate metals for Pt and Ti are 15 and 5 nm, respectively, which denote Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs, and the gate length Lg and width Wg are 20 and 300 μm, respectively, unless otherwise specified. Hereafter, we denote the Pt(15 nm)/Ti(5 nm) pair as (15/5) depending on the thickness of the Pt and Ti gate metals.

We have fabricated two types of sensor chips in the same Si wafers with different polarity of FETs and PN junction diodes. The conditions of channel ion implantations to determine Vth for n-type FETs and p-well, and also for p-type FETs and n-well are summarized in Table II. Three different channel doses for both type FETs are classified by (A) for #2, (C) for #8, and (B) for all other wafers. The standard FET is n-channel, unless otherwise specified.

The Si wafers were set in the chamber of thermal chemical vapor deposition (CVD) apparatus maintained at 390 °C in open air for a couple of minutes before starting the P-doped silicon glass (PSG) depositions.[1,2] By using plasma CVD, 1-μm-thick silicon nitride (SiN) film was deposited on top of 200-nm P-doped PSG film/400-nm P-free PSG film grown by thermal CVD at 390 °C on the Pt/Ti gate films as protection films. As a final step in device fabrication, the SiN/PSG layers were removed from the sensing gate area of the sensor FETs, but remained on the gate area of the reference FETs so as not to show hydrogen gas response. The sensor chips obtained after the dicing process are called "as-processed chips" in this paper.

B. Measurement conditions

The sensor chip was mounted on a ceramic substrate with high thermal conductivity. A capsule was attached to the ceramic substrate with inlet and outlet nozzles, which were fixed at a 45-degree angle to the substrate normal. The free volume of this capsule was about 3 mL, and the measuring unit was fixed on a heater substrate for monitoring the temperature using an infrared thermometer. Operation chip temperature T was 115 °C.[5]

We used pure air gas (G3 grade) and hydrogen gas of a predetermined concentration diluted with pure air gas. The change valve enabled the immediately switching of pure air gas to hydrogen gas and vice versa. The standard experimental procedure is as follows. The pure air gas continuously flows for two minutes to stabilize the FET sensor. Then the gas flow changes to hydrogen gas for a predetermined time

TABLE I. List of fabricated Pt/Ti-gate metals.

Lot No	H18-1	H18-2					H19				
Wafer No	#2,3,4,5,8,23,24	#11,13	#15	#18	#19	#22	#A2, A3	#B1	#C1	#D1	#E1
Pt (nm)	15	15	30	45	90	90	15	15	30	45	90
Ti (nm)	5	5	10	15	15	45	5	3	5	5	5

TABLE II. List of ion dose conditions.

Dose conditions	(A)	(B)	(C)	Implantation Energy
Chip no.	#2, #3	Others	#8	
n-type FET (cm^{-2})	0.8×10^{12}	1.0×10^{12}	1.2×10^{12}	P^+ 80 keV
p-well (cm^{-2})		7.6×10^{12}		BF_2^+ 60 keV
p-type FET (cm^{-2})	3.2×10^{12}	4.0×10^{12}	4.8×10^{12}	BF_2^+ 80 keV
n-well (cm^{-2})		1.15×10^{13}		P^+ 125 keV
Si substrate (cm^{-3})		8.0×10^{14} (p-type)		

and finally changes to pure air gas. The flow rate of the hydrogen gas and air gas is 0.5 L/min. The standard H_2 concentration is 1 000 ppm for device characterizations. To reduce power consumption, we selected enhancement-type FETs so that most of the operation range of the gate voltage Vg covers the saturated regions of the pentode I-V characteristics for the fabricated Si-MOSFETs at Vds = 1.5 V, where the source-drain currents are nearly independent of the source-drain voltage at around 1.5 V. We have used the tentative Vth defined by the gate voltage Vg for Ids = 10 μA at a source-drain voltage Vds = 1.5 V with short-circuiting source and p-well for n-type FETs. These measuring conditions are applied to evaluate ΔVg, unless otherwise specified.

III. DEVICE CHARACTERISTICS

A. Pt-Ti-O gate Si-MISFETs hydrogen gas sensors

In our previous papers,[1,2] we reported a significant increase in ΔVg by annealing sensor chips composed of Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs in air at 400 °C for two hours. In this section we have investigated optimum air-annealing conditions for Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs by changing annealing temperature and time. The experimental results in the Appendix show that the previous air-annealing conditions at 400 °C and two hours were nearly optimum to realize Pt-Ti-O gate Si-MISFETs hydrogen gas sensors.[2] Therefore, we have fixed tentatively the standard annealing temperature and time to 400 °C and two hours with little bit larger margins. Hereafter, this procedure is referred to as "air annealing".

Although the ΔVg of #2U, #3U, #8U, #23U, and #24U chips show extremely high values between 0.821 ~ 0.958 V after air annealing, there remains rather high residual sensing amplitudes ΔVgres (as annealed) to show slow damping tails in common.[1,2] As was discussed in our previous paper,[2] we found a stable response with reduced ΔVgres, 0.05 V, after 10 min of air-diluted 1000-ppm hydrogen exposure at 115 °C for the air- annealed samples. Hereafter, this procedure was referred to as "hydrogen post-annealing". The hydrogen post-annealing procedure decreases Vth by nearly the same value of ΔVgres (as annealed) in terms of terminating the deep traps generated around the gate insulator surface during air annealing. As a typical example, the response curves of ΔVg for #24 C before and after air annealing, and also after hydrogen post-annealing, are shown in Fig. 3. The sensing amplitudes of ΔVg for the hydrogen post-annealed Pt-Ti-O gate Si-MISFETs hydrogen gas sensors are well described by Eq. (1).

B. Oxygen invasion process for Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs

Our main concerns are to clarify the correlation among oxygen invasion process, Vth changes and sensor characteristics. In our tuning of Vth, phosphorus ions are implanted into the p-well. By considering channel ion implantation using P^+ with an implantation energy of 80 keV depending on the wafer for three different doses of Table II: (A) $0.8 \times 10^{12}\,cm^{-2}$, (B) $1.0 \times 10^{12}\,cm^{-2}$, and (C) $1.2 \times 10^{12}\,cm^{-2}$ for n-type FETs, the difference between adjacent two doses, N_{DS}, is $2.0 \times 10^{11}\,cm^{-2}$. In our doping conditions of the channel and the p-well, the depletion layer of the PN junction extends to the gate oxide SiO_2/Si interface, and the corresponding Vth shift, ΔVth, between adjacent two doses is given by the following equation,[8]

$$\Delta Vth = qN_{DS}/C_{OX}, \tag{2}$$

where q is the unit charge and C_{OX} is the gate capacitance per unit area. By using the relative dielectric constant and the thickness of gate silicon dioxide SiO_2 as 3.9 and 18 nm, Equation (2) leads to ΔVth = 0.167 V.

Figures 4(a) and 4(b) show the accumulated data of wafer distributions of Vth and ΔVg for several as processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs sensor chips, as processed Pt(90 nm)/Ti(5 nm)-gate #E-1 chips, and hydrogen post-annealed #A-2 chips after air-annealing at 400 °C for 8 h in Table I. The sensor chips are classified by three different doses of Table II. The sample #4 ref denotes the

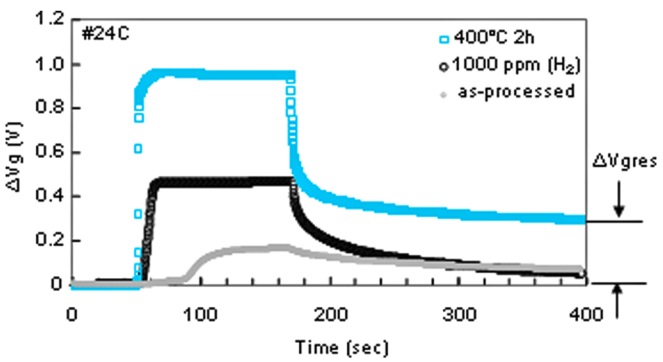

FIG. 3. (Color online) Response curves of ΔVg for #24 C sensor FETs: as-processed chip, air-annealed chip after 400 °C 2-h annealing in air, and hydrogen post-annealing chip (exposed to 10 min of air-diluted 1000-ppm H_2 at 115 °C after 400 °C 2-h annealing in air).

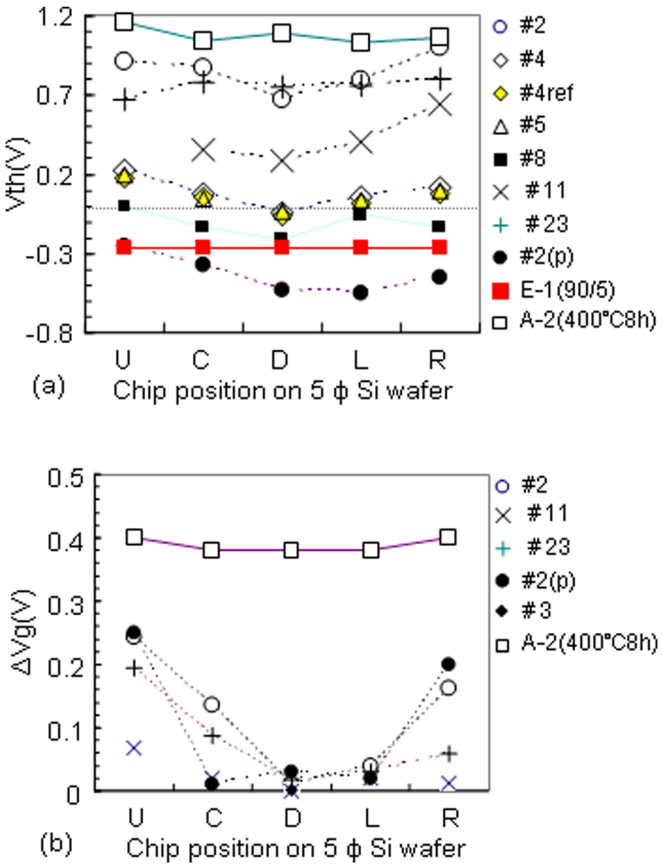

FIG. 4. (Color online) Accumulated device characteristics of as-processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs with different three doses of Table II, as-processed Pt(90 nm)/Ti(5 nm)-gate Si-MOSFETs, hydrogen post-annealed #A-2 chips after air-annealing at 400 °C for 8 h, denoted by A-2 (400 °C 8 h): (a) Threshold voltage Vth and (b) hydrogen sensing amplitude ΔVg.

reference FET in the #4 sensor chips. All of the Vth distributions for the as processed FETs except #E-1(90/5) show nearly the same shape in common. The accumulated data about Vth are in regular order in accordance with three doses. The variations of Vth for n-type FETs with the same (B) dose of $1.0 \times 10^{12}\,\mathrm{cm}^{-2}$ show a large value about 0.846 V from −0.04 V to 0.806 V among 4 wafers. It is direct evidence that there are large variations of the total dose of initial unintentional oxygen invasion into the Ti layer at the beginning of the PSG deposition.[1,2,7] The distributions of Vth for both sensor and reference FETs about as-processed #4 chips show nearly the same, where the Vth of sensor FETs shows a slightly larger value of about 25 mV in common comparing with that of the reference FETs in the same sensor chips. It means that the work functions of gates are nearly the same at least over the local areas of 1 mm × 1 mm on the Si wafers because the relative distance of both FETs is 1 mm as shown in Fig. 2(a).

On the other hand, the distribution of Vth for p-type FETs, #2(p), shows similar distribution in shape for n-type FETs. If the channel doses of P^+ for n-type FETs and $BF_2{}^+$ for p-type FETs are assumed to be uniform over the Si wafers, and the work functions of gates are nearly the same for two FETs, the difference of Vth between n-type FETs and p-type FETs will approximately be written by

$$\mathrm{Vth(n)} - \mathrm{Vt(p)} \approx \mathrm{Eg(Si)}, \tag{3}$$

where Vth(n) and Vth(p) denote the Vth for n-type FETs and p-type FETs, and Eg(Si) is the Si bandgap at the operation temperature.[9] The average Vth(n)–Vt(p) in the same chip position for #2 samples is 1.281 V with standard deviations of 0.116 V as shown in Fig. 4(a). As the relative distance of gate regions between #2 and #2(p) in the same chip positions is about 2.24 mm, over which areas the same work function cannot be assured, the average value of 1.281 V seems to be a close value, 1.10 eV of Eg (Si) at 115 °C.[9] These agreements between experiments and theories also support the oxygen invasion models of the as processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs.

The wafer distributions of ΔVg show strong correlation with that of Vth as shown in Figs. 4(a) and 4(b). The higher Vth has a tendency to show the larger ΔVg in general. It is not clear why most of the sensor chips such as #8 showed no responses over the wafer and a few sensor chips such as #2 showed weak hydrogen-responses with characteristic distributions linked to Vth distributions.[2] We have analyzed these points in Sec. III C.

The average Vth of the Pt-Ti-O gate Si-MISFETs denoted by "□ A-2(400 °C 8 h)" was 1.076 V with σVth of 52.2 mV. The Pt (90 nm)/Ti(5 nm)-gate Si-MOSFETs denoted by #E-1(90/5) showed an extremely high uniformity of Vth, −0.26 V, where σVth showed a small value of 4.5 mV. It means that the thicker Pt layers protect the Ti layer from oxygen invasion from open air. If we assume the proper Vth of Ti-gate Si-MOSFETs is realized by the sample #E-1(90/5), the Vth for the Ti-gate Si-MOSFETs denoted by Vth(Ti), is −0.26 V. It means that the proper Vth shift from Pt/Ti-gate MOSFETs without oxygen invasion to the Pt-Ti-O-gate Si-MISFETs should be estimated by the difference between the average Vth, 1.076 V, of the Pt-Ti-O gate Si-MISFETs and the Vth(Ti), −0.26 V, of the Pt(90 nm)/Ti(5 nm)-gate FETs. The resultant Vth shift is estimated to be 1.336 V, which is very close to the difference, 1.32 eV, of vacuum work function between 5.65 eV of Pt and 4.33 eV of Ti. [10] The flat distribution of Vth for the as processed Pt(90 nm)/Ti(5 nm)-gate Si-MOSFETs also means that EB evaporation of Pt/Ti does not cause the interface damages of the gate oxide SiO_2 and Si substrates.

On the other hand, it is difficult to determine the Vth without influences of oxygen invasions from the analysis of as processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs sensor chips in Fig. 4(a) because Pt thickness is so thin to protect oxygen invasions. In order to investigate the influence of Pt/Ti layer thicknesses and/or the oxygen invasion to device characteristics, we have prepared several sets of Pt/Ti pairs with different thicknesses of Pt and Ti films including the Pt (15 nm)/Ti(5 nm) pair for the gate metals of Si-MOSFETs, as listed in Table I. The Pt/Ti film deposition conditions were not altered, except deposition times. When the Pt and Ti thicknesses were changed from 15 to 90 nm and from 3 to 45 nm, respectively, we have applied the standard air-annealing at 400 °C for two hours to these sensor chips. The difference of Vth, ΔVth(s-r), between the sensor and

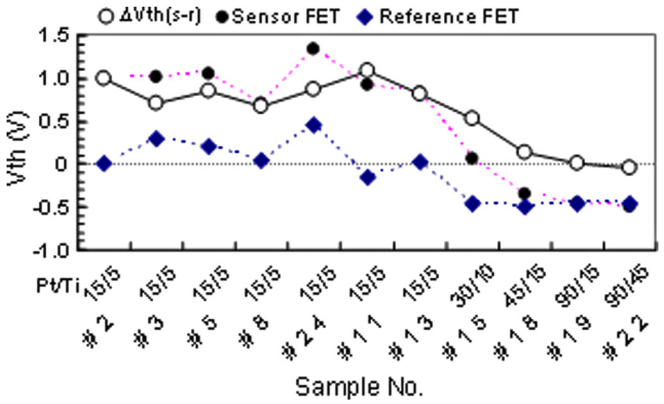

FIG. 5. (Color online) Comparison of Vth between sensor and reference FETs with various Pt/Ti thicknesses that are annealed in air at 400 °C for two hours. The ΔVth(s-r) (○) represents the Vth difference between sensor and reference FETs.

reference FETs in the same sensor chip position U for various Pt/Ti-gate Si-MOSFETs (Table I) after air annealing at 400 °C for two hours is summarized in Fig. 5, where the threshold voltages of sensor and reference FETs are also shown. The gate was 10 μm long and 150 μm wide for all the FETs of #11, #13, #15, #18, #19, and #22. The other sensor chips have the standard dimensions of $Lg = 20\,\mu m$ and $Wg = 300\,\mu m$. The positively correlated spreads of Vth between the sensor and reference FETs on the same sensor chips for the Pt(15 nm)/Ti(5 nm)-gate chips of #2, #3, #5, #8, #24, #11, and #13 with different channel ion doses indicate that the initial unintentional oxygen invasion to both sensor and reference FETs will be the same even if considering wafer to wafer or location to location spreads of the amount of oxygen invasion into the Ti-layers. It also means that the variations of ΔVth(s-r) will be expected to be small irrespective of channel ion doses or the large variations of initial unintentional oxygen invasion. The average ΔVth(s-r) for the Pt(15 nm)/Ti(5 nm)-gate chips of #2, #3, #5, #8, #24, #11, and #13 was 0.8579 V with $\sigma\Delta$Vth of 148.5 mV. Furthermore, ΔVth(s-r) decreased to about 0 V by increasing the Pt thickness from 30 to 90 nm. This behavior of ΔVth(s-r) means that the thicker Pt layers prevent oxygen invasion into the Ti layers from open air during the course of air-annealing process. In this case the Vth of both sensor and reference FETs will be determined by the work function of Ti instead of Pt due to the less influenced Ti contacts to the gate insulator of SiO_2. The average Vth of reference FETs for #15, #18, #19, and #22 was −0.47 V with $\sigma\Delta$Vth of 20.0 mV. It means that the proper Vth shift from the Pt(15 nm)/Ti(5 nm)-gate sensor FETs without oxygen invasion to the Pt-Ti-O-gate Si-MISFETs should be estimated by the difference between the above average ΔVth(s-r) of 0.8579 V and the average Vth, −0.47 V, of reference FETs for #15,#18,#19, and #22. The resultant Vth shift is estimated to be 1.3279 V, which is very close to the difference, 1.32 eV, of vacuum work function between 5.65 eV of Pt and 4.33 eV of Ti.[10]

The above two approaches from Fig. 4(a) and Fig. 5 indicate that the Vth change before and after annealing procedures can be well explained by a simple device model based on the difference of work functions of gate metals between 5.65 eV of Pt and 4.33 eV of Ti.

The above threshold voltages for Ti-gate Si-MOSFETs denoted by Vth(Ti) show two different values of −0.26 V by the sample #E-1(90/5) and −0.47 V by the reference FETs for #15,#18,#19, and #22. The difference of Vth(Ti), 0.21 V, will probably be derived from the reproducibility channel ion doses among different lots of #H18 and #H19 in Table I.

C. Control mechanism of Vth for Pt-Ti-O gate Si-MISFETs

The strong correlation between Vth and ΔVg in Fig. 4 suggests phenomenologically that the higher Vth has a tendency to show the larger ΔVg under the same channel ion dose conditions. The spacing of the I-V curves between #5U and #8U, 0.181 V, is close to the theoretical spacing of 0.167 V expected from Eq. (2). However, the spacing of the I-V curves between #2U and #5U, 0.740 V, is far from the theoretical spacing of 0.167 V. Two samples of #5U and #8U show no hydrogen response and the sample #2U shows hydrogen response as shown in Fig. 4(a). These results suggest the theoretical spacing of 0.167 V should be realized without any oxygen invasion into the Ti layer until near the gate oxide SiO_2.

All data of threshold voltages for the n-type as-processed FETs except #4ref and #E-1 in Fig. 4(a) are tuned to the Vth for (B) dose of $1.0 \times 10^{12}\,cm^{-2}$, that is, the Vth is replaced by Vth-0.167 V for (A) dose of $0.8 \times 10^{12}\,cm^{-2}$ and replaced by Vth + 0.167 V for (C) dose of $1.2 \times 10^{12}\,cm^{-2}$. These threshold voltages are denoted by Vtheff.

All data of ΔVg for the as processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs except #4ref in Fig. 4(b) are plotted by black circles (●) in Fig. 6. The data of ΔVg for the Pt-Ti-O-gate Si-MISFETs sensor chips are plotted by circles (○) in Fig. 6, which are derived from # A-2 (400 °C 8 h) in Fig. 4(b), and also derived from the sensor chips of #2, #3, #8, #23, and #24 chips; the basic sensing characteristics of Eq. (1) are obtained by these five sensor FETs with

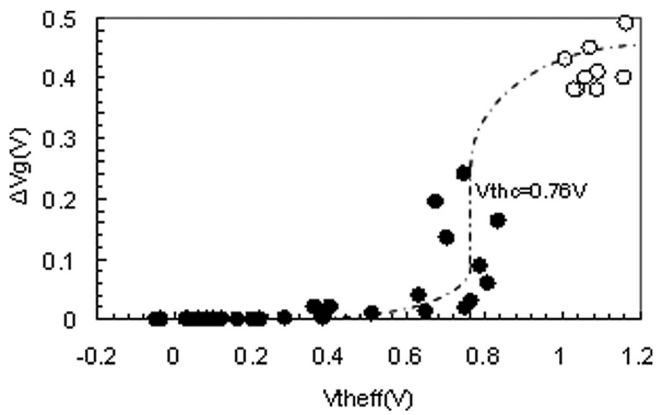

FIG. 6. The sensing amplitude of ΔVg for accumulated as-processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs in Fig. 4(a) and hydrogen post-annealed Pt-Ti-O gate Si-MISFETs as a function of Vtheff tuned to the dose of (B) $1.0 \times 10^{12}\,cm^{-2}$. The definition of Vtheff is derived from Vth as follows: The Vth is replaced by Vth-0.167 V for (A) dose of $0.8 \times 10^{12}\,cm^{-2}$ and replaced by Vth + 0.167 V for (C) dose of $1.2 \times 10^{12}\,cm^{-2}$, and the Vth is not changed for (B) dose of $1.0 \times 10^{12}\,cm^{-2}$.

Lg = 10 μm and Wg = 150 μm.[2] In case of the Pt-Ti-O-gate Si-MISFETs with Lg = 10 μm and Wg = 150 μm the Vth was about 89 mV less value in average than that of the standard FETs with Lg = 20 μm and Wg = 300 μm under the same ion implantation conditions. We have corrected Vth in Vtheff by 89 mV in the case of circles (○) in Fig. 6.

Figure 6 shows that the sensing amplitude ΔVg rises up sharply around 0.76 V of Vtheff (V), which is cited as Vthc. The value of Vthc is 0.316 V smaller than the average Vth, 1.076 V, of the Pt-Ti-O gate Si-MISFETs. When regarding the Vth of the Ti-gate Si-MOSFETs with (B) dose condition as Vth(Ti) discussed in Sec. III B, the difference of Vthc – Vth(Ti), 1.02(= 0.76−(−0.26)), is 0.3 V smaller than the difference, 1.32 eV, of vacuum work function between 5.65 eV of Pt and 4.33 eV of Ti.

The physical meaning of Vthc can be probably described by a following scenario of the Vth change due to oxygen invasion into Ti layers as shown in Fig. 7. When Ti layers contact with gate oxide SiO_2 uninfluenced by the oxygen invasion, uniform Ti contact will be realized over the gate oxides. Some parts of Ti layers, probably under the Pt grain boundaries, will be changed locally to the novel mixing layers of nanocrystalline TiOx and superheavily oxygen-doped amorphous Ti by the unintentional oxygen invasion at the beginning of PSG deposition. Figure 7(a) represents schematically this situation by a planar view of the surface of gate oxide SiO_2 contacted with gate metals; the dashed short lines represent the Pt grain-boundary triple junctions and the loops represent initial Ti novel mixing layers contacted with gate oxide SiO_2. In this case the metal contact regions over gate oxide SiO_2 are composed of Ti contact regions and effective Pt contact regions. The Ti novel mixing layers will grow laterally in accordance with increasing oxygen invasion; then the effective Pt contact regions will become dominant. Furthermore, the ratio of Ti contact regions and the effective Pt contact regions will be shrunken up to zero in accordance with increasing the dose of oxygen invasion, which point probably corresponds to the Vthc. Figure 7(b) represents schematically this situation around Vthc. Finally the Ti novel mixing layers fill up all the Ti layers that correspond to the Pt-Ti-O gate structures as shown by circles (○) in Fig. 6. In this case the electrical properties of the Ti novel mixing layer will be changed to semiconductor or insulator so that the thin Ti layer should be depleted without free carriers. These depleted Ti layers should make only a minor contribution to the Vth.

The uniformity and reproducibility of Vth for the hydrogen post-annealed Pt-Ti-O gate Si-MISFETs are shown in Figs. 8(a) and 8(b) among 18 chips of #A-2 including the five chips of #A-3. The average Vth and σVth of #A-2 and #A-3 are Vth = 1.081 V with σVth = 59 mV and Vth = 1.0415 V, and σVth = 39 mV, respectively. The gate was 20 μm long and 150 μm wide for both FETs. From the practical-application point of view, the hydrogen post-annealing procedure to the Pt-Ti-O gate Si-MISFETs is necessary to terminate the deep traps to reduce the residual sensing amplitude ΔVgres with slow tailing behavior after turning off the hydrogen exposure.[2] The hydrogen post-annealing procedure also contributes the uniform distribution of Vth over wafer, as shown in Fig. 8(b), where the data of σVth for the as-processed chips, the air-annealed chips, and hydrogen post-annealed chips of six different wafers are summarized. The average Vth and the standard deviation of the Vth, σVth, for as-processed chips and #A-3 among the representative five chip positions (U, C, D, L, R) on the 5-φ Si wafer were 0.5427 V and 183 mV, respectively. The larger spread of Vth for as-processed chips was originated from the initial unintentional spreads of oxygen invasion.

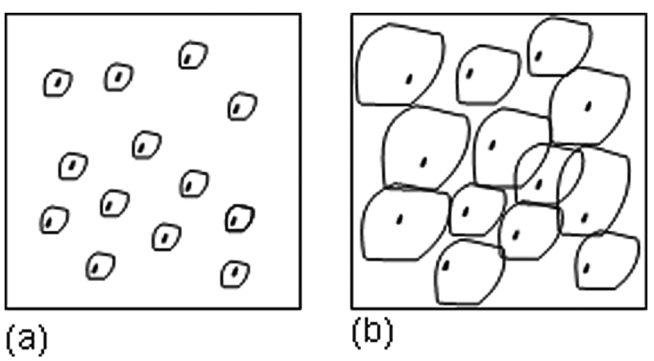

FIG. 7. Schematic planar view of the interface between gate oxide SiO_2 and Ti mixing layers about the proposed percolation model of the gate structures: (a) As processed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs and (b) oxygen invasion into Ti layers through Pt grain boundaries. The dashed short lines represent the Pt grain-boundary triple junctions and the loops represent Ti novel mixing layers contacted with both Pt-gate metals and gate oxide SiO_2.

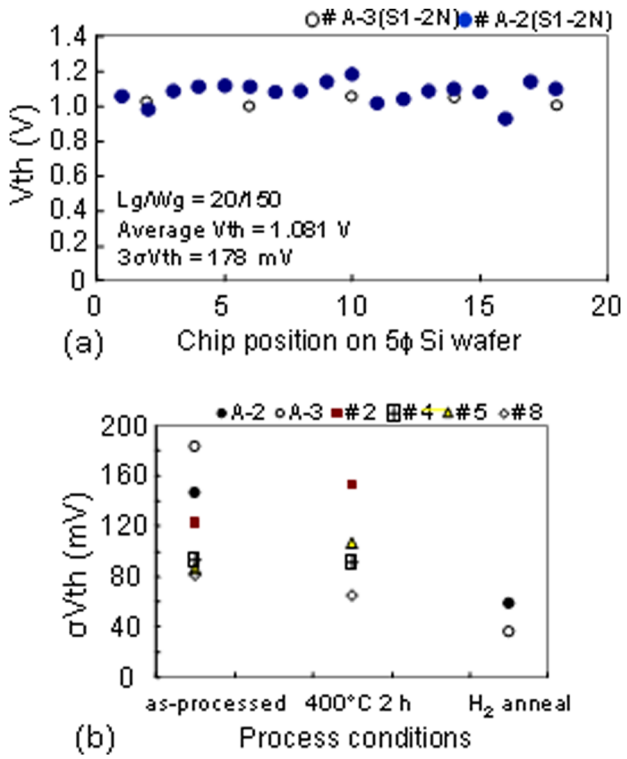

FIG. 8. (Color online) Uniformity and reproducibility of the Vth for Pt-Ti-O gate Si-MISFETs hydrogen gas sensors: (a) Wafer distribution and reproducibility of Vth for hydrogen post-annealed Pt(15 nm)/Ti(5 nm)-gate Si-MOSFETs for two sensor wafers, #A-2 and #A-3. Lg and Wg are 20 and 150 μm, respectively. (b) Standard deviations of Vth, σVth, for as-processed chips, air-annealed chips, and hydrogen post-annealed chips of six different wafers.

The improvement of uniformity of Vth after air annealing will be caused by the sufficient oxygen invasion into the Ti layer, because it will homogenize the initial oxygen distribution in the Ti-layers of as-processed sensor chips. Furthermore, more improvement of uniformity for Vth after hydrogen post-annealing will be achieved by the hydrogen compensation to deep traps generated around gate insulators. The uniformity and reproducibility of Vth is sufficient for most interface circuit designs.

IV. DISCUSSION AND CONCLUSIONS

The controllability of Vth for Pt-Ti-O gate Si-MISFETs hydrogen gas sensors is found to be unexpectedly excellent because of the following reasons. The oxygen invasion process through Pt grain boundaries to Ti layers is not so-called dopant diffusion process to control the carrier density of semiconductors such as Si or GaAs where the mother crystal structures do not change. During the course of oxygen invasion process, at the same time, titanium evacuates to the platinum surface through platinum grain boundaries. The invading oxygen is balanced with the evacuating titanium so that the titanium layer keeps nearly the same thickness as that of the as-grown state. The oxygen-invaded Ti layers change to a kind of new materials; Novel mixing layers of nano-crystalline TiOx and super-heavily oxygen-doped amorphous Ti formed on SiO_2/Si substrates. The annealing temperature is too low to grow crystalline TiOx filling up Ti layers. The Ti mixing layers change from metals to semiconductors or insulators. As the Ti layers are so thin like 5 nm, the total amount of oxygen invaded into Ti layers will be saturated and stabilized. From the device operation point of view, it is crucial to control the Vth precisely that the Ti novel mixing layers are thin and fully depleted; it is supported by the fact that the Vth change before and after air-annealing procedures can be well explained by the difference of vacuum work function between Pt and Ti. Our proposed percolation model to explain the above experimental results should be verified from various characterization methods in future works.

We have found that one of the advantages of the Pt-Ti-O gate Si-MISFETs is uniformity and reproducibility of Vth in addition to large sensing amplitudes at the practically important hydrogen concentration range between 100 ppm and 1% and the long intrinsic lifetime of more than 10 years.

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APPENDIX: TRIALS FOR BEST AIR-ANNEALING CONDITIONS OF PT(15 nm)/TI(5 nm) GATE SI-MOSFETS

We first selected ten sensor chips in the U regions presented in Fig. 2(b) for each of the three wafers with different doses, #3, #24, and #8. We investigated the annealing temperature dependence of device characteristics at a fixed annealing time of two hours in air. The experimental results of Vth and ΔVg for #3U, #8U, and #24U chips are shown in Fig. 9. Low-temperature annealing less than 300 °C for two hours did not improve ΔVg, but gradually increased the Vth. High-temperature annealing above 450 °C for two hours began to decrease ΔVg and Vth. The FET characteristics and sensing amplitudes of the air-annealed samples at 600 °C for two hours could not be measured due to the destroyed Al wirings.

According to this annealing temperature dependence, the optimum annealing temperature is around 400 °C or 425 °C at air annealing for two hours; therefore, we fixed the annealing temperature at 400 °C, as low as possible, for low-temperature annealing. In fact the resistances of Al wiring heaters begin to degrade the resistance for long heating at 425 °C.[5]

We also prepared ten sensor chips in the C regions of the 5 inch. Si wafers for #8 and #24, and then we measured ΔVg of two chips, #8 C, and #24 C, for various annealing times t under the fixed annealing temperature of 400 °C, as shown in Fig. 10, where the measurement times for the first five steps were 5, 10, 15, 30, 45 min. The initial value of ΔVg, i.e., t = 0 min, shows the ΔVg of the as-processed chips. The first 15 to 30 min reached saturated ΔVg, which means the oxidation process of Ti layer was so rapid.

The initial spreads of ΔVg observed at the as-processed chips in both Fig. 9(b) and Fig. 10 can be interpreted in terms of the initial unintentional spreads of oxygen invasion into the Ti layer, where oxygen invasion should be caused through open air at 390 °C for a couple of minutes before

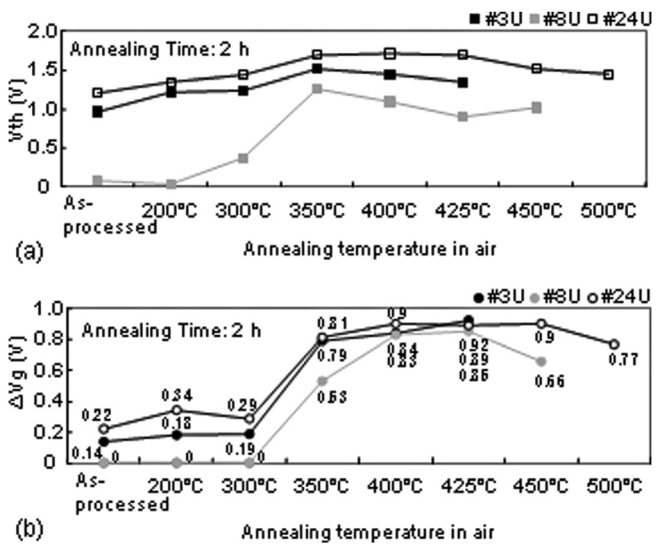

FIG. 9. Annealing temperature dependence of (a) Vth and (b) ΔVg in air at fixed annealing time of 2 h.

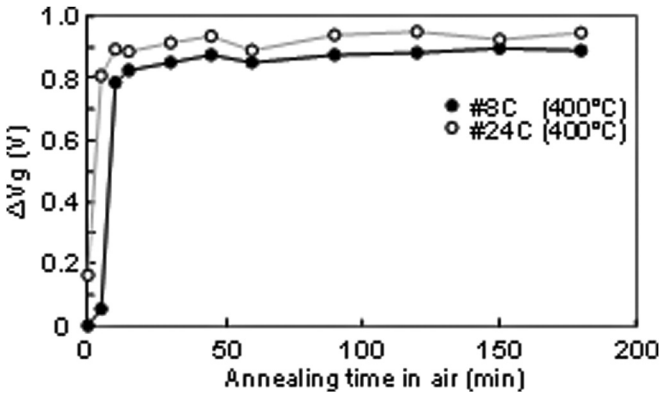

FIG. 10. Annealing time dependence of ΔVg in air at fixed annealing temperature of 400 °C.

starting thermal chemical deposition (CVD) of PSG as was discussed in the last works.[1,2] The initial large variations of Vth for #3U, #8U, and #24U chips, even if considering different doses of (A) 0.8×10^{12} cm^2, (B) 1.0×10^{12} cm^2, and (C) 1.2×10^{12} cm^2 for n-type FETs, will be explained by the same initial spreads of oxygen invasion into the Ti layer.

[1]T. Usagawa and Y. Kikuchi, Appl. Phys. Express **3**, 047201 (2010).
[2]T. Usagawa and Y. Kikuchi, J. Appl. Phys. **108**, 074909 (2010).
[3]T. Usagawa and Y. Kikuchi, Proc. IEEE Sensors Conf. **2010**, 2145 (2010).
[4]T. Yamaguchi, T. Kiwa, K. Tsukada, and K. Yokosawa, Sens. Actuators A **136**, 244 (2007).
[5]T. Usagawa, Y. Kikuchi, S. Nakano, and D. Kamoto, J. Fuel Cell. Technol. **8**, 88 (2009)[in Japanese].
[6]For examples, J. T. Clemens, Bell Labs. Tech. J. **2**, 76 (1997).
[7]T. Usagawa and Y. Kikuchi, Device Analysis of Pt/Ti gate Si-MOSFETs Hydrogen Sensors - Unintentional Oxygen Invasion into the Ti layers, Jpn. J. Appl. Phys. (submitted).
[8]J. F. Gibbons, Proc. IEEE **56**, 296 (1968).
[9]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley & Sons, New York, 1981), pp. 442–477.
[10]H. B. Michaelson, J. Appl. Phys. **48**, 4729 (1977).