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Triggering and sustaining of snapback in MOSFETs

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Abstract

This paper analyses the phenomenon of snapback (negative resistance portion of the output characteristic) in MOSFETs. It shows that the expansion of the base of the parasitic bipolar transistor provides the necessary basis for the understanding of the snapback mechanism. It also offers simple criteria for the snapback triggering and sustaining which have been lacking to date.

1. INTRODUCTION

The importance of snapback has still been rising, since it imposes severe limitations on a technologies down-scaling (especially acute in EPROMs [1]). Snapback also finds some useful applications such as input/output ESD (electrostatic discharge) protection circuits [2]. In the literature there are merely a few studies (e.g. [3] [4]) on snapback. Still, however, there is the lack of clear criteria for the triggering and sustaining of snapback. Both [3] and [4] prove that snapback must inevitably occur but do not point out what is the precise impulse which leads to its triggering at the very particular, well defined and reproducible point of the characteristic.

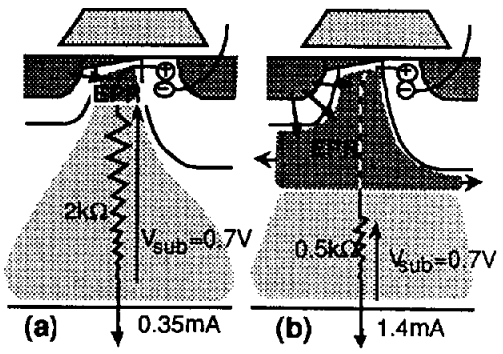

Figure 1. Evolution process of the EPR (equipotential region, and also base of the parasitic bipolar transistor), according to numerical simulation results.

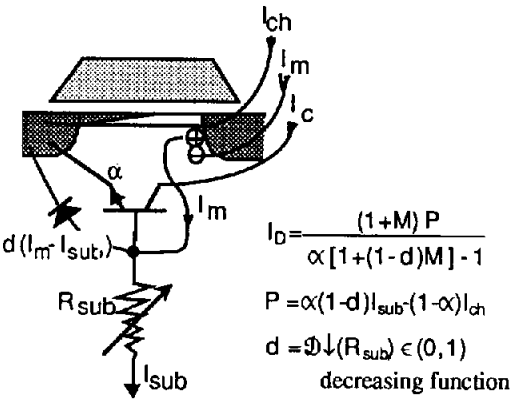

Figure 2. Equivalent circuit and corresponding current balance equation. d accounts for the expansion of the EPR.

2. PHYSICAL BASIS.

The expansion (see Fig. 1) of the EPR (equipotential region, being also the base of the parasitic bipolar transistor (BT)), has been shown in [5] to be the key point in the breakdown physics. The equivalent circuit, resulting [6] from the expansion, and a corresponding drain current expression (current balance) are shown in Fig. 2. As snapback can only occur in current-drive conditions, we have thus extracted the multiplication coefficient M as a function of I_D from the current balance (Fig. 2):

$$M = \frac{1 - \alpha d}{\alpha(1 - d) - P/I_D} - 1 \quad , \quad \text{where } P = \alpha(1 - d)I_{sub} - (1 - \alpha)I_{ch} \qquad (1)$$

The obtained expression is very suitable for the analysis of snapback since there is a direct correspondence between M and V_D. Indeed, as M is a monotonically increasing function of V_D, any variation in M (with I_D) imprints its image on V_D, comp. Fig. 3.

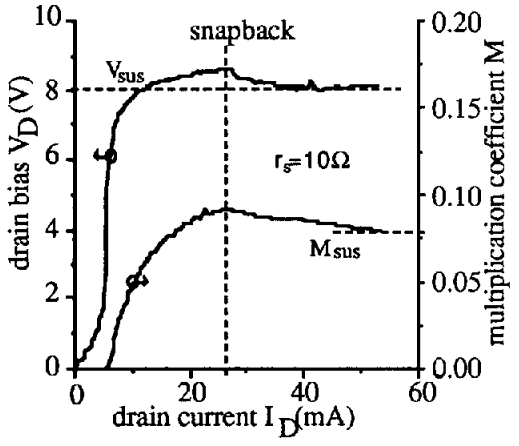

Figure 3. Illustration of the direct correspondence between the drain bias V_D and the multiplication coefficient M. The curves have been extracted from measured data taken on a MOSFET of L_{el}=1.2μm and Z=50μm at V_G=3V.

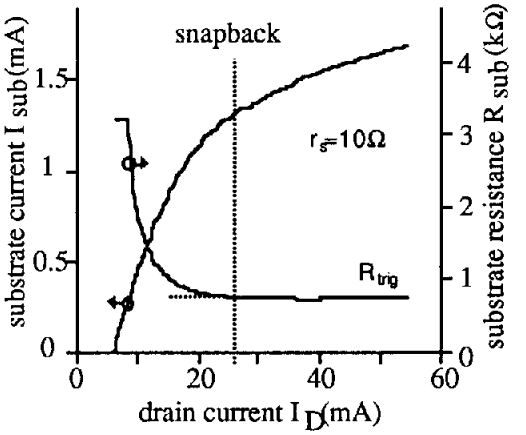

Figure 4. Measured substrate current and substrate spreading resistance (extracted from measurements according to (2)) versus drain current. The bottoming-out of R_{sub} determines very well the triggering of snapback. The dotted vertical line indicates the snapback triggering, as read-out from measurements. L_{el}=1.2μm, Z=50μm and V_G=3V.

3. TRIGGERING

Note that the forthcoming analysis is qualitatively independent of the existence or not of the parasitic diode (by putting d=0, single transistor scheme, in (1), one is led to the same physical interpretation of snapback, however ones'es quantitative results are then inaccurate).

Before snapback, P (defined in (1)) increases faster than I_D, mainly because of the increase in I_{sub}. I_{ch} saturates before, once the parasitic bipolar transistor is turned on [5,6]. As a result, P/I_D increases, which, according to (1), causes M to increase as well. Consequently, V_D also rises with I_D, as can be seen in Fig. 3. At a certain point (see Fig. 4), however, I_{sub} has been found to saturate (or at least to change considerably slope), which causes P/I_D to peak and then to turn down, thereby leading to a reduction in M, according to (1). As a result, V_D also starts to decrease (triggering of snapback) with a further increase in I_D, see Fig. 3. This brings the MOSFET into a strong positive feedback regime. The decrease in M further increases I_D (the relationship between I_D and M is shown in Fig. 2), which in turn reduces M even more, etc,etc..., this being the essence of snapback.

The saturation of I_{sub}, being the crux of the snapback physics, also results from the EPR expansion. As found in [5] and [6] this expansion is a kind of a self-adjusting mechanism. Expanding, EPR absorbs as much of the bulk spreading resistance R_{sub} as is necessary to ensure $V_{sub}=R_{sub}I_{sub}\cong 0.7V$ at its bottom edge. The decrease in R_{sub} is, however, highly nonlinear, since the upper part, squeezed between the source and drain domains, contributes to R_{sub} much more than the lower, bulk part. In addition, the initially downward expansion becomes more and more lateral, as it encroaches below the source and drain domains, comp. Fig. 1. Both these effects result in a bottoming-out of R_{sub} and consequently saturation of I_{sub}.

As shown in Fig. 4, the saturation of I_{sub} may be imperfect in spite of a distinct bottoming-out of R_{sub}. This is due to the effect of a non-zero source series resistance r_s:

$$I_{sub} = (0.7V + r_s I_S)/R_{sub} \tag{2}$$

which allows a certain increase in I_{sub} even after R_{sub} becomes constant. Nevertheless, the triggering of snapback is still determined by the bottoming-out of R_{sub}, see Fig 4, thus providing a simple snapback criterium: $R_{sub}\rightarrow R_{trig}$.

Fig. 5 shows that R_{trig} is almost constant in a wide range of channel lengths and gate biases, thus confirming its usefulness as a snapback criterium. The slight increase in R_{trig} with V_G, visible in Fig.5(b), results from the variation of r_s with V_G. This increase vanishes when assuming a reduction in r_s even as small as 1Ω per 2.5V increase in V_G, which then renders R_{trig}-versus-V_G perfectly constant.

4. SUSTAINING

The positive feedback between M and I_D, described in the previous Section, leads to a rapid increase in I_D, thus bringing M to its limiting value M_{sus} (see Fig. 3):

$$M_{sus} \equiv \lim_{I_D\rightarrow\infty} (M) = (1 - \alpha)/\alpha/(1 - d_{trig}) \tag{3}$$

where $d_{trig}=\mathfrak{D}(R_{trig})$. M_{sus} can be easily transposed into the corresponding V_{sus} voltage by means of the $M=\mathcal{M}(V_D)$ relationship, which can be provided by any reliable multiplication coefficient model. Table I shows that the V_{sus} voltage predicted in this way can agree very closely with the measured data. For this particular calculation, as well as those concerning the characteristics shown in Fig. 3, the multiplication model based on [7], and developed in [8], has been used. Note that (3) accounts for the observed experimentally by Beitman [3] decrease in V_{sus} with L. This decrease results from (3) when taking into account that α is a decreasing function of L.

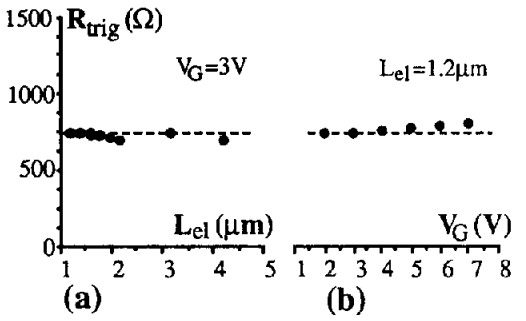

Figure 5. Substrate spreading resistance R_{trig} corresponding to the triggering of snapback, as extracted from measurements (according to (2)), for (a) - different channel lengths, and (b) - different gate biases.

Table I

sustaining voltage V_{sus} [V][§]

measured	calculated
8.05	**7.95**

§ In this experiment α and $\mathfrak{D}$ have been found in such the way so as to make I_D match the measured data in the region before snapback. I_{sub} and I_{ch} were measured values and L_{el}=1.2μm.

5. CONCLUSION

The bottoming-out of R_{sub} has been shown experimentally, as well as theoretically, to furnish that particular impulse which leads to the triggering of snapback. This finding offers simple criteria for the snapback triggering and sustaining, lacking to date.

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