ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Nanoscale Cross-Point Resistive Switching Memory Comprising p-Type SnO Bilayers

*Mrinal K. Hota, Mohamed N. Hedhili, Qingxiao Wang, Vasily A. Melnikov, Omar F. Mohammed, and Husam N. Alshareef**

Reproducible low-voltage bipolar resistive switching is reported in bilayer structures of p-type SnO films. Specifically, a bilayer homojunction comprising SnO_x (oxygen-rich) and SnO_y (oxygen-deficient) in nanoscale cross-point (300×300 nm^2) architecture with self-compliance effect is demonstrated. By using two layers of SnO film, a good memory performance is obtained as compared to the individual oxide films. The memory devices show resistance ratio of 10^3 between the high resistance and low resistance states, and this difference can be maintained for up to 180 cycles. The devices also show good retention characteristics, where no significant degradation is observed for more than 10^3 s. Different charge transport mechanisms are found in both resistance states, depending on the applied voltage range and its polarity. The resistive switching is shown to originate from the oxygen ion migration and subsequent formation/rupture of conducting filaments.

1. Introduction

Alternative architectures and materials for future memory devices are of particular interest because complimentary metal-oxide-semiconductor (CMOS) technologies are expected to reach their limits in the next decade. Among many candidates to replace the existing memory devices, resistance random access memory (RRAM) is assumed to be one of the promising candidates owing to its simple metal–insulator–metal structure, fast switching speed, low-power operation, excellent scalability potential, and high density along with its ability to combine the key features of established Flash, static random access memory (SRAM) and dynamic random access memory (DRAM) memory performances.[1–3] In general, the resistive switching memory devices show reproducible switching between high resistance state (HRS) and low resistance state (LRS) during one DC voltage sweeping cycle. In contrast, resistive switching devices have been categorized into two types, i.e., the bias amplitude dependent unipolar switching and the bias polarity dependent bipolar switching. The resistive switching behavior has been investigated by several research groups in different device architectures. Compared to different device designs, RRAM in cross-point design (in which top and bottom electrodes are placed at 90° angle to each other) with memory materials sandwiched in between has a great potential in the near future due to many attractive features. For example, it offers high-density integration ($4F^2$, where F = minimum feature size), 3D stacking and cost-effective fabrication.[4,5] Hence, nanocross-point architecture is considered to be one of the most exciting RRAM research directions.

The core of an RRAM device is the switching material, which is sandwiched between the two metal electrodes. There are several reported switching materials, which are mostly n-type oxides, such as TiO_x,[6] SiO_x,[7] AlO_x,[8] HfO_x,[9] TaO_x,[10] WO_x,[11] ZnO_x,[12] ZrO_x,[13] $SrTiO_3$,[14] and $Pr_{0.7}Ca_{0.3}MnO_3$.[15] In contrast, p-type oxides in RRAMs have received less attention. This is probably because the number of available p-type oxides is less and the resistive memory mechanism in p-type oxides has not yet been clearly revealed. However, few p-type oxide materials such as NiO_x,[16] CuO_x,[17] Co_2O_3,[18] $CuAlO_x$[19] have been reported so far for resistive switching applications. We have recently reported the resistive switching memory performance in another p-type oxide, SnO.[20] In terms of materials, SnO is very promising candidate for future cutting edge electronic device applications, especially as p-type semiconductor in thin film transistor applications due to its high mobility compared to other p-type oxides.[21] Therefore, SnO might be useful for 1T1R cell design in the RRAM memory chip. Hence, it is important to study the resistive switching memory performance of SnO-based devices in more details.

It has already been reported that a bilayer structure of two different oxides or same oxide with different oxygen contents exhibits better switching performances as compare to a single oxide layer in RRAM cell.[22] Among these reports, homojunction bilayer n-type oxide structure, such as Ta_2O_{5-x}/TaO_{2-x} and TiO_2/TiO_{2-x} have been found promising due to their control switching performance.[23,24] However, details of the physical mechanism are still debated. Though the exact microscopic mechanisms are still under controversial discussion, there exists a general agreement that the migration of oxygen ions

Dr. M. K. Hota, Dr. M. N. Hedhili, Q. Wang, Dr. V. A. Melnikov, Prof. O. F. Mohammed, Prof. H. N. Alshareef
Physical Sciences and Engineering Division
King Abdullah University of Science and Technology (KAUST)
Thuwal 23955-6900, Saudi Arabia
E-mail: husam.alshareef@kaust.edu.sa

DOI: 10.1002/aelm.201400035

or vacancies under an applied electric field play the key role in resistive switching process.

In this study, we prepare a bilayer homojunction based on p-type oxides. Specifically, SnO_x (oxygen rich)/SnO_y (oxygen deficient) homojunction oxide bilayer was fabricated in a nanoscale cross-point (300 × 300 nm^2) structure for resistive switching memory applications. To our knowledge, cross-point resistive switching memory effects in p-type oxide bilayers have not been reported. The device characteristics such as endurance, retention, conduction mechanism, local resistive switching study, etc. at room temperature are discussed. Finally, we propose a mechanism to explain the underlying physicochemical phenomena involved in the resistive switching behavior of SnO_x/SnO_y homojunction bilayer based memory devices.

2. Results and Discussion

2.1. Material Characterization

An optical microscope image of such a nanoscale cross-point structure with a device area of 300 × 300 nm^2 is shown in **Figure 1**a and corresponding scanning electron microscopy (SEM) image is shown in Figure 1b. The top and bottom electrode bars at right angles along with the contact pads are shown. In order to study the structure and composition of the device, cross-sectional transmission electron microscopy (TEM) along with electron energy loss spectroscopy (EELS) and energy-dispersive X-ray spectroscopy (EDS) elemental mapping were performed, as shown in Figure 1c–f. From EELS mapping, it is confirmed that a third O environment has formed at the interfaces of Al/SnO_x (bottom electrode interface with oxide) and SnO_y/Ti (top electrode interface with oxide). The interfacial layer between top/ bottom electrodes and oxide layers likely formed during the fabrication process via a local redox reaction process. However, no clear color contrast was found between two SnO layers.

The chemical composition of the SnO_x and SnO_y films were analyzed using high-resolution X-ray photoelectron spectroscopy (XPS) analysis. Binding energies were referenced to the C 1*s* binding energy of adventitious carbon contamination, which was taken at 285.0 eV. In order to determine the chemical state of Sn, Sn 4*d* core level spectrum was studied from the SnO_x and SnO_y films deposited on HF last Si wafer. The analysis of the Sn 4*d* spectra confirms that Sn is present in the form of three different chemical sates, such as Sn^0 (as metallic tin), Sn^{2+} (as SnO), and Sn^{4+} (as SnO_2) in both films,[25,26] as shown

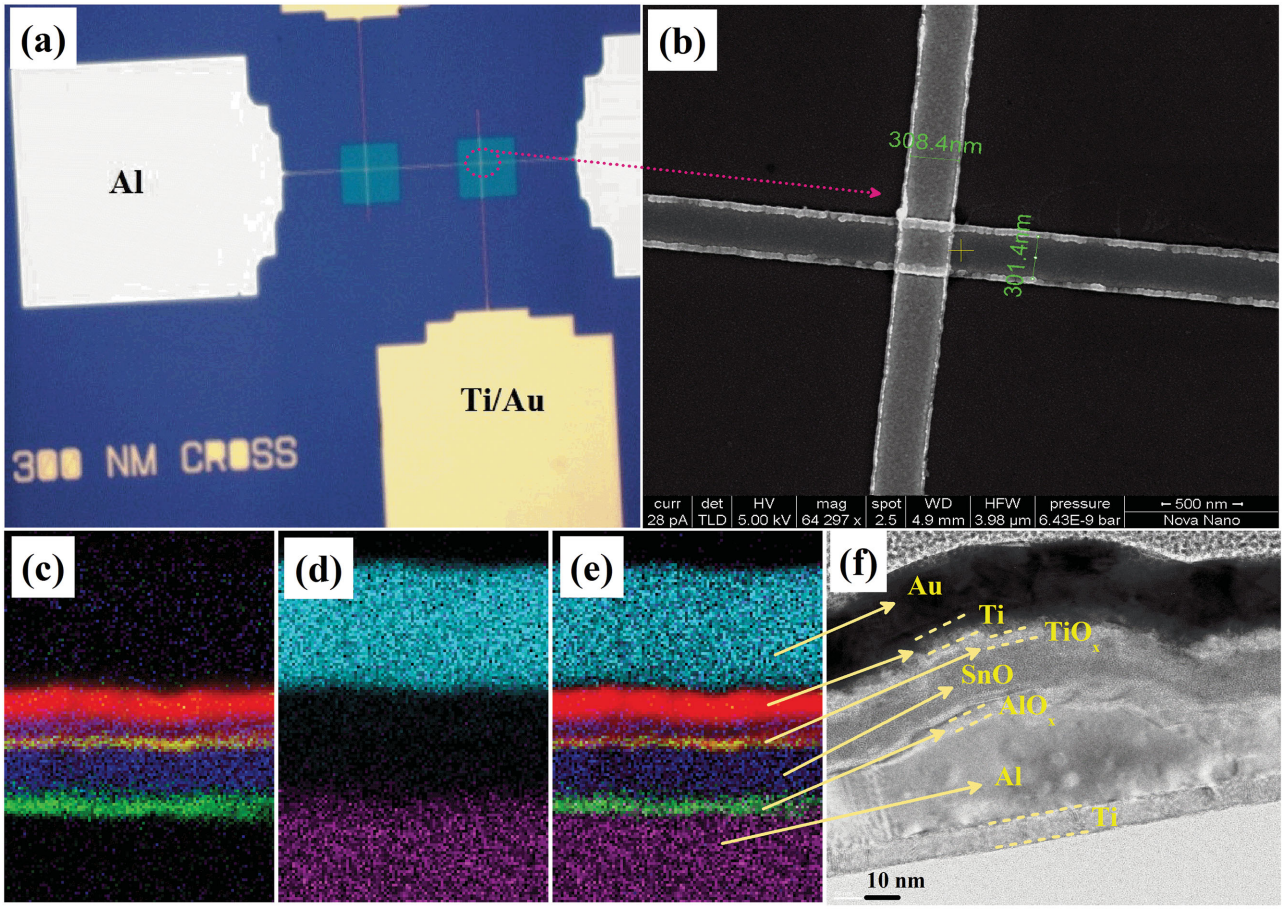

Figure 1. a) Optical microscopy image of the fabricated device. b) Scanning electron microscope imaging of a cross-point device structure (top view). c) EELS, d) EDS, and e) EELS + EDS combined mapping of different elements. f) Corresponding cross-sectional TEM image of the device.

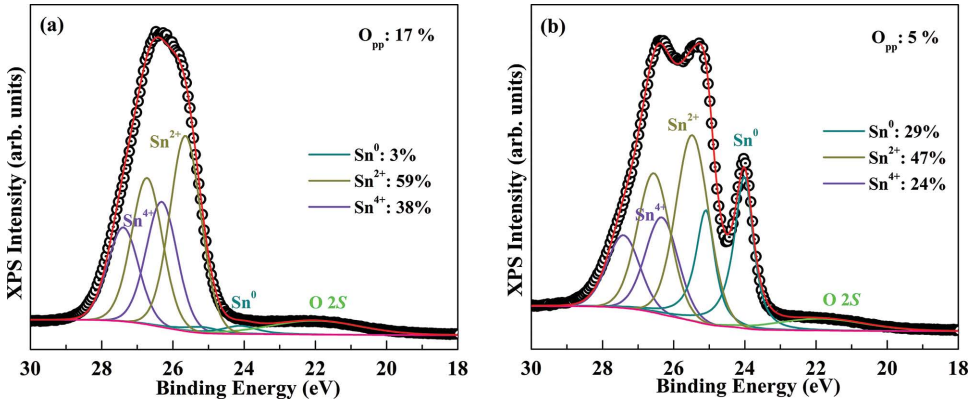

Figure 2. High resolution XPS spectra of Sn 4*d* from a) SnO_x (17% O_{pp}) and b) SnO_y (5% O_{pp}) films. XPS curve fitting analysis revels that SnO_y film is more conducting as compare to the SnO_x film.

in **Figure 2**a,b, respectively. Additional peak centered at ≈22 eV in both films was necessary to fit the Sn 4*d* and it corresponds to O 2*s*. The contents of metallic Sn in the deposited films were estimated from the Sn 4*d* spectrums which are 3% and 29% for SnO_x and SnO_y, respectively, indicating that SnO_x is oxygen rich as compare to SnO_y film. SnO_y is more conducting due to the presence of metallic Sn in higher amount.

Raman measurements were utilized to identify Raman active phonon modes of the films with 473 nm excitation wavelengths are shown in **Figure 3**. From SnO_y sample, two main peaks at ≈114 cm^{-1} and ≈211 cm^{-1} corresponding to the B_{1g} and A_{1g} vibrational modes, respectively, for the tetragonal SnO structure were observed.[27] However, a major loss in the Raman intensity and peak shifting to higher wavenumber side can be observed in SnO_x samples. The peak at 116 cm^{-1} are found as major peak which is assumed to be the blue shift of the SnO B_{1g}, which appears at 114 cm^{-1} in SnO_y sample. In addition, it

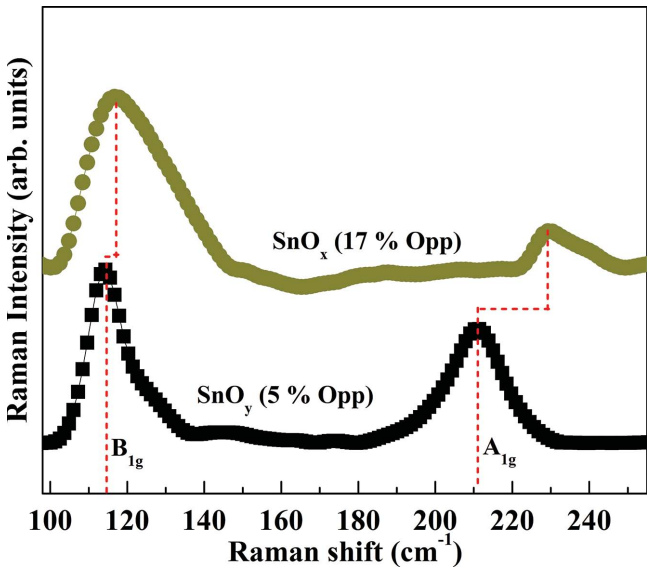

Figure 3. Raman spectra from oxygen rich (SnO_x) and oxygen deficient (SnO_y) films. The peak intensities for A_{1g} and B_{1g} decreases and shifted towards higher wavenumber side as a result of decreasing the amount of metallic Sn.

can be seen that the peak is broad as compared to SnO_y sample, which suggests that multiple oxidation states may exist in the SnO_x (oxygen rich) samples. The A_{1g} vibrational mode is also found to be blue shifted by an amount of 18 cm^{-1}, signifying the reduction of metallic Sn in the film.[28] Hence, the Raman analysis suggests that SnO_y has higher Sn content as compared to SnO_x, which agrees well with the XPS results.

2.2. Resistive Switching Memory Characterization

The typical current–voltage (*I–V*) characteristics of the resistive switching memory device are shown in **Figure 4**. The virgin state *I–V* characteristic shows the current order almost similar to that of HRS of the device (Figure 4a). However, it was observed that no significant resistive switching phenomenon exists in virgin devices and holds high cell resistance. Hence, the memory cell must be electroformed in order to activate it, as shown in Figure 4b. A current compliance of ≈1 mA was used to prevent the device from permanently breaking down during the high dc voltage electroforming step. Typical pinched hysteretic *I–V* characteristics obtained from the Al/SnO_x/SnO_y/Ti/Au memory cell are shown in Figure 4c. The direction of the switching bias was swept in a sequence of $0 \rightarrow V_{positive} \rightarrow 0 \rightarrow V_{negative} \rightarrow 0$ as indicated by the arrows. By applying a positive voltage to the Ti/Au top electrode, the resistance changed from the initial HRS to LRS state at around ≈1.6 V (V_{SET}). The device remains in the LRS until the voltage is reduced to another threshold voltage, –1.2 V (V_{RESET}), where the current decreases gradually and the device switches back from the LRS to the HRS. For memory applications, V_{SET} and V_{RESET} are used as the "writing voltages." If the device is in HRS, the current is relatively low, representing logic state "0" (OFF); if the device is in LRS, the current is relatively high, representing the logic state "1" (ON). The "reading voltage" is the small value of voltage can be chosen in the range between V_{SET} and V_{RESET} (for example, 0.5 V in this work) to avoid another switching during the reading process. In addition, it is interesting to observe that a sharp transition from the HRS to LRS occurs during the SET process (arrow 2 in Figure 4c), while a multiple partial RESET process occurs when the device undergo from LRS to HRS (arrow 5 in Figure 4c). The transition for this bilayer device

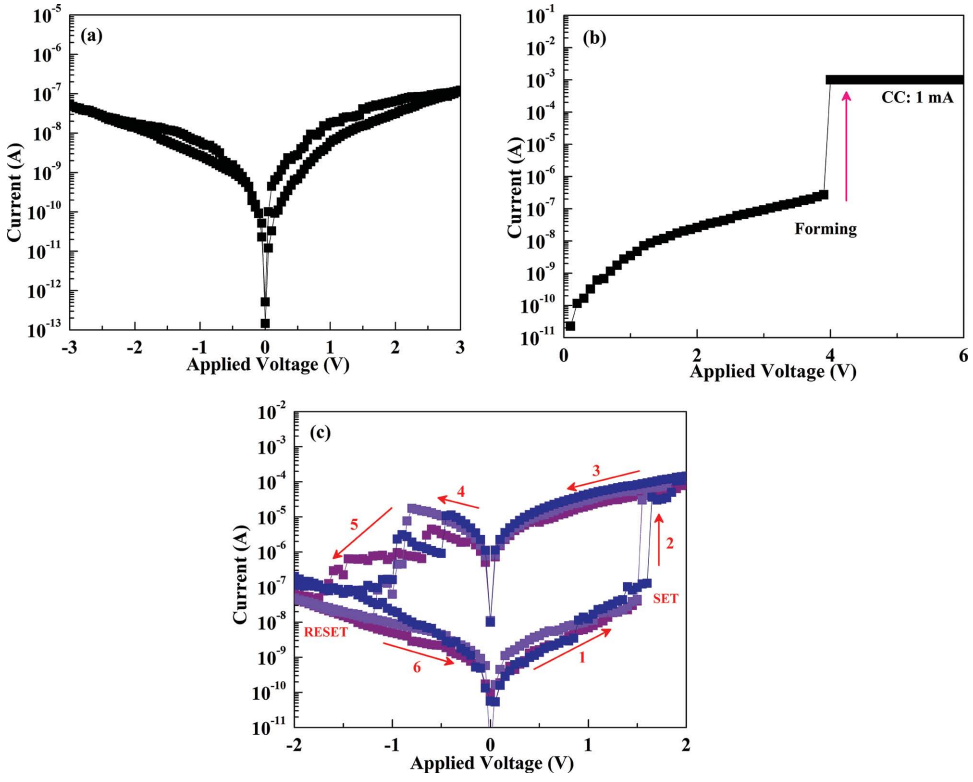

Figure 4. The hysteretic current–voltage (*I–V*) characteristics of the nanocross-point resistive switching device. a) The virgin state *I–V* characteristics show no significant memory performance. b) DC electroforming process of the device. It is necessary to activate the device. c) A typical hysteretic *I–V* characteristics. An abrupt change in the device resistance was observed during SET process, while a stepwise increase in the device resistance was observed in the RESET process.

from HRS to LRS, i.e., SET process occurs under positive bias, while the RESET process happens at the opposite polarity side, hence the cell reveals a well-known counter-clockwise resistive switching memory performance. Furthermore, it is observed that unlike conventional RRAM devices, this device does not require any current compliance limit for memory operation which indicates its built-in current overshoot reduction capability which may helpful in obtaining long pulse endurance without the use of a transistor as current limiter in a crossbar array architecture.[29]

Next to check the oxide bilayer effect, we prepared reference devices with individual SnO_x and SnO_y layers with identical thickness. The results are shown in Figure S2a,b, Supporting Information, respectively. It can be observed that both of these single oxide layer based devices do not show good resistive switching memory performance, which clearly shows that the bilayer SnO concept is more suitable for resistive switching memory applications. The details switching mechanism will be discussed later.

It is interesting to note that a self-rectifying effect can be observed in the LRS state (see Figure 4c) while it is missing in the HRS (asymmetric *I–V* curves in LRS signify self-rectifying effect). The self-rectifying effect suggests that a Schottky-like barrier might have been formed at the Al/SnO_x interface[30] (as also confirmed from EELS mapping), which blocks electrons flowing from bottom electrode to the oxide layer causing a negative current smaller than the positive one. The rectifying behavior is beneficial for the elimination of the cross talk (sneak path current) in the crossbar structure and, thus, misreading can be avoided.[31] Similar phenomenon has also been reported by Zuo *et al.* for Au/ZrO_2 interface.[32] Thus, without an embedded diode, the self-rectifying effect in $Al/SnO_x/SnO_y/Ti/Au$ nanocross-point memory device shows the potential to be used in crossbar array structures.

In order to understand the conduction process during resistive switching in the $Al/SnO_x/SnO_y/Ti/Au$ nanoscale cross-point device, the charge transport mechanism should be carefully examined due to the complexity of the conduction process in these types of memory structures. Many models of carrier transport for resistive switching devices have been reported; including space charge limited conduction (SCLC), Schottky emission, Poole–Frenkel emission, and Fowler–Nordheim quantum tunneling process, etc. The tunneling process can be ruled out due to the oxide film thickness of ≈20 nm in the present study.[33] Other mechanisms can be distinguished via logarithmic plot of *I–V* characteristics, as shown in **Figure 5**. It can be observed that charge transport mechanism is not identical in LRS and HRS; rather it follows bias dependent multiple conduction process. Three distinct regions can be observed in the logarithmic plot of *I–V* curve at HRS, which can be explained by considering the SCLC concept.[34] As shown in Figure 5, the current at HRS can be well fitted by the Ohmic conduction ($I \propto V$) with a slope of ~1 (denoted as region "A") for the applied voltage less than 0.5 V. The presence of the "tiny conducting

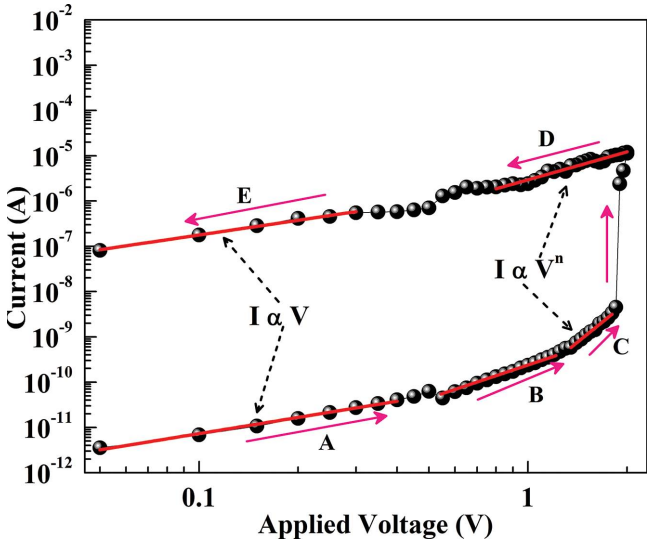

Figure 5. The electrical conduction mechanism of the nanoscale memory device. A bias dependent multiple charge transport phenomenon was observed in both LRS and HRS states.

filaments" existing in the oxide film during HRS state may result in the linear conduction at low-bias region. However, when the applied voltage is higher than 0.6 V, the *I–V* characteristics does not show the Ohmic conduction process and slope of the linear fitting increases with applied bias. A square dependence region with slope ~2, which is corresponding to Child's law ($I \alpha V^2$), can be observed at bias range between 0.6 and 1.3 V (denoted as region "B"). This may be due to the reason that the concentration of free electrons as a result of the carrier injection greatly increases with the applied voltage, which leads to the nonequilibrium charge concentration in the film and contributes to the increasing of current. The voltage values of 0.5 and 0.6 V represent the Ohmic conduction boundary voltage and SCLC onset voltage, respectively. The intermediate region represents the transition between Ohmic and SCLC behaviors. When the applied voltage is sufficiently high enough (i.e., higher then trap fill voltage, V_{TFL}) to fill the traps in the oxide film, a large voltage square-law conduction appears with slope of ~6 (denoted as region "C"), indicating a trap-controlled space charge limited conduction mechanism (TC–SCLC).[35] The electron concentration in the film increases with increasing voltage after filling all traps, and the sample finally achieve LRS at a threshold value of the applied voltage (V_{SET}). Although the current conduction at higher voltage can be explained by the TC–SCLC, the abrupt jump of current by almost 10^3 is not common in SCLC processes. It seems that additional effects such as filamentary conduction might affect the switching behavior, which will be discussed later. On the other hand, the current conduction process in the higher voltage region (higher than 0.7 V) in LRS (denoted as region "D") shows SCLC type behavior with slope of around 2. It can be noted that no current drop appears below the V_{TFL} during the reverse voltage sweeping, which indicates that the TC–SCLC state holds even below V_{TFL} in the LRS, resulting in the clear hysteresis in the positive-bias region. This high current level may be due to the existence of so-called conducting filaments (CF) and space charge effect in LRS. However, below 0.45 V, the current conduction process shows Ohmic with the slope of nearly 1 (denoted as region "E"), signifies the existence of conducting filaments only, with such a high current order as compare to HRS. Hence, it may be concluded that multiple conduction mechanism exists in the Al/SnO_x/SnO_y/Ti/Au cross-point memory structure, depending on the memory state and applied voltage.

Reliability is an important factor for memory applications. In order to investigate the reliability of our nanoscale resistive switching memory devices, the endurance and retention characteristics were studied. The endurance test was carried out by sweeping applied dc voltage and reading at 0.5 V in each DC sweep cycle, as shown in **Figure 6**a. The endurance characteristics of the device measured at room temperature for 180 switching cycles show no significant failure. Although the resistance values of both HRS and LRS show some fluctuations, the ON/OFF ratios remain constant around 10^3 throughout. Figure 6b depicts the retention stability of the device measured with a readout voltage of 0.5 V at room temperature. There is no significant degradation of the memory states, which implies that a sufficient memory margin remains, when the device undergoes over 6000 s operation. These results confirm the nonvolatile nature of the device.

Furthermore, the formation and rupture of conducting channels were studied using conductive atomic force microscopy (c-AFM). During the c-AFM measurements, the bottom Al electrode was kept grounded, while bias was applied through the tip

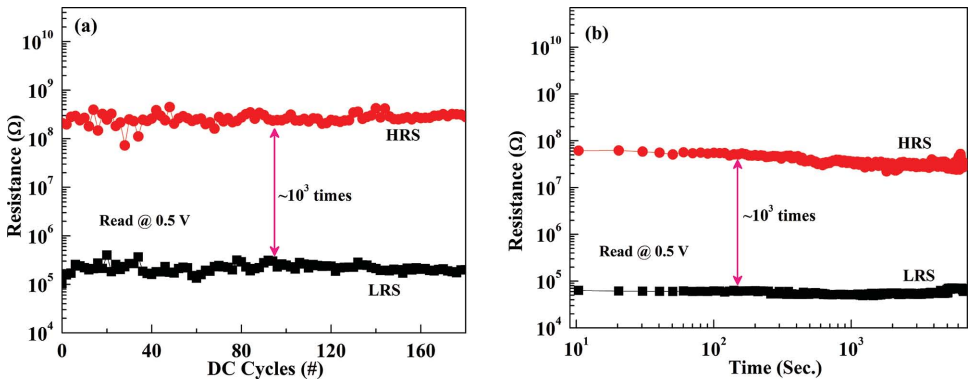

Figure 6. Reliability study of the device. a) Memory performance during DC cyclic process. b) Data retention performance of the device at room temperature. These two studies show nonvolatile nature of the device.

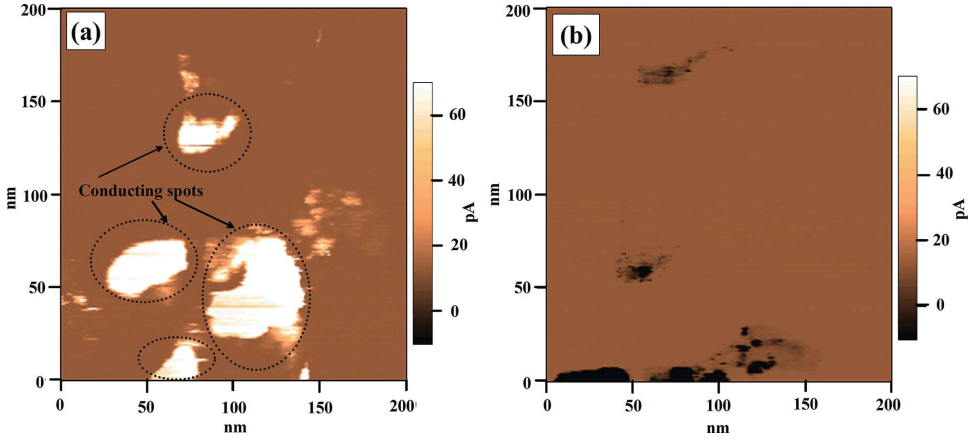

Figure 7. c-AFM images obtained under a) SET and b) RESET condition. Large numbers of conducting spots are observed during SET condition, which satisfies the results that obtained in *I–V* characteristics.

on the top electrode. The c-AFM images were captured over the scan area of 200 × 200 nm^2 with a constant voltage bias of +2 or –2 V, respectively, to obtain the LRS or HRS state. **Figure 7**a,b show the conductivity mapping results of the device in its LRS and HRS condition, respectively. The c-AFM indeed shows that there are many conducting channels or conducting spots (white color portions) with a higher density in the LRS as compare to HRS. However, it can be noticed that disappearance of almost all local conducting spots in Figure 7b, suggesting the onset of RESET condition that enables the device to return to its HRS, as is also evident from the observed *I–V* characteristics (Figure 4c). Moreover, the RMS value of this current mapping for LRS and HRS was estimated to be 26.2 and 12.4 pA, respectively, illustrating the conductivity difference between these two states. Hence, the switching cycle resembles a typical nonvolatile memory composed of ON and OFF states.

In light of the material analysis and electrical results described above, a possible physical model for resistive switching in our bilayer devices is proposed. The proposed switching mechanism is based on the formation/rupture of conducting filaments involving oxygen ion migration.[36] **Figure 8** shows three possible device conditions (Virgin, LRS and HRS) observed in this nanocross-point memory structure. Figure 8a shows the device condition during virgin state. The resistive switching layer used in this study is a homojunction bilayer of resistive SnO_x (oxygen rich) and conductive SnO_y (less oxygen). Hence, it is expected that the drift of oxygen ions (e.g., O^{2-}) from one layer to other, depending on the bias condition on the top electrode. Here, SnO_x layer can be considered as an oxygen ion reservoir raising the possibility that the oxygen ions could be trapped/detrapped within SnO_y layers. Possible defects that can trap mobile oxygen ions are oxygen vacancies (V_O^{2+}).[37]

During the application of a positive bias to the top electrode, as shown in Figure 8b, O^{2-} and free electrons in SnO_x start moving towards the top electrode through SnO_y layer. During the low positive bias ($V < V_{SET}$), the negative carriers (electrons) first fill any present traps (e.g., V_O^{2+}) in the SnO_y layer and generate V_O (electron occupied oxygen vacancy). The capture cross section of V_O to O^{2-} is very small due to electron shielding

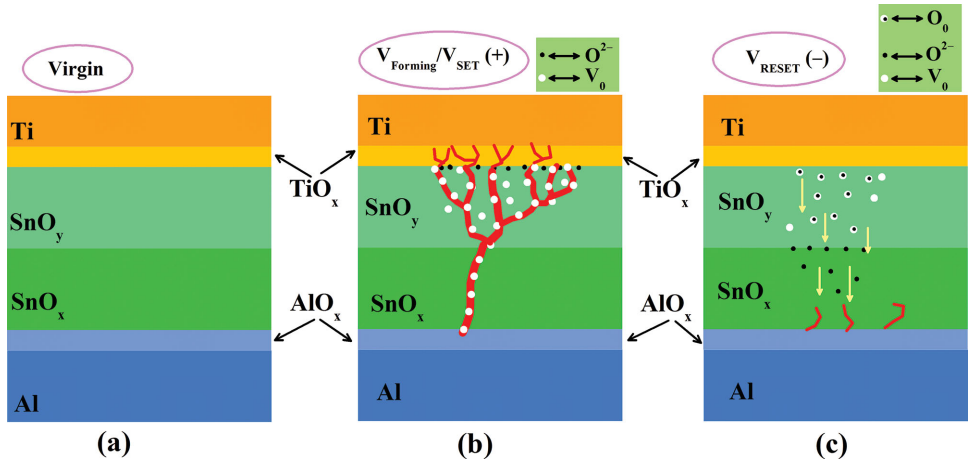

Figure 8. Schematic representation of the resistive switching process, showing the device under a) virgin state, b) SET, and c) RESET conditions. Migration of oxygen ions is assumed to be the origin of the resistive swithcing in this nanoscaled devices.

effect,[38] resulting in no interaction between V_O and O^{2-}. During this process when the density of V_O reaches a critical value, the CF forms by accumulating negative carriers. Since the interfacial layer (possibly TiO_x) between Ti and SnO_y (as confirmed from the EELS study) is very leaky (almost conducting), it will not prevent the charge carrier flow through it, and rather a secondary conducting path will form through it, which will keep the device in LRS. In this process, a partial oxidation of Ti electrode is expected after absorbing O^{2-}, resulting in an increment of TiO_x layer. This will enhance the V_O generation process. As soon as, the conducting paths or so called conducting filaments come into contact with top electrode the resistive state of the device dramatically changes, as the electrons now move freely through these channels like in metallic wires. In this condition, the memory device would have achieved its LRS or ON state.

On the other hand, when bias voltage reaches RESET condition (V_{RESET}), electrons occupied V_O near the cathode (i.e., top electrode) starts forming V_O^{2+} ($V_O - e = V_O^{2+}$) via detrapping mechanism of electrons, causing a significant increase of capture cross section for O^{2-}. Subsequently, V_O annihilation occurs when an electron depleted V_O^{2+} recombines with O^{2-} ($V_O^{2+} + O^{2-} = O_0$) and produces neutral oxygen ions (O_0). The nonrecombined O^{2-} ions from the $Ti/TiO_x/SnO_y$ interfaces and from the SnO_y layer will then move towards the bottom electrode through SnO_x/SnO_y interface. These will cause the rupture process of the CFs. Since, SnO_x layer is acting as oxygen reservoir, O^{2-} will be absorbed in the SnO_x/SnO_y interface and SnO_x layer. In this condition, the interface between bottom electrode and SnO_x may also play a significant role. As observed in the EELS study, an interfacial layer, possibly AlO_x, is formed at Al/SnO_x interface during the fabrication process. This layer can partially restrict the charge carrier flow, which leads to the lowering of the current in HRS (Figure 8c). Finally, the device returns to its fresh-like HRS condition when sufficient V_O annihilation takes place to "switch OFF" the remaining conducing path.

Moreover, it has been observed from the *I–V* characteristics that the transition from LRS to HRS is not abrupt and involves multiple steps. These successive RESET process can be explained by considering a CF with its several branches or existing of "tiny filaments."[39] It has been reported that the temperature along the CFs is nonuniform and filament dissolution starts in the hottest point of the CFs,[40] which leads to the local shrinking of CFs cross-section resulting in increment of current crowding and Joule heating effect. Finally a self-accelerated CFs rupture occurs. The different branches of a single CF may rupture in different time, causing the stepwise decreasing in the current during RESET process. Hence, the breakdown of one or more filaments (it can be consider as the partial rupture of a single CF) produces partial RESET processes characterized by the multiple current steps that lead to *I–V* curves in negative polarity side (see Figure 4c).

3. Conclusion

In conclusion, bipolar resistive switching behavior has been observed in bilayer p-type SnO thin films in nanoscale cross-point (300×300 nm^2) device architecture. By using a bilayer instead of single-layer SnO films, a satisfactory memory performance was observed with ON/OFF ratio of 10^3 times, more than 10^3 s retention time, stable DC switching cycling, and low voltage operation. It has been observed that multiple charge transport mechanisms exist in both LRS and HRS condition of the device, depending on the bias condition. The origin of the resistive switching in this previously unreported device structure is proposed to be the migration of oxygen ions along with successive Joule heating effect in different conducting filaments.

4. Experimental Section

The devices studied in this work were arranged in a nano cross-point (300×300 nm^2) structure fabricated on 400 nm SiO_2/Si substrates. The device fabrication process is schematically illustrated in Figure S1a–d, Supporting Information. Al bottom electrodes with thicknesses of 40 nm were deposited by thermal evaporation on SiO_2/Si substrates. Before the deposition of Al bottom electrode, 10 nm Ti buffer adhesive layers were prepared by e-beam evaporation system. For resistive switching layer, a bilayer of oxygen rich (deposited with 17% oxygen partial pressure, O_{pp}) and oxygen deficient (deposited with 5% O_{pp}) SnO layers were deposited by reactive DC sputtering from a 99.99% pure Sn target. The oxygen rich and deficient layers are denoted as SnO_x and SnO_y, respectively, in this work. Finally, Ti (10 nm)/Au (40 nm) was deposited as top electrode from e-beam evaporation system. The patterns for the bottom electrode, oxides layers and top electrodes were performed using a CRESTEC CABL-9520C high-resolution electron beam lithography system (details are given in the Supporting Information). The thicknesses of different films were measured by a surface profilometer (Veeco Decktak 150). The total thickness of the SnO bilayer was measured 20 nm. An FEI nova nano-SEM was used to analyze the device dimensions. The cross section, EELS, and EDS analysis of the device were performed using a FEI Titan ST TEM. The chemical composition and the structural analysis of two different oxide films were performed using XPS and Raman spectroscopy (Horiba aramis UV spectrometer). XPS studies were carried out in a Kratos Axis Ultra DLD spectrometer equipped with a monochromatic Al K_α X-ray source ($h_\nu = 1486.6$ eV) operating at 150 W, a multichannel plate and delay line detector under a vacuum of $1–10^{-9}$ mbar. The data were analyzed with commercially available software, CASA XPS. The c-AFM study was carried out using Asylum Research (model: MFP-3D) atomic force microscope operated at room temperature, atmospheric pressure, and using Pt-Ir coated tips. Before the c-AFM scanning, the device under test was activated (electroforing) using an external semiconductor parameter analyzer (Keithley 4200). The conventional electrical properties were measured using Keithley 4200 semiconductor parameter analyzer in combination with a semiautomatic probe station from Cascade microtech in voltage sweeping mode at room temperature. All of the operating voltages were applied on the top electrode (Ti/Au), while the Al, bottom electrode was grounded.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

Research reported in this publication was supported by King Abdullah University of Science and Technology (KAUST).

Received: November 26, 2014
Revised: January 18, 2015
Published online: February 23, 2015

[1] R. Waser, M. Aono, *Nat. Mater.* **2007**, *6*, 833.
[2] S. Dietrich, M. Angerbauer, M. Ivanov, D. Gogl, H. Hoenigschmid, M. Kund, C. Liaw, M. Markert, R. Symanczyk, L. Altimime, S. Bournat, G. Mueller, *IEEE J. Solid-State Circuits* **2007**, *42*, 839.
[3] K. Aratani, K. Ohba, T. Mizugushi, S. Yasuda, T. Shiimoto, T. Tsushima, T. Stone, K. Endo, A. Kouchiyama, S. Sasaki, A. Maeska, N. Yamada, H. Narisawa, *Proc. IEDM* **2007**, 783.
[4] A. Prakash, D. Jana, S. Samanta, S. Maikap, *Nanoscale Res. Lett.* **2013**, *8*, 527.
[5] G. Wang, A. C. Lauchner, J. Lin, D. Natelson, K. V. Palem, J. M. Tour, *Adv. Mater.* **2013**, *25*, 4789.
[6] W. Y. Park, G. H. Kim, J. Y. Seok, K. M. Kim, S. J. Song, M. H. Lee, C. S. Hwang, *Nanotechnology* **2010**, *21*, 195201.
[7] C. Y. Liu, J. J. Huang, C. H. Lai, C. H. Lin, *Nanoscale Res. Lett.* **2013**, *8*, 156.
[8] Y. Wu, S. Yu, B. Lee, P. Wong, *J. Appl. Phys.* **2011**, *110*, 094104.
[9] S. Long, L. Perniola, C. Cagli, J. Buckley, X. Lian, E. Miranda, F. Pan, M. Liu, M, J. Suńé, *Sci. Rep.* **2013**, *3*, 2929.
[10] M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, I. K. Yoo, K. Kim, *Nat. Mater.* **2011**, *10*, 625.
[11] S. Kim, K. P. Biju, M. Jo, S. Jung, J. Park, J. Lee, W. Lee, J. Shin, S. Park, H. Hwang, *IEEE Electron Device Lett.* **2011**, *32*, 671.
[12] H. Y. Peng, G. P. Li, J. Y. Ye, Z. P. Wei, Z. Zhang, D. D. Wang, G. Z. Xing, T. Wu, *Appl. Phys. Lett.* **2010**, *96*, 192113.
[13] Q. Liu, S. Long, W. Wang, Q. Zuo, S. Zhang, J. Chen, M. Liu, *IEEE Electron Device Lett.* **2009**, *30*, 1335.
[14] X. Sun, G. Li, L. Chen, Z. Shi, W. Zhang, *Nanoscale Res. Lett.* **2011**, *6*, 599.
[15] A. Sawa, *Mater. Today* **2008**, *11*, 28.
[16] D. C. Kim, S. Seo, S. E. Ahn, D. S. Suh, M. J. Lee, B. H. Park, I. K. Yoo, I. G. Baek, H. J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U. I. Chung, J. T. Moon, B. I. Ryu, *Appl. Phys. Lett.* **2006**, *88*, 202102.
[17] A. Chen, S. Haddad, Y. C. Wu, Z. Lan, T. N. Fang, S. Kaza, *Appl. Phys. Lett.* **2007**, *91*, 123517.
[18] A. Younis, D. Chu, X. Lin, J. Lee, S. Li, *Nanoscale Res. Lett.* **2013**, *8*, 1.
[19] L. Zhang, H. Y. Xu, Z. Q. Wang, H. Yu, X. N. Zhao, J. G. Ma, Y. C. Liu, *Appl. Phys. Lett.* **2014**, *104*, 093512.
[20] M. K. Hota, J. A. Caraveo-Frescas, M. A. McLachlan, H. N. Alshareef, *Appl. Phys. Lett.* **2014**, *104*, 152104.
[21] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlogl, H. N. Alshareef, *ACS Nano* **2013**, *7*, 5160.
[22] M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U.-I. Chung, I.-K. Yoo, K. Kim, *Nat. Mater.* **2011**, *10*, 625.
[23] M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. Chung, I. K. Yoo, K. Kim, *Nat. Mater.* **2011**, *10*, 625.
[24] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat. Nanotechnol.* **2008**, *3*, 429.
[25] L. Kövér, Z. Kovjcs, R. Sanjinés, G. Moretti, I. Cserny, G. Margaritondo, J. Pjlinkjs, H. Adachi, *Surf. Interface Anal.* **1995**, *23*, 461.
[26] P. Hanys, P. Janecek, V. Matolin, G. Korotcenkov, V. Nehasil, *Surf. Sci.* **2006**, *600*, 4233.
[27] J. Geurts, S. Rau, W. Richter, F. J. Schmitte, *Thin Solid Films* **1984**, *121*, 217.
[28] H. Luo, L. Y. Liang, H. Tao Cao, Z. M. Liu, F. Zhuge, *ACS Appl. Mater. Interfaces* **2012**, *4*, 5673.
[29] A. Prakash, D. Jana, S. Samanta, S. Maikap, *Nanoscale Res. Lett.* **2013**, *8*, 527.
[30] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[31] S. H. Jo, W. Lu, *Nano Lett.* **2008**, *8*, 392.
[32] Q. Y. Zuo, S. B. Long, Q. Liu, S. Zhang, Q. Wang, Y. T. Li, Y. Wang, M. Liu, *J. Appl. Phys.* **2009**, *106*, 073724.
[33] P. C. Joshi, S. B. Krupanidhi, *J. Appl. Phys.* **1993**, *73*, 7627.
[34] Y. J. Fu, F. J. Xia, Y. L. Jia, C. J. Jia, J. Y. Li, X. H. Dai, G. S. Fu, B. Y. Zhu, B. T. Liu, *Appl. Phys. Lett.* **2014**, *104*, 223505.
[35] Z. Chiguvare, V. Dyakonov, *Phys. Rev. B* **2004**, *70*, 235207.
[36] Y. Yang, P. Gao, S. Gaba, T. Chang, X. Pan, W. Lu, *Nat. Commun.* **2012**, *3*, 732.
[37] A. Togo, F. Oba, I. Tanaka, K. Tatsumi, *Phys. Rev. B* **2006**, *74*, 195128.
[38] R. L. David, *CRC Handbook of Chemistry and Physics*, 77th ed., CRC, Boca Raton **1996**.
[39] M. A. Villena, F. Jimenez-Molinos, J. B. Roldan, J. Sune, S. Long, X. Lian, F. Gamiz, M. Liu, *J. Appl. Phys.* **2013**, *114*, 144505.
[40] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, *IEEE Trans. Electron Devices* **2009**, *56*, 193.