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Barrier and seed layer coverage in 3D structures with different aspect ratios using sputtering and ALD processes

O. Lühn [a,b,*], C. Van Hoof [a,c], W. Ruythooren [a], J.-P. Celis [b,1]

[a] Interuniversity Microelectronics Center (IMEC), Kapeldreef 75, 3001 Leuven, Belgium
[b] Katholieke Universiteit Leuven, Department of MTM, Kasteelpark Arenberg 44, 3001 Leuven, Belgium
[c] Katholieke Universiteit Leuven, Department of ESAT, Kasteelpark Arenberg 10, 3001 Leuven, Belgium

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ABSTRACT

Established technologies for the deposition of barrier layers and seed layers for 3D interconnect technology were investigated for their limits of obtaining a continuous and conductive layer in 3D structures. Sputtering, and sputtering coupled with a self-ionized plasma as well as atomic layer deposition, in combination with direct-on-barrier electroplating were used. The diameter of the investigated vias and trenches was scaled from 100 to 5 μm with depths down to 360 μm, covering a large range of aspect ratio up to 29. The deposition technologies were investigated and evaluated by analyzing cross-sections of coated vias with optical microscopy, scanning electron microscopy, and focused ion beam. An aspect ratio technology map is presented that shows the limits of the investigated coating technologies to achieve a continuous conductive surface layer on the wall and bottom of vias and trenches of various aspect ratios. Vias and trenches were successfully coated with a continuous barrier and a copper seed offering electrical continuity for aspect ratios up to 29.

1. Introduction

The semiconductor industry focuses on small, light portable devices (cellular phones, PDAs, digital cameras) with high performance and high amounts of features. By consequence, a continuous improvement of the manufacturing technology for consumer electronics is required. Innovative 3D packaging concepts were introduced [1]. Three-dimensional (3D) chip stacking allows high density and direct stacking of thinned IC-s. The major motivation for using this interconnect technology is to provide shortest length and highest density connections (up to 10^6 cm^{-2}) [2]. 3D interconnects give rise to a reduced signal delay, a reduced power consumption and a reduced system size [3]. The interconnection of such 3D systems is achieved by Through-Silicon-Vias (TSV) that are filled with electrodeposited copper [4,5].

The future trend aims to thinned wafers in the range of 25–100 μm while the diameters of the vias will decrease down to a few microns, so that increased aspect ratios (a.r.) will be achieved. In our applications [6], vias are 1–50 μm in diameter and up to 100 μm deep. As the diameter of vias filled with electroplated copper for 3D integration decreases and the aspect ratio increases, the deposition of the requisite barrier and seed layers becomes one of the critical steps in copper interconnect fabrication, apart from filling these vias subsequently with copper by electrodeposition.

The filling of vias with electroplated copper with high aspect ratios up to 15 has been reported recently [7,8], but details on barrier and seed layer deposition processes are not clearly addressed up to now.

Dry etching techniques in silicon for the realization of tapered and vertical through the wafer vias with high aspect ratios was recently reported by us [9]. In the present study, barrier layer and copper seed layer were deposited in the earlier obtained 3D structures with diameter varying from 5 to 100 μm range and high aspect ratio up to 29 (360 μm depth at maximum).

As barrier layers, WCN and TiN were deposited by atomic layer deposition (ALD), Ti was deposited by sputtering, Ta by sputtering coupled with a self-ionized plasma (SIP), while nickel was electrodeposited (ECD). The copper seed layer was deposited by sputtering, sputtering with SIP as well as by direct-on-barrier (DOB) electrodeposition.

The objective of this study is to achieve 3D structures in silicon with high aspect ratios of which walls and bottom are coated with a dense and continuous barrier layer with a copper seed layer on top. That is a prerequisite for the subsequent filling of the 3D structures with electrodeposited copper.

* Corresponding author. Address: Interuniversity Microelectronics Center (IMEC), Kapeldreef 75, 3001 Leuven, Belgium. Tel.: +32 16 281195; fax: +31 16 281097.
E-mail address: Luhno@imec.be (O. Lühn).
[1] ISE member.

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2. Experimental

Vertical high aspect ratio vias and trenches with different diameter/width ranges from 5 to 100 μm and depths down to 360 μm were realized using the Bosch Deep Reactive Ion Etching (DRIE) technique [9]. The vias were etched on 200 mm diameter silicon wafers in a multiplexed ICP equipment (AdixenAMS 100 SE). After etching of the structures in silicon, the deposition of barrier and seed layers was done according to four different processing routes described in Table 1.

Barrier and seed layers consisting of 100 nm thick titanium and 300 nm thick copper (nominal value at wafer surface) respectively (process 1) were deposited by sputtering on top of each other (NEXX Nimbus 310). Barrier and seed layers consisting of 80 nm thick tantalum and 300 nm thick copper (nominal value on wafer surface) respectively were deposited by sputtering on top of each other (Applied Endura CuBS (Cu Barrier/Seed) PVD (Physical Vapor Deposition) with the SIP EnCoRe™ process (process 2). The atomic layer deposition for the barrier layers (process 3, 4) was provided by ASM Microchemistry Ltd. following processes described in [10,11].

A schematic of the deposited layer stack of the barrier layer and the copper seed layer into vias etched into silicon is shown in Fig. 1. Note, that in process 4, two barrier layers were used, namely a WCN layer deposited on silicon and a nickel layer deposited on top of that WCN layer.

2.1. Evaluation procedure for process 1 and process 2

A simplified procedure for testing the coverage of barrier and seed layer was elaborated and is shown in Fig. 2.

The wafer was diced after deposition of the barrier and seed layers (step 2b) into samples of $2 \times 2\ cm^2$. The sample was cleaved (step 2c) leading also to cleaved vias through their axis located on the cleaved edge of the sample. These samples were wetted with water containing a surfactant (polyethylene glycol; PEG; Sigma–Aldrich) and were subsequently degassed under reduced pressure to ensure a good wetting of the structures. Then, the samples were polarized in a three electrode cell filled with an electrolyte containing 0.2 M $CuSO_4 \cdot 5H_2O$ and 0.5 M H_2SO_4, and additives (NaCl, Sigma–Aldrich; SPS (bis(3-sulfopropyl) disulfide, Rasching); PEG) to enhance the copper seed layer (step 2d). A current density of 20 mA cm^{-2} (based on the face area) was applied during 450–600 s. After electrodeposition of copper onto the seed layer, the sample was rinsed with water and investigated with optical microscopy (OM) or scanning electron microscopy (SEM) (step 2e). This simplified method eliminates air entrapment that might take place in a regular via filling procedure and allows a fast detection of any discontinuity in the seed layer along the walls and bottom of the 3D structures.

2.2. Evaluation procedure of process 3

After deposition of TiN by ALD on a blanket wafer, the resistivity was measured. The deposition of TiN by ALD in patterned wafers was followed by dicing into samples of $2 \times 2\ cm^2$ which then were mounted on a rotating disk electrode (RDE). The oxide on TiN was removed by dipping the sample in 1 vol.%. HF for 2 min under reduced pressure to remove air from the vias. The RDE was then transferred into a plating cell. Copper was electrodeposited directly on TiN [12] at 3.1 mA cm^{-2} (based on face area) during 500 s. The rotation speed was 400 rpm. The sample was cleaved and cross-sections were investigated with SEM.

Table 1
Overview of technologies for barrier and seed layer deposition

Process	Barrier layer	Seed layer
#1	100 nm titanium (sputtered)	300 nm copper (sputtered)
#2	80 nm tantalum (sputtered + SIP)	300 nm copper (sputtered + SIP)
#3	18 nm TiN (ALD)	70–700 nm copper (DOB)
#4	40 nm WCN (ALD) & ~200 nm nickel (ECD)	~250 nm copper (DOB)

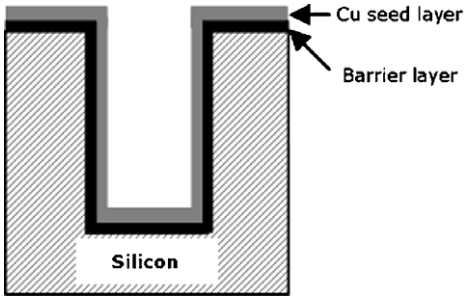

Fig. 1. Schematic of via in silicon with coated barrier layer and copper seed layer.

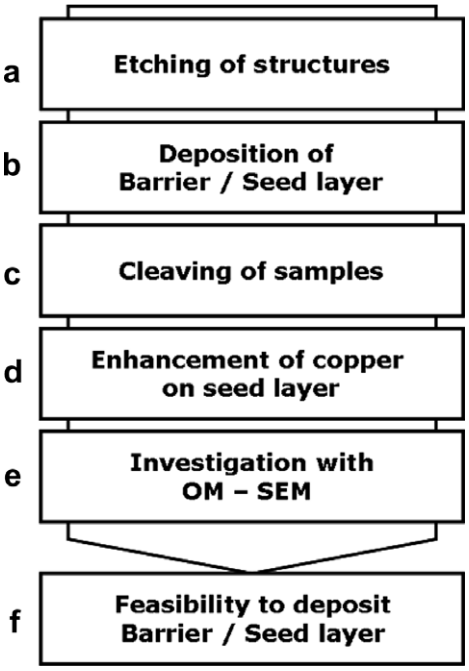

Fig. 2. Characterization procedure of barrier and seed layer deposited in 3D structures.

2.3. Evaluation procedure of process 4

The evaluation of WCN barrier layers deposited by ALD, on which subsequently an electrodeposited nickel layer was deposited as well as an electrodeposited copper seed layer by direct-on-barrier electrodeposition, was done as follows. After deposition of the barrier layer by ALD, the resistivity was measured on a blanket wafer. For WCN deposited by ALD, an XPS analysis was done to confirm the composition of WCN. Patterned wafers were diced into $2 \times 2\ cm^2$ samples. These samples were cleaved and the conformality of the barrier layer was investigated with SEM.

The samples were immersed in a solution of 3 vol.%. NH_4OH under reduced pressure for 2 min in order to remove surface contaminants or oxides. After cleaning, the sample was mounted on a RDE and placed directly in a three electrode cell filled with a nickel electrolyte containing 0.165 M $NiSO_4 \cdot 6H_2O$, 0.25 M sodium citrate dehydrate, at pH 6.9, to deposit nickel directly on WCN. The RDE

was then rinsed with water and directly transferred in a second three-electrode cell filled with a copper sulphate based electrolyte containing 0.2 M $CuSO_4 \cdot 5H_2O$ and 0.5 M H_2SO_4. Copper was electrodeposited on nickel during 250 s at ~15 mA cm^{-2} (based on face area). The copper seed layer was thickened up to a few micrometers by electrodeposition from a copper bath containing 0.8 M $CuSO_4 \cdot 5H_2O$, 0.7 M H_2SO_4 and additives (PEG; NaCl; SPS; Janus Green B (JGB, Sigma–Aldrich)). The sample was then embedded in epoxy resin. Cross-sections of the features were obtained by grinding down to the centre of via/trenches and subsequently polishing. Pictures were taken by optical microscopy. Cross-sections of the structures were also obtained by focused ion beam (FIB) and analyzed by SEM.

3. Results

3.1. Process 1

Cross-sections of cleaved vias coated with an additional electrolytic copper layer a few micrometers thick, are shown in Fig. 3. The bright layer shows the continuous copper layer, the dark layer is due to the imaging mode of the optical microscope.

The via with a diameter of 50 μm and a depth of 92 μm (a.r. = 1.84) was coated successfully displaying a continuous copper layer (Fig. 3a). The 40 μm via with a depth of 140 μm (a.r. = 3.5) displayed a discontinuous coated copper layer down to a depth of ~94 μm (Fig. 3b). Vias with diameters ranging from 5 μm to 100 μm and depths up to 360 μm, and thus having different aspect ratios, were also investigated. The applied sputter process appeared to be successful to achieve a continuous and conductive copper layer in the diameter/depth combinations investigated here up to a maximum aspect ratio of ~2.5 for vias. For trenches, the aspect ratio that can be covered successful is slightly higher to aspect ratios up to 3.5.

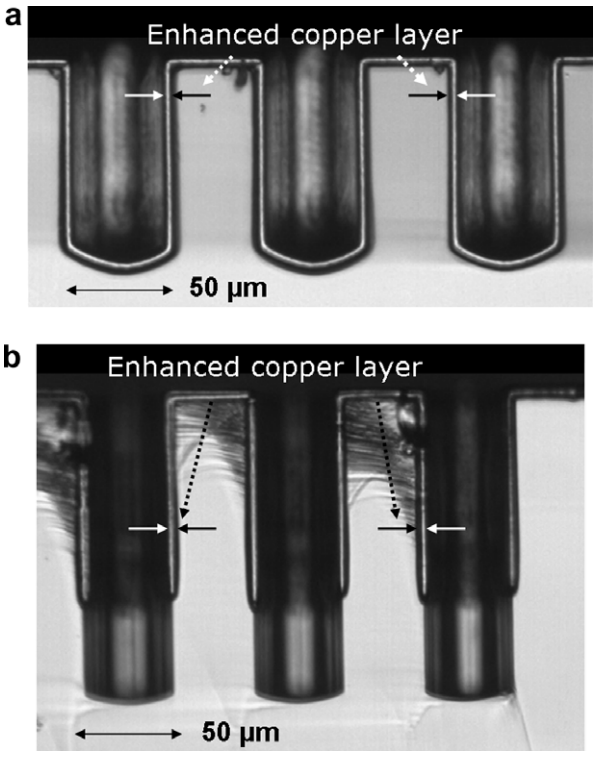

Fig. 3. Cross sections of (a) a 50 μm diameter via successfully coated with a continuous copper layer and (b) a 40 μm diameter via showing a discontinuous coated copper layer layer (process 1).

3.2. Process 2

An example of a continuous barrier and seed layer is shown after thickening up with electrodeposited copper in Fig. 4. The right via has a diameter of 30 μm and a depth of 140 μm. The left via has a diameter of 40 μm and a depth of 150 μm. The insets (4a, 4b, 4c) show that the coated layer is continuous down to and at the bottom of via.

The used sputter deposition process (with SIP) of 80 nm thick tantalum and 300 thick copper resulted in a continuous barrier layer and seed layer on the wall and bottom of vias with 5–100 μm in diameter, up to an aspect ratios of ~7.5 at maximum. That process can be successful applied to trenches with aspect ratios up to ~9.5.

3.3. Process 3

The resistivity measured on a flat wafer was ~200 μΩ cm for a 18 nm thick TiN layer. The results of direct-on-barrier copper electrodeposition on TiN are shown in Fig. 5. Here, the inserts show the top left corner (Fig. 5a), the side wall at half depth (Fig. 5b), and the lower left bottom (Fig. 5c) of a via 40 μm in diameter and 150 μm in depth. In Fig. 4 a cross-section of a 40 μm via with the same dimensions is shown and can be compared.

The seed layer process results in a continuous copper layer. At the top of the via, the copper layer is around 700 nm thick, at the centre around 410 nm thick, and at the bottom around 70 nm thick. The conformality and the adhesion are poor. The adhesion was checked by scotch tape test.

According to literature [13], a copper seed layer can be deposited on TiN by using electrografting of copper which is an electrochemical deposition technique. That process results in the growth of continuous copper seed layers on conducting surfaces with a good adhesion and this in vias of aspect ratios up to 32.

3.4. Process 4

The resistivity of WCN barrier layers deposited by ALD on blanket wafers was determined. The resistivity was ~340 μΩ cm for a 25 nm thick WCN layer. The composition of the deposited WCN barrier layer determined by XPS was $W_{62}C_{24}N_{14}$. The conformality of the deposited WCN by ALD was investigated by SEM and showed that a 40 nm thick WCN was deposited on the top surface, on the sidewall and at the bottom of the 3D structures.

The deposition sequence (process 4) consisting of WCN deposited by ALD followed by electrolytic Ni and direct-on-barrier copper was successful for vias over a large range of aspect ratio. The deposited layer stack passed the scotch-tape test. Polished cross-sections of trenches with diameters varying from 20 to 100 μm and aspect ratios from 3.5 to 12.5 with depths up to 360 μm are shown in Fig. 6 after the subsequent thickening of the copper seed layer with electrodeposited copper up to a few micrometers.

The electrolytic copper layer deposited on top of the copper seed layer is continuous down to the bottom of vias with aspect ratios up to 12.5 (Fig. 6).

This process results thus in continuous and conductive seed layers in 3D structures of aspect ratios up to 29 for trenches. Higher aspect ratios were not investigated in this study.

4. Discussion

The applicability of the investigated technologies for the deposition of barrier and seed layers in 3D structures etched in silicon, is summarized in Fig. 7 as an aspect ratio technology map.

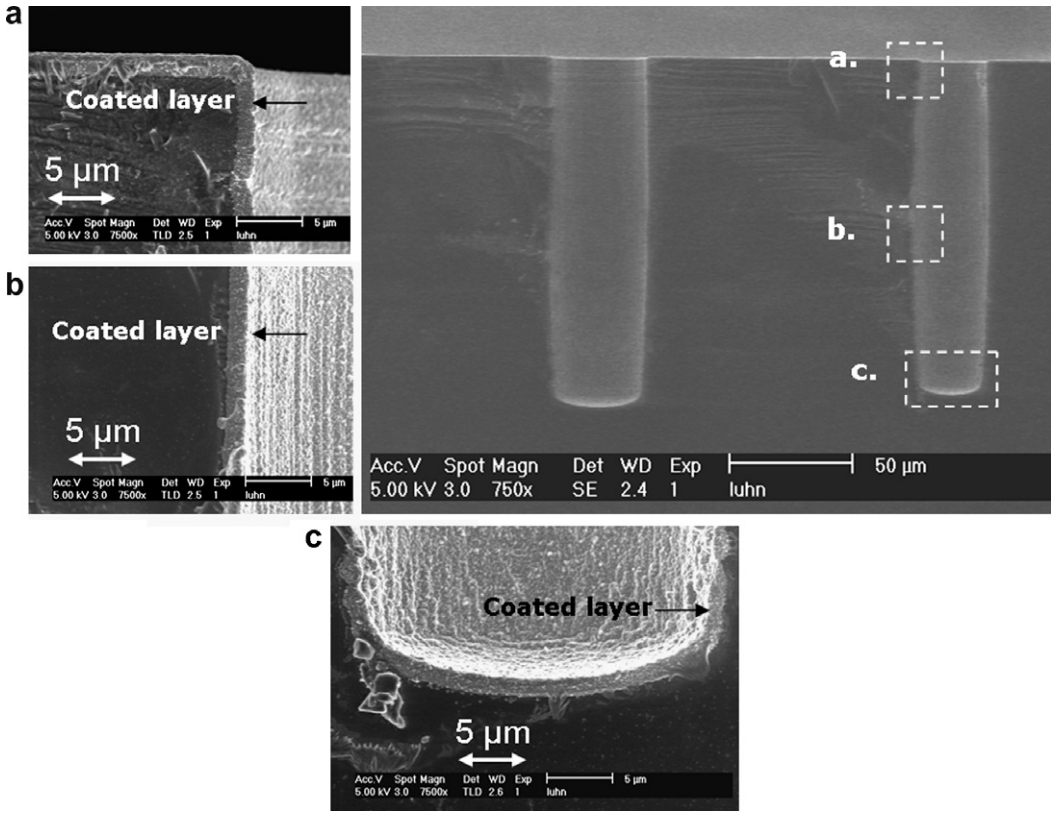

Fig. 4. Vias with (barrier and) coated seed layer deposited by sputtering with SIP (process 2) after performing the characterization procedure (steps 2a to 2e in Fig. 2).

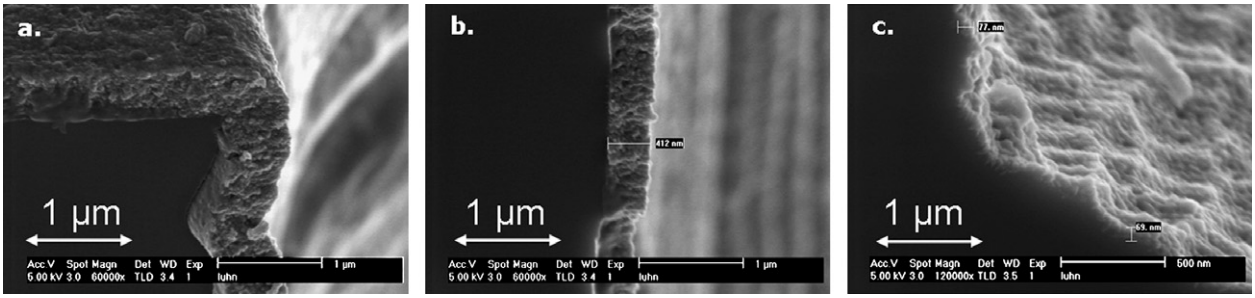

Fig. 5. Appearance of copper electrodeposited directly on ALD-TiN (process 3) in a 40 µm diameter via with a depth of 150 µm at different positions along the via: (a) at top corner, (b) at the sidewall at half depth, and (c) at lower left bottom.

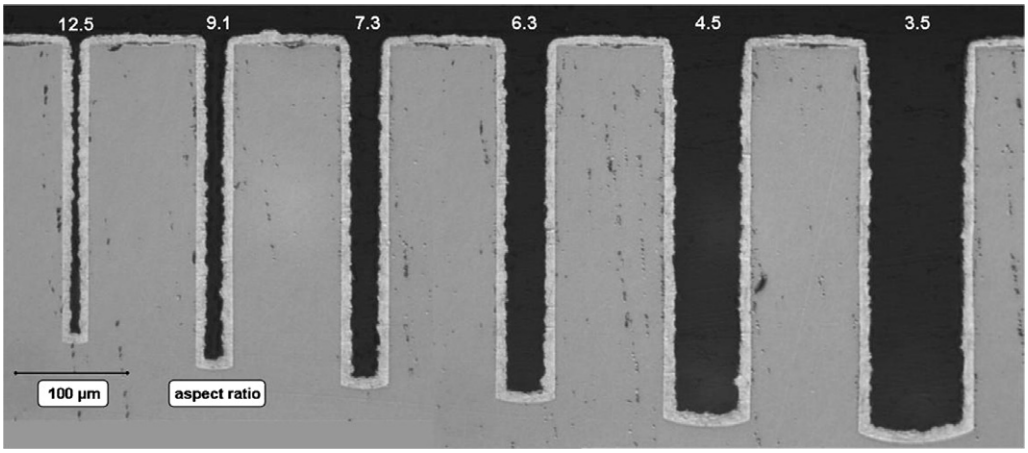

Fig. 6. Trenches in silicon with wide aspect ratio range coated with an electrodeposited copper layer using process 4 (see Table 1).

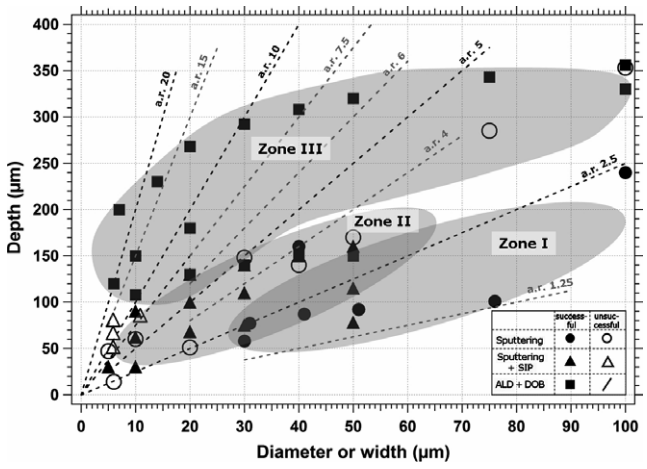

Fig. 7. Aspect ratio technology map showing applicability and limits of sputtering (Zone I; dots), sputtering with SIP (Zone II; triangles), and atomic layer deposition (ALD) with direct-on-barrier (DOB) (Zone III; squares) for barrier and seed deposition in structures etched in silicon. Closed symbols show successful process, open symbols show unsuccessful process.

This map shows clearly the limits of sputtering (a.r. ~2.5) and sputtering with SIP (a.r. ~7.5) for vias. A combination of ALD and DOB appears as suitable to coat walls and bottoms of deep 3D structures with aspect ratios up to 29 (trenches are shown).

For 3D vias with high aspect ratios above 10, ALD with DOB can be used for the deposition process of required barrier and seed layers suitable for a subsequent filling by electrodeposition. For trenches, sputtering (without and with SIP) was successful to an aspect ratio slightly higher than for vias. ALD processes with DOB was not limited for the deposition of barrier and seed layers.

5. Conclusions

The successful coating of deep 3D structures in silicon with a continuous and conductive seed layer depends on the deposition technology used for the growth of the barrier and seed layer. A simple but fast procedure for testing the presence of discontinuities in the barrier and seed layer deposited by sputtering and sputtering coupled with SIP, was proposed and used.

This work showed that 3D vias with diameters from 5 to 100 µm can be successfully coated by sputtering with barrier and seed layers up to a maximum aspect ratio of ~2.5. On the contrary, in the case of sputtering with SIP, a maximum aspect ratio of ~7.5 can be reached for vias. The SIP mode improves the sidewall coverage of structures to higher aspect ratios.

In order to cover vias with an aspect ratio above 7.5 with a barrier and seed layer, a combination of barrier layer deposition by ALD and direct-on-barrier electrodeposited copper was demonstrated to be successful. This combination was efficient to coat vias with diameters from 5 to 100 µm, and depths down to 360 µm; that corresponds to a maximum aspect ratio of 29, which was the maximum available aspect ratio in this study. A mapping of the experimental results obtained in this work is proposed as a useful tool to select the most suitable deposition technology for a given size of vias or trenches to be coated with dense and continuous metallic or ceramic layers.

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