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A 1.4GS/s 9-bit 45 dB power control RFDAC for digital radio transmitters

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Abstract This paper presents a high speed, 9-bit RF Digital-to-Analog Converter based on a new architecture implemented in a 0.13 µm BiCMOS process and able to adjust the output power by 45 dB to meet gain control requirements of the new communications standards with a SFDR >25 dBc. The maximum test-demonstrated frequency is 1.4 GHz and the chip dissipates <25 mW.

Keywords Control gain · Radio-frequency digital-to-analog-converter (RFDAC) · Spurious free dynamic range (SFDR) · Digital transmitter

1 Introduction

This paper presents a 9-bit Digital-to-Analog-Converter (DAC) to be included in a new full-digital transmitter architecture [1]. It should be able to support all the standards and applications that require efficient amplification. This transmitter needs a DAC to drive the power amplifier (PA) and to perform gain control (Fig. 1). The main features of this conversion block are:

- 9-bit resolution, related to the minimum required quantification of a complex multicarrier signal.
- High operating frequency (GHz) to perform the conversion of a transposed RF digitized signal.
- The output is a fully differential signal to drive the power amplifier.
- Simple architecture to meet the speed and cost constraints.
- Very high dynamic range; actually, in the case of standards requiring a gain control (e.g. UMTS), the output power of the radio transmitter can vary in a range of 80 dB. If the PA is supposed to have 35 dB dynamic, the DAC must provide ~45 dB gain control to adjust the transmitter power.

This paper is organized as follows. A first section reviews the basic principles of a DAC and gives details about the chosen conversion principle and the advantages with regards to a classical binary conversion [2–6]. Simulations and measurement performances are discussed in Sect. 3 with a conclusion at last.

2 DAC architecture principle

Among the different implementations (R-2R ladder, switched capacitors, weighted current sources), a conversion structure based on the weighted type has been chosen. The main advantages associated with this current-steering architecture are:

- Easy integration in CMOS process.
- High speed.
- High energetic efficiency.
- Low silicon area.

Among the different methods to implement a weighted DAC (binary weighted, segmented, hybrid), we have chosen an improved binary weighted current source solution which represents the best trade-off between speed, linearity and consumption.

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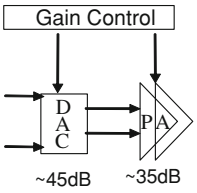

Fig. 1 DAC with gain control

The basic principle of a binary-weighted 9-bit DAC is given by Eq. 1. This classical converter contains nine current sources driven by each of the bits. The sources are designed so that each current is proportional to the bit weight.

$$I_{\mathrm{OUT}} = \sum_{n=0}^{n=8} 2^n.B_n.I_{\mathrm{LSB}} \tag{1}$$

with B_n = bit to convert, I_{LSB} = current corresponding to the least significant bit.

The main drawback of this classical binary structure is the high factor between the most significant bit current and the least-significant bit (256 in a 9bit DAC application). As a consequence, the non-linearity grows and the frequency is limited because of the use of big size transistors for design.

To overcome this, we propose to reduce the size ratios of the transistors by splitting the basic structure in two DACs with smaller sizes, this technique is known as "segmented current-mode DAC" (Fig. 2):

- DAC_1 (4bits): driven by the four least significant bits:

$$I_{\mathrm{OUT1}} = \sum_{n=0}^{n=3} 2^n.B_n.I_{\mathrm{LSB1}} \tag{2}$$

- DAC_2 (5bits): driven by the five most significant bits:

$$I_{\mathrm{OUT2}} = \sum_{m=0}^{m=4} 2^m.B_{m+4}.I_{\mathrm{LSB2}} \tag{3}$$

Assuming the least significant current is: $I_{\mathrm{LSB2}} = 2^4.I_{\mathrm{LSB1}}$

Then, the output current of the second DAC is given by (4):

$$I_{\mathrm{OUT2}} = \sum_{m=0}^{m=4} 2^{m+4}.B_{m+4}.I_{\mathrm{LSB1}} \tag{4}$$

Applying the superposition principle, we get:

$$I_{\mathrm{OUT}} = I_{\mathrm{OUT1}} + I_{\mathrm{OUT2}} = \sum_{n=0}^{n=8} 2^n.B_n.I_{\mathrm{LSB1}} \tag{5}$$

To obtained gain control for the DAC, currents I_{LSB1} and I_{LSB2} were generated from a 45 dB dynamic range variable reference current I_{REF}. To minimize the variation between the current flowing into the two conversion blocks and the transistors size, we choose:

$$I_{\mathrm{LSB1}} = \frac{I_{\mathrm{REF}}}{4} \text{ and } I_{\mathrm{LSB2}} = 4.I_{\mathrm{REF}} \tag{6}$$

instead of

$$I_{\mathrm{LSB1}} = I_{\mathrm{REF}} \text{ and } I_{\mathrm{LSB2}} = 16.I_{\mathrm{REF}} \tag{7}$$

Figure 3 shows the ratio $I_{\mathrm{LSB2}}/I_{\mathrm{LSB1}}$ from Eqs. 6 and 7 versus I_{REF} over 45 dB range.

3 Circuit design

The digital-to-analog converter circuit has been designed using 0.13 µm BiCMOS process from STMicroelectronics.

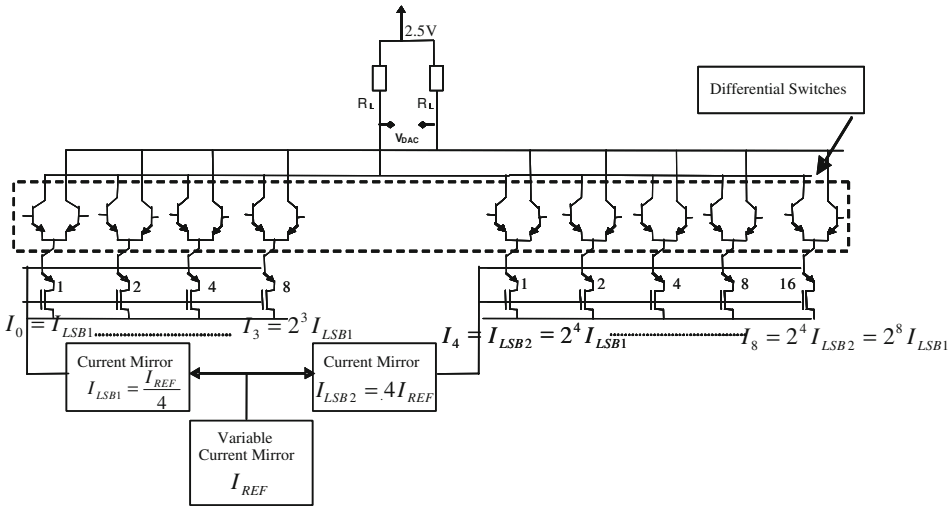

Fig. 2 Proposed architecture for a 9-bit Digital-to-Analog Converter

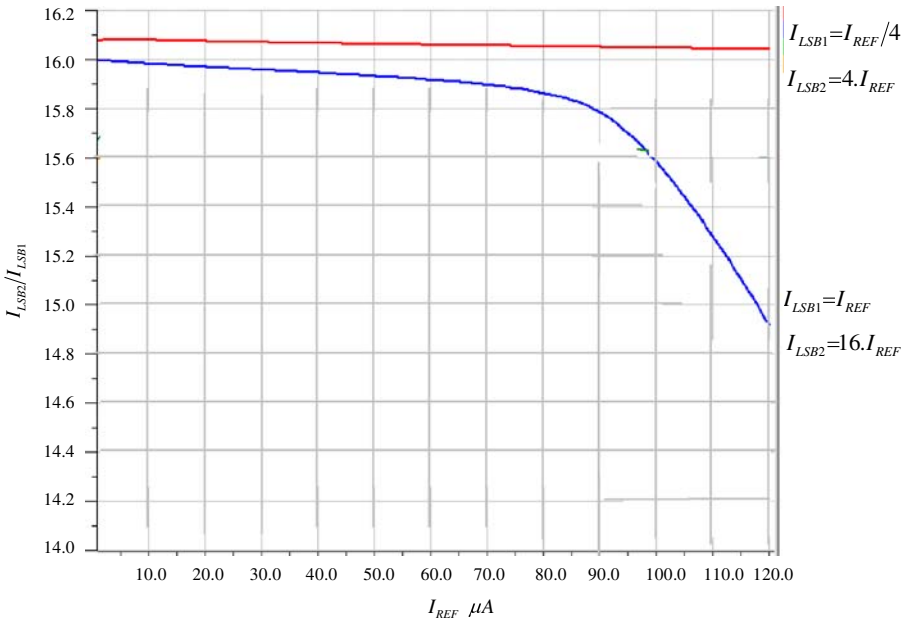

Fig. 3 High dynamic current mirrors performances

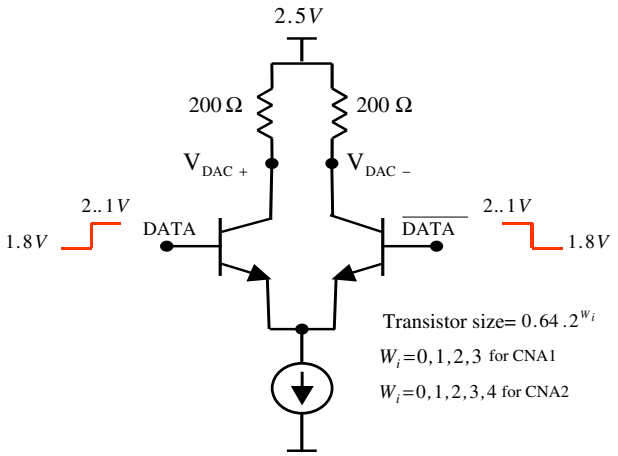

Fig. 4 Bipolar differential switches

To improve speed operation of the switches, we used differential bipolar circuit. Bipolar switches require small voltage difference of the driving signal. As shown in Fig. 4, "0" logic value correspond to 1.8 V and "1" logic value to 2.1 V.

So to interface switches to 1.2 V logic driving signals, we have to use level shifter designed by differentials bipolar circuits as shown in Fig. 5.

Switches and level shifter are differential circuits, so we have to generate complementary signals. This is done by D flip-flop circuits (DFF).

The structure of the DAC is shown Fig. 6.

The RFDAC conversion block has been designed, layout is shown Fig. 7.

To test the speed and the gain control of our circuit over 45 dB, we have designed on the chip a 1.4 GHz 9-bit CMOS ROM-less direct digital frequency synthesizer

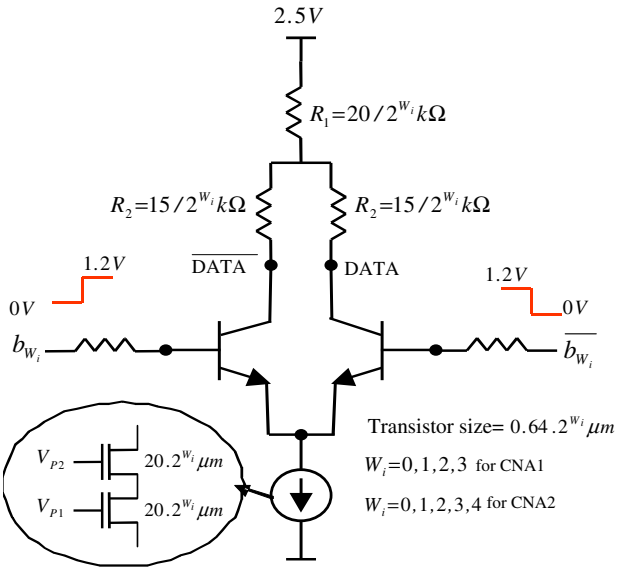

Fig. 5 Interface block level shifter

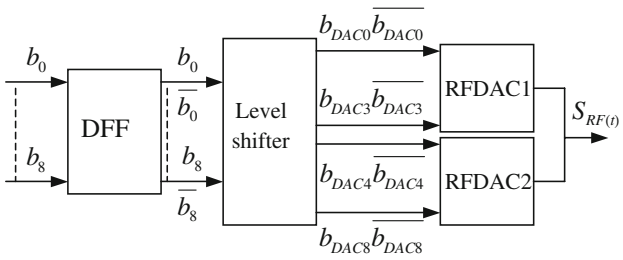

Fig. 6 Structure of the DAC

(DDFS) (Fig. 8). Logic CMOS gates have been used instead of area consuming Rom (sine look-up table) to convert phase word to sine wave amplitude directly [7].

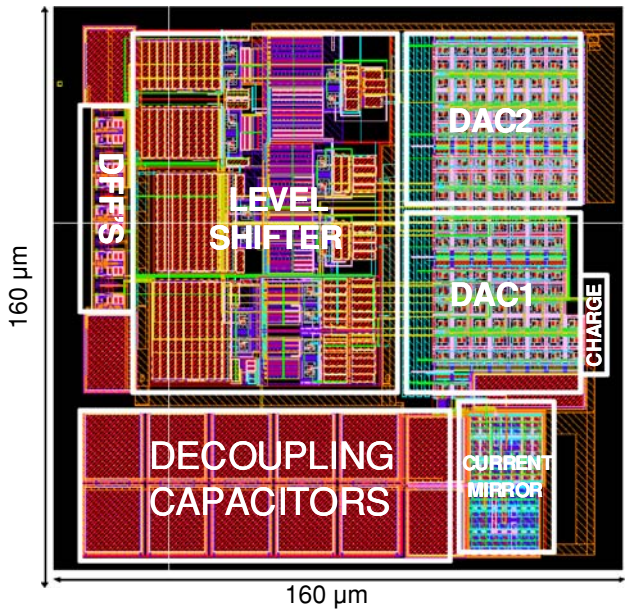

Fig. 7 RF 9-bit DAC (layout)

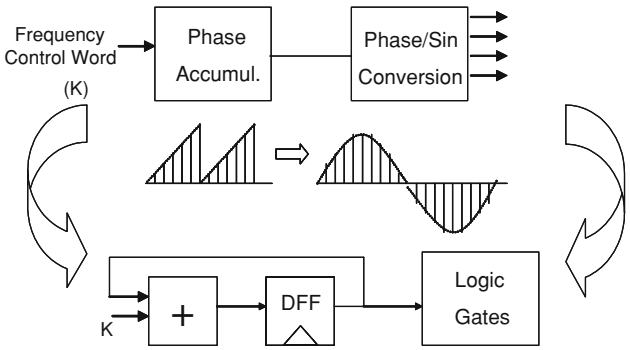

Fig. 8 Block diagram of the DDFS

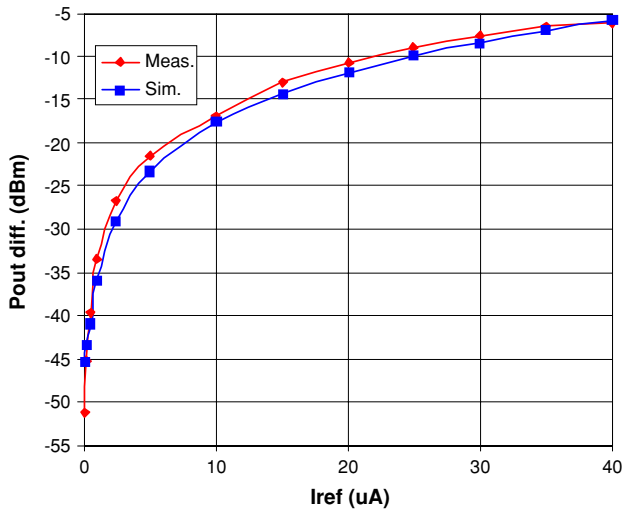

Fig. 9 Single-ended output power @ 100 MHz clock frequency

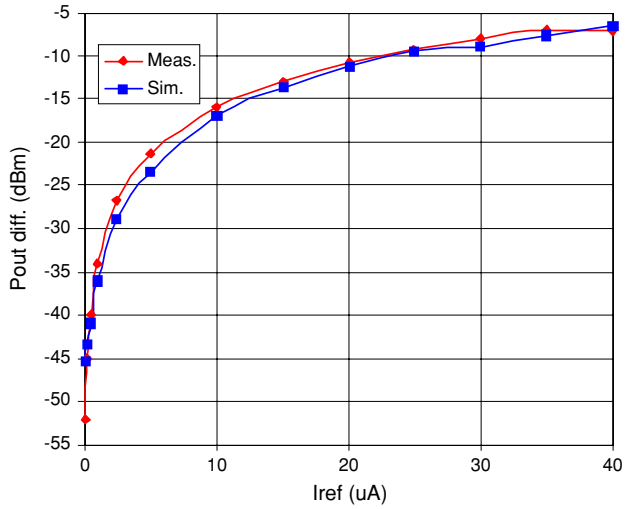

Fig. 10 Single-ended output power @ 1.4 GHz clock frequency

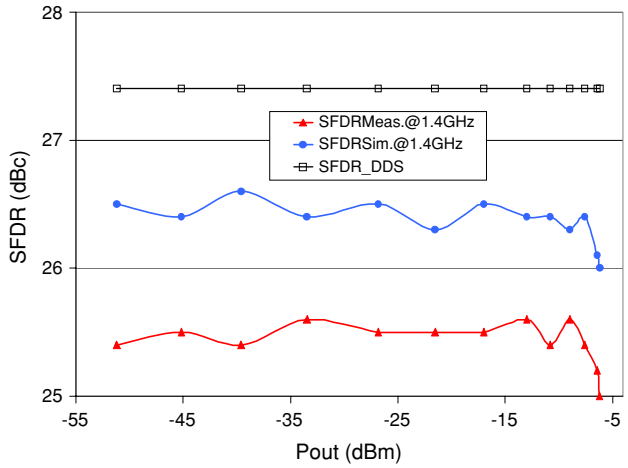

Fig. 11 SFDR @ 1.4 GHz clock frequency

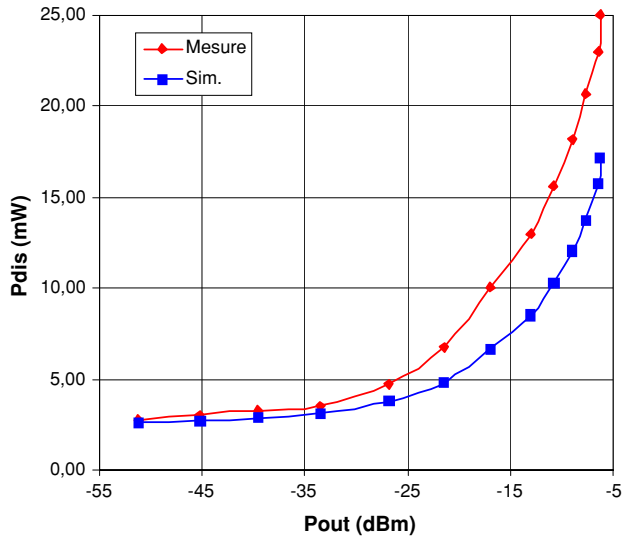

Fig. 12 Dissipated power over output power

Table 1 Summary of DAC performances

Resolution	f_{max}	$Pout_{max}$ (differential)	Power control	SFDR	Power dissipation	Power supply	Technologie.	Die size
9 bit	1.4GS/s	−3 dBm	45 dB	>25 dB	<25 mW	1.2 & 2.5 V	BiCMOS	160 × 160 μm^2

This generator allows measuring the performances of the DAC for a dynamic input. It synthesizes a variable frequency sine signal. SFDR is measured by taking the difference of the main signal tone and next highest tone in a band from DC to Nyquist frequency being the best case SFDR 27 dBc (simulation value). To minimize the effect of the parasitic inductances and resistors of the bounding, 20 pF decoupling capacitors are placed near each supply circuit.

4 Test versus simulation results

Figures 9 and 10 show the single-ended output power measured (50 Ω load) at the minimum frequency (f_{out} = 390 kHz with f_{clk} = 100 MHz) and at the maximum frequency (f_{out} = 10.93 MHz with f_{clk} = 1.4 GHz) synthesized sine waveforms after conversion by the DAC. They are compared to the simulations results obtained by ELDO simulation tool. The results are plotted over gain control (variable reference current Iref).

A SFDR plot over output power clocking at 1.4 GHz is plotted in Fig. 11.

Finally, the dissipated power is plotted over output power in Fig. 12.

Beyond an output power of −6.4 dBm (reference current value of 35 μA), the output power enters the saturation region. The DAC converts the digital input signal adjusting its output power from −51 to −6 dBm (R_L = 50 Ω) which means a power variation of 45 dB with a SFDR >25 dBc.

The circuit has been demonstrated to operate up to 1.4 GHz. This frequency limitation comes from the DDFS chip. This chip can synthesize sine waves at the before mentioned maximum clock frequency so we are not able to provide measured results at higher frequencies.

The circuit dissipates 25 mW for the maximum differential output power of −3 dBm.

5 Summary

We designed a 9-bit RF DAC with a gain control of 45 dB in 0.13 μm BiCMOS technology operating at a demonstrated maximum frequency of 1.4 GHz (limited by the sine wave generator). Over the output power range the DAC shows a SFDR >25 dBc. This chip dissipates <25 mW for a differential output power of −3 dBm (R_L = 50 Ω). The DAC circuit has an area of 160 × 160 μm^2 considering only the DAC block (DFF, level shifters and conversion block) and an area of 160 × 220 μm^2, if the 9-bit Rom-less direct digital frequency synthesizer is considered consuming <2.6 mW at the maximum frequency of 1.4 GHz.

This circuit is suitable for 3G radio transmitters performing a power control of 80 dB (the power amplifier being supposed to control the remaining 35 dB) (Table 1).

This DAC will be integrated in a new digital transmitter architecture employing a 1-bit Sigma-Delta modulator.

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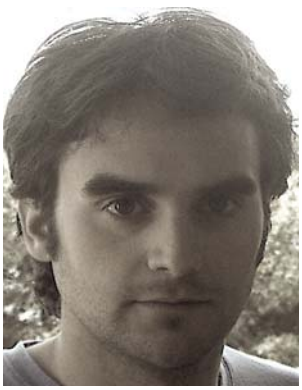

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Jean-Luc Gautier received the Electrical Engineering degree from L'Ecole Nationale Supérieure de l'Electronique et de ses Applications (ENSEA) Cergy, France in 1972, the Docteur en électronique and the Docteur d'état es sciences from the University of Paris-Sud Orsay, France in 1977 and 1987 respectively. Now, he is professor at ENSEA, microwave research laboratory, and his current fields of research are on active microwave circuits, mainly in the area of linear and non linear MMIC design.