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Invited Article

Quantum dots for memory applications

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In this paper, we review the fabrication and the electrical characteristics of metal–insulator–semiconductor (MIS) devices with semiconductor quantum dots (QD) embedded into the gate dielectric. Our results originate from experiments performed the last decade and cover Si QDs realized by low-energy ion-beam synthesis (IBS) as well as GaN QDs formed by molecular beam deposition (MBD). Besides the basic capacitance-to-voltage (*C*–*V*) and current-to-voltage (*I*–*V*) characterization, the memory properties of the fabricated MIS devices were investigated in terms of memory window under pulse operation and charge retention. The optimization of Si-QD memory cells is reviewed and a methodology for both the extraction of various device parameters and the identification of mechanisms governing the charge loss process are presented. GaN QDs, which exhibit negative conduction band-offset with respect to the Si conduction band, offer an interesting alternative to Si QDs as discussed herein based on our investigations of GaN-QD capacitors fabricated by a complementary-metal-oxide-semiconductor (CMOS) compatible process.

1 Introduction For more than two decades there has been increasing interest in the development of semiconductor quantum dots (QDs) in dielectric matrices for electronic and optoelectronic applications. In particular, major efforts have been placed on the realization of the so-called QD (or nanocrystal) memories in an attempt to overcome the scaling issues of conventional flash and primarily for embedded memory applications such as built-in memory arrays for microcontrollers (MCU) and system-on-chip (SoC). It should be noticed that there is a gap between the logic and the memories technology nodes. More specifically, memory technology node lags behind the leading logic technology by about three generations [1]. Embedded non-volatile memories (e-NVM) do not require high storage capabilities. Nevertheless, a technology for e-NVMs should support operation compatibility with the logic circuit transistors, design libraries, CMOS performance and reduced cost. The latest is strongly related to the additional masks and processing steps required in e-NVMs integration. The limitations in the scaling of conventional floating-gate (FG) MOSFET [Ref. [2], see Fig. 1(a)] as the unit memory cell, rise basically from reliability concerns [1]. Following the transistor scaling rules, the equivalent oxide thickness (EOT) of the gate dielectric above the channel (called *injection oxide*) should be smaller than 6–7 nm. In this case, the injection oxide becomes less resistant to defect formation which may cause, under operating conditions of the memory cell, the total loss of charge stored in the FG (made of conductive poly-Si), *i.e.*, the total loss of data. Moreover, for very small EOT the FG charge cannot be retained for a long time due to the quantum mechanical direct tunneling effect. Furthermore, scaling of transistors requires the scaling of the isolation between them in order to increase their density on a wafer. While for logic circuits this requirement can be implemented easily, in the case of FG NVMs the isolation between neighboring cells is not scalable due to significant capacitance coupling between the adjacent FGs which causes serious cross-talk interference [3].

Memory devices with Si-QDs have been demonstrated for the first time by Tiwari et al. [4]. Since then, a huge research effort has been devoted to this technology. According to the original QD-NVM concept [see Fig. 1 (b)], the charges are injected from the channel into the QDs where they are trapped. Utilizing a device with QDs as

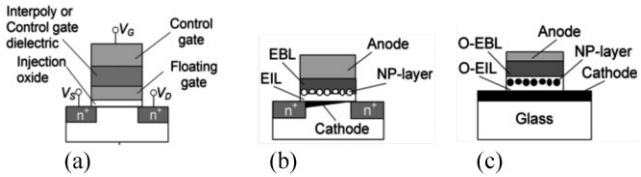

Figure 1 Schematic description of (a) a conventional FG-NVM cell, (b) a QD-NVM cell, and (c) a two-terminal organic bistable memory cell with QDs. The electron injection layer (EIL) and electron blocking layer (EBL) can be the same material.

discrete charge storage nodes it is possible to tackle the FG-NVMs scaling issues. First, the injected charges can be stored in deep traps of the QDs and therefore, their probability to tunnel back to the Si channel by direct tunneling is very low. Second, using an injection oxide thinner than 6–7 nm, a lower electric field is required for charge injection and thus the introduction of oxide defects due to electrical stress is minimized. Finally, the capacitance coupling between nanometer size QDs of adjacent memory cells is almost zero.

The most commonly used techniques to form two-dimensional (2D) arrays of QDs are the chemical vapor deposition (CVD) either at low-pressure (LP) or plasma enhanced (PE), the ion beam synthesis (IBS) and physical vapor deposition (PVD) either by sputtering or electron beam [1]. CVD is a well established technique in CMOS manufacturing and is mainly used to deposit Si-QDs. IBS is used to synthesize Si, Ge, or metal QDs while utilizing PVD mainly metal QDs can be deposited. The formation of QDs utilizing the previous techniques and materials is based on self-assembly mechanisms. For the preparation of QDs by CVD, the nucleation and growth mechanisms can be manipulated separately, thus allowing a good control of the QD's size and density [5]. For IBS, the implanted dose of atoms and their distribution profile inside the dielectric layer in combination with the annealing conditions control the size and the density of the QDs [6]. Finally, to realize metal QDs by PVD, an ultra-thin metallic wetting layer is properly annealed, generally under rapid thermal annealing (RTA) conditions [7]. It should be noticed that recently, Si QDs e-NVMs have been integrated successfully in MCU at 90 nm technology node [8], while preliminary results suggest that their integration at the 45 nm technology node is also functional.

Since the transistor scaling roadmap demands smaller device dimensions, the variability of the QDs distribution should become smaller too raising the serious question of whether the QD-NVM technology can provide reliable devices to technology nodes as short as 45 nm and below. Obviously, to answer this question the fluctuations induced by a self-assembly process should be eliminated, a task which can be fulfilled by developing template-assisted-deposition techniques. Relevant templates can be formed by e-beam lithography (EBL) or using diblock copolymers [9, 10]. Following the latter approach that is more cost effective, functional memory devices have been demonstrated using the PVD technique [10]. It should be noted that other non-CMOS techniques such as the Langmuir–Blodgett deposition technique have also been tested for the ordered formation of functionalized Au-QDs on SiO_2 over a Si channel [11]. Using the latter approach, hybrid devices (Si/organic materials) with very attractive memory characteristics have been demonstrated. Furthermore, the successful combination of QDs with organic materials leads to a new category of two-terminal memory devices as shown in Fig. 1(c) [12, 13]. The presence of charges in the QDs embedded in an organic layer modifies the conductivity of the device and the energy band-alignment of the materials. The new device exhibits two stable operating stages: one high-resistance stage (HRS) and a second low-resistance stage (LRS). Such devices have been demonstrated as standalone memory cells in electronic circuits [14].

In this work we address the development of group IV and III-N QDs embedded into very thin insulators with focus on their application to NVM devices. More specifically, we report on 2D arrays of Si and GaN QDs in SiO_2 formed by ultra-low-energy IBS (ULE-IBS) [15] and molecular beam deposition (MBD) [16], respectively. A review on the fabrication of Si and Ge QDs by ULE-IBS in different insulators has recently been published by Bonafos et al. [17].

The ULE-IBS technique allows the fabrication of 2D-arrays of Si QDs in thin SiO_2 layers but does not guarantee their effectiveness as charge storage centers and more generally, the memory functionality of the whole gate structure. The latter depends not only on the properties of the QDs (size, size uniformity, density, spatial distribution) but also on the properties (integrity, thickness) of the tunnel and control oxides. This requires a tight control over process parameters such as the thickness of the starting oxide and the implantation/annealing conditions. As emphasized throughout this communication, a challenging task for taking full advantage of the ULE-IBS technique is the fabrication of functional QD dielectric structures which do not necessitate the additional step of depositing a control (or blocking) oxide layer.

According to theoretical and experimental investigations, work-function engineering of the QDs may improve the performance of NVMs in terms of operating voltages and retention time [18, 19]. This can be achieved by forming semiconductor QDs which exhibit negative conduction band offset with respect to the substrate. Assuming a Si substrate with a thin SiO_2 tunneling layer, GaN QDs fulfill these requirements [16, 20]. As stressed herein the MBD technique is well adapted for making GaN QDs onto amorphous dielectrics with negligible cross-contamination effects under specific process conditions.

2 Experimental procedures

2.1 Preparation of Si-QD samples High quality 5, 7, 9, and 10 nm thick SiO_2 layers were first thermally grown on 8-inch p-type (100) silicon substrate (1–10 Ω cm) in dry

Table 1 The LE-IBS samples implanted with 1 keV Si atoms.

dose (cm^{-2})	0.5×10^{16}	1×10^{16}	2×10^{16}
SiO_2 thickness (nm)			
5	AX5114	AX5214	AX5314
7	X711	X721	X731
9	X911	X921	X931
10	X1011	X1021	X1031

oxidizing ambient. Ion implantation of Si atoms was performed at 1 keV in an Axcelis GSD-implanter under charge neutralization conditions. Three different doses of Si atoms were tested, namely 0.5, 1.0, and 2.0×10^{16} cm^{-2}. This set of samples is summarized in Table 1.

All samples were subjected to a post-implantation annealing (PIA) at 950 °C in N_2 for 30 min in atmospheric furnace. Following, MOS capacitors were fabricated using Al for the backside contact and control gate electrode. The latter of 10^{-4} cm^2 area was defined by photolithography and wet etching.

For each oxide thickness, a reference sample was fabricated for comparison purpose. The electrical properties of these reference samples exhibited no significant deviation from that of typical MOS structures and will not be further discussed herein. Furthermore, it should be emphasized that the integrity of the implanted oxide, which is altered due to excess Si atoms and implantation induced defects, as well as the quality of the QD/SiO_2 interface play a significant role in carrier dynamics, thus affecting the charge injection and trapping characteristics of the structures. It is so important to develop a post-implantation step for addressing these issues without adding process complexity. In that direction we examined the possibility of optimizing the PIA step by using different recipes. Emphasis is herein placed upon the case of the 7 nm-thick SiO_2 samples, which have been subjected to the five different PIA recipes (AP1-5) described in Table 2.

AP1 is the standard annealing process used for the formation of QDs and minimization of ion implantation induced defects [21, 22]. AP2 is a thermal treatment recipe in a mild oxidizing ambient, which allows simultaneously QDs formation, oxidation of part of the excess Si atoms and oxidation of the QD/SiO_2 interface. AP3–AP5 have been applied for understanding the structural and electrical changes resulting from a combination of thermal treatments in inert and oxidizing atmosphere.

Table 2 The different recipes used for PIA optimization of 7 nm-thick SiO_2 samples implanted with 1 keV Si atoms to a dose of 2×10^{16} cm^{-2}.

PIA ID	PIA recipe
AP1	950 °C N_2 30 min
AP2	950 °C N_2/O_2 30 min ($[O_2]/[N_2] + [O_2] = 1.5\%$)
AP3	950 °C N_2 30 min + 800 °C O_2 10 min
AP4	950 °C N_2 15 min + 950 °C N_2/O_2 15 min ($[O_2]/[N_2] + [O_2] = 1.5\%$)
AP5	950 °C N_2/O_2 15 min ($[O_2]/[N_2] + [O_2] = 1.5\%$) + 950 °C N_2 15 min

Table 3 The fabrication parameters of the MBD treated samples.

no.	tunnel SiO_2 (nm)	dose (GaN MLs)	control SiO_2 (nm)	gate stack CET (nm)
1	3.5	0	20	24.4
2	3.5	5	20	25.4
3	3.5	8	20	25.9
4	3.5	10	20	25.9
5	3.5	14	20	26.1
6	3.5	18	20	25.9

2.2 Preparation of GaN-QD samples The GaN-QDs were formed by radio frequency plasma assisted MBD (RF-MBD) onto 3.5 nm SiO_2 films grown on 4 inch. (100) n-Si substrates. Several deposition conditions were employed in order to evaluate a range of QDs size and density distributions. Table 3 summarizes the deposition conditions. It should be mentioned that the deposition conditions are determined by the GaN dose which was measured in equivalent number of monolayers (MLs) of epitaxial GaN. LPCVD SiO_2 layer of 20 nm in thickness was used as capping dielectric material. For comparison, a control sample without QDs, but treated in similar conditions and exposed to RF N-plasma was also fabricated. Standard Al-gate MOS capacitors were realized. The devices were MESA isolated using dry reactive-ion-etching (DRIE) process.

Transmission-electron-microscopy (TEM) investigations revealed the presence of crystalline GaN QDs and the variation of their characteristics with respect to the MBD conditions [16]. The variation of the number of MLs allowed tuning the size/density of QDs from discrete 3.5 nm in diameter up to poly-crystalline GaN layer.

3 Electrical characterization results and discussion Standard *C–G–V–f* (HP 4284) and *I–V* (HP 4140B, HP 4155) measurements were performed in order to investigate the electrical properties and memory characteristics of the produced QD-SiO_2 layers.

3.1 Si-QD samples Symmetric bi-directional *C–V* measurements at 1 MHz were applied to samples reported in Table 1 (AP1 PIA recipe). Typical *C–V* characteristics are presented in Fig. 2 for the 5, 7, and 9 nm-thick SiO_2 Si-implanted samples. The flat-band voltage V_{FB} shifts with respect to the fresh sample as extracted from the measured *C–V* hysteresis, ΔV_{FB}, are shown in Fig. 3.

ΔV_{FB} is a measure of the memory effect. Starting the gate voltage sweep from a positive value on a p-MOS memory capacitor, electrons are expected to be injected from the inversion layer, formed at the SiO_2/p-Si substrate interface, into the QDs where they are trapped. As a result of

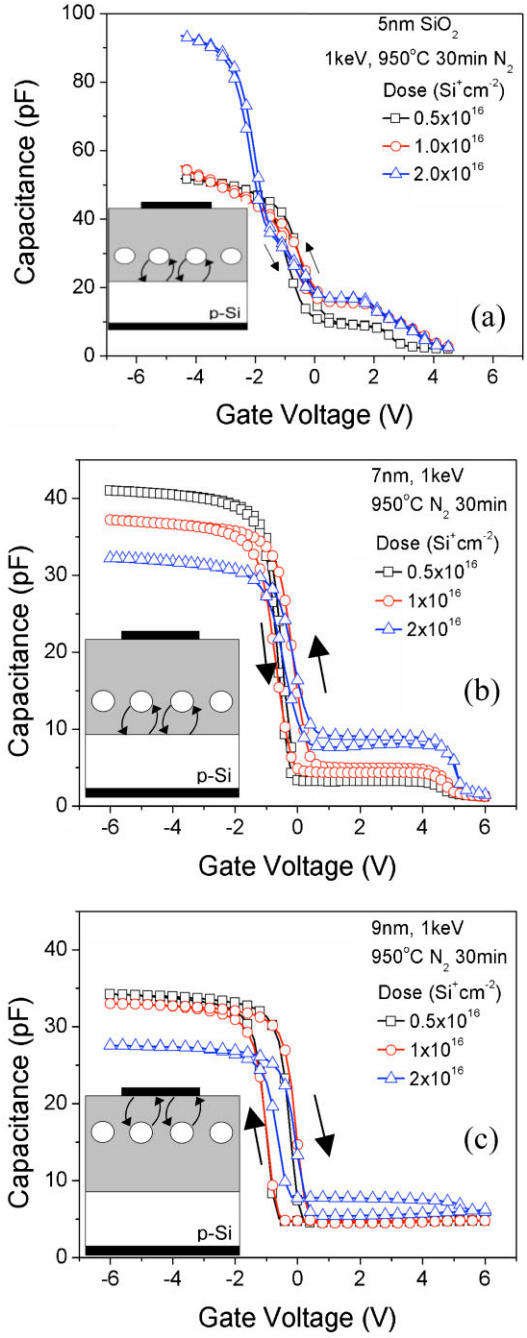

Figure 2 Typical 1 MHz *C–V* hysteresis curves for samples with initial SiO_2 thickness (a) 5 nm, (b) 7 nm, and (c) 9 nm.

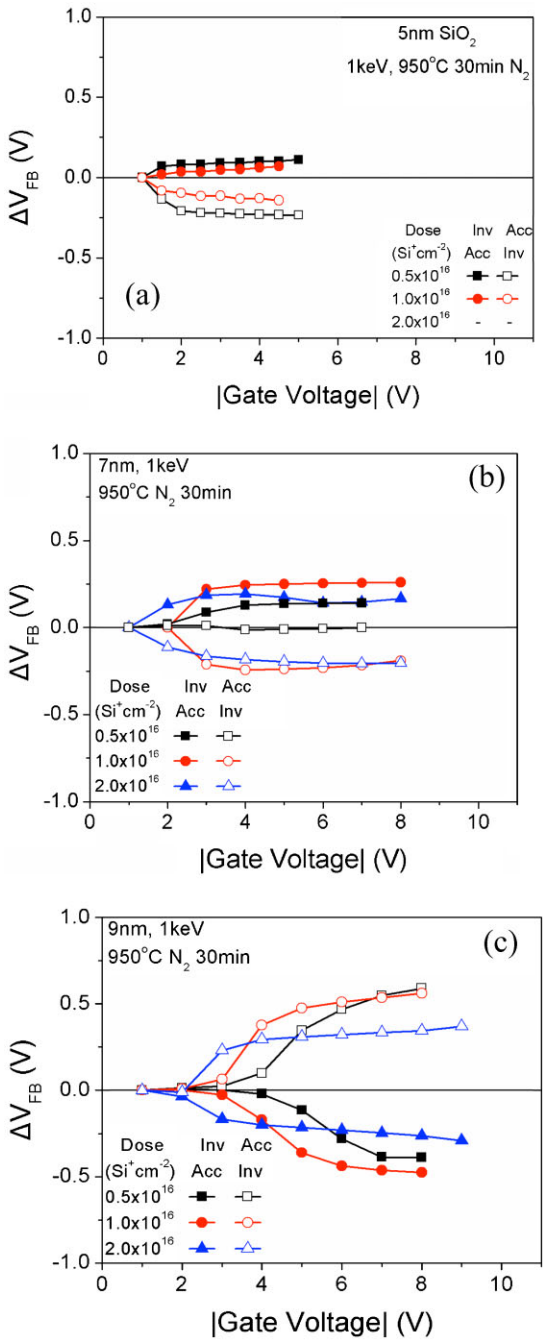

Figure 3 Dependence of the flat-band voltage shift on voltage sweep limits during *C–V* measurements, obtained for samples with initial SiO_2 thickness (a) 5 nm, (b) 7 nm, and (c) 9 nm.

this negative charge trapping event, the depletion layer will initiate earlier causing a shift in the flat-band voltage (or threshold voltage, V_{TH}) of the capacitor to a higher value, V_{FB}^{+} (or V_{TH}^{+}), compared to the flat-band voltage, V_{FB0} (or V_{TH0}), of the capacitor with uncharged QDs (fresh or virgin capacitor). Under negative voltage sweep conditions, the trapped electrons may be ejected from the QDs back to the p-Si substrate and/or hole injection from the accumulation layer, formed at the SiO_2/p-Si substrate, into the QDs may take place. In the latter case, positive charges are trapped into the QDs. Next, the backward voltage sweep is applied, *i.e.*, the gate voltage is swept from negative to positive values. With positive charges trapped into the QDs, the depletion layer is formed at a much lower voltage (*i.e.*, at a more negative voltage), V_{FB}^{-} (or V_{TH}^{-}), compared to V_{FB0}. As the voltage becomes less negative towards to zero, the

positive trapped charge may be ejected back to the p-Si substrate. The *C–V* branch with the high V_{FB} value is called "programming" or "write branch" while the branch with the low V_{FB} value is called "erase branch". The memory window, ΔV_{FB}, in this case is defined as $\Delta V_{FB} = V_{FB}^{+} - V_{FB}^{-}$. In the above example the hysteresis of the *C–V* characteristic is counterclockwise. Clockwise hysteresis is observed when electrons are injected from the gate electrode into the QDs [see *e.g.*, Fig. 1(b)]. During the reverse voltage sweep, the previously injected charges return back to their original sites.

Obviously, the characteristics obtained from the 5 nm-SiO_2 implanted samples are suffering from significant stretch-out, which can be attributed to interface traps. The strong increase of capacitance in the accumulation regime for the high-dose implanted sample (AX5314) indicates an effective oxide thickness of 3.7 nm (C_{max} ~93.6 pF). This is due to the strong coupling between the Si substrate and the Si-QDs layer which is formed very close to the SiO_2/Si interface (~2 nm) as revealed by TEM analysis [23, 24].

The counter-clockwise *C–V* hystereses for the 5 and 7 nm SiO_2 implanted samples point out that charge exchange takes place between the QDs and the Si substrate, while for the 9 nm samples the clockwise *C–V* hysteresis indicates that charge exchange occurs between the QDs and the control gate. The latter can be due to a larger or/and better quality of the tunnel oxide compared to the control oxide [23]. Plots in Fig. 3 demonstrate that both electron and hole trapping in the Si-QDs occur under *C–V* sweep measurements. For the 5 nm SiO_2 sample implanted at the highest dose (AX5314), the extraction of V_{FB} was not possible due to the misleading value of the capacitance maximum. For the rest of the samples, we found that the higher the implantation dose, the lower the voltage needed for charge injection. Further, analyses of the *C–V* characteristics allow calculation of the oxide thickness, t_{ox}, as well as extraction of the density of interface states, D_{it}. Results for the 7, 9, and 10 nm SiO_2 samples are shown in Fig. 4.

Clearly, t_{ox} increases as the implantation dose increases mainly due to the space taken by the Si implanted atoms and, in the case of oxidizing conditions, to the oxidation of the implanted Si-atoms and/or their aggregates. This phenomenon is known as *oxide swelling*. The expansion of the implanted SiO_2 layers depends mainly on the implanted dose [22]. The D_{it} remains at acceptable levels (1–3 × 10^{11} eV^{-1} cm^{-2}) and exhibits a weak dependence on implantation dose for all samples. Evidently, the samples with a 7 nm initial oxide thickness are the most attractive in terms of QDs array position, charge injection characteristics and related memory window.

Typical high-frequency *C–V* characteristics of the 7 nm-samples annealed under the different PIA conditions described in Table 2 are shown in Fig. 5. The corresponding flat-band voltage shifts are presented in Fig. 6. In the case of low implanted dose [Fig. 5a, Fig. 6(a)], a very narrow hysteresis is observed after application of the AP1 recipe, which is mainly due to trapping and de-trapping

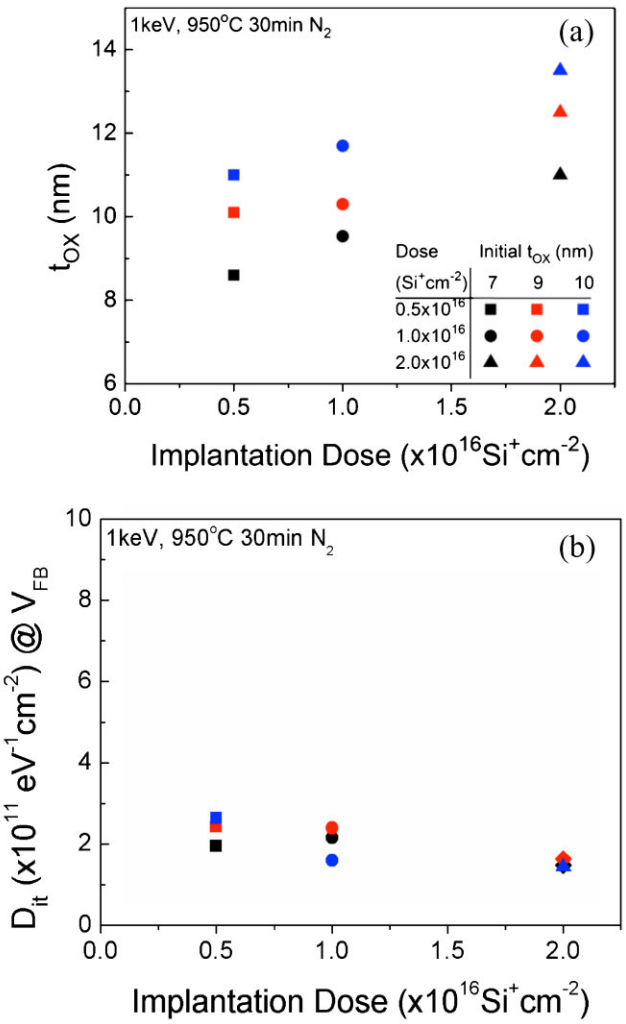

Figure 4 The dependence on the implantation dose of (a) the implanted oxide thickness, t_{ox}, and (b) the density of interface states, D_{it}, after PIA (AP1).

of electrons. The annealing environments used in the AP2–AP5 recipes eliminate this hysteresis effect and lead, at voltages higher than 6 V, to electron injection and cumulative charge trapping without effective charge detrapping [see inset Fig. 6(a)]. In the case of the medium dose (1 × 10^{16} cm^{-2}) implanted sample, both electron and hole trapping occur [Fig. 5(b), Fig. 6(b)]; the latter being more efficient than the former, especially after the AP4 and AP5 treatments. Finally, in the case of the high dose (2 × 10^{16} cm^{-2}) sample [Fig. 5(c), Fig. 6(c)], the memory windows attainable after the AP2, AP4, and AP5 treatments are significantly enhanced compared to the medium dose samples. While charge injection and trapping occur at lower applied gate bias for the AP4 and AP5 treatments compared to the AP2 recipe, the latter leads to larger memory windows and better charge retention characteristics (not shown).

TEM investigations [24] revealed that after AP2 PIA (mild oxidizing ambient) the control oxide slightly increases

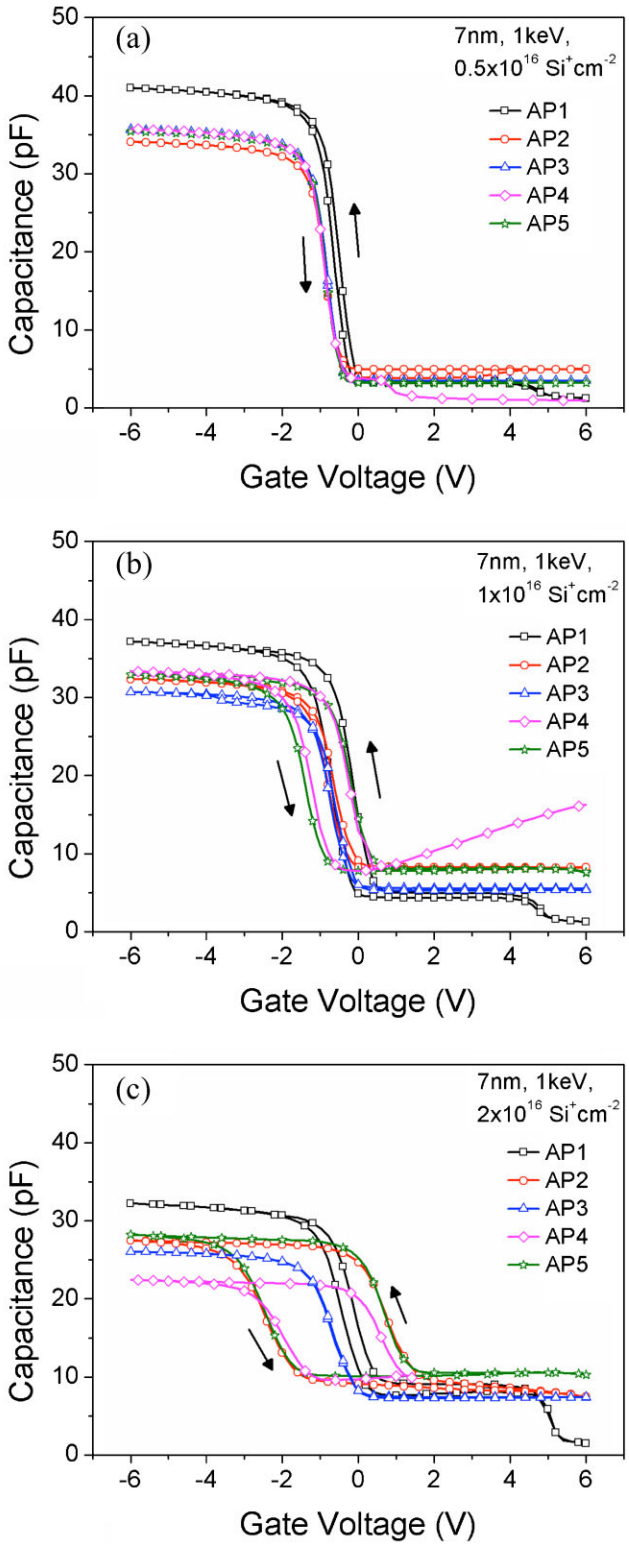

Figure 5 Typical 1 MHz *C–V* hysteresis curves for 7 nm samples implanted with 1 keV Si atoms to doses of (a) 0.5×10^{16}, (b) 1.0×10^{16}, and (c) 2.0×10^{16} cm^{-2} and annealed under different conditions (Table 2).

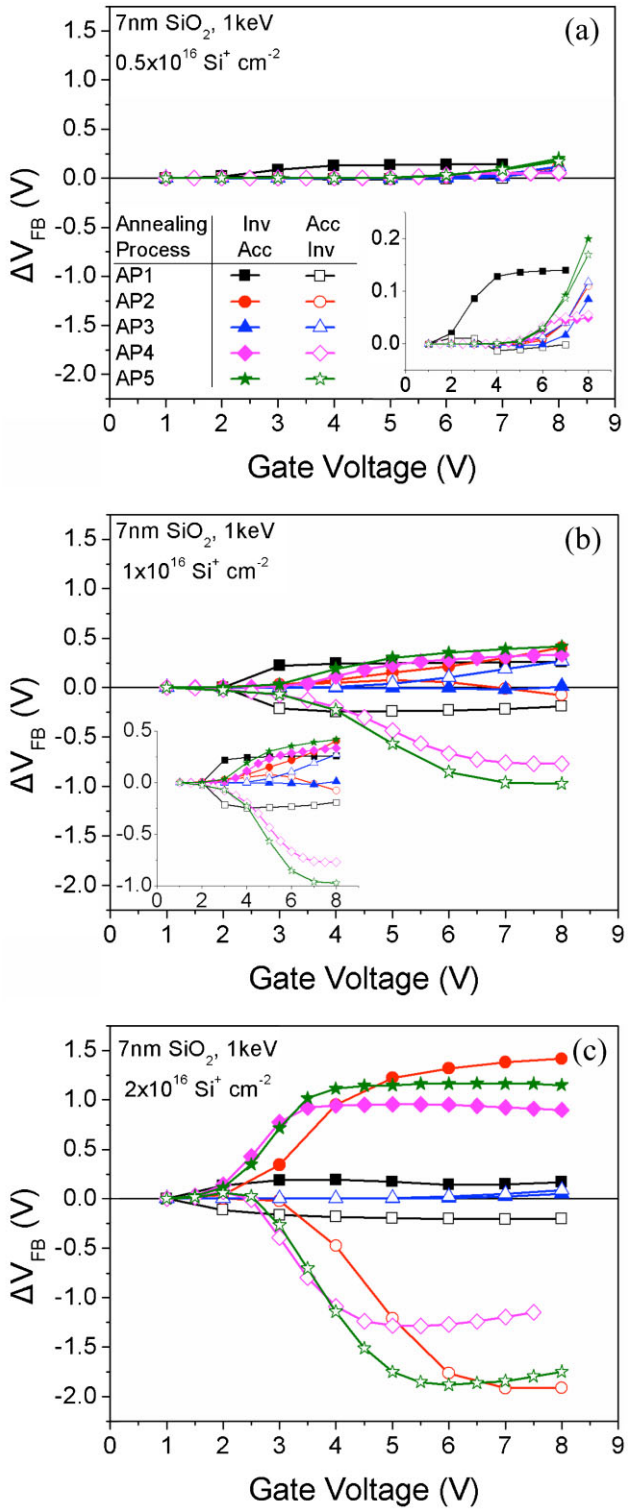

Figure 6 Dependence of the flat-band voltage shift on voltage sweep limits during *C–V* measurements, obtained for 7 nm samples implanted with 1 keV Si to doses of (a) 0.5, (b) 1.0, and (c) 2×10^{16} cm^{-2} and subjected to the annealing conditions described in Table 2. Insets emphasize details of the main plots.

to 5 nm compared to 3.7 nm achieved after the AP1 treatment (inert ambient), whereas the tunnel oxide thickness remains almost constant, ca. 6.5 nm. Furthermore, while no significant dependence of the QD mean-size between the AP1 and AP2 treatments was detected, TEM examination showed that the AP2 recipe leads to a more uniform QD size distribution and slightly larger QD separation; a trait important for memory operation since it mitigates the lateral transport of the trapped carriers from QD to QD. The density of QDs after the AP2 treatment was found to be around 1.7×10^{12} cm^{-2}. Combining ToF-SIMS and XPS analyses, Perego et al. [25] have shown that for 9 nm-thick SiO_2 layers implanted under the same conditions and subsequently AP1 and AP2 annealed, the density of Si nano-aggregates in the control oxide (*i.e.*, above the QD plane) is reduced and the presence of sub-stoichiometric oxide in the QD layer is enhanced in the case of the AP2 treatment. These results suggest a possible scenario for the effect of AP2 treatment on the specific samples: at the early annealing stages, phase-separation and QD formation is taking place. Meanwhile, the oxygen species oxidize part of the excess Si atoms in the control oxide and because their concentration is low (1.5%), the majority of them are blocked by the interconnected Si islands and subsequently oxidize them providing mutually isolated QDs. It is so expected that only a small number of oxidizing species can cross the QD layer, thus limiting their reaction with the excess of Si atoms present in the tunnel oxide. The above could explain why effective charge injection from the substrate to the QD layer is detected during *C–V* sweep measurements (see Fig. 5) despite the thinner physical thickness of the control oxide compared to that of the tunnel oxide.

Further analysis of the experimental *C–V* characteristics shown in Fig. 5 reveals the effect of the annealing treatment on the total oxide thickness, t_{ox} (see Fig. 7). Note from Fig. 7 that the AP2 and AP3 treatments have the strongest effect on t_{ox}. No significant differences are observed between the AP4 and AP5 recipes.

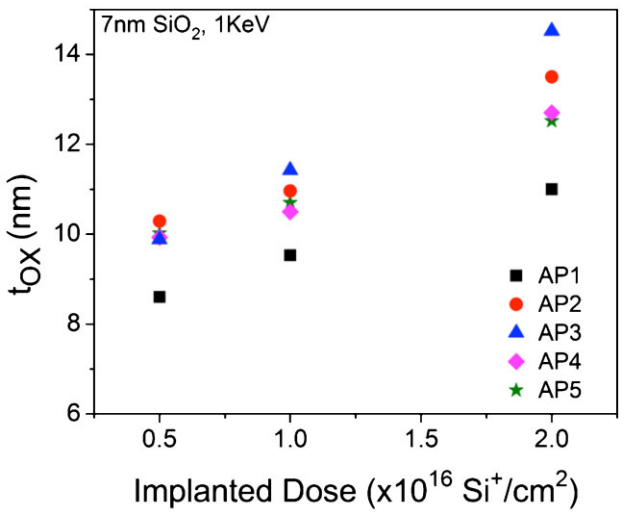

Figure 7 The dependence of the oxide thickness, t_{ox}, on the implanted dose after different PIA.

Figure 8 presents the current density versus electric field (*J–V*) characteristics of the 7 nm-SiO_2 samples implanted to low, medium and high Si doses after the AP1–AP5 treatments [26]. Clearly, samples subjected to the AP3 treatment (pure oxidizing ambient) exhibit the highest dielectric strength while the samples annealed following the AP1 treatment (neutral ambient) exhibit the lowest. This is because during the AP3 treatment the majority of the implanted Si atoms are oxidized preventing the formation of Si-QDs. Thus any parasitic conduction due to excess Si atoms and implantation-induced-defects is minimized and charge storage in Si-QDs is omitted (Figs. 5 and 6). Furthermore, the samples treated following AP2 annealing conditions combine acceptable dielectric strength with remarkable memory windows.

As presented in Fig. 8(c), the *J–E* characteristics of the high-dose implanted samples after the AP2 and AP5 treatments are comparable. Nevertheless, the AP5 treated samples have slightly higher conductivity especially at low electric fields (<5 MV cm^{-1}). This low electric field conduction can explain the large memory windows observed at low voltages shown in Fig. 6(c). This direct link between oxide conductivity and charge injection signifies the crucial role of the remaining Si atoms inside the oxide matrix.

If the concentration of un-clustered Si atoms and/or tiny Si nano-aggregates [25] is significant after PIA, the silicon dioxide can be regarded as a silicon rich oxide with poor dielectric properties. It is necessary to develop a methodology utilizing electrical characterization methods that allows the evaluation of the oxide's insulating properties after the PIA. For this purpose, we consider two methods based on the analysis of the *J–E* characteristics shown in Fig. 8. The first method is based on the high electric field conduction [Fowler–Nordheim (F–N) regime] where the energy barrier Φ_B that the electrons have to overcome in order to tunnel through the silicon dioxide can be estimated according to the F–N approximation [27],

$$J = AE^2 \times \exp(-B/E), \tag{1}$$

$$\Phi_B = \left(\frac{\sqrt{2}B}{6.83 \times 10^7}\right)^{2/3}, \tag{2}$$

where A (A V^{-2}) and B (V cm^{-1}) are the F–N constants both dependent on the electron effective mass, $E = V/t_{ox}$, V is the applied voltage across the dielectric, t_{ox} is the oxide thickness after the PIA (see Fig. 7). The un-cluster Si atoms modify spatially the dielectric constant of the SiO_2 layer contributing to the reduction of the potential energy barrier at Si/SiO_2 and SiO_2/Al interfaces. In addition, excess Si atoms are responsible for the formation of oxide traps [28] which may contribute to trap-assisted tunneling. For these reasons, the tunneling resistance of the Si-rich SiO_2 layers is reduced and become transparent for electrons with relatively low

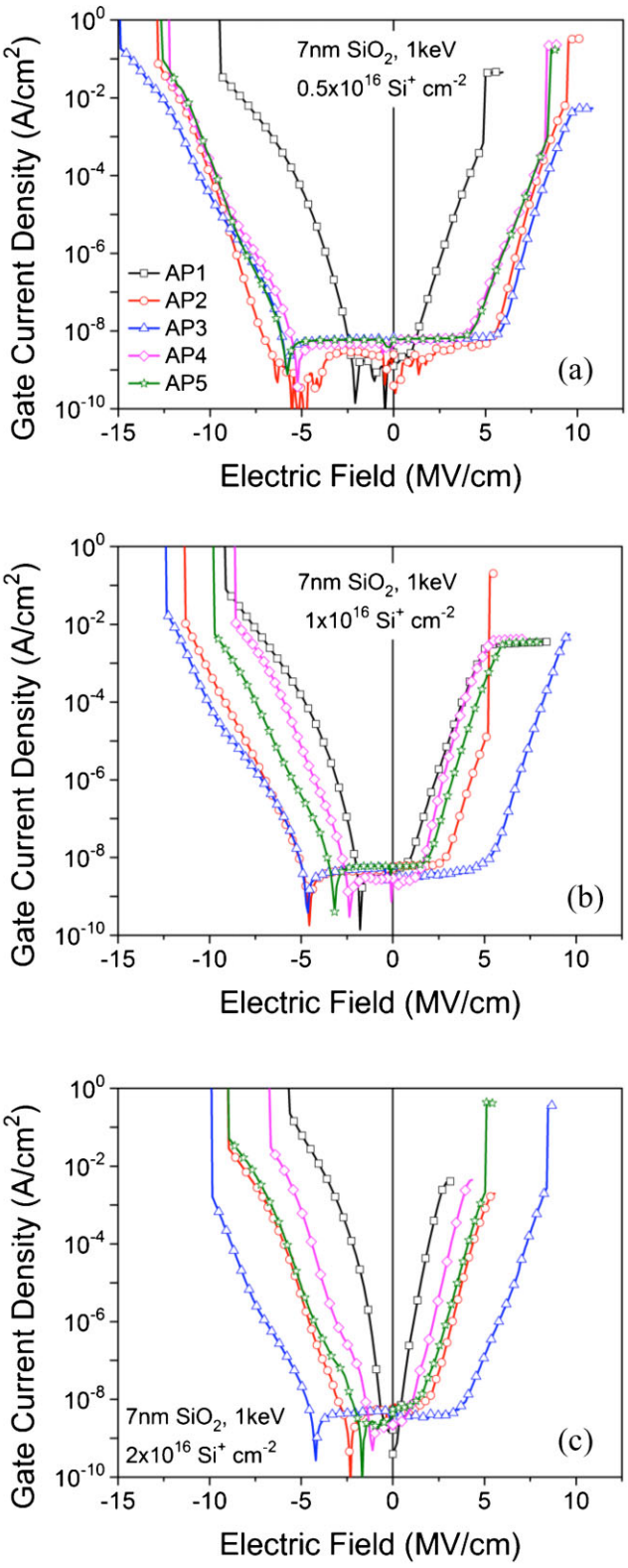

Figure 8 *J–E* characteristics obtained for 7 nm samples implanted with 1 keV Si to doses of (a) 0.5, (b) 1.0, and (c) 2.0 × 10^{16} cm^{-2} and subjected to the annealing processes described in Table 2.

potential energy. This method has been presented in Ref. [29].

The second method is based on the comparison of the electric field needed to achieve a certain value of leakage current density. Figure 9 presents the electric field E after the applied PIA treatments at which the current density flowing through the SiO_2/Si-QDs/SiO_2 is 1 μA cm^{-2}. The higher the electric field, the better the oxide insulation properties. At this point, we introduce the dielectric resistivity [30], $\rho(=E/J)$ as a figure of merit for the insulation properties. Following this representation, the physical interpretation of data shown in Fig. 9 is more evident: the dielectric resistivity after AP2 PIA treatment is higher than any other PIA treatment for which memory effects are detected.

Briefly summarizing, we found that the LE-IBS technique can provide attractive memory characteristics when a 7 nm SiO_2 layer is implanted with 1 keV Si ions to a fluence of 2 × 10^{16} cm^{-2} and subsequently annealed at 950 °C for 30 min in mild oxidizing ambient, *i.e.*, 1.5% O_2 in N_2.

Further, optimization of the annealing process requires an experimental study on the effect of the relative percentage of O_2 in N_2. For this purpose we performed the PIA experiments shown in Table 4 [26]. As depicted in Fig. 10, application of gate voltage sweeps of ±8 V and higher lead to similar memory windows in the case of 1, 1.5, and 2% O_2 PIA treatments, while charge injection and trapping initiate at highest gate voltages as the oxygen content increases; a trait which relates mainly with tunnel oxide conductivity. Figure 10 reveals also that the charge trapping capabilities of the samples subjected to the 3 and 5% O_2 PIA treatments are significantly reduced. This can be attributed not only to the quality of the tunnel oxide but also to the properties of the QDs. Further investigations of the effect of the O_2 content on the memory properties of the 1, 1.5, and 2% O_2

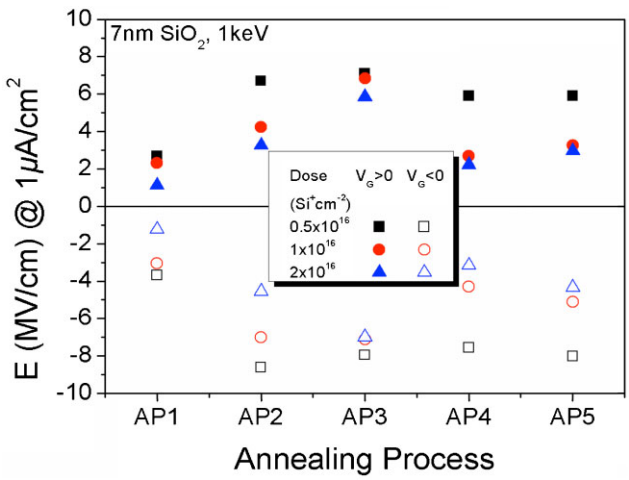

Figure 9 Plot of the electric field E at which the current through the gate oxide of the memory capacitor is 1 μA cm^{-2} as a function of the annealing process. The experimental data (symbols) were obtained for from *J–E* characteristics presented in Fig. 8.

Table 4 The conditions for the optimization of the oxygen percentage diluted in N_2 during the PIA of samples with 7 nm SiO_2 implanted with 1 keV Si to a fluence of 2×10^{16} cm^{-2}.

no.	temperature (°C)	time (min)	$[O_2]/([N_2] + [O_2])$ (%)
1	950	30	1
2	950	30	1.5
3	950	30	2
4	950	30	3
5	950	30	5

PIA treated samples have been conducted through charge retention measurements at 85 °C. The capacitors were previously programmed and erased using +9 V/10 ms and −9 V/10 ms pulses. The results are shown in Fig. 11. For the erase state, the V_{FB} transients have almost the same decay rate for all samples. For the program state, the V_{FB} transients after annealing in 1.5 and 2% O_2 ambient are comparable after 10^5s while a much faster transient is detected in the case of the 1% O_2 PIA treatment. Because a larger programming window at a lower applied electric field is obtained for the sample annealed in 1.5% O_2, we conclude that 1.5% $[O_2]$ in diluted $[N_2]$ is the most appropriate annealing atmosphere for a 7 nm SiO_2 implanted at 1 keV using a dose 2×10^{16} cm^{-2}.

The last optimization parameter is the annealing time. For this purpose dedicated experiments were performed in 1.5% O_2 ambient, as shown in Table 5.

Typical normalized *C–V* characteristics (1 MHz) obtained from samples annealed for different time durations are shown in Fig. 12. For comparison, a reference sample is presented.

As reference sample we consider a MOS capacitor with 7 nm dry SiO_2, non-implanted and annealed in the same oxidizing ambient for 30 min. According to our expectations, the part of the reference *C–V* characteristic in depletion regime is very similar to that of the Si-implanted samples after 120 min PIA in 1.5% O_2, because under these conditions the majority of the implanted Si atoms

Table 5 The conditions for the optimization of the PIA time for samples with 7 nm SiO_2 implanted with 1 keV Si to a fluence of 2×10^{16} cm^{-2}.

no.	temperature (°C)	time (min)	$[O_2]/([N_2] + [O_2])$ (%)
ref	950	30	1.5
1	950	5	1.5
2	950	15	1.5
3	950	30	1.5
4	950	120	1.5

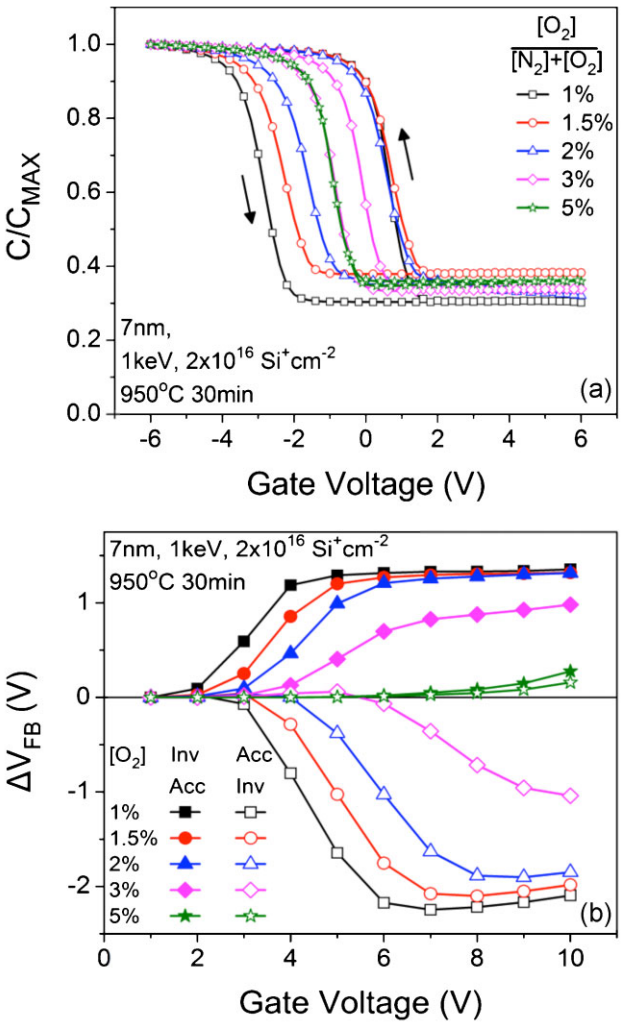

Figure 10 (a) Typical normalized bidirectional *C–V* (1 MHz) characteristics and (b) flat-band voltage shift diagrams obtained from MOS capacitors annealed in different oxidizing environments.

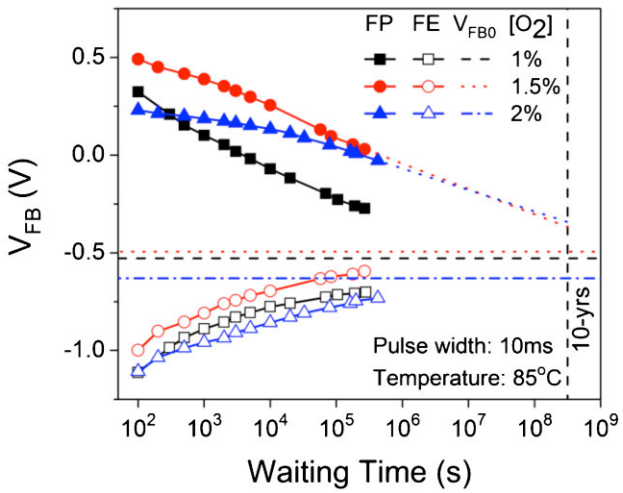

Figure 11 (a) Charge-retention transients for samples annealed at different oxidizing ambient. The horizontal lines define the flat-band voltage V_{FB0} for each one of the tested memory capacitors.

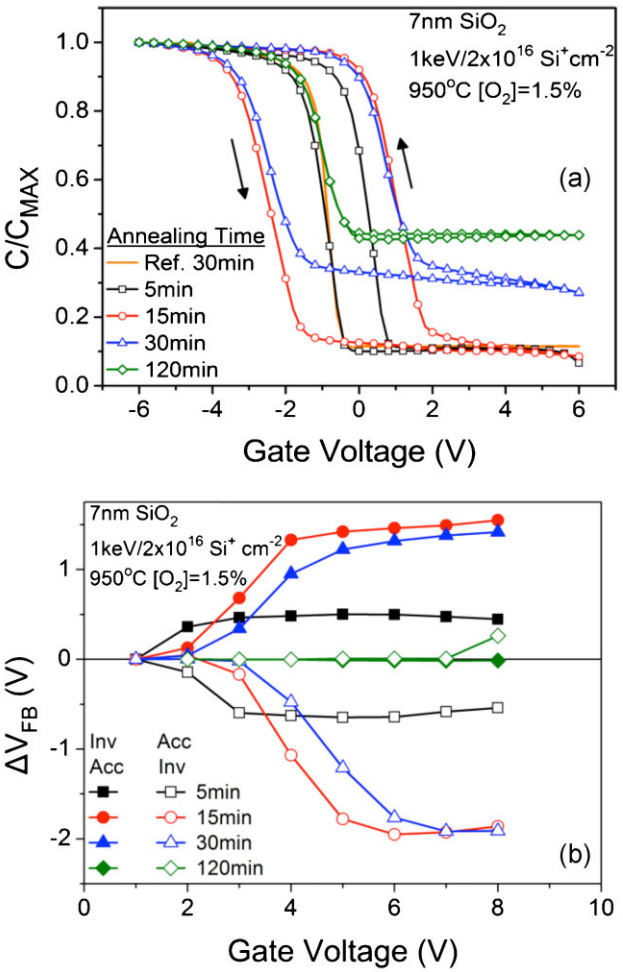

Figure 12 (a) Typical normalized bidirectional *C–V* (1 MHz) characteristics and (b) flat-band voltage shift diagrams obtained from MOS capacitors annealed for different time durations in mild (1.5% O_2) oxidizing environment, utilizing *C–V* measurements.

are oxidized. According to TEM investigations [24] for annealing durations shorter than 30 min elongated and connected Si islands were observed; a trait which affects the retention time characteristics. For long annealing durations such as 120 min descrete spherical (2 nm in diameter) Si-QDs were found. In the latter sample the surface coverage is as low as 6% compared to 23% after 30 min PIA.

The above processing conditions have been utilized for the realization of NMOS field-effect transistors with self-alligned n^+ poly-Si gate. All the required details for NMOSFET fabrication as well as their performance as single-memory cells are described in Ref. [31]. Further investigations on charge retention at elevated temperatures have been presented in Ref. [32]. It was found that the cells exhibit true-nonvolatile characteristics after application of programming (*P*) and erasing (*E*) voltage pulses of +9 V/10 ms and −9 V/10 ms, respectively. Under these conditions, the cells can withstand more than 10^6 *P/E* cyles and exhibit a significant 10-year extrapolated memory window.

The threshold voltage shift for QD-NVM devices is described by [15]

$$\Delta V_{\mathrm{TH}} = \left(\frac{t_{\mathrm{CO}}}{\varepsilon_{\mathrm{CO}}} + \frac{1}{2}\frac{t_{\mathrm{qd}}}{\varepsilon_{\mathrm{qd}}}\right) Q_{\mathrm{qd}} = K \cdot Q_{\mathrm{qd}}, \tag{3}$$

where K is a constant depending on the gate dielectric stack characteristics, t_{CO} and t_{qd} are the thickness of the control oxide and the diameter of the QDs, $\varepsilon_{\mathrm{CO}}$ and $\varepsilon_{\mathrm{qd}}$ are the dielectric constants for the control oxide and the QDs, respectively. Charge loss is estimated by threshold voltage V_{TH} transients. Detailed studies [15, 33] have shown that Eq. (3) should be corrected dividing the constant K by the surface coverage R of the QDs,

$$R = 0.25\pi \cdot t_{\mathrm{qd}}^2 \cdot n_{\mathrm{qd}}, \tag{4}$$

where n_{qd} is the surface density of the QDs. Typical, V_{TH} transients at room and elevated temperatures on a pre-cycled device are shown in Fig. 13(a). Obviously, V_{TH} has a logarithmic dependence on time

$$V_{\mathrm{TH}}(t) = V_{\mathrm{TH}}(0) - M \cdot \log(t), \tag{5}$$

where M is the decay rate of V_{TH}. Comparable charge loss rates or equivalently V_{TH} decay rates, $\mathrm{d}V_{\mathrm{TH}}/\mathrm{d}t$, are found for V_{TH} transients from the erase state. Contrary, the decay rates of V_{TH} transients from the program state are temperature dependent. Figure 13(b) shows the Arrhenius plots for the decay rates obtained from V_{TH} transients for the program and erase states. Considering a simple Arrhenius relation, $\mathrm{d}V_{\mathrm{TH}}/\mathrm{d}t \propto \exp(-E_{\mathrm{A}}/k_{\mathrm{B}}T)$, the activation energies for the charge loss rates from the program and erase states are estimated to 40 and 5 meV, respectively. The activation energy represents the minimum energy required to initiate a reaction or a physico-chemical mechanism. It is a measure of the sensitivity of the mechanism to temperature. In our case, the calculated values indicate that the decay rates of the charge loss process are strongly affected by the ambient temperature. Retention time t_{R} is defined as the time required for V_{TH} to reach the threshold voltage of a fresh (unstressed) cell, V_{TH0}, and can be extracted from the extrapolation of the V_{TH} ransient [see Fig. 13(a)]. Figure 13(c) represents the Arrhenius plot of t_{R}, from which activation energies of 1.48 and 0.21 eV can be extracted for the program and erase states, respectively. The physical interpretation of these activation energies denote that the trapping sites for electrons are deeper compared to holes and therefore more thermal energy is required for electron detrapping to occur.

A charge loss transient defines an equivalent charge loss current, J_{det}, corresponding to de-trapped charges (electrons or holes) that escape back to the Si substrate at a given time

$$J_{\mathrm{det}}(t) = R^{-1}\frac{\mathrm{d}Q_{\mathrm{qd}}}{\mathrm{d}t}. \tag{6}$$

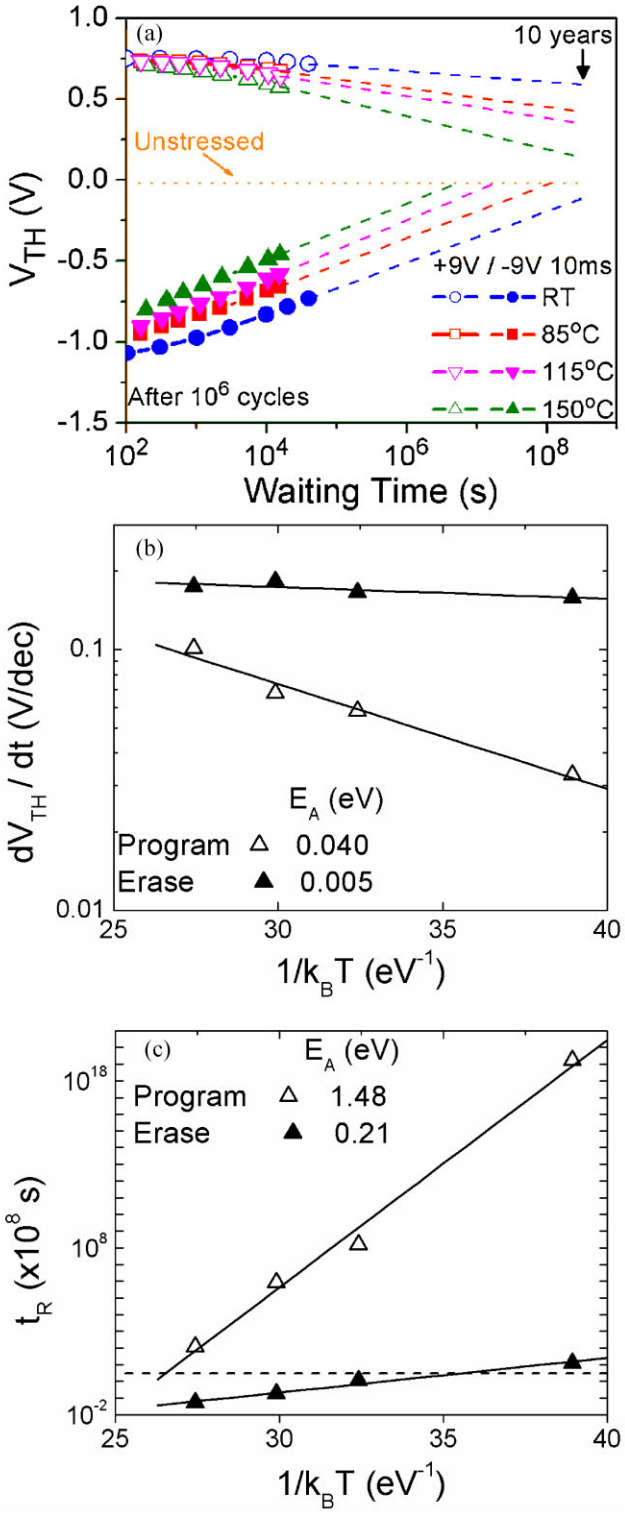

Figure 13 (a) V_{TH} transients from the program and erase states due to thermally activated charge loss, (b) Arrhenius plots for the decay rates of the previous transients and (c) Arrhenius plots for the charge retention time from the program and the erase states.

In Fig. 14, J_{det} transients at various temperatures are presented. The experimental data can be fitted by lines in log–log plot, revealing that

$$J_{det}(t) = H \cdot t^m, \tag{7}$$

where H is a constant and the values of the exponent m are given in Table 6.

According to the previous experimental results on the properties of tunnel and control oxides, we assume that the charge loss is taking place through the tunnel oxide. The internal electric field across the tunnel oxide is given by

$$E_{TO} = Q_{qd} / \left(\varepsilon_{CO} \frac{t_{TO}}{t_{CO}} + \varepsilon_{TO} \right) R. \tag{8}$$

In order to investigate the charge loss mechanism, J_{det} is plotted following F–N representations and Poole–Frenkel (P–F) as shown in Fig. 15. The linear least-squares fitting of the experimental data in both representations revealed that the trapped charge is lost more probably via a P–F current mechanism [see Fig. 15(b)] than an F–N mechanism [see Fig. 15(a)]. This is an indication that charge loss is taking

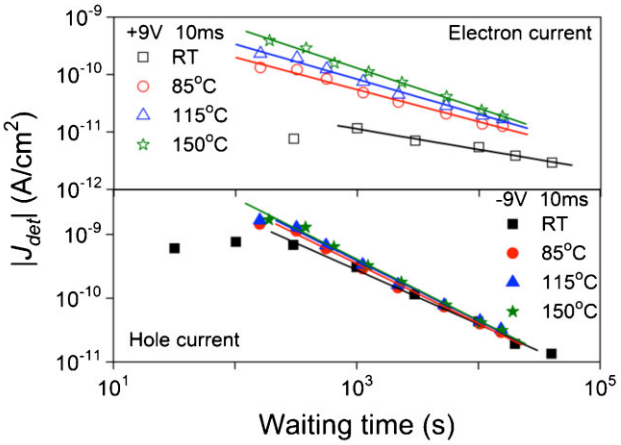

Figure 14 Current transients due to charge loss from program (electrons) and erase (holes) states at various temperatures. Excellent linear fitting were obtained in all cases.

Table 6 The values of exponent m at various temperatures for de-trapping current due to electron and hole loss as extracted from data in Fig. 15.

temperature (°C)	m	
	electrons	holes
25	0.359	−0.848
85	0.560	−0.936
115	0.610	−0.945
150	0.700	−0.958

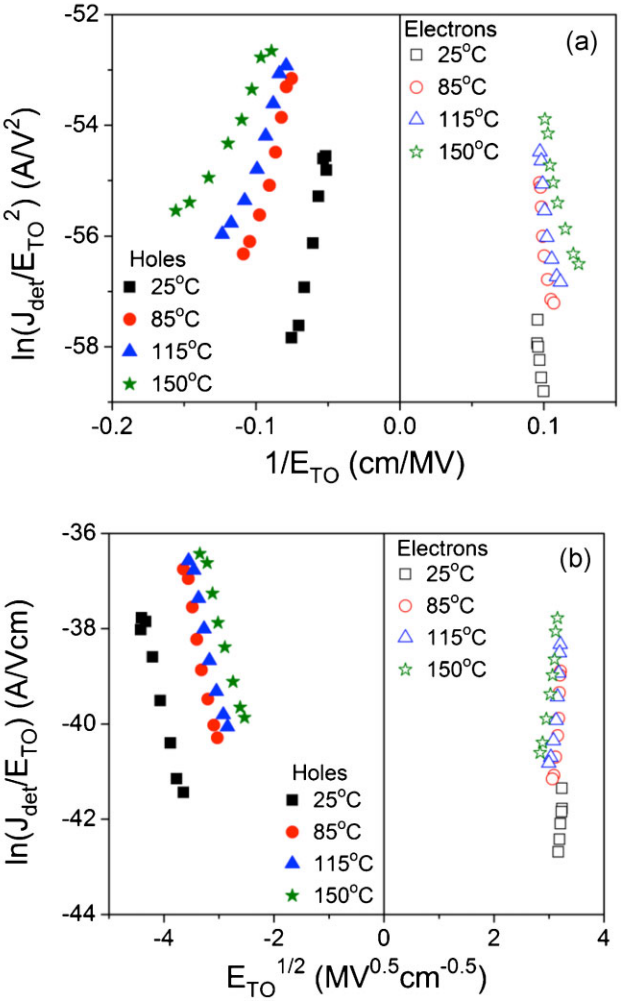

Figure 15 Current due to charge loss from program and erase states plotted in (a) F–N and (b) P–F representations.

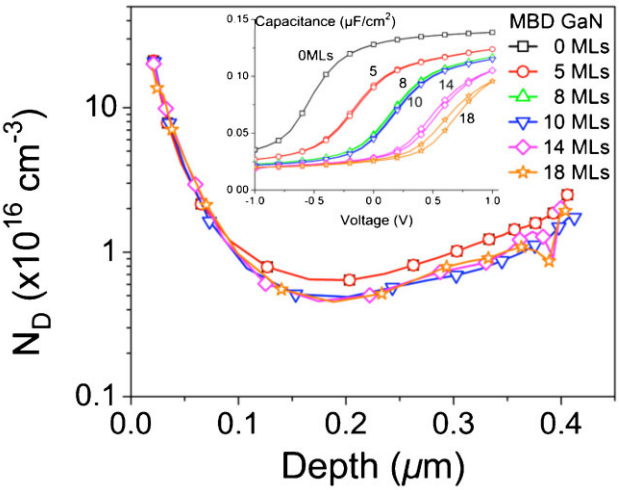

Figure 16 Effective doping profile calculated from *C–V* characteristics at 1 MHz (see inset) for all examined samples.

place through the TO via a trap-assisted current conduction mechanism.

3.2 GaN-QD samples As already mentioned standard memory capacitors having Al as front (gate) and backside contact electrodes were tested. TEM cross-sectional and plane-view studies revealed that in the dose range from 5 MLs up to 18 MLs, we can achieve 2D layers having discrete nanocrystalline (QDs of 3.5 nm in diameter) to continuous poly-crystalline structure [16]. The capacitance equivalent thickness of the tested structures is shown in Table 3 as extracted from the maximum capacitance value at +5 V using 1 MHz test signal. In order to investigate the effect of deposition conditions (*e.g.*, RF nitrogen plasma, Ga atom diffusion) on the properties of the oxide as well as the substrate characteristics, we measured the *C–V* characteristics in a short voltage range (from −1 to 1 V and back to −1 V) to avoid the influence of the injected and subsequent trapped charges at the QDs. Figure 16 presents the effective doping profiles obtained from *C–V* characteristics measured at 1 MHz, which are shown in the inset plot. Obviously, no change in the doping concentration profile is observed among the reference and the samples with QDs, suggesting that cross-contamination in the process is negligible. This is an evidence for the CMOS compatibility of the fabrication steps.

Nevertheless, the *C–V* curves shown in the inset of Fig. 16 denote that V_{FB} depends on the fabrication conditions. More specifically, V_{FB} is getting higher with respect to the V_{FB} value of the reference sample. This dependence is shown in Fig. 17 (right axis), where the V_{FB0} values are calculated according to Ref. [34]. In the same figure (left axis), we plot the calculated density of fixed oxide charges, Q_f, and interface charges, Q_{ss}, which are responsible for the observed V_{FB0} shift. Furthermore, our

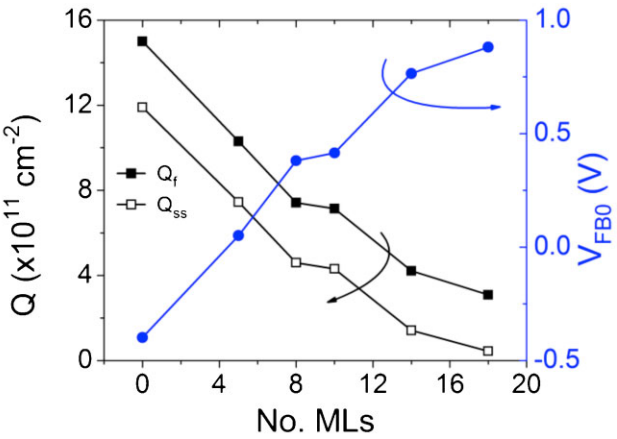

Figure 17 Dependence of the flat-band voltage V_{FB0} (right axis) and the density of oxide charges (left axis) on the number of deposited GaN MLs as obtained from the *C–V* characteristics shown in Fig. 16 (inset).

recent investigations [20] suggest that it is possible to minimize the adverse effect of the inversion layer these charges induced beyond the area of the capacitor by making MESA isolated structures. Note also that the latter structures prohibit any possible communication among neighboring QDs and lead to stable and repeatable memory windows.

In Fig. 18(a), we present the *C–V* characteristics (1 MHz) for the tested samples with and without MESA isolation after a ±5 V sweep. The difference between the *G–V* peaks under forward and reverse sweep directions is equal to the V_{FB} clockwise hysteresis. A typical example is shown in Fig. 18(b) for MESA isolated structures. No *C–V* hysteresis or *G–V* peak shift is observed for the control sample. The *C–V* hysteresis and *G–V* peak shifts detected for the 5 and 18 MLs capacitors are attributed to electron traps in GaN QDs or at the interface QD/SiO_2 and not to states at the substrate/tunnel oxide interface [35]. Comparing the memory windows between MESA and non-MESA isolated structures, such as extracted from the *C–V* curves in Fig. 18 (a), we found a more efficient electron detrapping under negative voltages for the latter structures, which may be attributed to the permanent inversion layer surrounding each memory capacitor.

The memory windows for all samples calculated from bi-directional *C–V* characteristics (1 MHz) under symmetric voltage sweeps are shown in Fig. 19. For all samples, we observe that the symmetric voltage sweeps do not allow the full discharge of the trapped electrons; *i.e.*, $V_{FB}^{-}-V_{FB0} > 0$. The interpretation of this experimental evidence is that the electric field used to detrap an electron from the GaN QDs should be larger than the electric field used to inject this electron. This may be attributed to the higher energy barrier that the trapped electron should overcome compared to an electron in Si substrate.

It should be stressed herein that detrapping of electrons is not enhanced during *C–V* measurements under white light illumination conditions. The interpretation of this experimental result is twofold. First, the change in surface potential and electric field under illumination is not enough to reduce the energy barrier for the trapped electrons. Second, the generated minority carriers (holes) in the Si substrate cannot be injected and subsequently compensate the stored negative charges in GaN QDs.

C–V measurements with a ±5 V voltage sweep at different frequencies were carried out for all samples and the V_{FB} hysteresis (ΔV_{FB}) was extracted. The results are summarized in Fig. 20. Obviously, ΔV_{FB} exhibits no dispersion as a function of the applied frequency. This is consistent with our assumption that at room temperature the observed hysteresis (charge trapping) is not due to interface traps, which generally give rise to frequency dependent characteristics.

Room temperature charge retention measurements (Fig. 21) of the program state were performed in samples with 5 and 18 MLs. Both devices were programmed by a single voltage pulse +15 V/100 ms. In the case of sample with a poly-crystalline GaN layer (18 MLs), an electron loss

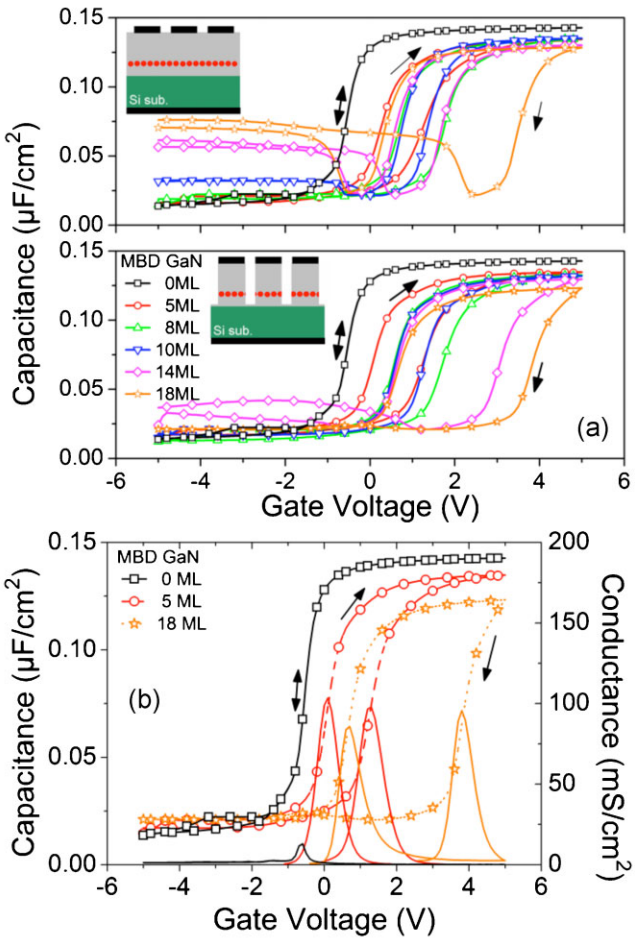

Figure 18 (a) *C–V* characteristics (1 MHz) for samples without (top) and with (bottom) MESA structures. No hysteresis is observed for the reference device. (b) Typical *C–V* and *G–V* characteristics (1 MHz) for three different samples.

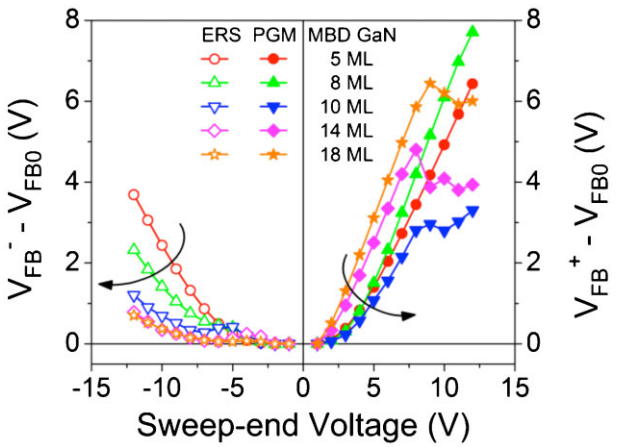

Figure 19 Extracted memory windows from hysteresis obtained from *C–V* characteristics (1 MHz) under symmetric voltage sweeps for MESA isolated samples.

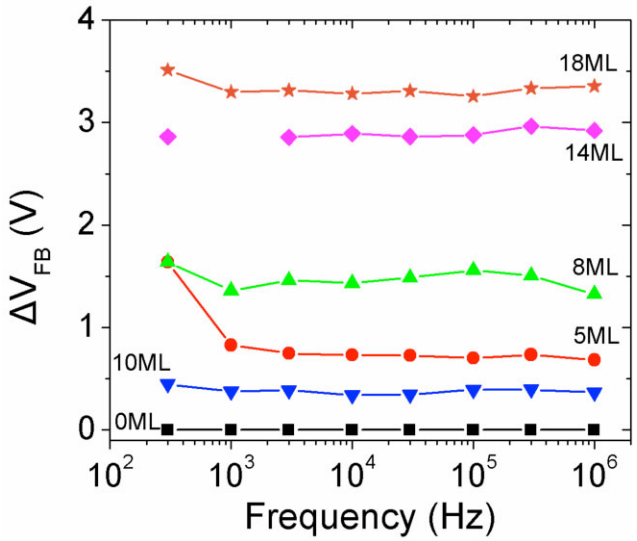

Figure 20 Memory windows as a function of the test signal frequency of the *C–V* measurements for all tested samples.

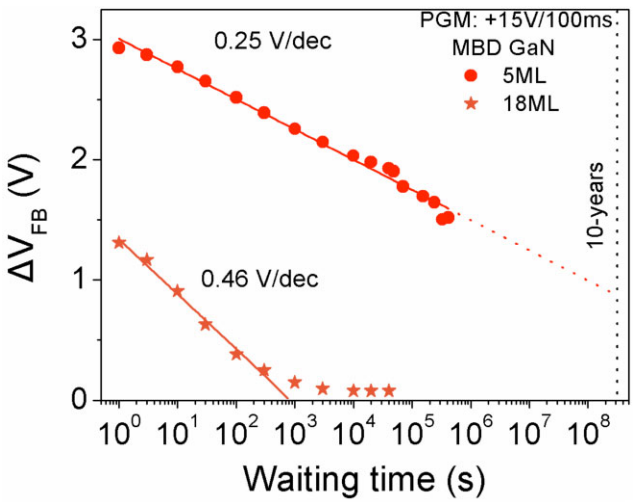

Figure 21 Charge retention measurements for sample separated GaN-QDs (5 MLs) and continuous polycrystalline GaN layer (18 MLs).

rate of 0.46 V dec^{-1} was measured for the first 1000 s corresponding to a 70% loss of the initial stored charge. For longer time the memory window remains constant at 0.071 V. Sample with discrete QDs (5 MLs) exhibited a charge loss rate of 0.25 V dec^{-1} and can retain data for 10 years with an extrapolated remaining memory window of about 1 V.

4 Conclusions The application of QDs as discrete charge storage nodes in nanofloating memory devices is a promising alternative for scalable NVM devices. Among the different materials utilized to fabricate QDs, Si seems to be the most promising. However, the employment of QDs from materials having negative conduction band-offset with respect to the Si conduction band are also very attractive. In this direction, we developed a CMOS compatible process to fabricate MOS memory capacitors with GaN QDs embedded in SiO_2 with excellent charge retention properties at room temperature.

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