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Reconfigurable CMOS with undoped silicon nanowire midgap Schottky-barrier FETs

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ABSTRACT

In this paper we report on a newly developed multi-gate nanowire-field-effect device (NWFET) in which the transistor type (i.e. PMOS and NMOS) is freely selectable by the application of a control-voltage. This significantly adds to flexibility in design of integrated circuits and their fabrication, respectively. We will show, that the use of midgap Schottky-barrier source and drain contacts are the key enabler for this device concept to be functional. A fully functional freely configurable CMOS-NWFET inverter circuit is presented, demonstrating the capability of this SOI technology platform. All this makes the presented NWFET-technology suitable for the fabrication multi-purpose devices for many applications.

1. Introduction

Today's aggressively size-scaled basic building blocks of integrated circuits, namely MOSFETs, seriously suffer from bulk-leakage and PN-junction alike. This leads to an increase in OFF-state current [1,2] and becomes more and more dominant in the device characteristic. Even worse, when increasing the operating temperature these leakage currents are enhanced. To reduce bulk-leakage currents one possible solution is the use of silicon-on-insulator (SOI) technologies, with very thin silicon top layers. However, thermally generated PN-junction leakage is still present even in modern SOI MOSFETs. To circumvent this problem, the PN-junction itself has to be removed from the device, leaving classic source and drain formation via doping behind, moving towards Schottky-barrier (SB) source/drain contacts. Therefore, our fabricated NWFETs exhibit Schottky-barrier contacts as non-conventional source/drain junctions. An additional advantage of the midgap Schottky-barrier source and drain configuration is its robustness against high temperature environments as previously reported in [3]. Usually, for conventional Schottky-barrier MOSFETs, each type of transistor (i.e. NMOS or PMOS) has its dedicated metal, corresponding to a specific metal-semiconductor workfunction. The proper workfunction difference from metal to semiconductor selects whether hole injection (e.g. PtSi), or electron injection (e.g. ErSi) is dominant [4]. In other words, the source/drain Schottky-barrier workfunction determines if a NMOS or PMOS is formed. With this type of barriers at source and drain a significant amount of junction related leakage can be suppressed. Moreover, high temperature annealing steps that are mandatory to activate the dopant atoms subsequent to ion implantation are obsolete which simplifies processing. Typical silicidation temperatures to create Schottky-barrier contacts are significantly lower than the pn-junction annealing temperatures for dopant activation. The use of high-k gate dielectrics becomes more feasible with decreasing temperature, hence in most high-k materials the dielectric properties are known to severely degrade or even vanish with increasing process temperatures [5]. These advantages combined with the atomic abruptness of a Schottky-barrier compared to a conventional PN-junction adds to the long-term scalability of the devices [6]. Additionally to the before mentioned advantages our devices only use one type of source/drain metal, so that the device type becomes voltage-selectable (i.e. NMOS or PMOS). This adds to the versatility of the device architecture, whereas the two complementary device types are interchangeable on the fly, by the application of a proper select-voltage at the backgate. Fig. 1(a) gives a schematic view of the device cross-section on a commercially available SOI substrate. Note that during the entire fabrication process no doping is required, making this process independent of statistic dopant fluctuation typically arising in modern MOSFET fabrication. Fig. 1(b) shows the complete voltage-selectable CMOS-NWFET inverter on a MultiSOI^{TM} substrate [7].

2. Fabrication

The devices are fabricated on PremiumSOI^{TM} [8] substrates with the lowest background boron doping of 10^{15} cm^{-3} available to us. Unfortunately, by now no intrinsic SOI material is

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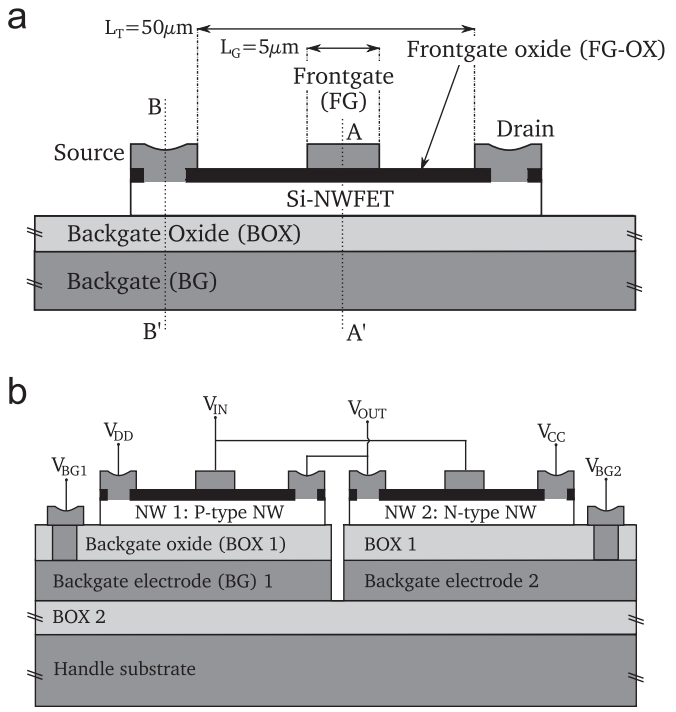

Fig. 1. (a) Schematic cross-section of the NWFET device on a SOI substrate. The frontgate is formed in a tri-gate configuration. The section line A−A′ corresponds to the cut presented in Fig. 2(a), section line B−B′ corresponds to the cross section presented in Fig. 2(b). (b) Proposed layout of a CMOS-NWFET inverter on Multi-SOI substrate. Note that the devices are identical in terms of fabrication technology. The device type (P- or N-FET) is determined freely by a select-bias V_{BG1} and V_{BG2} applied to the corresponding backgate terminals.

commercially available. The devices are patterned using a dedicated electron-beam-lithography process. Only three lithographic layers are needed to pattern the devices. The channel area is defined by reactive ion etching in a high density hydrogen bromide plasma. The gate oxidation is performed at 1000 °C in a dry oxidizing ambient horizontal tube furnace. Source and drain Schottky-barriers are formed via physical vapor deposition of a SB metal with the desired metal semiconductor workfunction difference. The workfunction optimized metalization layer consists of nickel that is silicided in a subsequent anneal at a temperature of 500 °C, forming a Ni_xSi_y [9] at the metal semiconductor interface. For reasons of comparison, reference devices have been metallized with pure aluminum source/drain contacts, exhibiting asymmetric barriers for charge carrier injection at source and drain, respectively. The total NW width, which includes the gate oxide, is characterized to 90 nm by means of scanning electron microscopy, resulting in a Silicon-Fin width of ~75 nm. The Si-Fin height, with the oxide thickness already subtracted, is measured to 60 nm by atomic force microscopy. The total gate width can be calculated, as shown in Fig. 2(a) for the tri-gate configuration. Summing up the Fin height (I and III) and the Fin width (II) yields to a gate width of $W_G = 210$ nm. The overall NW length of the device is $L_T = 50$ μm, the gate length is $L_G = 5$ μm as shown in Fig. 1(a).

3. Results and discussion

For a better understanding of the device functionality, the NWFET is considered as a composition of two interacting transistors. Each of those two distinguished transistors is represented by its own gate contact, the frontgate and backgate, respectively. Fig. 2(a) shows a cross section through the NW-transistor that represents the transistor formed by the frontgate electrode. The

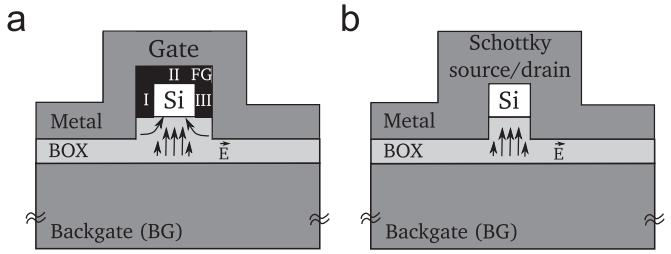

Fig. 2. Schematic cross section through the nanowire channel as indicated with section lines (A−A′ and B−B′) in Fig. 1(a). (a) Cross section of the NW channel beneath the frontgate contacted area. The frontgate is formed in a tri-gate configuration (I–III). (b) Cross section through the source/drain areas. The SB metal is in direct contact with the silicon NW. In both cases the underlying oxide (BOX) insulates the backgate electrode. The electric field $\vec{E}$ resulting from a voltage at the backgate electrode is illustrated with arrows. The section line A−A′ corresponds to the cut presented in (a), section line B−B′ corresponds to the cross section presented in (b).

respective backgate transistor can be found in Fig. 1(a). The transistor formed by the backgate electrode interacts with the entire NW channel region (L_T in Fig. 1(a)). However, the gate control of the transistor formed by the frontgate electrode is spatially limited in the center of the NW channel (L_G in Fig. 1(a)). The source and drain contacts are formed as illustrated in Fig. 2(b). The Schottky-barrier metal is in direct contact to the silicon NW channel. Following the discussion of the single NWFET device, the necessity of midgap Schottky-barrier source/drain contacts for CMOS operation will be discussed. Subsequently, results of a versatile voltage-selectable CMOS-NWFET inverter logic circuit will be presented.

3.1. Backgate control

First, experimental results on devices with midgap source/drain NiSi-SBs are presented. In this case, the barrier for electrons and holes is almost identical $\Phi_{B,h} \approx \Phi_{B,e}$ [9,10]. Fig. 3 shows a backgate voltage sweep of a NW channel from $-20\,V < V_{BG} < +20\,V$ at a constant drain bias of $V_{DS} = |2\,V|$. The measurements are performed at floating frontgate conditions. Well below the threshold voltage of the backgate transistor $V_{BG,T} = |4\,V|$, no significant current flow is observed between source/drain. This observation confirms that as without applied backgate voltage the source/drain current (I_{DS}) is negligible, despite the low background boron doping. The concept of an undoped NW channel helps to understand the functionality of the NWFET. The source/drain current flow drastically changes when a voltage $V_{BG} > |V_{BG,T}|$ is applied to the backgate (BG) electrode of the device resulting in a significant raise in source/drain current with an applied drain bias of $V_{DS} = |2\,V|$. The current in the left branch of Fig. 3 is due to hole conduction (filled squares), the right branch is attributed to electron conduction (open circles). The maximum hole current is slightly lower than the maximum electron current, $I_{DS,h,max} = 0.7\,\mu A < I_{DS,e,max} = 1.2\,\mu A$. This difference of $I_{DS,e}/I_{DS,h} = 1.8$ points towards different carrier mobilities for the two different backgate voltages. In fact, the current ratio does correspond well to a fundamental difference in electron and hole mobility in silicon with $\mu_e \approx 2\mu_h$ further supporting the presence of different charge carrier types.

Fig. 4 illustrates the three distinguished backgate conditions from a band diagram perspective. The schematic is based on simulations of the band structure with Synopsis Sentaurus [3]. In Fig. 4(a) no voltage is applied to the backgate and charge carriers originating from source or drain are not able to surmount the barriers at the respective metal semiconductor interfaces. Except for the thermally generated intrinsic electron–hole pairs, the NW channel is lacking of free charge carriers and no significant

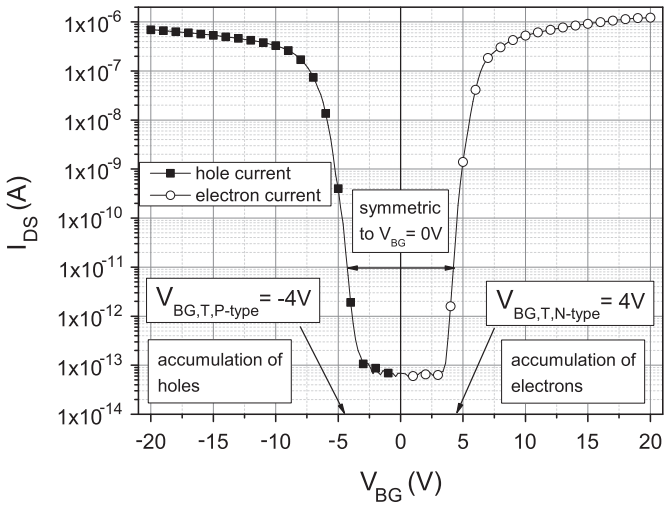

Fig. 3. Measured backgate characteristic of a fabricated NWFET device. The backgate is swept from $-20\,\mathrm{V} < V_{BG} < 20\,\mathrm{V}$, $V_{DS} = |2\,\mathrm{V}|$. The frontgate contact is intentionally left in floating condition. Two different symbol types are used for plotting the data of a single sweep to emphasize the difference in charge carrier type. The onset of conduction between source/drain is observed at $V_{BG,T} > |4\,\mathrm{V}|$. Here: $\Phi_M = 4.7$ eV, therefore $\Phi_{B,h} \approx \Phi_{B,e}$.

source/drain current is observed. When decreasing the backgate voltage below $V_{BG,T} < -4$ V as shown in Fig. 4(b), holes can tunnel through the source/drain barriers and accumulate at the backgate-oxide/NW interface. The mechanism of carrier injection is further illustrated in the inset in Fig. 4(b). In this case a hole channel is formed at the backgate-oxide/NW interface. Reversing the backgate voltage polarity to $V_{BG,T} > 4$ V as in Fig. 4(c), complementary inverse band bending is observed and electrons are able to tunnel from the source/drain contacts into the NW channel, as shown in the inset in Fig. 4(c). In this case an electron-channel is formed. For both cases the charge carriers are originating from the respective source and drain midgap Schottky-barrier contacts. These simulations support the idea that the backgate contact can be used to select the charge carrier type within the channel region. Obviously, the backgate transistor acts as an accumulation mode transistor, accumulating charge carriers (holes or electrons) at the backgate-oxide/NW interface depending on the polarity of the applied backgate bias. With the additional application of a source/drain voltage the injection of either holes or electrons is provided. As a result, the backgate determines the unipolar P-type and N-type FET behavior.

3.2. Frontgate control

When including the frontgate electrode to the device structure a single voltage selectable CMOS-NWFET is completed. The frontgate controls the flow of accumulated charge carriers from the source to the drain contact through the NW channel. The frontgate is implemented as a tri-gate structure providing very good electrostatic control over the entire cross-section of the NW channel area (see Fig. 2(a)). When the NW channel is selected as P- or N-type 'doped' by the backgate, the input characteristic of the frontgate can be measured.

In Fig. 5 the input characteristics of a NWFET at two different backgate voltages with appropriate polarities is shown. With the backgate voltage set to $V_{BG} = -20$ V, a P-type NWFET (P-NWFET) is formed, and a typical PMOS input characteristic is observed (filled squares). When the backgate voltage is interchanged in terms of polarity to $V_{BG} = +20$ V, the input characteristic of a N-type NWFET (N-NWFET) is observed (open circles). As expected from the measurements in Fig. 3 the maximum source/drain

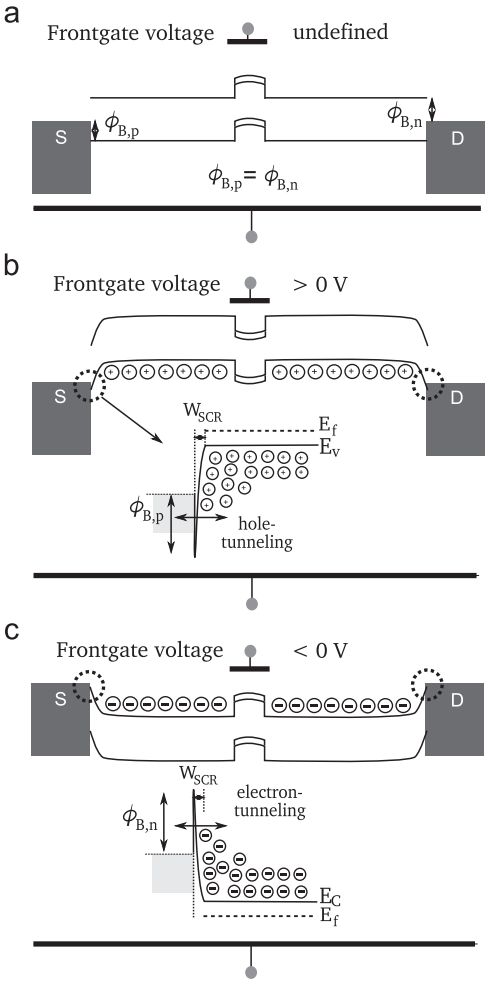

Fig. 4. Schematic banddiagram of the influence of the backgate voltage on the NW channel based on simulations with Synopsis Sentaurus. (a) No or insufficient voltage applied to the backgate $V_{BG,T} \sim 0$ V, (b) accumulation of holes in the NW channel for $V_{BG} < V_{BG,T,P} = -4$ V (inset: hole tunneling), (c) accumulation of electrons in the NW channel for $V_{BG} > V_{BG,T,N} = 4$ V (inset: electron tunneling). The impact of the frontgate on the band diagram is illustrated at different voltages.

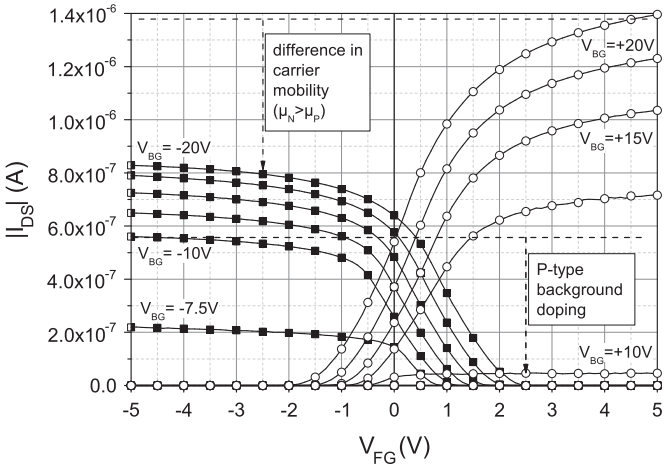

Fig. 5. Measured input characteristic of a CMOS-NWFET at contrary backgate bias polarity. The backgate voltage is stepped in $|2.5\,\mathrm{V}|$ steps from $|7.5\,\mathrm{V}|$ to $V_{BG} = |20\,\mathrm{V}|$, $V_{DS} = |2\,\mathrm{V}|$. Here: $\Phi_M = 4.7$ eV, therefore $\Phi_{B,h} \approx \Phi_{B,e}$.

current of the P-NWFET is lower than that of the N-NWFET discussed before by the difference in carrier mobility. This also supports the statement, that the low boron background doping

does hardly effect the device properties in the ON-state and the carrier mobilities determine the current ratio of NWFETs at equal W/L-ratio. When the transconductance is used to extract the charge carrier mobilities a ratio $\mu_e/\mu_h = 1.5$ is calculated. This value is in good agreement to the difference in source/drain current of 1.8 calculated in Section 3.1.

At $V_{BG} = |20\ \mathrm{V}|$ typical values for the subthreshold slope are in the range of $S_P = 100$ mV/dec and $S_N = 150$ mV/dec. The smaller the applied backgate voltage the better the subthreshold slope. This can be explained with an increase of scattering effects at the backgate oxide/NW interface with increasing backgate voltages. However, higher backgate bias automatically generates a higher maximum source/drain current as a result of the increased charge carrier density along the NW channel cross-section. Using the applied voltages various parameters of the NWFET transistor parameters can be tuned, which may be desirable for a specific application. The difference in source/drain current for the P-NWFET at $V_{BG} = -10$ V and the N-NWFET at $V_{BG} = +10.0$ V, is a residual effect of the low background boron doping of the used substrate and is related to the used prototype technology. Again, the use of very low-doped or even intrinsic SOI wafers will help to circumvent this issue.

Ultimatively, both a PMOS and NMOS can be represented by a single voltage-selectable NWFET device. This significantly reduces the complexity in circuit fabrication technology.

3.3. Non-midgap Schottky-barrier source/drain contacts

In the case that non-midgap Schottky-barriers are present at source/drain, one type of charge carriers (electrons or holes) will be preferred, depending on the workfunction asymmetry. To illustrate the effect of asymmetric barriers for electrons and holes reference devices have been fabricated with aluminum contacts at source and drain, where $\Phi_{B,h} \neq \Phi_{B,e}$. Aluminum is known to have different barriers for electrons and holes and it is not a midgap metal to silicon. The aluminum workfunction is $\Phi_{M,Al} = 4{,}2$ eV [11], so that the barrier for electrons is higher than for holes, $\Phi_{B,h} = 0.46\ \mathrm{eV} < \Phi_{B,e} = 0.65$ eV.

The backgate characteristic of such a reference device is shown in Fig. 6. As expected, the electron channel is not well established since the source/drain current of the N-NWFET is largely reduced. Neglecting the small difference in mobilities between electrons and holes, the electron carrier density induced at identical backgate bias is approximately four orders of magnitude lower than the hole carrier density, as obvious from the difference in source/drain current ΔI_{DS} in Fig. 6.

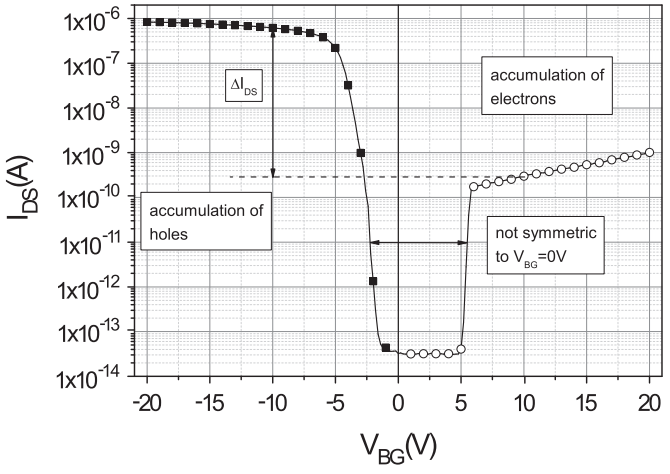

Fig. 6. Measured backgate characteristic of a fabricated NWFET reference device with aluminum contacts at source/drain. The backgate is swept from $-20\ \mathrm{V} < V_{BG} < 20\ \mathrm{V}$, $V_{DS} = |2\ \mathrm{V}|$. The frontgate contact is intentionally left in floating condition. Two different symbol types are used for plotting the data of a single sweep to emphasize the difference in charge carrier type. Here: $\Phi_M = 4.2$ eV, therefore $\Phi_{B,h} \neq \Phi_{B,e}$.

When looking at the complete NWFET, including the frontgate electrode in the reference devices with aluminum at source/drain, the difference is quite obvious when comparing the input characteristics of the N-NWFET and the P-NWFET at linear scale as shown in Fig. 7. Only the P-NWFET (filled squares) exhibits a swing to the maximum possible amount of source/drain current. The maximum current of the reference P-NWFET is $I_{DS,ref,max} = 1.35$ μA. This is notably higher than the maximum source/drain current of the device presented in Fig. 5 (filled squares) with $I_{DS,midgap,max} = 0.82$ μA, indicating that the hole barrier of aluminum is lower than that of the midgap Ni_xSi_y. In contrast, the N-NWFET (open circles) is severely degraded, as indicated by the difference in source/drain current ΔI_{DS}. The input characteristic of the device is no longer symmetrical with respect to the ON-current when compared with a midgap source/drain metal as shown in Fig. 5.

Consequently, only when midgap source/drain contacts are used, a suitable voltage-selectable CMOS-NWFET can be ralized by the very same NWFET device structure.

3.4. CMOS-NWFET inverter

To demonstrate the capabilities of the invented device concept, two workfunction optimized midgap Ni_xSi_y NWFETs are electrically connected to form a CMOS-NWFET inverter. A schematic of such a setup is shown in Fig. 1(b). Both NWFETs in this schematic are identical from a fabrication point of view. Using an adjusted backgate bias, such as shown in Fig. 8, two almost perfectly matching transistor characteristics are achieved. Therefore, the backgate voltage of the N-NWFET (open circles) has been slightly reduced to $V_{BG,N} = 18$ V in order to adjust the maximum source/drain current to those of the P-NWFET (filled squares) where $V_{BG,P} = -20$ V. These electrically adjusted and matching NWFETs are used to demonstrate the resulting CMOS-NWFET-inverter functionality by means of the inverter transfer characteristic (open stars). The input voltage is varied from $-2\ \mathrm{V} < V_{IN} < +2$ V and switching with respect to the input signal occurs at 0.75 V. The transfer characteristic is typical for a CMOS inverter, as identified from the characteristic cross current I_{CC} (filled stars). In fact these observations indicate that the NWFET circuit operates as a true CMOS inverter and not as an inverter with resistive load, where

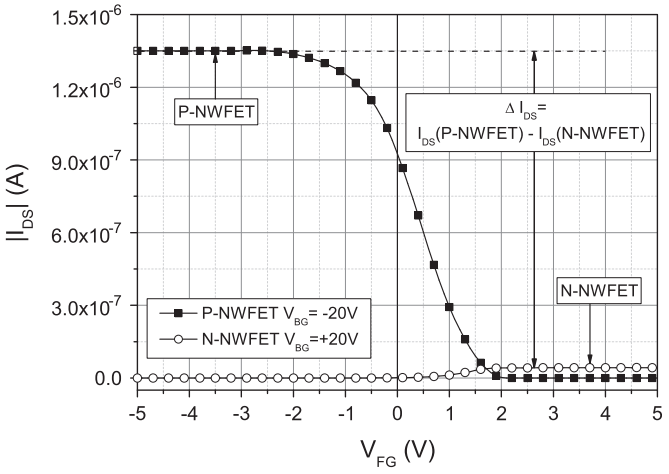

Fig. 7. Measured input characteristics of a NWFET at contrary backgate bias polarity $V_{BG} = |20\ \mathrm{V}|$. Here: $\Phi_M = 4.2$ eV, therefore $\Phi_{B,h} \neq \Phi_{B,e}$, $V_{DS} = |2\ \mathrm{V}|$. ΔI_{DS} is the difference in source/drain current from P-NWFET and N-NWFET.

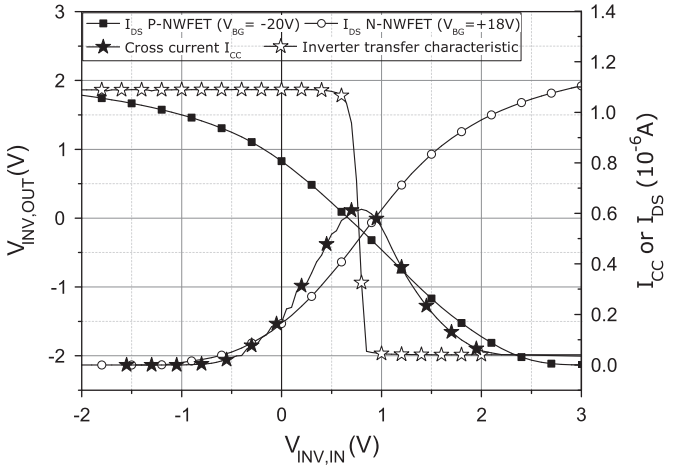

Fig. 8. (Open stars) Inverter transfer characteristic of a CMOS-NWFET inverter and (filled stars) inverter cross current. The backgate voltage of the N-NWFET was slightly reduced to achieve the same source/drain current levels of the separate devices (squares and circles).

permanent current flow would be present when providing a logic '0' at the inverter output.

When interchanging the backgate bias, i.e. *NW*1 is selected to work as N-NWFET and *NW*2 as P-NWFET and after interchanging the supply voltage, again well established CMOS-NWFET inverter behavior is observed.

This supports the usability of the presented NWFET device for the use in versatile, voltage selectable, freely reconfigurable logic circuits.

4. Conclusion

We fabricated and demonstrated the advantages of a versatile CMOS-NWFET device concept on SOI with midgap Schottky-barrier source and drain contacts. CMOS-NWFETs can serve as supplemental building blocks in logic circuits, regarding its possibility to select the transistor type, i.e. P-NWFET and N-NWFET. The selection process is reversible and can be repeated as often as needed. The full potential of the circuit architecture is expected on MultiSOI^{TM} substrates, consisting of two stacked layers of silicon and BOX as illustrated in Fig. 1(b). Using these substrates each backgate electrode of the NWFETs can be selected individually.

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