The Electrical Properties and Stability of the Hafnium Silicate/$Si_{0.8}Ge_{0.2}$(100) Interface

S. ADDEPALLI,[1,2] P. SIVASUBRAMANI,[1,3] M.J. KIM,[1,3] B.E. GNADE,[1,3] and R.M. WALLACE[1,3,4]

1.—Department of Materials Science and Engineering, University of North Texas, Denton, TX 76203. 2.—Present address: GE John F. Welch Technology Center, Bangalore-560066, India. 3—Present address: University of Texas at Dallas, Department of Electrical Engineering, Richardson, TX 75083. 4.—E-mail: rmwallace@utdallas.edu

The effect of post-oxidation N_2 annealing and post-metallization forming-gas annealing on the electrical properties of Pt/Hf-silicate (3 nm)/$Si_{0.8}Ge_{0.2}$(100)/n-type Si(100) metal-oxide semiconductor (MOS) capacitors is reported. Capacitance-voltage (C-V) and current density-voltage (J-V) measurements of as-grown, 3-nm-thick, hafnium-silicate films containing ~12at.%Hf indicate a large number of bulk and interface traps with a current density of $\sim 10^{-2}$ A/cm^2 at V_{FB} + 1 V. Post-ultraviolet (UV)/O_3 oxidation annealing in N_2 at 350°C for 30 min leads to a significant improvement in the electrical characteristics of the film. A post-metallization anneal (PMA) at 450°C for 30 min in forming gas (90% N_2:10% H_2), however, degraded the electrical properties of the films. X-ray photoelectron spectroscopy (XPS) analyses of the forming-gas-annealed films indicate that a possible cause for the degradation in electrical properties is the hydrogen-induced reduction of GeO_2 in the interfacial $Si_xGe_{1-x}O_2$ oxide layer to elemental germanium. Implications for the introduction of hafnium silicate as a viable gate dielectric for SiGe-based devices are discussed.

Key words: High-k, dielectric, complementary metal-oxide semiconductor (CMOS), SiGe, silicate

INTRODUCTION

The rapid reduction in silicon-based integrated circuit dimensions to produce high-speed, high-performance devices operating at low power has necessitated the implementation of new materials into the existing complementary metal-oxide semiconductor (CMOS) technology.[1] Strained Si_xGe_{1-x}(100) epilayers on Si(100) have attracted considerable interest because of hole mobility enhancement as well as their compatibility with existing Si-based CMOS technology that makes manufacturing very large-scale integrated circuits feasible.[2] However, because of the complex oxidation chemistry[3,4] of Si_xGe_{1-x} and the instability[5–7] of $Si_xGe_{1-x}O_2$, devices have been fabricated with the strained Si_xGe_{1-x} channel covered with a Si capping layer that is subsequently oxidized to produce the gate oxide.[8] While the Si buffer layer affords a gate oxide (SiO_2) with outstanding electrical properties as well as a stable, high-quality Si/SiO_2 interface, it can also result in a parasitic, decreased mobility conduction channel, limiting the ultimate mobility that could be achieved with strained Si_xGe_{1-x}(100).[8,9] In addition, because of direct tunneling and concerns regarding dielectric reliability and breakdown strength as well as resistance to dopant penetration, ultrathin SiO_2 must be replaced by a physically thicker gate oxide material with a higher dielectric constant.[10] Therefore, in order to fully exploit the high carrier mobility in the case of high-performance SiGe-based devices, it is desirable to deposit a stable high-κ dielectric material in direct contact with Si_xGe_{1-x}(100).

Some of the high-κ dielectric materials investigated so far as viable candidates for Si_xGe_{1-x}-based CMOS technology are gadolinium gallium garnet, Gd_2O_3, Ga_2O_3, Y_2O_3,[11] nitrided La_2O_3,[12] HfO_2,[13] and ZrO_2.[14,15] Hole mobility enhancement relative to

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control samples prepared with a Si(100) channel layer was reported for surface-channel, p-metal-oxide semiconductor field-effect transistors fabricated with nitrided La_2O_3,[12] HfO_2,[13] and ZrO_2[15] deposited directly on Si_xGe_{1-x}(100). Apart from low leakage current and high reliability, the desirable material properties of a gate dielectric include a higher permittivity than SiO_2 (i.e., $\kappa > 3.9$), thermodynamic stability in direct contact with the underlying channel, negligible out-diffusion into the channel region, and an amorphous structure under the processing conditions used.[10] Based on these requirements, the pseudobinary alloy of SiO_2 and HfO_2 (hafnium silicate) has been identified as a promising gate-dielectric candidate for Si-based devices. [10,16–19]

We previously demonstrated that ultrathin hafnium-silicate films could be produced in direct contact with Si_xGe_{1-x}(100) substrates at room temperature by ultraviolet (UV)-O_3 oxidation of sputter-deposited hafnium silicide.[20] In this paper, we report the electrical properties of the hafnium silicate (HfSiO) films deposited on Si_xGe_{1-x}(100) using the UV-O_3 oxidation approach, and the effect of post-oxidation annealing (POA) in N_2 and postmetallization annealing (PMA) in forming gas. Implications for the introduction of hafnium silicate as a viable gate dielectric for SiGe-based devices are also discussed.

EXPERIMENT

The 250-Å thick, undoped, strained $Si_{0.8}Ge_{0.2}$ epitaxial layers were grown onto Sb-doped, n-type Si(100) substrates (ρ = 0.01–0.02 Ω-cm).[21] Prior to epitaxial layer growth, the wafers received a dilute (100:1) H_2O:HF dip to remove the native oxide, followed by a deionized water rinse and spin dry. After loading into the epitaxial reactor, each wafer received a brief 850°C bake in reduced pressure hydrogen, then was cooled to 700°C, and the $Si_{0.8}Ge_{0.2}$ epitaxial layer was grown from germane and dichlorosilane in hydrogen. From the lattice constant obtained by high-resolution transmission electron microscopy (HRTEM) imaging, the Ge concentration in the epitaxial layers was deduced to be 17–20%.

The $Si_{0.8}Ge_{0.2}$(100) substrates were subjected to a methanol degreasing step,[22] followed by a 0.5% HF etching step to remove the native oxide. Hafnium silicate (3-nm thick) films were grown on these $Si_{0.8}Ge_{0.2}$(100) substrates at room temperature by direct current (DC)-magnetron sputtering from a pressed-powder hafnium-silicide target with subsequent in-situ UV-O_3 oxidation.[20] The UV-O_3 oxidation conditions were optimized to minimize the formation of a $Si_xGe_{1-x}O_2$ interfacial layer within the detection limit of x-ray photoelectron spectroscopy (XPS), by monitoring the Ge(L_3MM) x-ray-excited Auger feature.[20] The XPS spectra presented in this paper were acquired with a standard Al Kα x-ray source, operated at a power of 280 W, and an electrostatic analyzer, operated in the constant pass-energy mode (20 eV). All spectra were referenced to the Si 2p feature from the $Si_{0.8}Ge_{0.2}$(100) substrate at 99.5 eV.

Metal-insulator semiconductor (MIS) capacitors of Pt (100–120 nm)/Hf-silicate/$Si_{0.8}Ge_{0.2}$(100)/n-type Si(100) with areas ranging from 2×10^{-3} to 8×10^{-5} cm^2 were fabricated by electron-beam evaporation of Pt through a shadow mask, followed by aluminum sputtering on the backside to reduce contact resistance between the substrate and the measurement probe. Capacitance-voltage (C-V) and current density-voltage (J-V) characteristics of the dielectric films were measured at room temperature using Agilent 4294A precision impedance and 4156B precision semiconductor parameter analyzers (Palo Alto, CA), respectively. The C-V curves were recorded by sweeping the Pt electrode voltage from the inversion to the accumulation region and then in the reverse direction to obtain hysteresis data. The C-V results reported here were measured at a frequency of 100 kHz. All electrical measurements were conducted in an electrically shielded dark box. Dielectric constants were calculated from capacitance density maxima in the accumulation region.

RESULTS AND DISCUSSION

The C-V and J-V characteristics of the MIS capacitor structures fabricated with an unannealed HfSiO film are presented in Fig. 1. This film was grown by sputter deposition of a ~1.3-nm-thick, hafnium-silicide film onto clean $Si_{0.8}Ge_{0.2}$(100) followed by in-situ UV-ozone oxidation at room temperature.[20] The fully oxidized HfSiO film is 3-nm thick as verified by cross-sectional HRTEM.[20] By using ex-situ XPS analysis, it was confirmed that, within the detection limit of the technique, the oxidation parameters used did not lead to the growth of a low-κ interfacial-oxide layer because of the oxidation of the $Si_{0.8}Ge_{0.2}$(100) substrate.[20] The C-V curve with the unannealed HfSiO film (Fig. 1a) exhibits substantial stretch-out, indicative of interface trapped charges.[23,24] In addition, the C-V curve indicates hysteresis with the flat-band voltage (V_{FB}) shifted toward a relatively positive value by ~150–200 mV when the voltage is swept from accumulation to inversion. The flat-band voltage (V_{FB}), defined as the gate voltage corresponding to the flat-band capacitance (C_{FB}), is estimated from the equation $V_{FB} \cong W_{ms} - \frac{Q_f}{C_{ox}}$, where W_{ms} is the difference in work function between the metal gate and the semiconductor, Q_f is the fixed charge, and C_{ox} is the oxide capacitance per unit area. Because the work function of the $Si_{0.8}Ge_{0.2}$ substrate is not available, V_{FB} was obtained by plotting dC/dV versus the applied voltage. Such hysteresis of C-V curves is commonly observed in the electrical characteristics of as-deposited, high-κ dielectric films.[25,26] The existence of hysteresis is associated with trapped charges and defects in the oxide film.[23] The insulator-trapped charge density (N_{ot}) in the unannealed HfSiO film

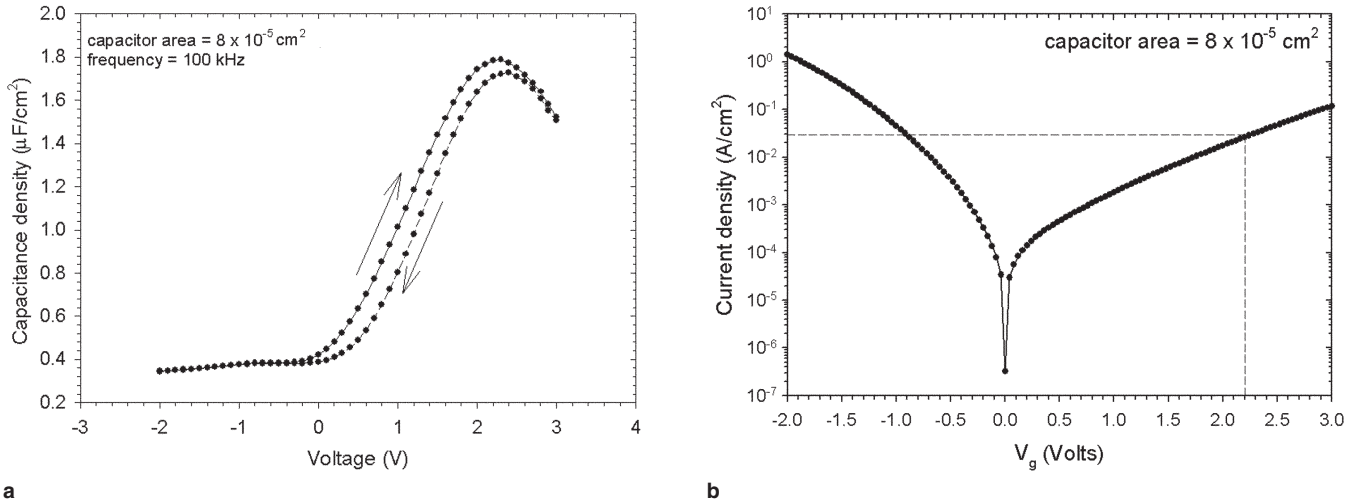

Fig. 1. (a) The C-V trace showing hysteresis and (b) J-V characteristics of Pt/Hf-silicate (3 nm, as-deposited)/$Si_{0.8}Ge_{0.2}$(100).

was evaluated to be $1.7 \times 10^{12}-2.4 \times 10^{12}$ cm^{-2} using the following equation:[24]

$$N_{ot} = C_{acc} \times \Delta V_{FB}/(qA) \qquad (1)$$

where C_{acc} is the accumulation capacitance, ΔV_{FB} is the shift in the flat-band voltage, q is the electronic charge, and A is the effective capacitor electrode area. The rollover in the C-V curve at high gate voltages ($V_g > 2$ V; Fig. 1a) is ascribed to a high leakage current,[27] as confirmed by the J-V results shown in Fig. 1b ($J = 10^{-2}$ A/cm^2 at $V_g = V_{FB} + 1$ V). The dielectric constant ($\kappa = 6.1$) is consistent with the value expected for the hafnium and silicon content (both Hf and Si are ~12–13 at.%) in the as-deposited hafnium-silicate film.[28] The capacitance-equivalent thickness of this film (i.e., without quantum mechanical correction) is 1.9 nm.

The electrical properties of the HfSiO films subjected to a post-UV/O_3 oxidation anneal are presented in Fig. 2. No significant improvement in the electrical properties of the hafnium-silicate films relative to the unannealed film was observed after a POA in N_2 at 250°C (not shown). In comparison with the C-V results recorded for unannealed HfSiO films (Figs. 1a and 2a), the stretch-out in the C-V curves is considerably lowered after N_2 annealing at temperatures ≥350°C (Fig. 2a), indicating a decrease in the interface trap density. In addition, a significant reduction in hysteresis is observed. A ΔV_{FB} of ~30–35 mV is observed for the HfSiO film subjected to a POA in N_2 at 350°C for 30 min while the hysteresis is <20 mV in the case of films subjected to a POA in N_2 at 450°C or for 1 h at 350°C. In contrast to the C-V behavior observed in case of the unannealed HfSiO films, the accumulation capacitance of the N_2-annealed hafnium-silicate films does not decrease at high gate voltages (Fig. 2a). The absence of rollover in the C-V curves of the POA films is consistent with a decrease in the leakage current relative to the unannealed HfSiO films ($\sim 5 \times 10^{-3}-8 \times 10^{-3}$ A/cm^2 at $V_g = V_{FB} + 1$ V; Fig. 2b). The accumulation capacitance of the sample annealed in N_2 at 350°C for 30 min corresponds to a dielectric constant (κ) of 7.2 and a capacitance

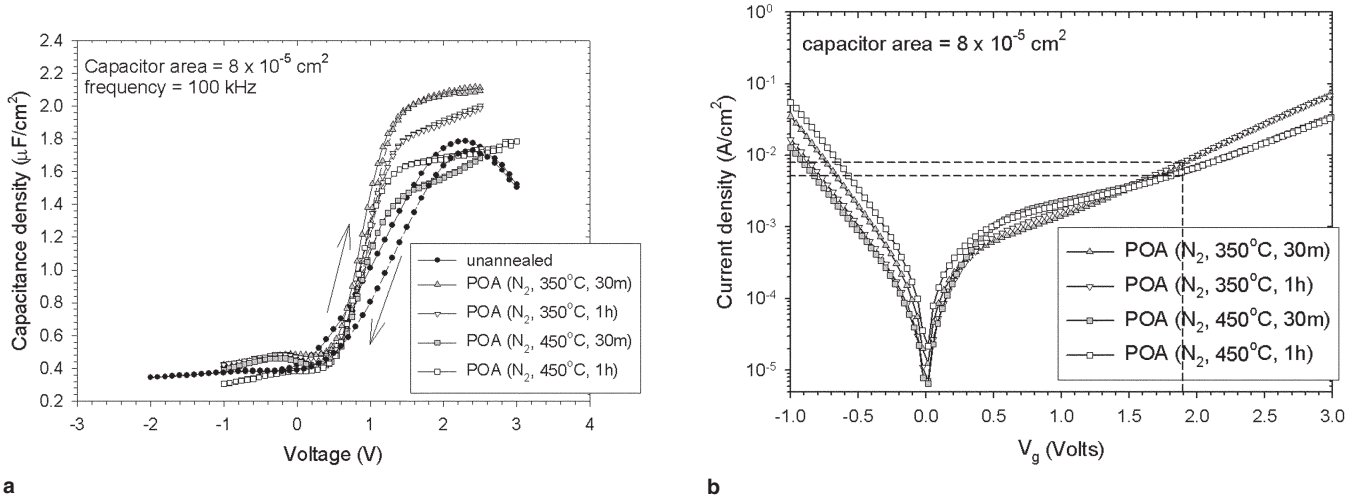

Fig. 2. Effect of POA for various time intervals in N_2 at T ≥ 350°C on the (a) C-V properties and hysteresis and (b) J-V properties of Pt/Hf-silicate/$Si_{0.8}Ge_{0.2}$(100) capacitor.

equivalent thickness (i.e., no quantum mechanical corrections have been made to the data) of 1.6 nm.

The enhancement in accumulation capacitance and the simultaneous reduction in leakage current density caused by N_2 annealing are attributed to the densification and improvement in the atomic network of the hafnium-silicate film. Improvement in C-V characteristics and leakage current density of high-κ dielectrics as a result of annealing in N_2 has been previously reported.[25,29–31] Refractive index measurements demonstrated that annealing in a N_2 ambient leads to the densification of the dielectric films.[31]

Post-oxidation N_2 annealing at 450°C or for a longer time period at 350°C induces the growth of an interfacial-oxide layer, as evidenced by the decrease in the accumulation capacitance density in the C-V data (Fig. 2a). However, this is not accompanied by a dramatic decrease in the leakage current density (Fig. 2b). The formation of an interfacial-oxide layer caused by the presence of trace levels of O_2 present in N_2 has been reported by several research groups.[32–34] Studies have also demonstrated that an oxygen-enriched dielectric film is a potential source for oxygen, and at adequately high annealing temperatures, the excess oxygen in the dielectric could react with the underlying substrate to produce a low-κ interfacial-oxide layer.[35] Based on the electrical results obtained, annealing in N_2 at 350°C for 30 min was chosen as the optimum POA condition.

Post-metallization forming-gas sintering at 400–450°C is generally employed in Si-based MOS devices to minimize contact resistance between the backside Al contact and the substrate and to passivate unsaturated bonds within the dielectric, particularly at the dielectric/substrate interface.[36] In addition to the desirable interface-trap passivation effect, several studies have demonstrated that annealing in hydrogen at temperatures >500°C is associated with the degradation of MOS device performance caused by the generation of interface traps under hot-carrier or radiation-stress conditions.[37–39]

In this study, the post-oxidation N_2-annealed (350°C and 450°C) HfSiO films were subjected to a PMA in forming gas (90% N_2 + 10% H_2) at 450°C for 30 min. The results for this anneal are given in Fig. 3. A comparison of the C-V curves for the unannealed HfSiO film, the HfSiO film subjected to POA (N_2 at 350°C for 30 min), a HfSiO a film subjected to a POA (N_2 at 350°C for 30 min), and PMA in forming gas (450°C, 30 min) is shown in Fig. 3b. The C-V curves are distorted in shape after a PMA (Fig. 3a and b). In addition, forming-gas annealing causes a stretch-out of the C-V curves, indicating the generation of interface traps.[23,24] Similar trends were observed in the case of $Si/SiO_2/Si$ structures subjected to forming-gas annealing at temperatures >500°C.[37,40] Moreover, the leakage current measured for the forming-gas annealed Pt/hafnium silicate/$Si_{0.8}Ge_{0.2}$(100) capacitors ($J \cong 8 \times 10^{-2}$ A/cm^2 at $V_g = V_{FB} + 1$ V) is an order of magnitude higher than that of the hafnium-silicate samples annealed in N_2 only (Fig. 3c). In sharp contrast, PMA in forming gas under identical conditions improves the electrical properties of metal/HfSiO/Si(100) capacitors.[18,19,28] Therefore, the degradation in the electrical properties of these MIS capacitors after annealing in forming gas is likely to be associated with the thermally induced relaxation of the strained $Si_{0.8}Ge_{0.2}$(100) substrate or the stability of the hafnium silicate/$Si_{0.8}Ge_{0.2}$(100) interface and not the hafnium-silicate film. The generation of misfit dislocations as a result of substrate relaxation is not expected to occur at the temperatures used in this study.[41] Moreover, if the thermally induced relaxation of the strained $Si_{0.8}Ge_{0.2}$ substrate was the cause for the degradation in electrical properties, one would expect to observe this behavior even in the case of hafnium-silicate films annealed in N_2 at 450°C. The C-V and J-V results for Pt/HfSiO/$Si_{0.8}Ge_{0.2}$(100) annealed at 450°C in N_2 (Fig. 2) rule out this possibility.

One possible explanation for the degradation in electrical properties of Pt/hafnium silicate/$Si_{0.8}Ge_{0.2}$(100) annealed at 450°C in forming gas could be the interaction of H_2 with Ge-related defects at the hafnium silicate/$Si_{0.8}Ge_{0.2}$ interface, as has been reported in the case of GeO_2-SiO_2 (germanosilicate) glasses. The reaction, which occurs at temperatures as low as 100°C, is controlled by the diffusion of hydrogen in the germanosilicate glass.[42–44] It is proposed that hydrogen molecules mainly react at

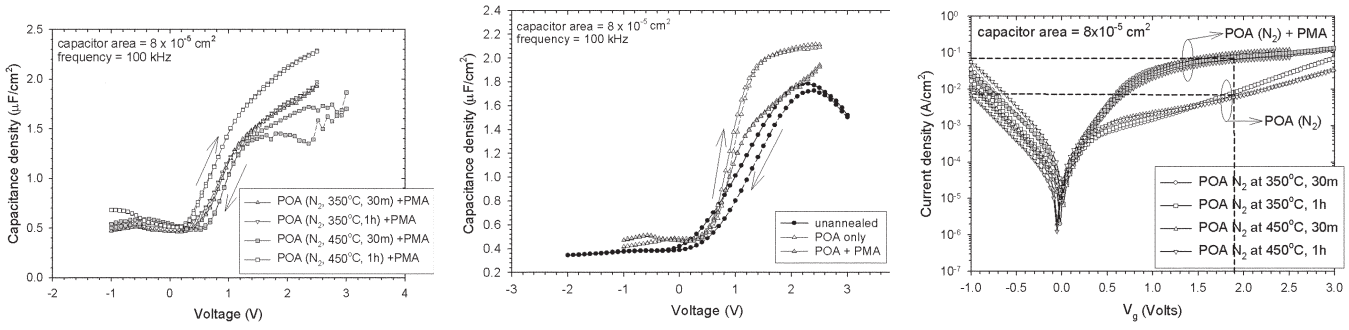

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Fig. 3. (a) Effect of PMA in forming gas at 450°C for 30 min on the C-V properties of Pt/Hf-silicate/$Si_{0.8}Ge_{0.2}$(100). (b) Comparison of the C-V curves for as-deposited, POA in N_2 (350°C for 30 min) and additional PMA in forming gas. (c) Effect of annealing in forming gas on the J-V properties.

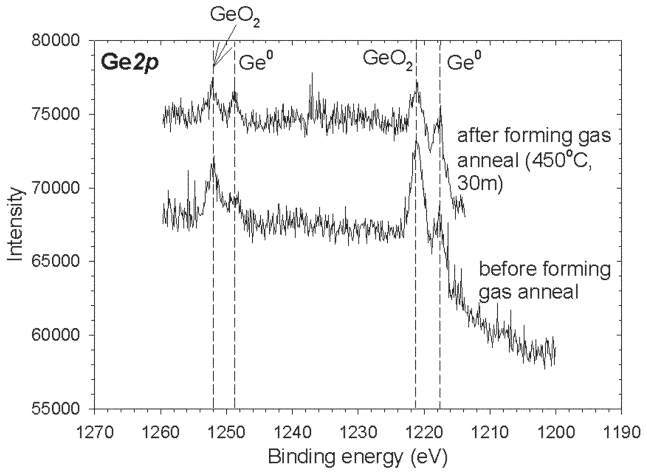
Ge-related defects, such as (1) a three-fold coordinated germanium atom with an unpaired electron on an sp^3 orbital (GeE'); (2) Ge-O deficient centers, such as Ge-Si bonds; or (3) a divalent Ge atom with a lone-pair electron (germanium lone-pair center (GLPC)).[44] The actual reduction mechanism is temperature dependent.[44] At temperatures <200°C, H_2 molecules react with GeE' centers to produce germanium monohydride defects (Ge-H). At annealing temperatures >200°C, hydrogen molecules react concurrently with Ge-O-Si bonds to form Ge-H as well as GLPC defects.[44]

To understand whether the degradation in electrical properties caused by PMA in forming gas is related to the interaction of H_2 with the HfSiO/$Si_{0.8}Ge_{0.2}$(100) interface, a ~1-nm-thick hafnium-silicide film was deposited on $Si_{0.8}Ge_{0.2}$(100) by DC magnetron sputtering at 25 W power for 2 min with subsequent UV/O_3 oxidation for 15 min. This film was then subjected to a POA in N_2 at 450°C for 1 h to intentionally produce a low-κ $Si_xGe_{1-x}O_2$ interfacial-oxide layer, followed by annealing in forming gas at 450°C for 30 min. A similar sample was prepared for HRTEM and capped with a ~60-nm-thick Pt film prior to forming-gas annealing. The Ge 2p spectra of the uncapped hafnium-silicate film before and after the forming-gas anneal are shown in Fig. 4a.[20] A significant decrease in the intensity of the peak corresponding to GeO_2 is observed after forming-gas annealing while the relative intensity of the Ge^0 feature increased, indicating reduction of germanium oxide to elemental germanium. Therefore, the degradation in the electrical properties of the Pt/hafnium silicate/$Si_{0.8}Ge_{0.2}$(100) capacitors annealed in forming gas may be attributed to the hydrogen-induced reduction of GeO_2 in the $Si_xGe_{1-x}O_2$ interfacial-oxide layer to elemental germanium according to the chemical reaction:

$$GeO_2 + 2\,H_2 \rightarrow Ge + 2\,H_2O \qquad (2)$$

Earlier studies have demonstrated that GeO_2 in $Si_xGe_{1-x}O_2$ is thermodynamically unstable and readily converted to elemental germanium either upon aging or annealing in a hydrogenic environment.[5–7,45] The formation of Ge nanocrystals when a $Si_xGe_{1-x}O_2$ film is annealed in H_2 at temperatures ≥700°C has been confirmed by cross-sectional TEM[6] and cross-sectional atomic force microscopy (AFM).[45] In our experiments, analysis of cross-sectional TEM images (Fig. 4b) of Pt/HfSiO/$Si_xGe_{1-x}O_2$/$Si_{0.8}Ge_{0.2}$(100) structures annealed in forming gas at 450°C for 30 min showed two layers of slightly different contrast. We note that in HRTEM imaging, variations in contrast strongly depend not only on projected atomic potential but also on the local specimen thickness variation as well as imaging conditions. From the results of the Ge 2p spectra of the film shown in Fig. 4a, combined with angle-resolved XPS analyses,[20] the film of lighter contrast closer to the $Si_{0.8}Ge_{0.2}$(100) substrate is attributed to a $Si_xGe_{1-x}O_2$ interfacial layer designated as SiGeO IL in the HRTEM image. The film with a slightly darker contrast is the hafnium-silicate film, labeled HfSiO in the HRTEM image (Fig. 4b). In sharp contrast to the Ge 2p XPS spectra shown in Fig. 4a, the HRTEM images did not detect nanocrystallite formation possibly because of the annealing temperature used.

The dielectric/semiconductor interface plays a crucial role in determining the overall electrical performance of the MOS gate stack in all high-performance devices.[10] In the case of Si-based devices, the presence of a thin, interfacial SiO_2 layer is beneficial because it enhances the electrical properties of the stack caused by the high-quality Si/SiO_2 interface although the overall capacitance would be compromised. In the case of Si_xGe_{1-x}-based devices, however, the formation of an interfacial oxide ($Si_xGe_{1-x}O_2$) would be detrimental because of the inherent thermodynamic instability of GeO_2. The results of this study indicate that hafnium silicate



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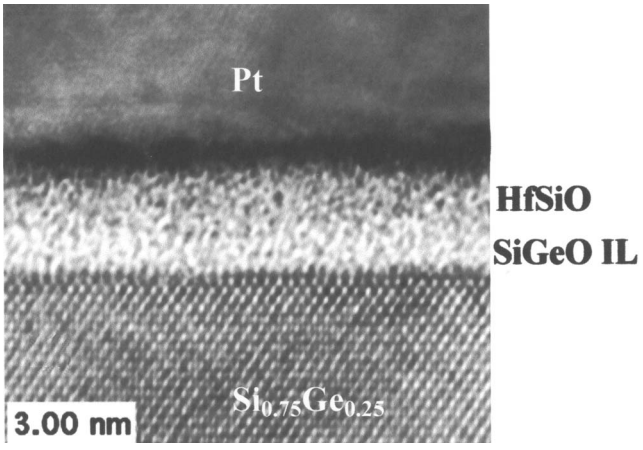

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Fig. 4. (a) The Ge 2p XPS spectra of a hafnium-silicate film (subjected to post-UV/O_3 anneal in N_2 at 450°C for 1 h) before and after annealing in forming gas at 450°C for 30 min. (b) The HRTEM image of Pt/Hf-silicate/$Si_xGe_{1-x}O_2$/$Si_{0.8}Ge_{0.2}$(100) annealed in forming gas at 450°C for 30 min after Pt deposition.

does not form a stable interface with $Si_{0.8}Ge_{0.2}$(100) upon forming-gas anneals at 450°C.

CONCLUSIONS

The effects of N_2 and forming-gas annealing on the electrical properties of Pt/hafnium silicate (3 nm)/$Si_{0.8}Ge_{0.2}$(100) capacitors were examined. While POA in N_2 improved the electrical properties of the hafnium silicate-$Si_{0.8}Ge_{0.2}$(100), PMA in forming gas resulted in the formation of interface traps, as evidenced by the shape of the C-V curves as well as an increase in leakage current. The degradation in electrical properties after forming-gas anneal is attributed to the interaction of hydrogen with germanium oxide or germanium-related defects at the hafnium silicate/$Si_{0.8}Ge_{0.2}$(100) interface.

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