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Digital Self-Calibration Technique Based on 14-Bit SAR ADC*

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Abstract: An error correction technique to achieve a 14-bit successive approximation register analog-to-digital converter (SAR ADC) is proposed. A tunable split capacitor is designed to eliminate the mismatches caused by parasitic capacitors. The linearity error of capacitor array caused by process mismatch is calibrated by a novel calibration capacitor array that can improve the sampling rate. The dual-comparator topology ensures both the speed and precision of the ADC. The simulation results show that the SAR ADC after calibration achieves 83.07 dB SNDR and 13.5 bit ENOB at 500 kilosamples/s.

Keywords: SAR ADC; capacitor mismatch; error correction technique; split capacitor DAC

The successive approximation register analog-to-digital converter (SAR ADC) with comprehensive advantages of low power consumption and moderate resolution[1], has been widely used in modern very large scale integration (VLSI) and system on chip (SoC)[2]. However, at resolutions of 10 bit and beyond, the precision of the SAR ADC is limited by the linearity error caused by parasitic capacitors[3] and process mismatch[4,5]. Currently, the main method to improve the precision of the SAR ADC is to use digital calibration technique[6-9]. This paper presents an error correction method based on a 14-bit SAR ADC to correct the mismatches of the main digital-to-analog converter (DAC). The split capacitor is digitally tuned to eliminate the mismatches caused by parasitic capacitors. A novel calibration capacitor array is used to improve the sampling rate. The dual-comparator topology of ADC ensures the speed and precision.

1 Principle

The linearity error of the main DAC is mainly due to two factors, namely parasitic effect caused by split capacitors and capacitor mismatch caused by manufacture process.

Fig.1 shows the structure of the proposed main DAC, which is a 14-bit split capacitor array designed with the high 6-bit, middle 4-bit, and low 4-bit arrays. C_{p1} is the parasitic capacitor caused by the split capacitor C_b, while C_{p2} is the parasitic capacitor in the middle arrays[10]. The mismatch caused by C_a is negligible[11]. In the ideal condition with no parasitic capacitors, the equivalent capacitor C_H from V_H to ground is 4 080 C/4 081 when the low-bit capacitors are all grounded. Taking C_{p1} and C_{p2} into consideration,

$$C_H = (4\,080\,C + 3\,825C_{p1} + 240\,C_{p1}\,C_{p2}) / (4\,081 + 240C_{p1} + 240C_{p2}) \quad (1)$$

From Eq.(1), it is obvious that the existence of parasitic capacitors will cause mismatch when ADC converts from high-bit to low-bit capacitors, which leads to serious error to the final value code.

An N-bit weighted capacitor DAC is shown in Fig.2. Due to the process variation, the capacitors would not completely match with others. The specific calibration principle of process mismatch of capacitors based on the 14-bit SAR ADC is described below. In the sampling phase, as Fig.3 shows, the top plate of high-bit capacitors is connected to V_{CM}. In addition, the reference voltage V_{ref} is sampled on all the capacitors except the MSB capacitor C_{14}. Assuming that the equivalent value of all capacitors except C_{14} is C_Y, the voltage on high-bit capacitor array, which is denoted as V_{X_n}, will be V_{CM}. Next, in the con-version phase, the charge is redistributed by reversing the switch configuration.

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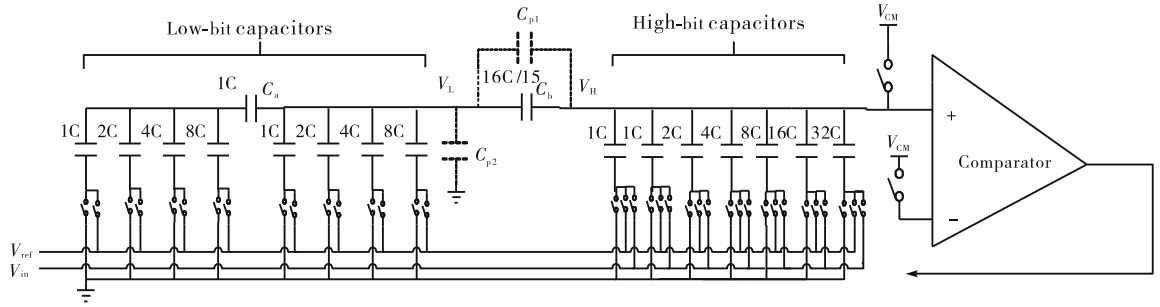


Fig.1 Proposed split main DAC array considering parasitic capacitors

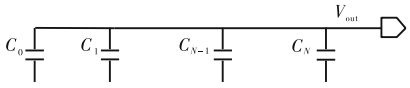


Fig.2 *N*-bit weighted capacitor DAC

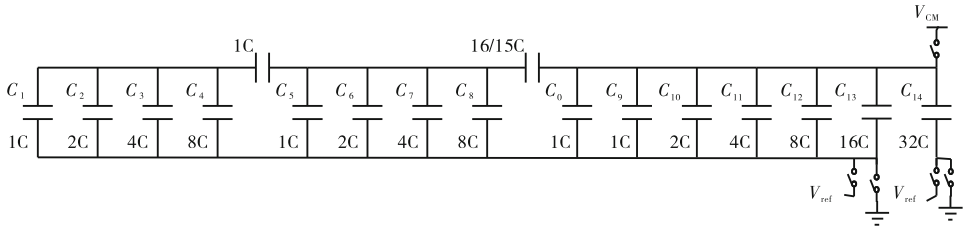


Fig.3 C_1 calibration

In the ideal case with no capacitor mismatch, the charge on the top plate should be unchanged, and the voltage at this moment is still V_{CM}. However, due to capacitor mismatch, the voltage becomes

$$V'_{X_{14}} = V_{\mathrm{CM}} + V_{\mathrm{ref}}(C_{14} - C_Y)/(C_{14} + C_Y) \tag{2}$$

The error voltage ΔV_{X_n} is the difference between ideal and actual voltage:

$$\Delta V_{X_{14}} = V'_{X_{14}} - V_{X_{14}} = V_{\mathrm{ref}}(C_{14} - C_Y)/(C_{14} + C_Y) \tag{3}$$

Due to $\sum_{i=0}^{13} 2^{i-1}\sigma_i = -2^{13}\sigma_{14}$ [12],

$$\Delta V_{X_{14}} = \sigma_{14} V_{\mathrm{ref}} = 2V_{\sigma_{14}} \tag{4}$$

According to the above-mentioned method, the mismatch voltage of the ith capacitor V_{σ_i} is calculated by

$$V_{\sigma_i} = 1/2\left(V_{X_i} - \sum_{j=i+1}^{14} V_{\sigma_j}\right) \tag{5}$$

2 Implementation

2.1 Calibration of split capacitor

In the ideal condition with no parasitic capacitors, the split capacitor C_{b} should be 16C/15 (300 fF) when the unit capacitor of the main DAC is 281 fF. However, the mismatch on the split capacitor can greatly affect the precision of ADC. A solution to this problem is to make the split capacitor tunable[13]. The schematic of the tunable capacitor C_{b} is shown in Fig.4. The value of the split capacitor is given by

$$C_{\mathrm{b}} = \left[\left(2+S_1\right)^{-1} + \left(2+S_2\right)^{-1} + \left(2+S_3\right)^{-1}\right]\mathrm{C} \tag{6}$$

where the unit capacitor C is 211 fF; and S_1, S_2 and S_3 are 1 or 0.

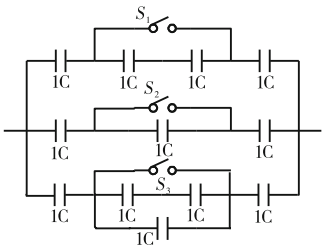


Fig.4 Tunable capacitor C_{b}

There are 8 combinations of S_1, S_2 and S_3 when each of them switches on or off. And for each combination, 300 times Monte Carlo simulations are implemented. Tab.1 presents the simulation results, which indicates that there is always an attenuation capacitor value which is very close to the ideal value (300 fF).

Tab.1 Values of attenuation capacitor after 300 times Monte Carlo simulations

Combination serial No.	1	2	3	4	5	6	7	8
The maximum value / fF	255	284	298	307	320	334	346	375
The minimum value / fF	218	241	249	270	272	298	303	331
The average value / fF	237	263	275	291	299	315	325	353

The calibration principle of the split capacitor C_b is shown in Fig.5. At the beginning of calibration, C_b is given a maximum capacitance. All the low-bit capacitors (C_1—C_8), all the high-bit capacitors (C_9—C_{14}) and the positive terminal of the comparator are connected to V_{ref}, ground and V_{CM}, respectively. Then, the positive terminal of the comparator is disconnected from V_{CM}, and C_9 is switched to V_{ref}; besides, all the high-bit capacitors except C_9 are connected to ground. If C_b is larger than 16C/15, the weight of the low-bit array will be larger than C_9, and the output of the comparator is high. So C_b will be given a smaller value. The above steps are repeated until the comparator output changes. At this time, one tunable capacitance value is selected to offer the best performance.

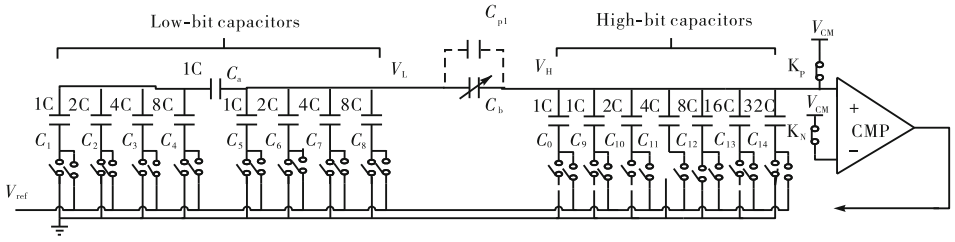


Fig.5 Calibration principle of split capacitor

2.2 Calibration of process mismatch of capacitors

The calibration capacitor array consists of multiple capacitor arrays which are shown in Fig.6. The top plate of the calibration capacitor arry is connected to the negative terminal of the comparator. Each calibration sub-DAC array corresponds to a capacitor in the main DAC that needs to be calibrated. After all the error voltages are calculated, the compensation phase begins. The calibration sub-DAC is connected to ground when the error voltage of the corresponding capacitor is positive. Otherwise, it is connected to V_{ref}. Then the negative terminal of the comparator will be disconnected from V_{CM}. If the comparator judges the result as "H", the switching status of the sub-DAC remains unchanged. However, if the comparator output is "L", the switches need revert to the initial state.

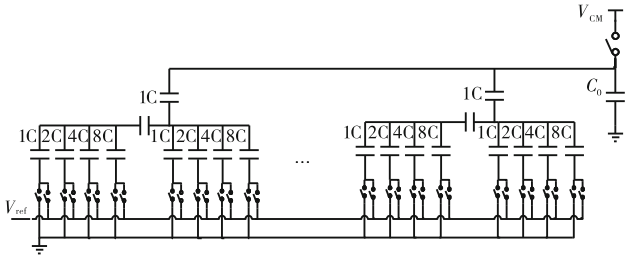


Fig.6 Calibration capacitor array

2.3 Implementation of digital calibration technique based on 14-bit SAR ADC

Fig.7 shows the block diagram of the SAR ADC. The main DAC employs segmented architecture with three parts, which reduces the number of unit capacitors[14]. The calibration DAC arrays consist of six sub-DAC arrays with the same structure. The dual-comparator topology ensures the speed and precision. A comparator with high precision is used in the calibration phase. The other comparator, the precision of which is a little lower, is used in the converting phase to ensure the speed of the ADC. At the beginning of the working process, the switch that controls the negative terminal of the comparator is connected to V_{CM}. Other switches are all connected to ground. Then when the six high bits are being converted, the error-correction voltages should be compensated to the negative terminal of the comparator. The above steps are repeated until the six high bits are all calibrated. Fig.8 shows the timing waveform of the calibration process. The six thick line rectangles show the phase of obtaining the calibration code of the six high bits. The output result of the SAR ADC after calibration is in the oval region.

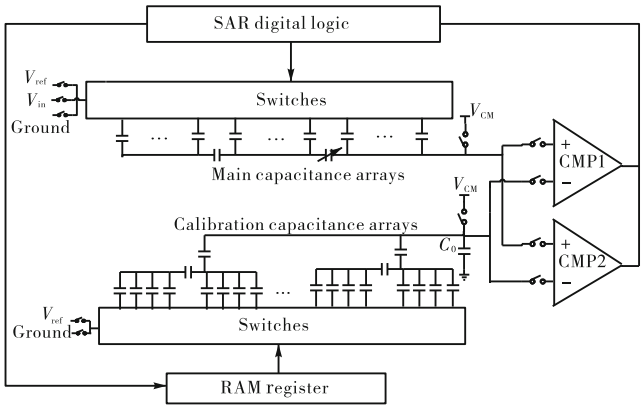


Fig.7 Block diagram of SAR ADC with calibration

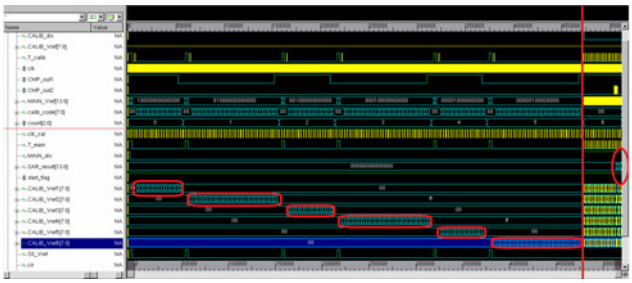


Fig.8 Timing waveform of calibration

3 Simulation result

A 14-bit 500 ksamples/s prototype SAR ADC with 0—2.5 V input signal swing was simulated and calibrated in Simulink to demonstrate the effectiveness of the proposed calibration technique. The capacitor mismatch rate σ was set to be 0.5%. Firstly, a 6.17 kHz sine wave was input into the ADC. Then the output data were processed by related MATLAB programs. Fig.9 illustrates the results of the dynamic performance simulation for different input frequencies at 500 ksamples/s and 5 V supply voltage. The FFT spectra of the SAR ADC output before and after calibration are shown in Fig.10. The SNDR is improved from 71.23 dB to 83.07 dB.

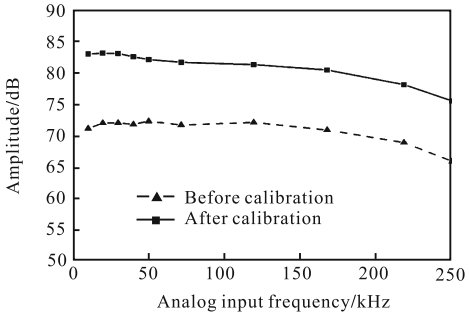
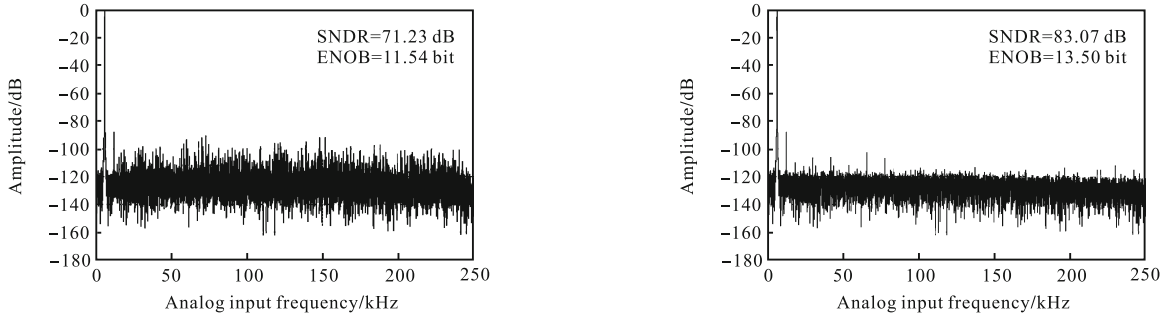


Fig.9 SNDR for various input frequencies at 500 ksamples/s



(a) Before calibration (b) After calibration

Fig.10 Simulated ADC output spectra at 6.17 kHz input

4 Conclusions

The main DAC of the SAR ADC adopts a three-stage discrete structure for reducing the area of capacitor array[15]. The calibration DAC arrays consist of six sub-DAC arrays with the same structure, which can increase the speed of calibration at the expense of area relative to the single calibration DAC array. The existing method for calibrating the split capacitor adds an adjustable capacitor in parallel with the lower weight side of the DAC to compensate for mismatches. However, it will bring mismatches to the lower weight side. The method proposed in this paper makes the split capacitor tunable and chooses the value that can offer the best performance, which avoids the defect of the existing method.

A digital calibration technique is proposed based on a 14-bit SAR ADC. The technique not only eliminates the impact of parasitic capacitor of split capacitor, but also calculates and compensates the mismatch voltage of capacitor array. The ADC was fabricated in Global Foundry 0.35 μm CMOS process (Fig.11). The active area of the ADC was 3.23 mm^2. All the digital calibration circuits were implemented on a chip measuring 0.68 mm^2, which was 21% of the ADC area. When the supply volt-

Fig.11 Chip layout

age was 5 V and the reference voltage was 2.5 V, the power consumption of the ADC was 15 mW. The simulation results show that the SAR ADC with calibration achieved ENOB of 13.5 bit at 500 ksamples/s.

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