New Pixel Circuits for Controlling Threshold Voltage by Back-gate Bias Voltage using Crystalline Oxide Semiconductor FETs

Makoto Kaneyasu*, Kouhei Toyotaka*, Hideaki Shishido*, Toshiyuki Isa*, Shingo Eguchi*, Hiroyuki Miyake*, Yoshiharu Hirakata*, Shunpei Yamazaki*, Masayoshi Dobashi**, Chieko Fujiwara**

***Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa 243-0036, Japan**
****Advanced Film Device Inc., 161-2 Masuzuka, Tsuga-machi, Tochigi-shi, Tochigi 328-0114, Japan**

Abstract
We devised a threshold voltage compensation pixel circuit using back-gate bias voltage. Variations in threshold voltage can be reduced to 10% while improving the saturation characteristics of a driving transistor. We fabricated a 5.29-in Quad-VGA OLED display using this pixel circuit.

Author Keywords
oxide semiconductor; CAAC-IGZO; OLED; threshold voltage compensation

1. Introduction

Kimizuka et al. synthesized $InGaO_3(ZnO)_m$ (IGZO) for the first time in 1985, and proposed its use as a semiconductor element and stated the necessity of increasing the purity of IGZO in 1987 [1]. Cillessen et al. disclose the application of InO_x, GaO_x, or ZnO_x or mixtures or compounds of these oxides to liquid crystal displays (LCDs) [2].

Transparent amorphous oxide semiconductors (TAOS) are proposed by Kamiya, Hosono, et al. and they claim amorphous structures to be ideal [3,4], while we have proposed crystalline IGZO.

We discovered c-axis-aligned crystalline IGZO (CAAC-IGZO) and nanocrystalline IGZO (nc-IGZO), which have crystal morphologies different from those of single crystal IGZO and amorphous IGZO [5,6]. Characteristics of the CAAC- and nc-IGZOs have been revealed [7], and they appear to be formed by arranged or stacked nanocrystals (pellets) (1–3 nm thick and 0.7–0.8 nm wide each) [8]. In CAAC-IGZO films, atomic arrangement parallel to a substrate surface is observed by cross-sectional transmission electron microscopy (TEM). By X-ray diffraction (XRD) analysis, a peak at approximately 31°, which indicates the c-axis alignment, is detected, but a-b plane alignment is not observed [8]. No clear grain boundary is observed by plan-view TEM [8]. CAAC-IGZO field-effect transistors (FETs) have an extremely small off-state current on the order of yoctoamperes per micrometer (10^{-24} A/μm) because of low carrier density [9,10]. These FETs are less likely to suffer from short-channel effects and therefore very suitable for miniaturization [10].

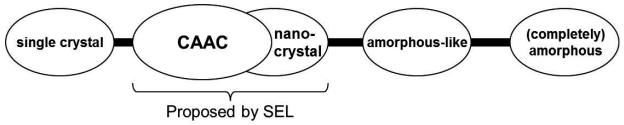

Figure 1. Classification of IGZO in terms of crystal morphology

We have reported on LCDs and tandem OLED displays using IGZO transistors with an ultra-low off-state current [11-14]. Regarding OLED displays, we have studied threshold voltage compensation for pixel circuits [14].

Generally, the threshold voltage (V_{th}) of a Si transistor is easily controlled by impurity doping. However, the fabrication process of IGZO FETs does not include such a step by which V_{th} is easily controlled. Variation in V_{th} makes it difficult to keep the value of current flowing through an OLED constant. This might decrease the quality of an OLED display whose emission luminance depends on the value of the current. Using a V_{th} compensation circuit is a useful way of suppressing a decline in display quality due to V_{th} variation.

A possible cause of the declining quality of an OLED display is poor saturation characteristics of a driving transistor. When a transistor has poor saturation, the current value of the transistor depends on the drain–source voltage even in a saturation region. Furthermore, current flowing through the OLED changes accordingly when the operating point of the OLED changes because of variables such as time degradation.

We devised a novel pixel circuit for compensating V_{th} of a driving transistor considering these two causes and increasing the saturation of the transistor. Each pixel circuit includes six transistors and has a driving transistor V_{th} compensation function using back-gate bias voltage. We built a prototype of a 5.29-in Quad-VGA OLED display using this pixel circuit.

2. *I–V* Characteristics of CAAC-IGZO FETS

Fig. 2 shows the *I–V* characteristics of CAAC-IGZO FETs. The FETs used for the measurement have a channel width of 3 μm, a channel length of 3 μm, and a back-gate. The FET characteristics were measured in 9 points in a 3.5th generation mother glass. The median and variation 3σ of the V_{th} were 0.44 V and 0.30 V, respectively. The FETs exhibited mobilities of 30 $cm^2/V{\cdot}s$ or higher. The advantage of including a back-gate in an FET is that FET saturation characteristics are improved and the drain-induced barrier lowering effect is thus

reduced. A channel-length modulation coefficient of a single-gate FET without a back-gate is approximately 0.05 V^{-1}, whereas that of a back-gate FET is approximately 0.009 V^{-1}, i.e., the saturation characteristics are improved [15]. Another advantage is that V_{th} of an FET can be electrically controlled. Fig. 3 shows the measurement results of the back-gate dependence of V_{th} of a pixel FET. We measured the *I–V* characteristics while changing the V_{bgs} and fixing the source potential of an FET to calculate V_{th} that are plotted. As shown in Fig. 3, the V_{th} decreases as V_{bgs} increases, whereas the V_{th} increases as V_{bgs} decreases.

The V_{th} amount shifts linearly with respect to the V_{bgs}. Note that the shift amount of V_{th} here depends on the thickness and the relative permittivity of an intermediate layer between the channel and back-gate portions. As the thickness of the intermediate layer increases and the relative permittivity decreases, V_{bgs} has less influence on the V_{th}.

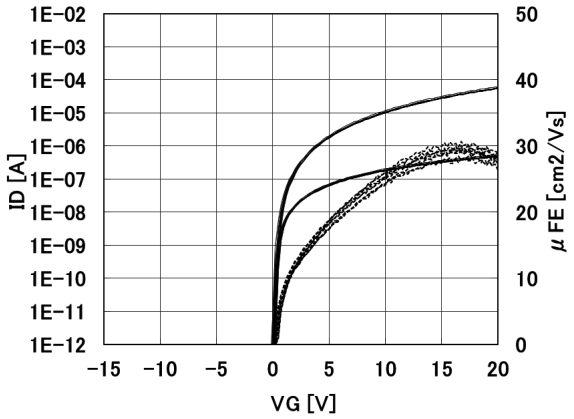

Figure 2. *I–V* characteristics of CAAC-IGZO FETs (W/L = 3 μm/3 μm, V_{ds} = 0.1 V, 20 V)

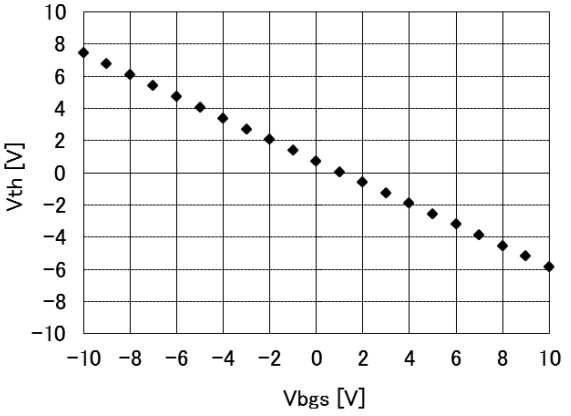

Figure 3. Back-gate dependence of the V_{th} of FET (W/L = 3 μm/3 μm, V_{ds} = 20 V)

3. Threshold Voltage Compensation Circuit for Pixels of OLED Display

We designed the pixel circuit shown in Fig. 4. Each pixel includes six transistors (Tr1 to Tr5 and DrTr), two capacitors (C1 and C2), three power supply lines (ANODE, V_0, and V_1), one data line (DATA), three scan lines (G1, G2, and G3), and an OLED. Fig. 5 shows the operation of the pixel circuit.

In Period I, initialization is performed. Tr2, Tr3, and Tr4 are on; Tr1 and Tr5 are off; and V_0 is applied to a back-gate of DrTr in Period I. The source potential is the sum of the CATHODE potential and threshold of the OLED (V_{thOLED}), so that V_{bgs} can be large; V_{th} of the driving transistor negatively shifts to make the transistor normally on.

In Period II, the V_{th} of the DrTr is compensated. Here only Tr2 and Tr3 are on, the gate-source node of the DrTr is thus electrically connected, and the back-gate potential of the DrTr remains V_0. The DrTr is turned on because it is normally on, and the source potential gradually increases. Because the potential V_0 is fixed, V_{bgs} gradually decreases and the negative V_{th} increases to 0. The gate-source potential (V_{gs}) is 0 V here, and the V_{th} is equal to V_{gs} when V_{th} is 0 V, whereby the driving transistor is turned off. At this time, the back-gate voltage is held by C2, so that the characteristics of the DrTr can be fixed in the state of V_{th} = 0 V.

In Period III, data writing is performed. Tr1 and Tr5 are turned on, and the potential of V_{data}–V_1 is held by C1.

Finally, light is emitted in Period IV. Only Tr4 is turned on, and the DrTr accordingly supplies current depending on V_{gs}–V_{th}. However, current depending only on V_{gs} with which V_{th} variation is canceled, i.e., V_{data}–V_1, flows because the V_{th} of the DrTr is compensated to be 0 V. Consequently, light emission can be performed without dependence on the V_{th} of the DrTr.

Note that this pixel circuit can be driven with five transistors other than Tr2. However, if it is driven by a transistor other than Tr2, only when the source potential of the DrTr is charged in Period II does V_{gs} become 0. This method requires consideration of current flowing into the OLED in Period I that depends on V_{data}, which is written in the previous frame.

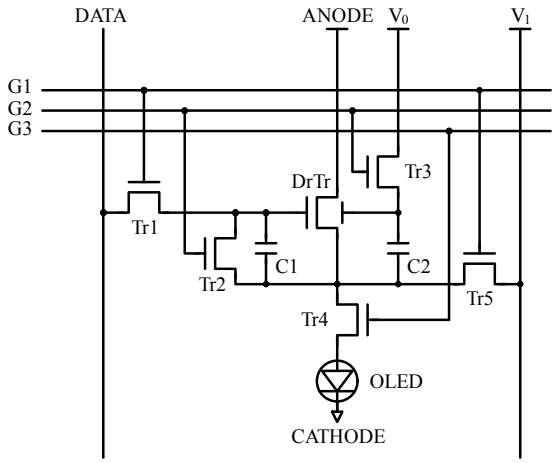

Figure 4. Pixel circuit diagram

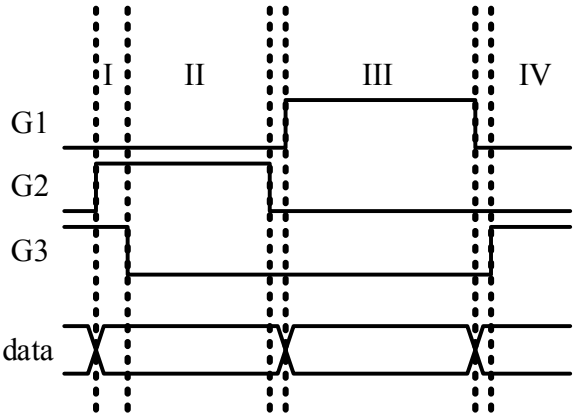

Figure 5. Timing chart of pixel circuit

4. Panel Configuration

We built a prototype of a 5.29-in Quad-VGA OLED display. The panel specifications are listed in Table 1. The pixel density and aperture ratio are 302 ppi and 61.0%, respectively. Top emission white electroluminescence (EL) elements and color filters (CF) were employed for the full-color panel (Fig. 6). The white EL element has a two-layered tandem structure in which an emission unit containing a blue fluorescent material and an emission unit containing green and red phosphorescent materials are connected in series (Fig. 7). A scan driver is integrated on the glass substrate, and the source driver is a chip on film (COF). The pixel circuit we designed achieves a temporal separation between an operation in a V_{th} compensation period and that in a data writing period, corresponding to not only linear sequential driving but also dot sequential driving. The prototype of the OLED panel is driven with dot sequential driving in which a demultiplexer separates three colors, RGB.

Table 1. Panel specifications

Specifications	
Screen diagonal	5.29 in
Driving method	Active matrix
Number of effective pixels	960 × RGB × 1280 (Quad-VGA)
Pixel density	302 ppi
Pixel pitch	28 μm × RGB × 84 μm
Aperture ratio	61.0%
Pixel arrangement	RGB stripe
Pixel circuit	6Tr + 2C/cell
Source driver	COF + DeMUX
Scan driver	Integrated

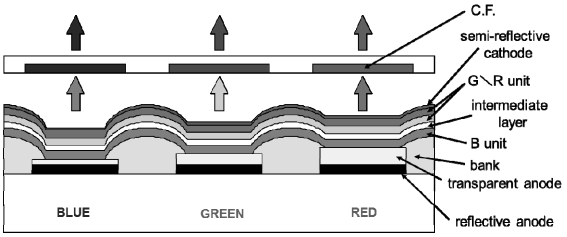

Figure 6. Cross section of EL elements with coloring method

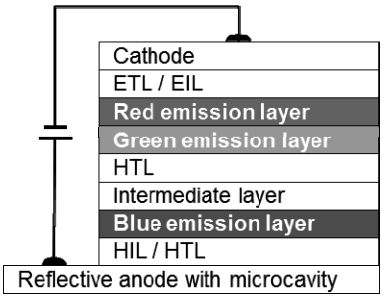

Figure 7. Cross-sectional structure of white EL layer

5. Results

Fig. 8 shows a picture displayed by the panel that we fabricated. The panel displays images without problems such as display unevenness. Fig. 9 shows simulation results with the changing V_{th} of the driving transistor. Here we obtain V_{gs}–V_{th} plotted on the vertical axis by subtracting the V_{th} of the driving transistor from that of the transistor in an emission period in Period IV. The slope of the graph is 0 when the V_{th} compensation is completed because V_{gs}–V_{th} is independent of the V_{th}. The simulation results show that, in the circuit we designed, variation in a range from the typical V_{th} to ±1.5 V can be suppressed to approximately 10%. In principle, the pixel circuit can compensate the V_{th} variation in a range of V_{th} from 0 to a value positively shifted by a potential of V_0–(Cathode+V_{thOLED}) in the normally off transistor, and in a range of V_{th} from 0 to a value negatively shifted by a potential of Anode–V_0 in the normally on transistor. Note that when the effect of V_{th} control by a back-gate bias is small depending on the conditions of the intermediate layer between the channel and back-gate portions, the amount of variation ranges within this V_{th} control. Although the V_{th} compensation range is not wide, a CAAC-IGZO transistor with less variation even in a 3.5th generation mother glass is capable of high-accuracy compensation. If variation in the V_{th} of the driving transistor is limited in the range of the normally off transistor, the anode can serve as a power source of the power supply line V_0, in which case one power supply line V_0 in a pixel can be removed.

Figure 8. Display picture

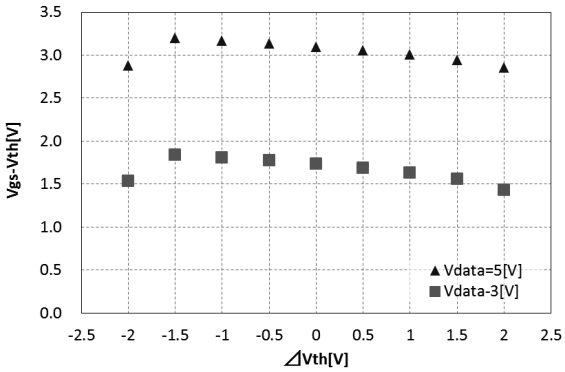

Figure 9. V_{th} variation dependence of gate-source voltage of driving transistor

6. Conclusions

We devised a novel pixel circuit for compensating threshold variation in a driver transistor using a back-gate. We demonstrated that threshold variation was suppressed within approximately 10%, and succeeded in fabricating a 5.29-in Quad-VGA OLED display.

7. References

[1] N. Kimizuka and T. Mohri, Japanese Published Patent S63-239117.

[2] J. F. M. Cillessen et al., US Patent 5744864.

[3] T. Kamiya, K. Kimoto, N. Ohashi, et al., "Electron-Beam-Induced Crystallization of Amorphous In-Ga-Zn-O Thin Films Fabricated by UHV Sputtering," IDW/AD'13 Digest, 280–281 (2013).

[4] K. Nomura, T. Kamiya, H. Ohta, et al., "Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-O: experiment and ab *initio* calculations," Phys. Rev. B **75**, 035212 (2007).

[5] S. Yamazaki, J. Koyama, Y. Yamamoto, et al., "Research, Development, and Application of Crystalline Oxide Semiconductor," SID Symposium Digest **43**, 183–186 (2012).

[6] M. Takahashi, M. Nakashima, T. Honda, et al., "C-Axis Aligned Crystalline In-Ga-Zn-Oxide FET with High Reliability," Proc. AM-FPD'11 Digest, 271–274 (2011).

[7] S. Yamazaki, "Crystalline Oxide Semiconductor Using CAAC-IGZO and its Application," ECS Trans., **64**, 155–164 (2014).

[8] S. Yamazaki, T. Hirohashi, M. Takahashi, et al., "Back-channel-etched thin-film transistor using c-axis-aligned crystal In–Ga–Zn oxide," Journal of SID, **22**, 55–67 (2014).

[9] S. Yamazaki, H. Suzawa, K. Inoue, et al., "Properties of crystalline In–Ga–Zn-oxide semiconductor and its transistor characteristics," Jpn. J. Appl. Phys. **53**, 04ED18 (2014).

[10] S. Yamazaki, T. Atusmi, K. Dairiki, et al., "In-Ga-Zn-Oxide Semiconductor and Its Transistor Characteristics," ECS J. Solid State Science and Technology, **3**, Q3012–Q3022 (2014).

[11] S. Kawashima, S. Inoue, M. Shiokawa, et al., "13.3-in. 8K x 4K 664-ppi OLED Display Using CAAC-OS FETs," SID Symposium Digest **45**, 627-630 (2014).

[12] K. Toyotaka, K. Kusunoki, T. Nagata, et al.,"6.0-Inch Extended Graphics Array Reflective Liquid Crystal Display Using Oxide Semiconductor Thin Film Transistors for Electronic Paper Display," Jpn.J.Appl.Phys.**50**.03CC09 (2009).

[13] H. Shishido, S. Amano, K. Toyotaka, et al., "Color Sequential LC Display Using High Reliable Oxide Semiconductors with Monochrome Electronics," SID Symposium Digest **42**, 369-372 (2011).

[14] T. Tanabe, S. Amano, H. Miyake, et al., "New Threshold Voltage Compensation Pixel Circuits in 13.5-inch Quad Full High Definition OLED Display of Crystalline In-Ga-Zn-Oxide FETs," SID Symposium Digest **43**, 88-91 (2012).

[15] H. Miyake, S. Kawashima, S. Inoue et al., "Ultra High-definition OLED Display Using C-axis Aligned Crystalline Oxide Semiconductor FETs," Proc. IDW/AD'14 Digest, 181–184 (2014).