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Advanced CAD methodology for history effect characterization in partially depleted SOI libraries

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Abstract

To design large digital circuits in partially depleted SOI technology, worst and best case propagation delays of digital cells induced by floating body effects must be predicted. In this paper, we propose a time efficient and accurate method based on a smart transistor initialisation technique. This solution allows dividing by a factor 2^{n-1} the number of simulations required to completely characterize an n-input gate. This method offers the opportunity to build CAD tools suitable for industrial PD-SOI standard cell libraries characterization.

Keywords: SOI; Digital; Performance; Design; Reliability

1. Introduction

Partially depleted SOI technology offers significant advantages over bulk technology [1,2], but needs dedicated tools and methods to manage the impact of floating body effect [3]. The amount of charge stored in the floating bodies of transistors depends on previous switching activity of circuits, resulting in different threshold voltages and drain currents [5]. At circuit level, the drain current variations induce propagation delay fluctuations; this PD-SOI behaviour is called "history effect". Specific computer-aided design tools must be developed to determine the minimum and the maximum delay induced by history effect and to avoid timing errors in large-scale PD-SOI circuits [1,3,4].

Circuit design using digital synthesis requires an accurate characterization of PD-SOI standard cells libraries. As a library may contain about 500 gates having 10 inputs or more, a fast and robust methodology is mandatory for industrial characterization. Several CAD methods have been developed to help designers to predict best and worst case propagation delays caused by body potential variations. Most of the time, these methods are based on gate inputs initialisation techniques, such as the well known 1st/2nd switch methodology [6–8]. Unfortunately, the 1st/2nd switch approach is not able to bound the history effect caused by complex inputs patterns [9–11].

Alternative tools have been proposed to go beyond the 1st and 2nd switch methodology [13,14]. These methods are based on charge evaluation at transistor level. Maximum and minimum charges are applied at gate level by initialising body potentials [13] of transistors or using high or low drain current abstractions of MOSFET models [14]. These approaches have some limitations because nodes of the circuits are considered

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to be at high or low logic level. In complex topologies such as stacked transistors or high impedance stages, nodes of circuits may reach any values between GND and VDD.

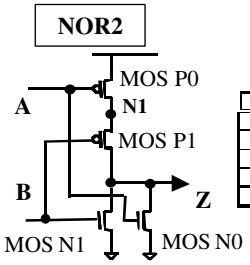
This paper exposes the challenge of history effect characterization in standard cells after static equilibrium and during transient operations. In this study, time efficiency and/or accuracy limitations of standard methodologies, based on gates inputs initialisation, are discussed. Then, a new circuit initialisation technique [15] at transistor level is proposed to overcome the issue of industrial standard cells library characterization. In the proposed solution the polarizations of each transistor of a logic gate are determined by considering all possible input vectors. Then the body charge variation range is evaluated thanks to these lists of polarizations, by measuring body potentials in single transistors. Lastly, a custom combination of minimum/maximum charge of transistors is created inside the circuit by preconditioning body potentials (Section 4). Combining the speed of 1st/2nd switch method with the accuracy of a complete study by considering all initial conditions (Section 5), this approach offers an efficient solution to bound history effect in PD-SOI digital circuits.

2. History effect

In PD-SOI technology, electrical characteristics of circuits depend on the previous switching activity. The amount of charge stored in floating bodies of SOI transistors, and thus threshold voltages and drain currents, depends on several physical phenomenon generating carriers, like gate to body tunnelling currents, impact ionisation and gate induced drain leakage (GIDL), or causing carriers recombination, like body drain and body source junction currents. The balance between all those mechanisms depends on drain, gate and source bias.

2.1. Static states

In SOI digital circuits, complex topologies, such as stacked transistors, not only increase the body potential variation range [12] but also the complexity of history effect characterization. Each different input vector generates a unique combination of transistor D/G/S bias, as shown in Fig. 1, in case of a stacked PMOS of a NOR2 gate. After a long time of inactivity, a static equilibrium is reached. The input vector and related D/G/S MOS polarizations are memorized as a combination of threshold voltages. This combination determines propagation delays as well as static and dynamic consumption. It is important to notice that n-input gates have 2^n different input vectors, leading to 2^n different propagation delays in SOI, as shown in Table 1 for NOR2,



All initial polarizations for MOS P1 (V) at vdd=1.2V

MOS P1	Drain	Gate	Source
A B	Z	B	N1
1 0	0	0	0.09
1 1	0	1.2	1.12
0 1	0	1.2	1.2
0 0	1.2	0	1.2

Fig. 1. Impact of topology on MOS polarizations.

Table 1
Delays in ps at VDD = 1.2 V, load = 50 fF, slope = 250 ps

Inputs A B	*NOR 2 inputs A rising Z falling*
After DC10	360.8
After DC11	360.6
After DC01	351.1
After DC00	398.3
Inputs A B CI	*Full adder CI falling Z rising*
After DC110	455.2
After DC111	428.0
After DC101	473.2
After DC100	417.2
After DC000	439.6
After DC001	410.1
After DC011	467.4
After DC010	415.3
Inputs A B C D	*OR 4 inputs C falling Z falling*
After DC0000	362.25
After DC1000	381.50
After DC0100	383.79
After DC1100	381.20
After DC0010	396.64
After DC1010	394.00
After DC0110	393.79
After DC1110	391.52
After DC0001	390.77
After DC1001	388.81
After DC0101	388.62
After DC1101	386.61
After DC0011	385.63
After DC1011	383.42
After DC0111	383.21
After DC1111	381.12

OR4 and full adder gates in 0.13 μm technology. For example, DC1100 means $A = 1$, $B = 1$, $C = 0$ and $D = 0$.

When switching signals are applied to the gate, propagation delays remain the image of the initial input vector with a duration depending on technology related generation and recombination mechanisms.

2.2. Transient operation

Another key issue appears in transient operation, body potentials exhibit different variation speed. To demonstrate and physically understand what may

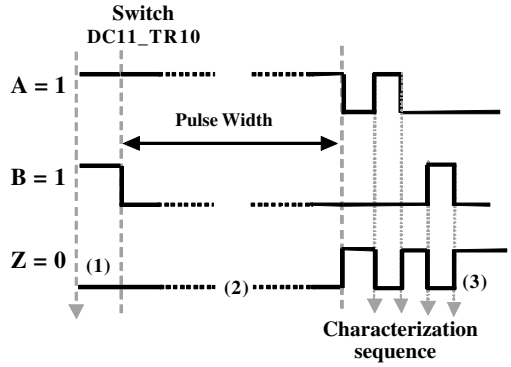


Fig. 2. Example of input pattern in transient operation.

happen in a digital gate during transient operations, various pulse widths have been applied in a NOR2 gate. Fig. 2 describes one of these patterns. Inputs are set to DC11, ($A = \mathrm{VDD}$ and $B = \mathrm{VDD}$) as initial state and are switched to another state TR10 ($A = \mathrm{VDD}$ and $B = 0$) in transient operation. The second state is applied during 10 ns up to 10 s and followed by a characterization sequence to extract propagation delays.

The switching of inputs changes D/G/S polarizations of transistors and, as a consequence, it modifies the balance between aforementioned carrier generation and recombination mechanisms, resulting in a slow body potential shift, as shown in Fig. 3(a). The body potential VBP0 of P0 transistor reaches its new static equilibrium much faster than VBP1 (P1 transistor) generating a new combination of body potentials not predicted by static states. This combination corresponds to a DC11 related body potential for the MOS P1 and a DC10 related body potential for P0. This behaviour explains non-monotonous evolutions of propagation delays as a function of pulse width observed in Fig. 3(b). A worst case propagation delay occurs for 84 ms pulse width during DC11_TR10 evolution because PMOS are both discharged (high body potentials) and drive less drain current.

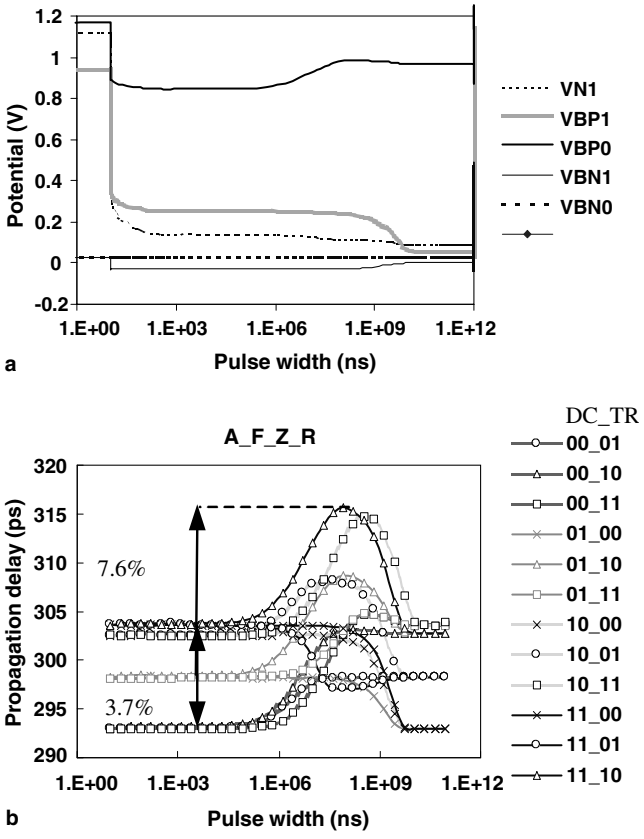


Fig. 3. Body potentials and propagation delays.

In transient operation infinity of different input patterns may be applied, resulting in a propagation delay dispersion, which is not bounded by inputs initial conditions. Propagation delay dispersion during transient operation (7.6% in Fig. 3(b)) can reach more than twice the history effect measured only after static states (3.7%). Unfortunately, standard computer-aided design tools are most of the time based on DC initialisation at input level and are unable to characterize that dispersion.

2.3. Weaknesses of standard CAD solutions

CAD tools based on initialisation techniques at inputs level not only neglect transient effects but are also unable to combine speed and accuracy to bound the history effect after initial conditions. For example, 1st/2nd switch method proposes to apply two waveforms on the input that has to be characterized in order to extract best and worst case propagation delays. An example is given in Fig. 4, the first waveform starts initially high (DC1) and the second initially low (DC0); the event "A falling Z rising" occurs respectively at first and second switch. Multiple input cells are forced to behave like inverters to apply this method. Tools based on 1st/2nd switch approach are very fast; only two simulations are used to predict best and worst case propagation delays of any switching event.

Unfortunately, 1st/2nd switch approach is valid only for inverters because n-input cells have 2^n different initial conditions. It appears clearly in Fig. 5 for a 6 inputs AO gate that 1st/2nd switches are only particular cases of initial conditions. This approach is equivalent to randomly choose 2 among 2^n propagation delays.

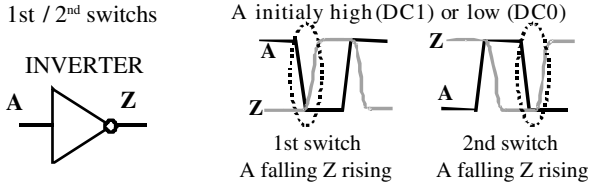


Fig. 4. 1st/2nd switch methodology.

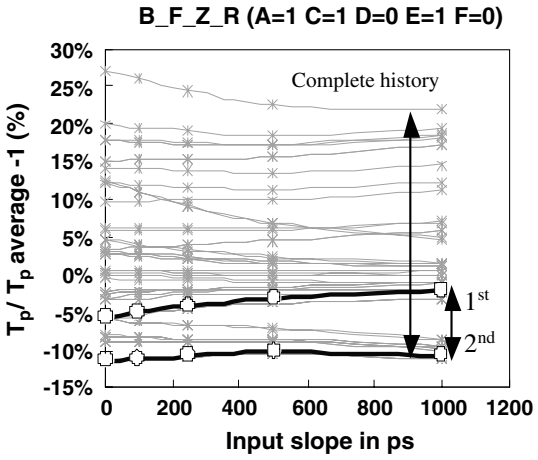


Fig. 5. Complete history effect after static states in an AO gate (triple 2 inputs AND in a 3 inputs NOR).

Designing large circuits with a 1st/2nd switch approach may cause timing errors, resulting in circuit non-functionality. A more accurate characterization can be achieved by using a complete initialisation of inputs. However, a complete study of initial conditions is nearly impossible, especially for industrial standard cells characterization. For example a 9 input and-or-invert gate requires $2^9 = 512$ simulations, which is equivalent to characterize a full standard cells library. Indeed, best and worst vectors depend on the input considered, the event (rising or falling edge) and PVTSC conditions (process, voltage, temperature, input slopes and load capacitance) as shown in Table 2. Input vectors giving best and worst case propagation delays cannot be selected in one PVTSC corner and applied to all corners. By initialising inputs of gates, there is no general rule to simplify characterization tool; a complete study of initial conditions must be performed for each input, event and PVTSC.

A complete study of initial conditions not only neglects random transient operation but also exponentially increases the number of simulations. Standard approaches consider circuits as black boxes, while history effect is an intra-gate fluctuation. Each transistor may have a significant impact on propagation delays. An alternative solution has to be found to achieve an efficient and accurate characterization. This can be done by working at transistor level, as explained in the next section.

3. TMOS level initialisation

The history effect prediction at gate level is complex; it depends not only on process, voltage, temperature, slope and capacitance parameters (PVTSC) but also on initial conditions applied on the logic gate. No clear rule can be easily found when transistors of a gate are combined all together. However, the history effect contribution of each transistor in a gate can be easily predicted, as an increasing amount of charge stored in the floating body of a transistor increases its drain current: to find a best case propagation delay of a gate, the basic idea is to minimize drain currents of transistors involved in the parasitic short cut current and maximize drain currents of transistors driving the output load. The worst case is found by strengthening short cut and weakening drive current. Charge and drain currents can be maximized and minimized by preconditioning body potentials. Table 3 summarises the influence of body potentials on drain currents.

Alternative CAD solutions have been developed to exploit these simple rules. The basic idea of these methods is to evaluate body potential maximum and minimum values and then to build combinations of these minimum and maximum values to have the fastest and the slowest propagation delays through two simulations. Body potentials and charge of transistors obtained after different bias conditions have to be compared. Firstly we explain how body potentials can be compared (Section 3.1) using a reference state, secondly we discuss limitations of alternative CAD solutions presented in [13] and [14] (Section 3.2). Finally the characterization flow

Table 3
Impact of body potentials on drain current

	High VB	LowVB
NMOS	High current	Low current
PMOS	Low current	High current

Table 2
Delays of a NOR2 gate with initial conditions

Corner	Worst	Worst	Worst	Worst	Typical
Event	A rising Z falling	A falling Z rising	B rising Z falling	B falling Z rising	B falling Z rising
After DC10	360.8	450.1	**347.1**	433.2	296.6
After DC11	360.6	452.5	355.7	456.8	**307.7**
After DC01	**351.1**	**463.7**	355.7	**464.9**	299.1
After DC00	**398.3**	**431.5**	**392.8**	**426.1**	**291.7**
Best Tp after DC	01	00	10	00	00
Worst Tp after DC	00	01	00	01	11

is presented (Section 3.3) including a new preconditioning methodology (step 2.4) that allows an optimal accuracy at a low CPU and data storage cost.

3.1. Comparison of body potentials

History effect depends on the charge Q stored in the bodies of transistors. The charge is linked to voltages drain-body V_B, gate-body V_G, source-body V_S and also body storage capacitances: body-drain C_D, body-gate C_G and body-source C_S, Eq. (1.1). At any time, body potential $V_B(t)$ is proportional to the body charge $Q(t)$, determined by slow generation and recombination mechanisms (from the μs up to a few second), and is modulated by the fast capacitive coupling phenomenon (a few ps) caused by D/G/S bias variations Eq. (1.2) $V_D(t)$, $V_G(t)$ and $V_S(t)$.

$$Q = C_D(V_B - V_D) + C_G(V_B - V_G) + C_S(V_B - V_S), \tag{1.1}$$

$$V_B(t) = \frac{Q(t)}{C_T} + \frac{C_D}{C_T}V_D(t) + \frac{C_G}{C_T}V_G(t) + \frac{C_S}{C_T}V_S(t), \tag{1.2}$$

where $C_T = C_D + C_G + C_S$.

The charge stored in the body cannot be directly compared after different initial condition due to the parasitic contribution of external bias. This is highlighted in Fig. 6 for two initial bias conditions applied to an NMOS ($V_{G1} = V_{S1} = 0$ V, $V_{D1} = 1.2$ V) and ($V_{D2} = V_{S2} = 0$ V, $V_{G2} = 1.2$ V) and leading respectively to two initial charges Q_1 and Q_2.

$$\text{At time} = 0\text{ ns}: V_{B1} = \frac{Q_1}{C_T} + \frac{C_D}{C_T} \times V_{D1};$$

$$V_{B2} = \frac{Q_2}{C_T} + \frac{C_G}{C_T} \times V_{G2}.$$

To compare the charge stored after different initial conditions, D/G/S bias are quickly (10 ns) translated in a reference bias Vdref = 1.2 V, Vgref = 0 V, Vsref = 0 V, which correspond to the first initial condition (V_{B1} and $Q1$). The difference of body potentials $\Delta V_B = V'_{B2} - V_{B1}$ measured just after the transition is the image of the difference of charge ΔQ:

$$V'_{B2} = V_{B2} - \frac{C_G}{C_T} \times 1.2 + \frac{C_D}{C_T} \times 1.2 = \frac{Q_2}{C_T} + \frac{C_D}{C_T} \times 1.2,$$

$$V'_{B2} - V_{B1} = \frac{Q_2 - Q_1}{C_T} = \frac{\Delta Q}{C_T}.$$

Body potentials must be measured immediately (a few ps) after the switch of D/G/S bias so that the charge variation due to recombination and generation mechanisms is negligible. In the next section, alternative CAD solutions based on this concept of reference voltage for D/G/S is discussed and the preconditioning methodology is exposed.

3.2. Alternative CAD solutions

Methods described in [13,14] are based on transistor level initialisation techniques using a reference voltage, as described in the previous section. Maximum and minimum body charges are evaluated through body potential values. A first step performs a DC analysis in a single transistor with a sample of initial conditions $VD_{DC}/VG_{DC}/VS_{DC}$ allowed by the topology of gates. In transient operation drain, gate and source nodes are brought back to a reference state Vdref/Vgref/Vsref before extracting body potential values. In both works [13] and [14] the authors consider only six different drain, gate, source polarizations VD_{DC}, VG_{DC} and VS_{DC} to calculate body potentials and charge variation ranges. In fact, to simplify the body charge evaluation step, nodes of gates are considered to be equal to low or high logic level GND or VDD.

It is important to notice that, in stacked transistors, floating nodes may reach any voltage between GND and VDD, as shown in Fig. 7. Approximating the voltage

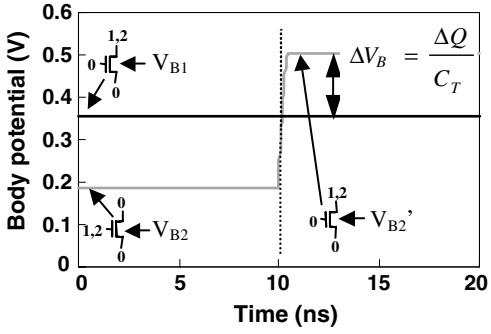


Fig. 6. Body potentials after two initial conditions.

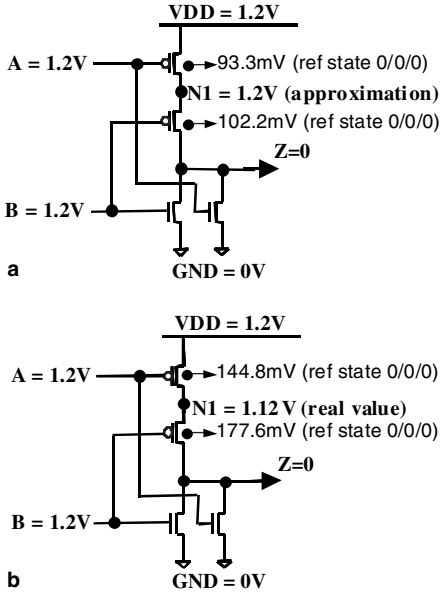


Fig. 7. Floating nodes and body potentials.

of these floating nodes at GND or VDD, as proposed in [13] and [14], strongly modifies the equilibrium of current that flows in the body, and as a consequence the calculation of the body charge. In this example (Fig. 7(b)), for stacked transistors P0 and P1, it leads to body potentials of 93.3 mV and 102 mV, respectively (Fig. 7(a)), instead of 144.8 mV and 177.6 mV (Fig. 7(b)) when real nodes voltages are taken into account. These body voltage misevaluations are about 51.5 mV and 75.6 mV for P0 and P1 and cannot be neglected compared to the variation range (minimum to maximum of body potential), respectively 144.5 mV and 177.8 mV in this example. In some cases, simplifying the charge evaluation step by considering nodes to be at GND or VDD may cause imprecision in the evaluation of the charge of transistors and the timing of circuits, even in simple stacking like NOR2 gate. It may be an important issue in complex topologies such as high impedance stages like tri-state buffers, IO libraries, complex MOS stacking in AO gates or multiple V_T and/or VDD structures.

In [14] the authors propose to build high and low drain abstractions of MOS models by building lookup tables of drain current as a function of drain to source and gate to source voltages. For each maximum or minimum value, gate length and width, process, voltage and temperature, an additional bi-dimensional characterization of drain current must be done. Again only a sample of polarization can be taken into account to avoid huge calculation and heavy database.

The method proposed in this paper allows using exact polarizations of transistors, including node values between GND and VDD. This can be achieved by choosing a common reference voltage for all nodes of transistors, both PMOS and NMOS, and also by applying this common reference voltage to all nodes in the gates when preconditioning body voltages. The most important concept introduced in the next part is the global reference voltage, all nodes except bodies of transistors are forced to the same potential value to measure and initialise body potentials.

3.3. Preconditioning and characterization

3.3.1. Characterization flow

Fig. 8 shows the characterization flow. Step 1.1 builds a database of body potential values that will be used to initialise the transistors of the gates. These values are extracted through a quick transient simulation of single MOS transistors. Step 2.1 collects data about the gate to be characterized. This step includes an analysis of the netlist of the gate to list the transistors and their parameters: gate length and width and type NMOS or PMOS. This step also runs a simulation of the gate to extract, for each possible input vector, the DC drain, gate, source (D/G/S) polarizations of each transistor. These data are next used during step 2.2 to calculate body potential values in the aforementioned database and determine a maximum and a minimum value for each transistor. Step 2.3 build custom combinations of minimum/maximum body potentials; fast and slow propagation delays are found in only two simulations by preconditioning gates with these combinations (step 2.4).

3.3.2. Body potentials lookup tables

In step 1.1, body potentials are measured in single transistors for different drain and source voltage, and compiled in database, as shown in Fig. 9. An initial bias is applied on drain, gate and source (Fig. 10(a)). In transient operation, drain, gate and source are quickly (a few ps) brought back to the reference polarization VREF/VREF/VREF (Fig. 10(b)) to extract the body

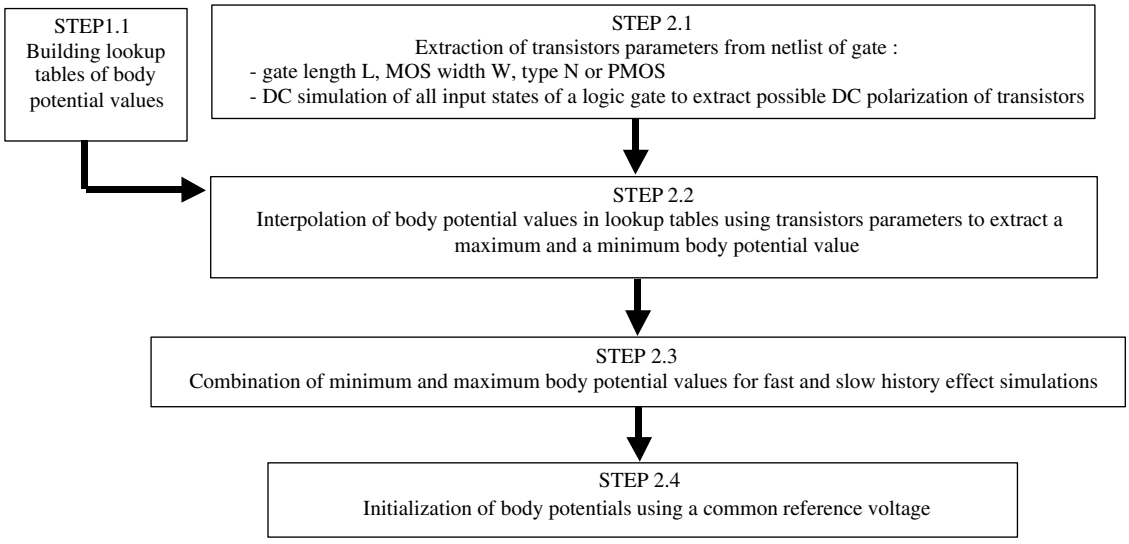


Fig. 8. Characterization flow.

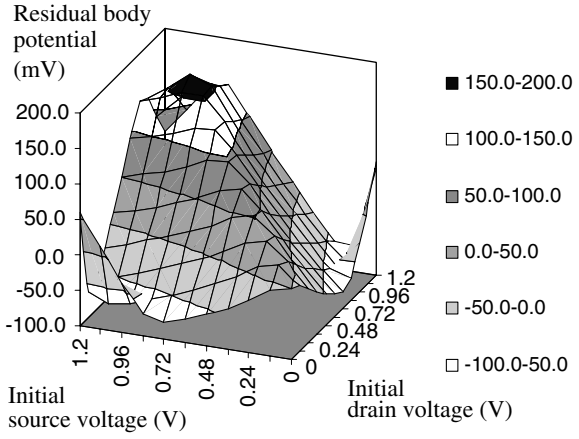


Fig. 9. Table of residual body potential, NMOS transistor, $L = 1$ μm, $W = 1$ μm, Vgate = VDD, VDD = 1.2 V.

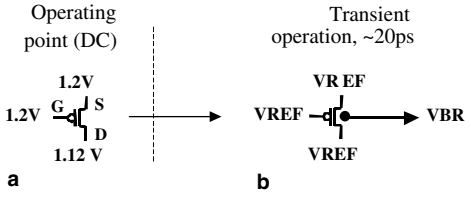


Fig. 10. Body potential extraction.

potential, called residual body potential. During this transition from a DC polarization to a reference bias in transient operation, the charge variation is considered as negligible because generation and recombination currents that modify the charge are extremely weak. This reference polarization cancels the contribution of capacitive couplings as explained in Section 3.1. By this way the difference between residual body potentials and VREF is the image of the charge:

$$Q = (V_B - \mathrm{VREF}) \times C_T \text{ from Eq. (1.2)}$$
$$\text{with } V_D = V_G = V_S = \mathrm{VREF}.$$

The proposed method has been implemented with VREF=0, but any value between GND and VDD can be used

$$Q = V_B \times C_T \text{ if } \mathrm{VREF} = 0.$$

This reference voltage, common to all transistors, allows simplifying the comparison and initialisation procedure. To exploit residual body potential values compiled in this database, the gate must be analysed to collect data about transistors and their possible initial polarizations induced by different initial conditions applied on the gate.

3.3.3. Extraction of real DC polarizations

In step 2.1 of the characterization flow, the real DC polarizations (drain, gate and source voltages) of transistors for the 2^n different input vectors are extracted.

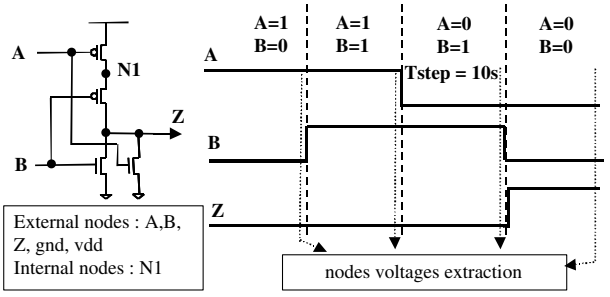


Fig. 11. Input stimuli applied to collect information about initial conditions in a 2 input gate (NR2).

Fig. 11 shows the simulation used for DC nodes voltage extraction. Time step of the input patterns must be sufficient to establish a static equilibrium in the gate before measuring nodes voltages.

This improvement, compared to the methods described in [13] and [14], gives an optimal precision in the evaluation of maximum and minimum body potential values that will be used to initialise a custom combination of charge in the circuit.

3.3.4. Global reference voltage

Fig. 12 introduces the concept of global reference voltage illustrated by an example of state reconstruction using the lookup tables. Fig. 12(a) and (b) shows for one input vector and one transistor in a NOR2 gate the extraction of a residual body potential. Residual body potential values are characterized using a 0 V/0 V/0 V reference state in tables. To retrieve the charge corre-

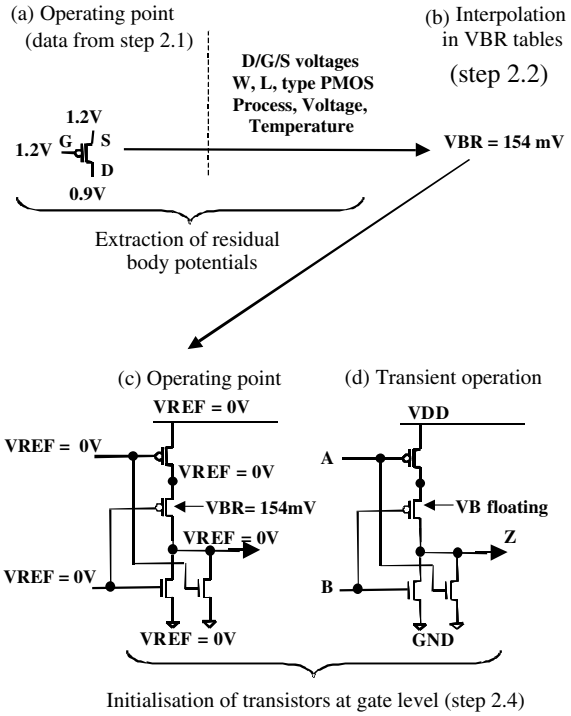


Fig. 12. Preconditioning methodology.

sponding to this initial state in the circuit the method (step 2.4) applies a global reference voltage 0 V (Fig. 12(c)) to all nodes of the circuit, except bodies of transistors, which are forced to their residual body potential values. Power supplies and outputs are also forced to this reference voltage but, in transient operation, internal nodes, body potentials and output are released (Fig. 12(d)) and power supply is conveniently polarized at GND/VDD.

To check the ability of this method to recover the initial charge of a transistor, reconstruction of initial conditions have been compared to standard gate initialisations. Fig. 13 represents body potential evolution after a standard initialisation of inputs (1) and by rebuilding the initial condition using residual body potential (2) as described in Fig. 12. When the gate is conveniently polarized at GND/VDD with same input conditions (3), body potentials are identical, proving that the charge of the transistor has been recovered. Same validations have been done for all transistors and all initial conditions, as shown in Table 4 for a NOR2 gate, proving the validity and the accuracy of this method.

The proposed global reference voltage allows directly using residual body potentials in circuits without calculating displacement caused by capacitive couplings. As a consequence body potential lookup tables are reduced. Only one VB value per initial polarisation VD_{DC}/VG_{DC}/VS_{DC}, W, L, type N or PMOS and PVT have to be calculated and used to set the charge of transistors inside circuits. This simplification of the preconditioning sequence offers the possibility to consider real voltages of floating nodes at a low CPU and data storage cost.

The global reference voltage allows creating any combination of body potentials. Standard initial conditions (input vectors) can be rebuild but also merged by selecting the maximum or minimum body charge among different initial conditions. For example, boundaries of non-monotonous variations of the propagation delays in transient operation (Section 2.2) can be easily reconstructed by selecting the minimum charge of transistor P0 (input DC state 10) and the minimum charge of P1 (input DC state 11). The characterization flow merges all initial conditions by creating a custom combination of minimum/maximum body charge to maximize or minimize propagation delays (step 2.3 of the characterization flow), following the rules defined in Table 3.

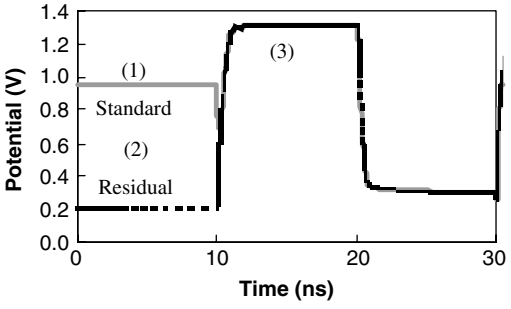


Fig. 13. Results of body potential rebuilding compared to standard initialisation in a NOR2 gate.

3.4. Merging initial conditions

In addition to the previous procedure, in the example of the MOS P0, all 2^n initial conditions are taken into account (Fig. 14(a)) to extract residual body potentials and find the minimum and the maximum values (Fig. 14(b)). Only two sets of maximum and minimum body potentials are necessary to run one simulation best case and one simulation worst case propagation delay (Fig. 14(c) and (d)). Step 2.3 of the characterization flow exposed in Fig. 14 selects a set of minimum/maximum body potential values to minimize/maximize the parasitic short cut current and maximize/minimize the output drive current, according to behavioural rules described in Section 3. For example, for a given event, to obtain fast propagation delay, all transistors having

Table 4
Rebuilt body potential versus body potential after standard initial condition in a NOR2 gate

AB	Body potential (mV)	MOS P1	MOS P0	MOS N1	MOS N0
Initial condition DC10	Real	104.9	997.6	0.0	29.1
	Rebuilt	104.8	997.6	0.0	29.1
	Difference	0.0	0.0	0.0	0.0
Initial condition DC11	Real	295.2	870.5	−30.1	29.1
	Rebuilt	295.2	870.5	−30.1	29.1
	Difference	0.0	0.0	0.0	0.0
Initial condition DC01	Real	192.0	881.0	−30.1	58.2
	Rebuilt	192.1	881.0	−30.1	58.2
	Difference	−0.1	0.0	0.0	0.0
Initial condition DC00	Real	110.2	877.1	−36.1	23.3
	Rebuilt	110.6	877.3	−36.1	23.3
	Difference	−0.4	−0.3	0.0	0.0

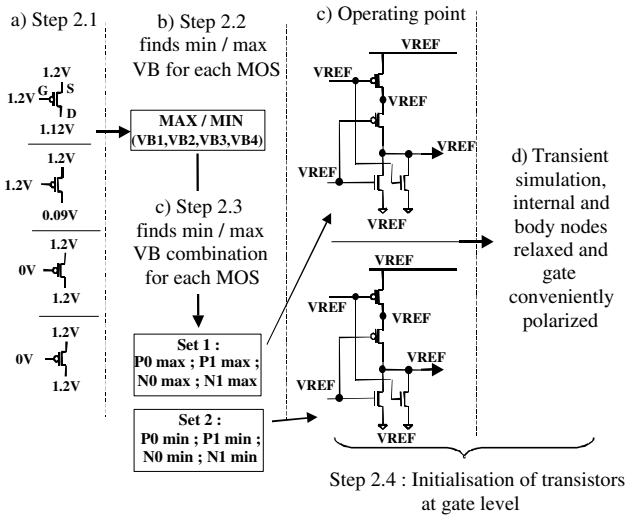


Fig. 14. Characterization flow.

a rising edge on their gate are set to the maximum body voltage and all transistors having a falling edge on their gate are set to the minimum body voltage. In Fig. 14, propagation delays obtained with "Set 1" will be the fastest when inputs rise and the slowest when inputs fall. Residual body potentials are able to accurately bound the body potential variation range caused by 2^n different input initialisations.

4. Results and discussion

4.1. Results

Results of this method have been checked through a subset of standard cells from a low power digital library, including state dependent and sequential cells. In a first example, the proposed method is applied in a NOR2 gate. Boundaries of all input vectors are created through only two simulations, as shown in Table 5.

Compared to all initial conditions, the maximum overestimation of history effect is about 4%, but corresponds to the behaviour observed in Section 2.2 in transient operation. Indeed, custom vectors built by merging initial conditions represent asymptotes of the dispersion caused by random input patterns. Propagation delays measured after any random sequence of input states are outside the range of 2^n initial conditions but always inside boundaries defined by the proposed method as shown in Fig. 15 for a NOR2 gate.

This preconditioning methodology is also functional in complex cells such as full-adder, as shown in Fig. 16. In Fig. 17, this method has been checked over a subset of 15 standard cells at −40 °C/VDD = 1.32 V in Fig. 17(a) and 125 °C/VDD = 1.08 V in Fig. 17(b). Each event of this subset has been characterized once for various input slopes (5 ps to 1 ns) and load capacitances (5–200 fF). These events are sorted by increasing history effect values. History effect characterized with the proposed method is always above the 2^n initial conditions. At −40 °C/VDD = 1.32 V in Fig. 17(a) custom initial conditions are close to the 2^n DC conditions. However, at 125 °C/VDD = 1.08 V in Fig. 17(b), propagation delays present a larger dispersion due to random input stimulus. The proposed method detects a 15%–20% history effect instead of about 10% by considering only DC initial conditions.

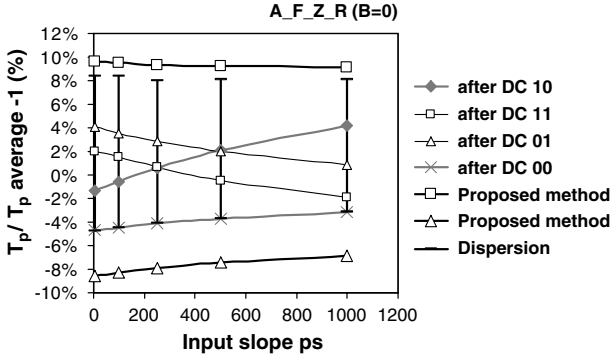


Fig. 15. Dispersion of propagation delays caused by random input sequences.

Table 5
Propagation delays after standard and custom initial condition in ps

	Comer	Typical	Typical	Typical	Typical
	Event	A rising Z falling	A falling Z rising	B rising Z falling	B falling Z rising
Standard initial conditions	After DC10	249.5	302.4	243.8	296.6
	After DC11	249.7	303.5	246.2	307.7
	After DC01	246.8	298.2	246.3	299.1
	After DC00	250.2	293.0	246.9	291.7
Custom vectors	Method best	246.71	291.35	243.59	290.57
	Method worst	250.06	314.92	246.92	313.77
Std/cust (%)	Underestimation	0.04%	0.56%	0.09%	0.40%
	Overestimation	−0.04%	3.76%	0.00%	1.99%

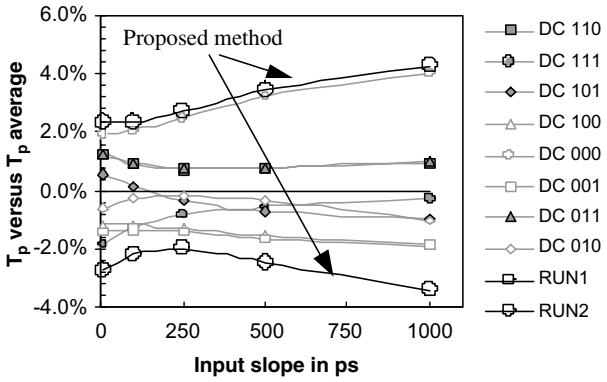


Fig. 16. Proposed method applied in a full adder.

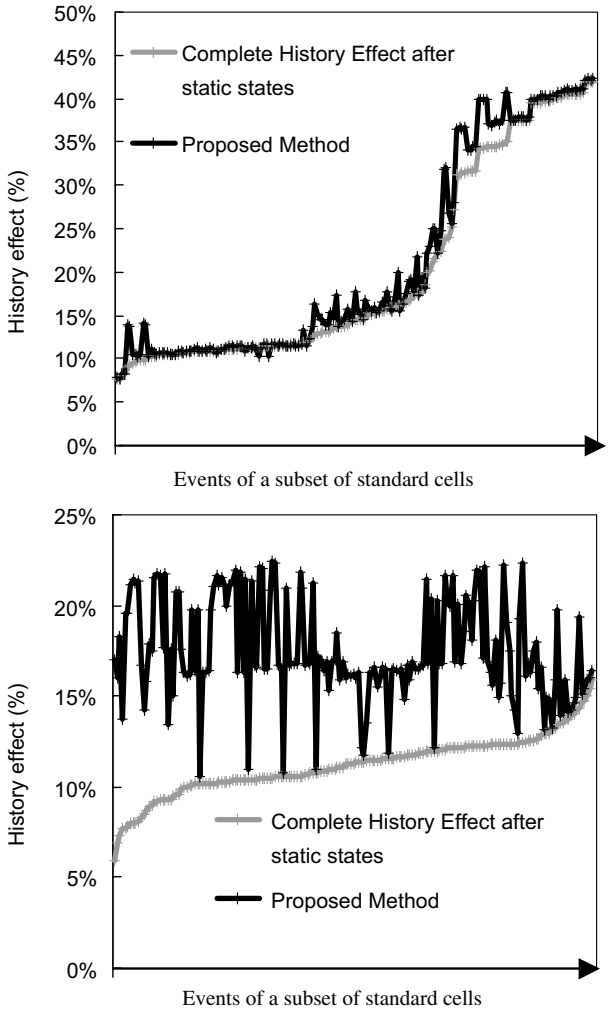


Fig. 17. History effect in a subset of 15 standard cells.

4.2. Accuracy of the method

Fig. 18 shows, as a function of input slopes, a NOR2 gate delay variability for all 2^n initial input vectors and for custom initial conditions build by the proposed

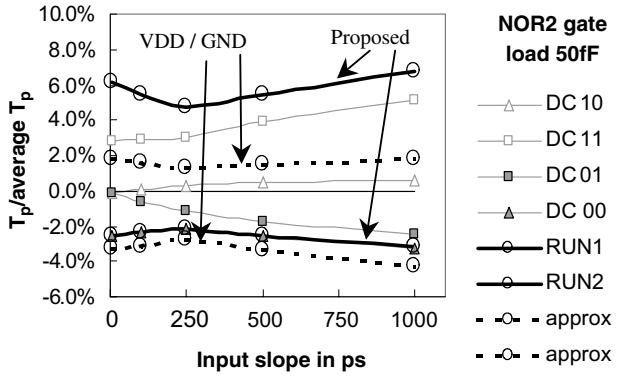


Fig. 18. Proposed method compared to VDD/GND approximation in a NOR2 gate, event A_F_Z_R.

method. The preconditioning methodology is able to accurately determine propagation delays upper and lower bounds. In dashed line, results obtained by considering drain, gate and source nodes at GND or VDD are also presented. As explained in Section 3.2, this approximation leads to an inaccuracy of about 4%–5% in this example. Almost half of the history effect is ignored, due to misevaluation of the body potential range, which is about 94 mV instead of 144.5 mV for P0 MOS transistor and 102 mV instead of 177.8 mV for P1.

5. Conclusion

The smart transistor initialisation methodology described in this paper offers an efficient CAD solution for history effect characterization. It allows finding best and worst cases propagation delays caused by any input pattern through only two runs at a low cost in term of complexity and CPU time. It allows dividing by a factor 2^{n-1} the number of propagation delays to be extracted in an n-inputs logic gate compared to an exhaustive simulation of 2^n initial conditions. Thanks to the global reference voltage also applied to nodes of gates, residual body potential values can be directly used to initialise the transistors of circuits. By this way a precision improvement of the evaluation of the body potential variation range can be achieved at a low cost of CPU and database size. This method allows industrial characterization of PD-SOI digital static CMOS and domino logic libraries, including state dependent cells and timing constraint in sequential cells.

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References

[1] Pelella MM, et al. Advantages and challenges of high performace CMOS on SOI. In: Proceedings of IEEE international SOI conference, Oct 2001. p. 1–4.

[2] Shahidi GG et al. SOI for a 1-V CMOS technology and applications to a 512-Kb SRAM xith 3.5 ns access time. IEDM Tech Dig 1993:813–6.

[3] Chuang CT, Lu PF, Anderson CJ. SOI for digital CMOS VLSI: design considerations and advances. In: Proceedings of IEEE, April 1998;86(4):689–720.

[4] Suh D, Fossum JG. Dynamic floating-body instabilities in partially depleted SOI CMOS circuits. IEDM Tech Dig 1994: 661–4.

[5] Gautier J, Jenkins KA, Sun JYC. Body charge related transient effects in floating body SOI NMOSFETs. In: Int Electron Devices Meeting, Dec 1995. p. 623–6.

[6] Houston TW, Unnikrishnan S. A guide to simulation of hysteretic gate delays based on physical understanding. In: Proceedings of IEEE international SOI conference, Oct 1998. p. 121–2.

[7] Fung SKH et al. Controlling floating-body effects for 0.13 μm and 0.10 μm SOI CMOS. IEDM Tech Dig 2000:231–4.

[8] Pelloie JL. Designing with partially depleted SOI/CMOS. In: Short course international SOI conference, 2002.

[9] Redman-White B, Bernstein K. SOI CMOS circuit design exposed—another dirty tricks campaign? In: Proceedings of European solid state circuit conference, Aug 2000.

[10] Assaderaghi F. Circuit styles and strategies for CMOS VLSI design on SOI. In: Proceedings of international symposium on low power electronics and design (ISPLED), Aug 1999. p. 282–7.

[11] Liot V, Flatresse P. Limits of the 1st and 2nd switch method for history effect characterization in digital circuits. EUROSOI 2005 2005:97–8.

[12] Das KK, Brown RB. Novel circuit styles for minimization of floating body effects in scaled PD-SOI CMOS. In: Proceedings of IEEE computer society annual symposium on VLSI, Feb 2003. p. 29–34.

[13] Shepard KL. CAD issues for CMOS VLSI design in SOI. In: Proceedings of international symposium on quality electronic design, March 2001. p. 105–10.

[14] Chuang CT, Curran B, Smith G. Method for statistically timing SOI devices and circuits. US patent application US20030078763.

[15] Flatresse P, Liot V, Di Maria JL, Gilgenkrantz P. SALTO: a new CAD methodology for history effect characterization in partially depleted SOI technology. EUROSOI 2005 2005: 97–8.