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Dark C–V and I–V characteristics of silicon multi-junctions prepared by liquid-phase epitaxy

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Abstract

The dark capacitance–voltage (C–V) and current–voltage (I–V) characteristics of p–n Si multi-junctions are measured over a reasonable temperature range. Analysis of data suggests that multistep tunneling is the current conduction mechanism due to a high interface density of charges.

1. Introduction

Noticeable interest has been paid to p–n Si multi junctions [1–6] due to their potentiality as solar cells of promising high conversion efficiencies. However, little work has been done on the dark C–V and I–V characteristics of these multi-structure homojunctions.

The aim of the present work is to investigate both the dark C–V and I–V characteristics of five p–n Si multi-junctions.

2. Experimental procedure

The test samples were prepared using the method developed by Ashery as previously described [7]. Fig. 1 shows the arrangements. Growth solutions Si, In, and Sb are in well 1 to produce n-type Si and Si. In and Al are in well 2 to produce p-type Si.

The solutions are initially raised to 850°C for half an hour. The substrate (p-Si) is placed on a movable slide in its well in the multibin graphite boat (Fig. 1).

The substrate is moved to the right to become under well 1 to grow the n-Si layer at 830°C, then it is moved to the left to become under well 2 to grow the p-Si layer at 810°C. This procedure is followed until the 5 p–n junctions are produced with the desired thickness as indicated in Fig. 2. The In added in both wells 1 and 2 is used as a solvent, while the Sb in well 1 and the Al in well 2 are used as impurities to yield n- and p-Si, respectively.

Metalization of the back surface of Si was carried out by vacuum deposition of an Al film (~ 1 μm thick), the top electrode was made in a finger shaped by vacuum deposition of gold. The evaporation was performed in a vacuum $\sim 10^{-5}$ mbar, using an evaporation plant model E306A manufactured by Edwards high vaccum.

The dark C–V characteristics of the p–n Si multi-junctions were performed over a temperature range 290–423 K at 1 M Hz using Model 410 C–V Meter provided by a certain program based on the following relationships [8–10]:

$$N(x) = 2[1 + N(x)/N_{\mathrm{known}}]/q\varepsilon A^2[\mathrm{d}(1/c^2)/\mathrm{d}v],$$

$$N(x) = c^3[1 + N(x)/N_{\mathrm{known}}]/q\varepsilon A^2[\mathrm{d}c)/\mathrm{d}v],$$

$$W = \varepsilon A\{1/[1 + N(x)/N_{\mathrm{known}}]\}/c$$

and

$$V_b = kT/q \log[N(x) - N_{\mathrm{known}}]/N_i^2,$$

where $N(x)$ is the net semiconductor impurity dopant concentration, N_{known} is the known dopant concentration on one side of a p–n junction, A is the area of the junction under test, ε is the permitivity of the semiconductor, q is the charge of an electron, W is the width of the depletion region, k is the Boltzman constant, T is the temperature on Kelvin scale and N_i is the intrinsic carrier concentration.

The I–V characteristics were also measured over a temperature range 290–380 K.

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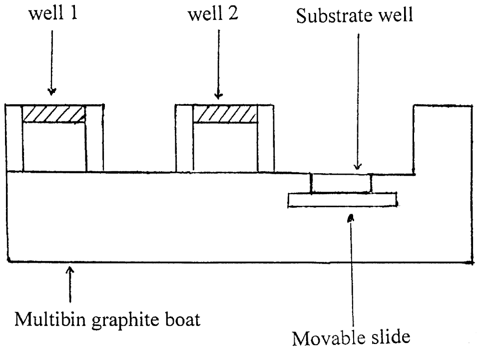

Fig. 1. Boat structure for one-step LPE growth.

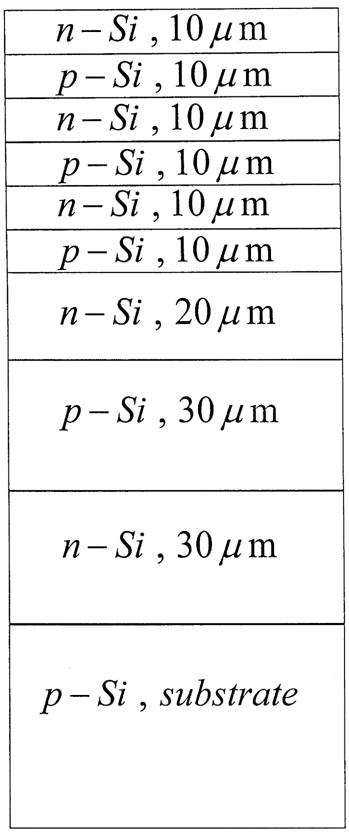

Fig. 2. Schematic diagram of Si multi-junction.

3. Results and discussion

First, the analysis of the dark C–V characteristics performed automatically leads to investigation of several temperature dependencies.

(i) The temperature dependence of the capacitance. Fig. 3 illustrates the capacitance C as a function of the junction temperature T. As shown, the capacitance increases linearly with increasing temperature. This behavior can be explained on the basis of variation of the width of the depletion region with temperature.

(ii) The temperature dependence of the width of the depletion region. It was found that the width of the depletion region (w) of the p–n Si multi-junctions decreases linearly with increasing temperature as shown in Fig. 4.

The obtained results are in harmony with those obtained in the previous section, as the increase in the width of the depletion region will decrease the capacitance and vice versa.

(iii) The temperature dependence of the built-in voltage. The interface density of charges has a considerable effect on the apparent built-in voltage [8] (V_D). As expected, increasing the interface density of charges decreases the built-in voltage. The high interface density of states also behaves as effective tunneling centers. So, the predicted conduction mechanism may be single-step or multi-step tunneling mechanism. This operating mechanism may depend on the method of the sample preparation, the quality of materials and the type of the two components composing the junction under test.

It was found that the built-in voltage V_D decreases linearly with increasing temperature as shown in Fig. 5. This indicates that the interface density of charges $\sigma\,\mathrm{cm}^{-2}$ increases from about 10^{12} to $10^{14}\,\mathrm{cm}^{-2}$ on increasing the temperature from 290 to about 425 K.

Such behavior is confirmed as shown in Fig. 6, as observed σ increases linearly with increasing the temperature.

From the data of Fig. 5, we find that the rate of change $\mathrm{d}V_D/\mathrm{d}T$ is about 1.1×10^{-3} V/K.

The analysis of the dark I–V characteristics is used to define the operating current transport mechanism as follows.

Second, typical dark forward I–V characteristics of the five p–n Si multi-junctions measured over the temperature range 290–380 K is shown in Fig. 7. This figure indicates an exponential dependence of current–voltage in the voltage range up to about 60 mV. The forward I–V characteristics in this exponential region is first described by the standard diode relationship [11]

$$I_f = I_o(T)\exp[qV/nkT]\,. \tag{1}$$

So, graphical representations of log I_f versus V reveal parallel straight lines in the temperature range studied. This result indicates that the diode quality factor n decreases from about 6 to 4.65 as the temperature increase from 290 to 377 K.

This behavior suggests that the dominant current transport mechanism through the p–n Si multi-junctions is a tunneling mechanism [12].

The temperature dependence of the dark forward current for different values of the applied forward voltage is illustrated in Fig. 8.

The linearity of this dependence indicates that the current transport through the test junction is due to multistep tunneling process [13].

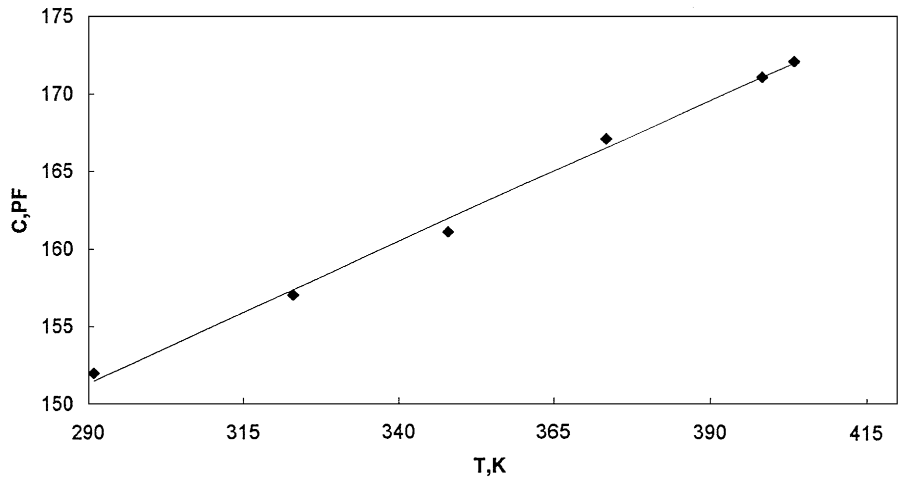

Fig. 3. Capacitance as a function of temperature.

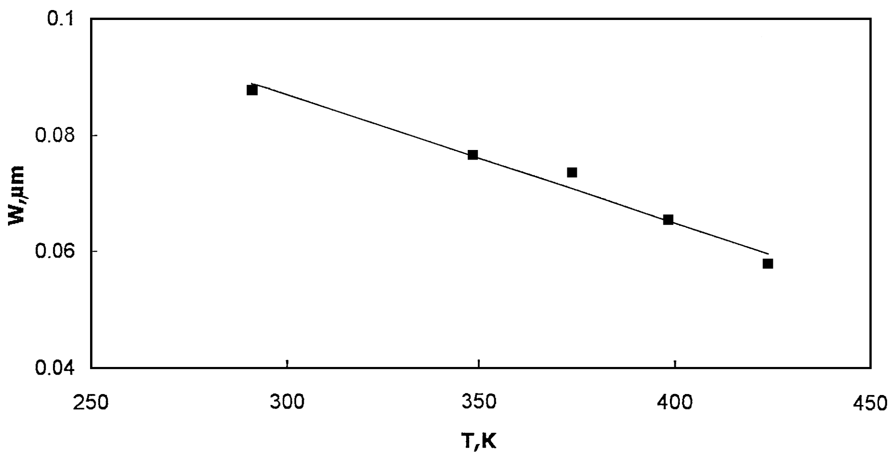

Fig. 4. The width of the depletion region as a function of temperature.

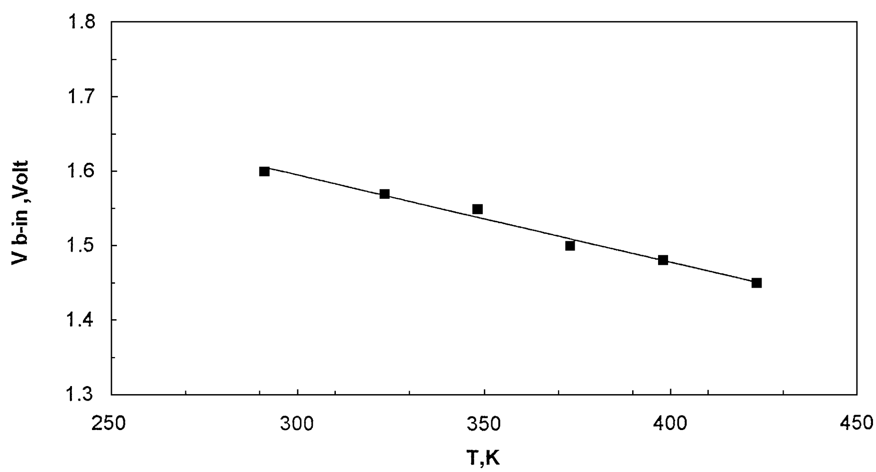

Fig. 5. The built-in voltage as a function of temperature.

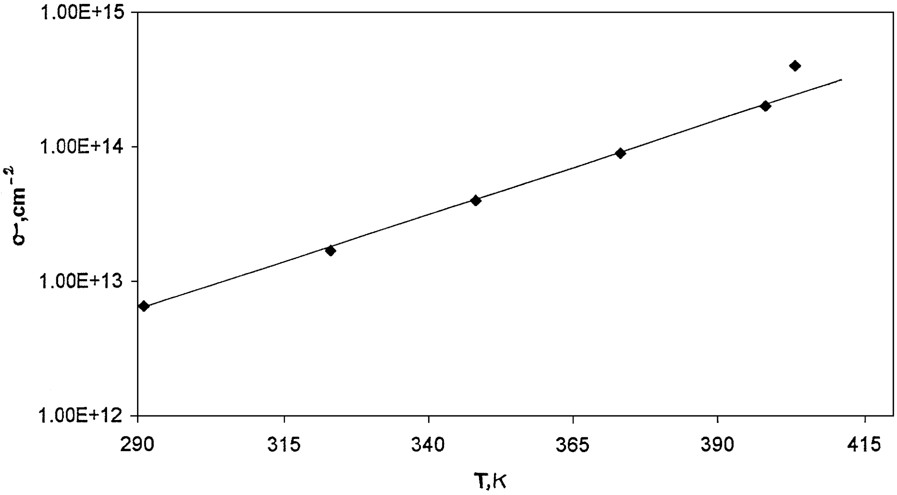

Fig. 6. The interface density of charges σ as a function of temperature.

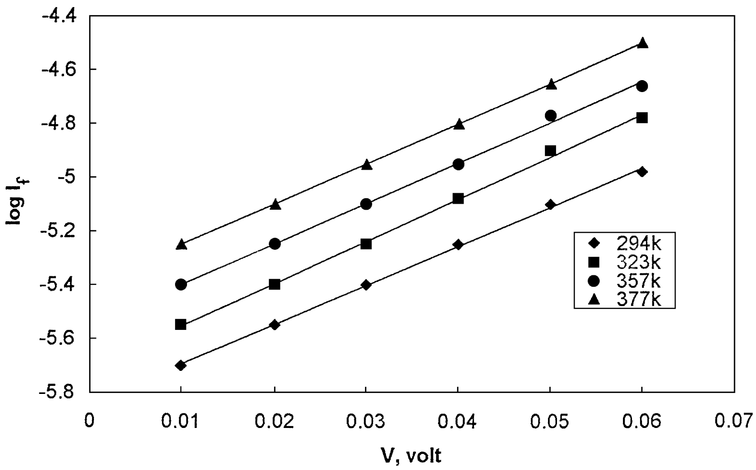

Fig. 7. Dark forward current–voltage characteristics.

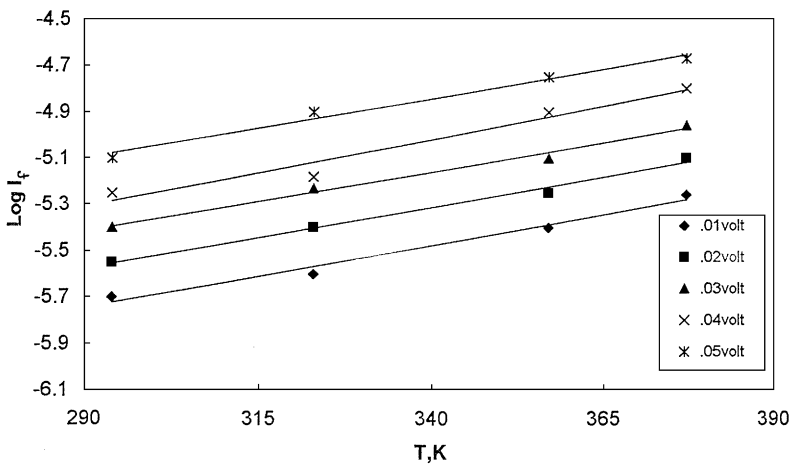

Fig. 8. Temperature dependence of the dark forward current for different values of forward voltage.

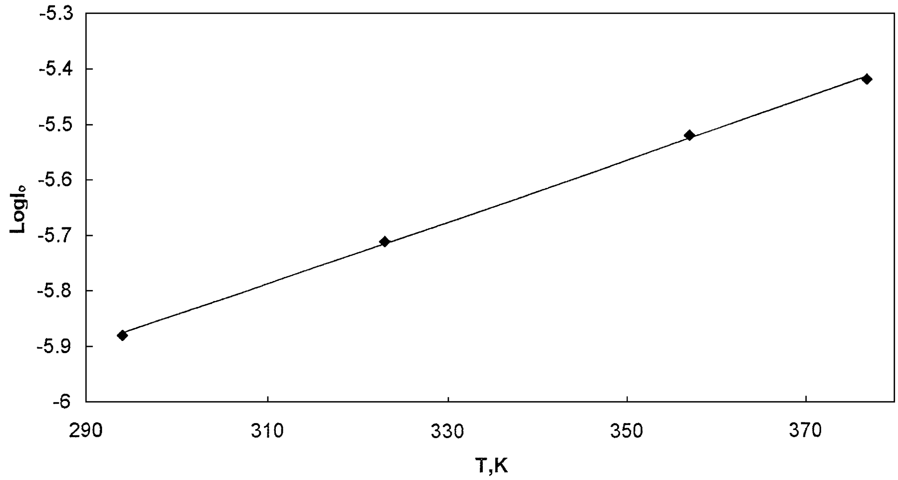

Fig. 9. Saturation current I_o as a function of temperature.

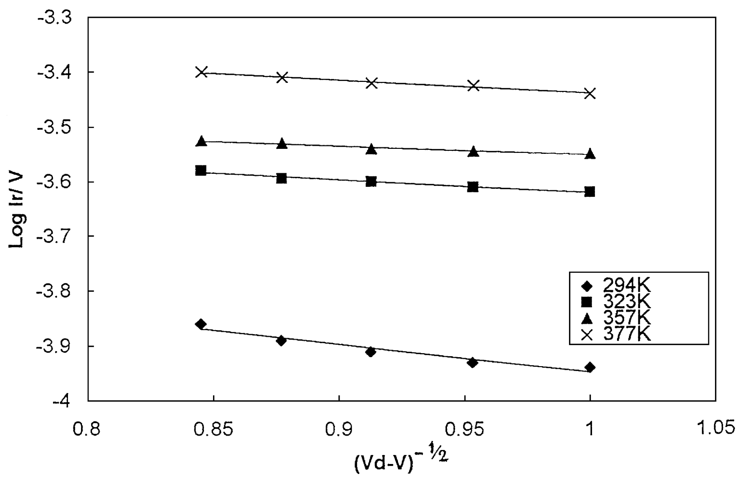

Fig. 10. $\log I_r/V$ as a function of $(V_D - V)^{-1/2}$.

Assuming that the electric field is constant in the depletion region, the trap levels are uniformly distributed over the band gap; the forward current is described by the relationship [14]

$$I_f = I_t \exp[\alpha(V - V_D) = I_o \exp(\alpha V), \quad (2)$$

where I_o is a constant proportional to the trap density required for the multistep tunneling and α is a constant given by

$$\alpha = d(\ln I_f)/dV. \quad (3)$$

From the data of Fig. 7, it was found that α is independent of temperature with a value of about 6.6 V^{-1}.

But

$$\alpha = (\tfrac{8}{3}\, h)\,(m^* \varepsilon / R N_d)^{1/2}, \quad (4)$$

where h is planck's constant, $m*$ is the effective mass in Si, and R is the number of steps to transverse an electron through the deplection region.

Using Eq. (4), the number of tunneling steps was calculated. It was found that $R = 492$.

The temperature dependence of the saturation current I_o is illustrated in Fig. 9. The linearity of this dependence shows that the temperature dependence is not an activation process. Hence, we assume that the temperature dependence of I_o is only due to the temperature dependence of V_D. Accordingly, from Eq. (2), one can obtain

$$d(\ln I_o)/dT) = -\alpha(dV_D/dT) = \gamma. \quad (5)$$

The value of γ can be obtained from Fig. 9 representing $\log I_o$ as a function of temperature. It was found that γ is about 5.25×10^{-3} K^{-1}. Using Eq. (5), dV_D/dT is found to be -0.8×10^{-3} V/K, which is close to the value 1.1×10^{-3} V/K determined from C–V measurements. Fig. 10 shows the graphical representation of $\log I_f/V$ as a function of $(V_D - V)^{-1/2}$.

The linearity of these plots suggests that the reverse current could also be explained by the multistep tunneling mechanism [14]. The trap density N_t required for the multistep tunneling can be obtained from the relationship [14]

$$I_r V^{-1} \exp[-\lambda(V_D - V)^{-1/2}] = q^2 a N_t / h, \quad (6)$$

where

$$\lambda = \alpha(RE_t/q)^{3/2}, \quad (7)$$

q is the elementary charge, a is the lattice constant of Si ($a = 5.41$ A) and E_t is the barrier corresponding to each tunneling step. λ was found to be $0.27\ V^{1/2}$. From this experimental value of λ, using Eqs. (6) and (7), the values of N_t and E_t can be calculated. It was found that $N_t = 1.13 \times 10^{10}\ m^{-3}$ and $E_t = 1.4 \times 10^{-7}$ eV.

4. Conclusion

Both dark C–V and I–V characteristics of p–n Si multi-junctions measured over a reasonable temperature range reveal that the operating conduction mechanism is multistep tunneling mechanism. This conduction mechanism indicates that in these devices the interfaces have a high density of defects which behave as effective tunneling centers.

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