New Platform for Testing Candidate Materials for Organic Field-Effect Transistors

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Received: March 8, 2004

A field-effect transistor platform has been designed and fabricated from silicon that allows for the testing of organic semiconductors (OS) as potential materials for organic field-effect transistors (OFET) and as the gate conductor in chemically sensitive field-effect transistors (CHEMFET). Once the OS is deposited, the device can be operated in either mode. This platform should aid in the search for the semiconductor field effect in a variety of organic materials. The effects of contact resistance, surface conductivity, and gate leakage current have been demonstrated and analyzed. No semiconductor field effect has been observed in OFET mode using poly(phenylenesulfidephenyleneamine) as the organic semiconductor.

Introduction

Molecular electronics based on organic semiconductors (OS) and solid-state chemical sensors are very closely related.[1] Of particular interest are insulated gate field-effect transistors (IGFET), which in their conventional implementation are fabricated from silicon. They are the building blocks of modern electronics. The overall transistor operation and characteristics do not change when the gate metal of conventional IGFET is replaced with OS. This replacement offers the opportunity to develop devices that are sensitive to the environment. In other words, it becomes a chemical sensor. The modulation of the electronic properties of the OS arises from the ability of OS to sorb electron donor/acceptor molecules from the environment. Such interactions then lead to changes in the Fermi level in the gate OS and a shift in the threshold voltage of the transistor. As such, these devices have been termed "chemically sensitive field-effect transistors" (CHEMFET).

It is also possible to reverse the roles of the components and to use the OS as the current-carrying part of the FET while the Si substrate becomes the gate. In such a configuration, the device operates as an "organic FET" (OFET).[2] The modulation of the electronic properties of the OS by the chemical environment remains. The key to the operation of all FET devices is the so-called semiconductor field effect. It represents the modulation of conductivity at the interfacial region between the gate dielectric and the semiconductor by (i) the transverse electric field resulting from an applied gate voltage, (ii) the trapped charges in the gate dielectric, (iii) the surface states, and (iv) the difference in the work function of the silicon and the gate metal.[3] In this paper, we describe the design and fabrication of a platform to investigate both the field modulation and the chemical modulation of the FET devices. This allows for a direct comparison of the IGFET and OFET functions.

The test platform shown in Figure 1 has all of the features of conventional silicon IGFET except that it has two gold contacts to the gate over which the layer of OS is deposited (Figure 1a). In normal IGFET operation, the common gate-to-source voltage, V_G, is applied to both Au contacts. In this configuration, the transistor drain-to-source current flows between the conventional n-doped drain and source electrodes in the p-silicon substrate. Because the Au/OS contacts are ohmic and because no current flows through the OS, the electric field develops in the gate insulator separating the OS from silicon according to the applied V_G. The gold leads are deposited over a thin layer of Ti. The gate dielectric has sufficient thickness and quality to ensure that there is no parasitic gate leakage current even when unusually high voltages are applied across it.

The device can be operated as a regular IGFET, exhibiting normal I_D-V_D and I_D-V_G characteristics described by eqs 1a and 1b, respectively.

$$I_D = \frac{\mu C_0 W}{2L}(V_G - V_T)^2 \tag{1a}$$

for $V_D > V_G - V_T$, the saturation region, and

$$I_D = \frac{\mu C_0 W}{L}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \tag{1b}$$

for $V_D < V_G - V_T$, the subthreshold (or linear) region. The parameters in eq 1 are W and L, the width and length of the channel, respectively, C_0 is the capacitance of the gate, and μ is the mobility of the minority carriers in the semiconductor channel.

This device can be also operated as OFET when it is connected as shown in Figure 1b. In this case, the two Au contacts are designated as the drain and source, respectively. The V_G is applied to the p-Si substrate. The drain-to-source current then flows between the Au contacts, through the OS, and the field modulation can take place only in the OS above the gate dielectric. Equations 1a and 1b should again apply. The platform described in this paper has been designed and fabricated according to the norms and standards of silicon device fabrication. The contacts between the OS and the metal are ohmic and are located outside the electric field of the gate. This is the single most important difference between our platform and interdigitated test platforms, which are routinely used for OFET testing. It helps to eliminate experimental artifact due to the field modulation of contact resistance.

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10.1021/jp0402028 CCC: $27.50
Published on Web 06/04/2004

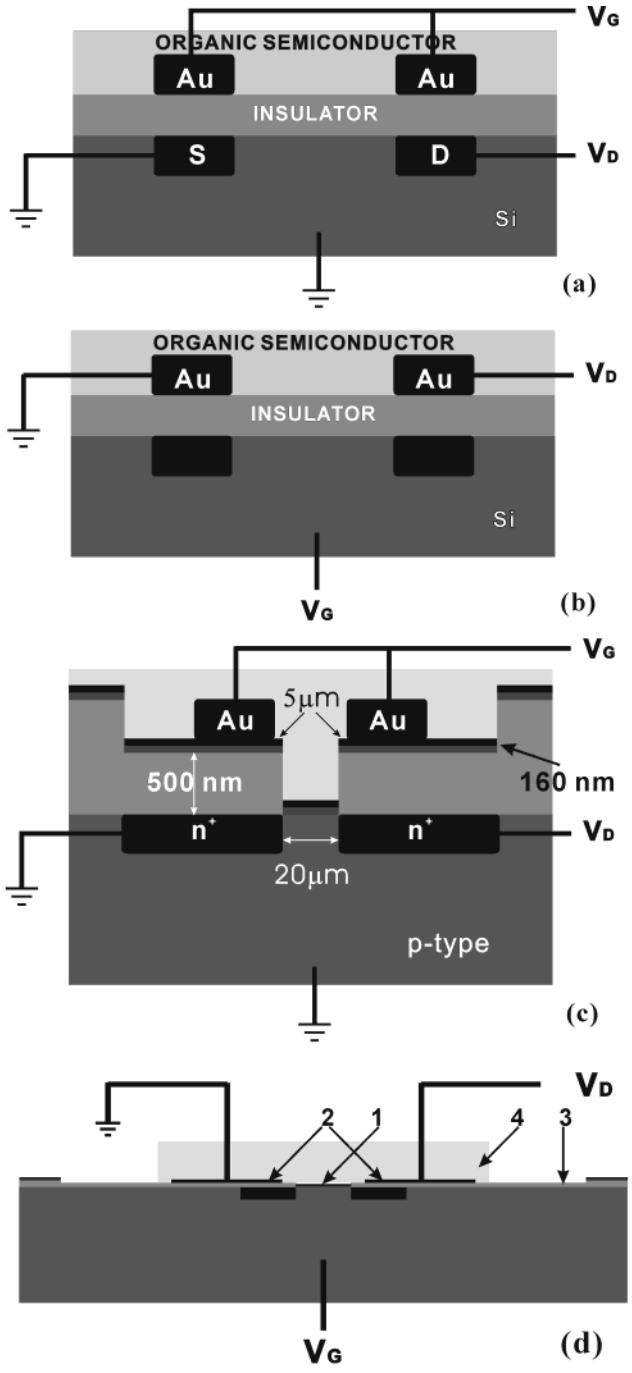


Figure 1. Schematic of the IGFET/OFET platform operated in (a) IGFET mode and (b) OFET mode. (c) Schematic cross section of the IGFET/OFET platform. (d) Representation of the gate area in real dimensions.

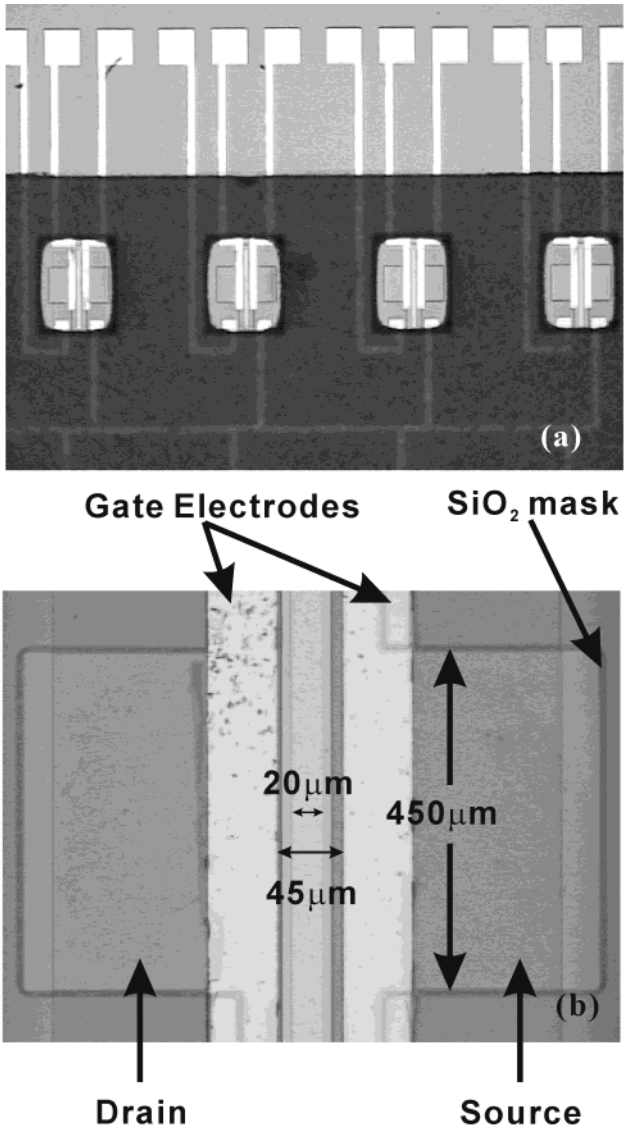


Figure 2. Photograph of the chip with dimensions as indicated. (a) Array of eight (only four are shown) IGFET/OFET gate areas defined by epoxy wells (Taiyo PSR-4000BN, Taiyo America, Inc.) The "cross" inside each well is the outline of the SiO_2 mask deposited over the Au contacts. It defines the contact area between the Au and the organic semiconductor. (b) Detail of the gate area with two Au electrodes separated by 45 μm.

Experimental Section

Fabrication. The fabrication of the IGFET/OFET platform is similar to a standard n-MOS process. It consists of eight identical modules on each chip. There are some unconventional steps due to the use of a conducting polymer as the gate material. First, a noble metal (Au) is used as a contact for its chemical inertness and high work function. Second, the gate insulator consists of 80 nm of silicon oxide and 80 nm of silicon nitride (Figure 1c). The nitride layer reduces the possibility of pinhole defects and ensures good passivation. It is deposited by a high-temperature, low-pressure chemical vapor deposition (LPCVD) process. Third, 150-μm-deep wells are formed around each transistor module (Figure 2a) to facilitate the solvent-casting deposition of organic semiconductors. The photomask used for this application is a permanent negative epoxy (Taiyo PSR-4000BN).[4] An approximately 1% solution of trimethoxy aminopropyl silane (Aldrich) in methanol is used as an adhesion promoter. It is spin coated onto the wafer before the application of the epoxy mask. There is a 1000-nm-thick SiO_2 mask deposited over the gold contacts. Its purpose is to define the contact area between the OS and Au to limit more precisely the geometry of the conducting path for the measurement of the conductivity of OS (Figure 2). The solvent casting of OS results in a film of nonuniform thickness across the well, which is due to the formation of a meniscus at the well walls. However, the thickness of the OS film is relatively uniform between the Au leads, in the region defined by the SiO_2 mask. Two versions of the platform were fabricated—one with the Au leads separated by 120 μm and one with a separation of 45 μm. The channel length in Si was 20 μm in both versions.

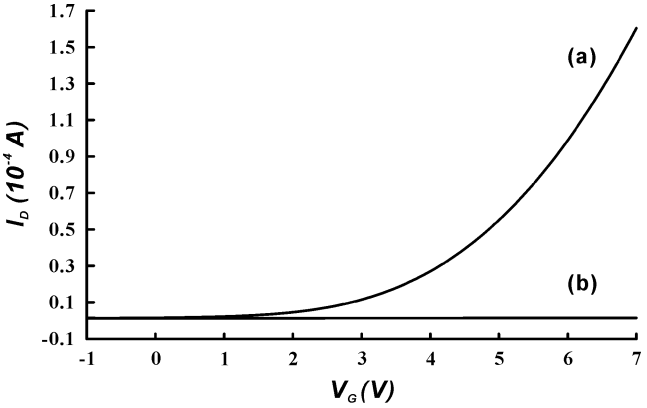
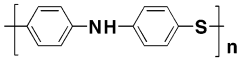


Figure 3. IGFET drain current−gate voltage characteristics of the device without any gate conductor (a) when the surface of the silicon nitride layer is conductive because of hydration. The gate voltage is applied to both Au electrodes. (b) I_D-V_G characteristics obtained after removing the physisorbed water from the surface.

By necessity, the schematic cross section of IGFET is always shown out of scale. Thus, the horizontal dimensions in Figure 1c are shrunk by a factor 1:125 with respect to the vertical dimensions. In Figure 1d, we show the in-scale dimensions of our device where all dimensions are normalized to the thickness of the SiO_2 (and Si_3N_4) (1). The Au electrodes (2) are separated by 45 μm, and the field oxide (3) is 0.82 μm thick. The thickness of the OS (4) is approximately 2 μm. Figure 1c and particularly the detail of the gate (Figure 1d) are useful in showing where the electric fields are located.

In the CHEMFET, the organic semiconductor fulfills the role of the metal in a conventional transistor. Prior to the deposition of OS into the gate wells by solvent casting or by sublimation, the well area must be cleaned to remove any impurity that may act as an unintentional insulator. This is accomplished by ultrasonic cleaning. When exposed to water, silicon nitride forms a conducting layer of hydrated silicon oxynitride, which is up to 100 Å thick. A conducting hydrated layer is also formed on SiO_2.[5,6] A nearly normal I_D-V_G modulation can be observed when a gate voltage is applied to Au contacts of such a "hydrated" device (Figure 3a). The hydrated layer and surface conductivity can be removed by baking the device for 1−4 h at 200 C. This treatment leads to a loss of modulation in the absence of a genuine gate conductor (e.g., OS (Figure 3b)). This is a particularly important step because the surface conductivity of hydrated devices could cause an artifact in the OFET mode, particularly when highly resistive (i.e., undoped) OS are used.

After the completion of the cleaning step, the organic semiconductor to be tested is deposited into the wells. In this study, a thin layer of poly(phenylenesulfidephenyleneamine) (PPSA)[7,8] was dispensed onto the gate area to test the device function.



PPSA

The chips were wire bonded to 28-pin dual-in-line ceramic headers using 50 μm gold wires. Different pin assignments were made under different measurement modes. In the IGFET mode, the two gold electrodes were connected, and gate voltage V_G was applied. The substrate and source were grounded, and drain voltage was applied to the other n region. In the OFET mode, the gate voltage was applied to the substrate, one of the gold electrodes was grounded as the source, and drain voltage was applied to the other gold electrode. Measurements were performed on an HP 4155A semiconductor parameter analyzer in air at room temperature.

Results and Discussion

Ideal IGFET Characteristics. Figure 4a shows the I_D-V_D characteristics of IGFET with PPSA as the gate conductor. In agreement with eq 1, the drain current first increases and then reaches saturation. Note that the drain current is $I_D = 0$ at $V_d = 0$ for all applied gate voltages and that it rises linearily with increasing V_D. This is indicative of ohmic OS/Au contacts and zero leakage current through the gate insulator. The dashed line in Figure 4A separates the linear region (eq 1b) from the saturation region (eq 1a).

Another important characteristic of a FET is the I_D-V_G dependence (Figure 4b). For this measurement, V_D is kept constant, and V_G is scanned. The applied gate voltage at which the current begins to flow is called the threshold voltage, V_T. For $V_D > V_G - V_T$ (saturation region), the drain current becomes a quadratic function of the applied gate voltage (Figure 4b). It is the key operational characteristic of any FET and can be evaluated from the SQRT(I_D)$-V_G$ plot (eq 1a). As can be seen from the results shown in Figure 4, the IGFET with OS behaves ideally. This means that the OS layer together with the two gold electrodes works as a conventional gate.

Using the OS instead of metal as the gate material allows these devices to be used for gas sensing.[1,9] Gases that diffuse into the OS film change its work function, as is reflected in a shift in V_T. This is the underlying principle of gas sensing with CHEMFET. A selective and sensitive sensor can be made by tuning the doping level of the conducting polymer.[9]

Effect of Contact Resistance. The effect of nonohmic contacts is demonstrated in Figure 5. A device was fabricated, identical to the one used for measurements reported in Figure 4, except that a thin layer of SiO_2 was left in the contact holes between n-Si and the Ti/Au metal, creating resistance in the path of the drain current. This, of course, is undesirable under normal circumstances, and such a device would be discarded. Here it serves the purpose of demonstrating the effect of nonohmic serial resistance on transistor characteristics. In the I_D-V_D plots (Figure 5a), the current does not increase linearly with applied V_D from the origin but shows a significant voltage shift between 0 and 0.5 V. This is caused by the breakdown of the SiO_2 barrier on the contacts. This effect is more evident in the I_D-V_G curves. Instead of rising exponentially, as predicted by eq 1a, the current saturates at $V_G = 3$ to 4 V (Figure 5b).

The drain-source path can be modeled as three resistors in series. The first two represent the contact resistance R_c, and the third represents the effective variable resistance R_{Si} of the channel at the Si/SiO_2 interface. It is the latter that is modulated by the electric field and by the semiconductor field effect. The transconductance g_m of the IGFET in saturation is obtained from eq 1 as the slope of the I_D versus $(V_G - V_T)$ curve (Figure 4b) at constant V_D:

$$g_m = \left(\frac{dI_D}{dV_G}\right)_{V_D} = \frac{\mu C_0 W}{L}(V_G - V_T) \qquad (2a)$$

Similarly, the channel conductance g_D can be obtained as the slope of the I_D versus V_D curve at constant V_D in the linear

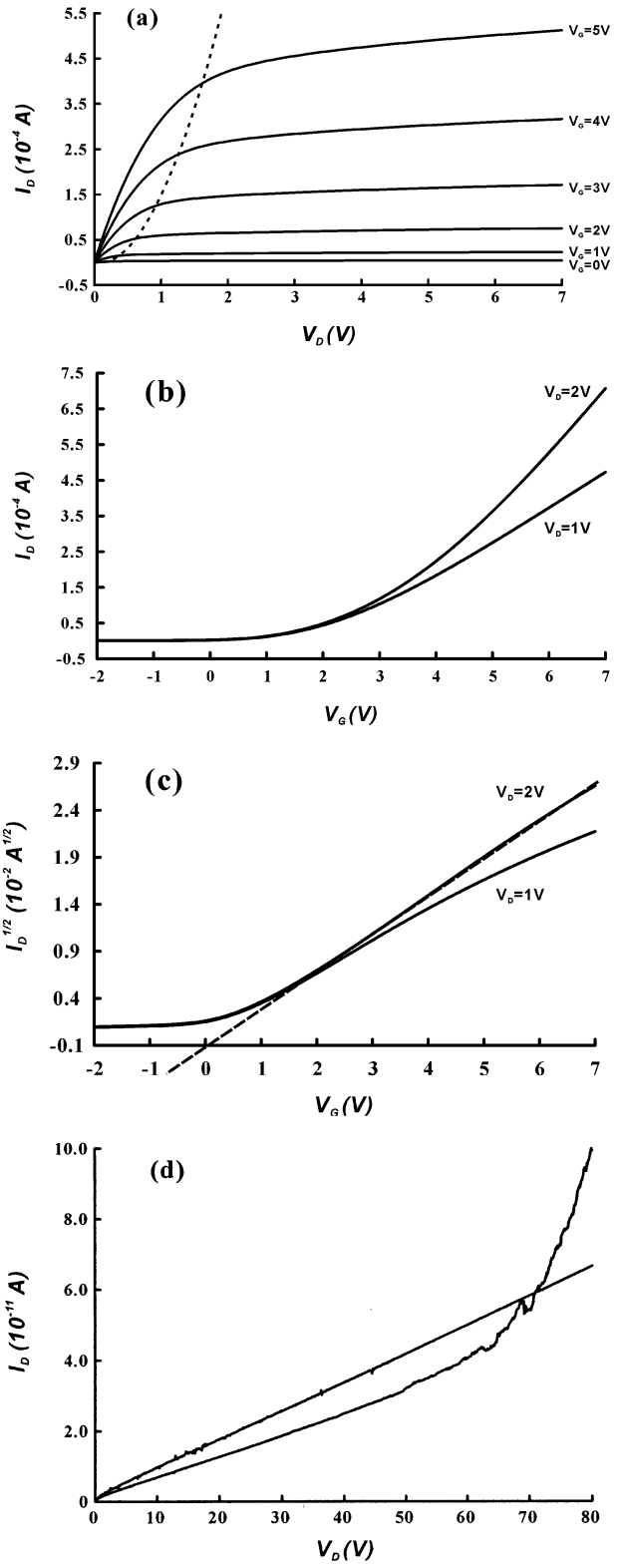


Figure 4. IGFET tests: (a) normal I_D-V_D characteristics; (b) normal I_D-V_G; (c) normal $\sqrt{I_D}-V_G$ characteristics used to evaluate the threshold voltage; (d) leakage current through the gate before and after "dielectric breakdown" recorded for two different transistors on the same chip. The voltage scan rate was 130 mV s^{-1}.

region (Figure 4a):

$$g_D = \left(\frac{dI_D}{dV_D}\right)_{V_G} = \frac{\mu C_0 W}{L}(V_G - V_T) \qquad (2b)$$

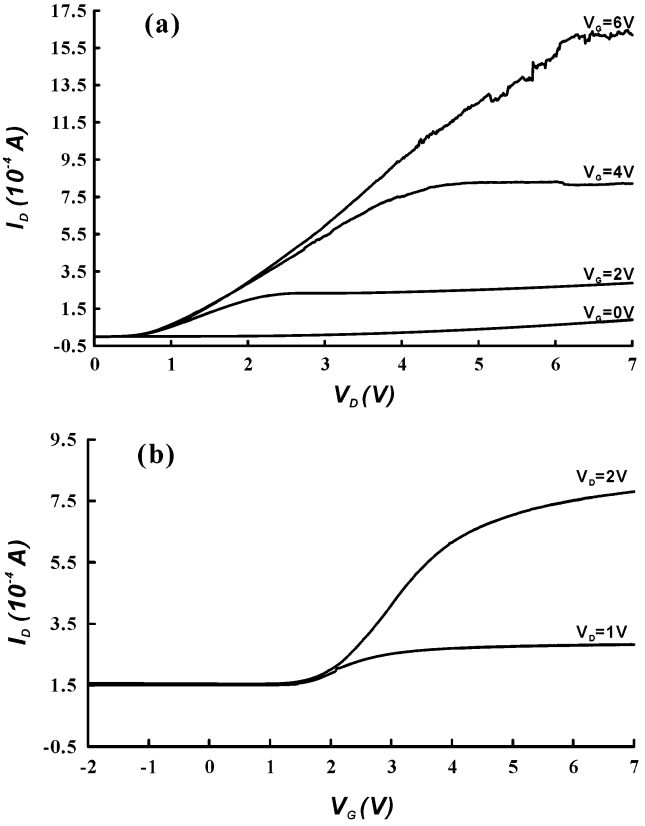


Figure 5. Transistor characteristics of the IGFET with contact resistance $R_C = 1.2 \times 10^4$ Ω. (a) I_D-V_D characteristics. The distortion due to the contact resistance is seen at low V_D. (b) Distorted I_D-V_G characteristics exhibiting typical "flattening" at $V_G > 3$ V.

Both g_m and g_D can be used to estimate the carrier mobility, μ, in the semiconductor.

If there is contact resistance R_C in series with channel resistance R_{Si}, then eq 2 must be written as

$$\left(\frac{dI_D}{dV_G}\right)_{V_D} = \left(\frac{dI_D}{dV_D}\right)_{V_G} = \left(\frac{1}{R_C + R_{Si}}\right)_{V_D} \qquad (3a)$$

As V_G increases, R_{Si} decreases until it becomes negligible compared to R_C. At that point, the transconductance is dominated by the resistance in series, and it is no longer dependent on the field modulation. More importantly, the value of g_m is not related to the mobility of the carriers in the semiconductor. The appearance of curves in Figure 5 illustrates this problem. The contact resistance, R_s, estimated from Figure 5b is 1.2×10^4 Ω. A visual inspection of the curve (i.e., a voltage shift) can provide a direct indication as to whether the experimental characteristics correspond to eq 1 and can be used for the estimate of mobility. Another cause of flattening of the I_D-V_G curve is the velocity saturation due to the variation of mobility at high applied longitudinal electric field.[10] In silicon, that onset of velocity saturation appears at much higher currents than reported here. Most importantly, velocity saturation does not give rise to the voltage shift in the I_D-V_D characteristics (Figure 5a), and the two effects can be easily distinguished from each other.

Effect of Leakage Current. An ideal FET should have zero current passing through the gate insulator. However, breakdown, facilitated by the defects in the gate dielectric, can occur under real conditions, leading to the catastrophic failure of the device. When this happens, the equations describing ideal IGFET

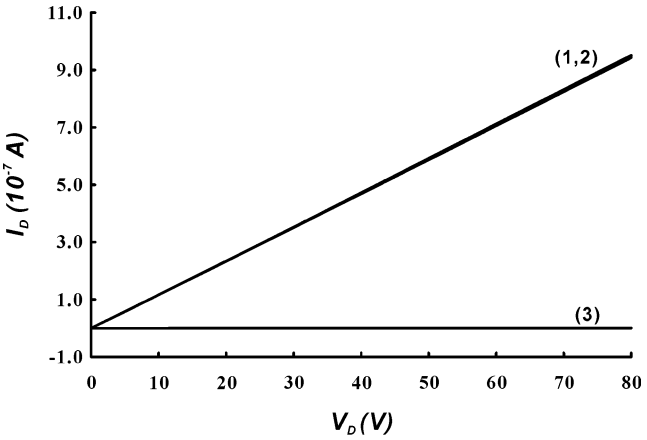


Figure 6. OFET "transistor" with (1, 2) doped and (3) undoped PPSA. The I_D-V_D at (1 and 2) $V_G = +40$ and -40 V, respectively. In both cases, the OFET behaved as a resistor showing no effect of applied gate voltage.

behavior no longer apply and cannot be used for any evaluation, including the characterization of material properties. The presence of a small leakage current is seen as the finite drain current at $V_D = 0$ V. There are many reports in the literature of devices exhibiting such behavior.[11−14] The dielectric breakdown for high-quality (dense, thermally grown) SiO_2 is estimated at a field strength of 6×10^5 V cm^{-1}. In our devices, this may occur at an applied gate voltage of around 60 V (Figure 4d). Once the device has been damaged by dielectric breakdown, it usually leaks at lower voltages on subsequent scans. This is illustrated by the erratic current observed in Figure 5a (the curve for $V_G = 6$ V).

Organic Field-Effect Transistor (OFET). To investigate the function of OS as the current-carrying semiconductor as a field-effect transistor, the device used for the IGFET characterization was configured as an OFET (Figure 1b). It is important to note that the Au source and drain contacts with PPSA are located 8200 Å above the silicon gate, essentially outside the electric field. In other words, only the portion of PPSA in the gate region is subjected to the applied gate field. The characteristics of this OFET using both a doped (curves 1 and 2) and an undoped (curve 3) conducting polymer, PPSA, are shown in Figure 6. In these measurements, a drain voltage of 80 V was applied, but no effect of applied gate voltage has been detected for $V_G = \pm 40$ V. The only difference between doped and undoped PPSA was its resistivity; otherwise, the OS behaved like a resistor, and the I_D-V_D dependence followed Ohm's law.

Conclusions

The universal platform described in this paper can be used to test a wide range of organic semiconductors as candidate materials for the fabrication of OFETs. It allows for a direct comparison with conventional IGFETs with similar geometry. The distinguishing features of this structure are the verifiable integrity of the gate dielectric resulting in zero gate leakage current and the placement of the contacts outside the electric field. Moreover, the contact metal is high-work-function Au, which is suitable for making ohmic contact to most p-type organic semiconductors. Both solvent-castable and sublimable OS can be used.

Ideal IGFET characteristics were obtained when PPSA was used as the gate conductor in the normal IGFET configuration. However, no field-effect modulation was observed when the device was configured as OFET. It behaved as a resistor over a wide range of applied V_G. The apparent failure of this material to undergo field-modulated changes in conductivity does not imply that other materials cannot be modulated by an electric field. However, it does point out that candidate OS should be tested under conditions that eliminate experimental artifacts.

When the observed experimental I_D-V_G and I_D-V_D curves depart from the normal characteristics described by eq 1a, it is an indication of a potential problem. The gate leakage current and the contact resistance are the most common culprits. Unfortunately, the leakage current is seldom measured and/or reported despite the fact that I_D-V_D curves clearly indicate its presence. Because of the highly variable nature of the onset of the breakdown of the gate dielectric, the results obtained for "leaky" field-effect transistors must be accepted with caution. The surface conductivity of the hydrated passivation layer can be another source of artifacts.

The presence of contact resistance and its effect on the transistor characteristics have been recognized and discussed by several authors.[15−18] The test platform described in this publication allows one to distinguish between the field modulation in the gate channel (i.e., in the OS) and/or at the contacts. From an operational point of view, such a distinction may not seem to be important, particularly if devices are fabricated in large batches and under scrupulously reproducible conditions. However, it is critically important in deciding where the optimization effort of OFET should be directed: at the quality of the contacts or at improvements in the electronic properties of the organic semiconductor.

The chemical modulation of the OS by atmospheric electron donor/acceptor molecules is of paramount importance.[9] When it occurs, it leads to the shift of the threshold voltage, which is seen as a shift in the position of the I_D-V_D curve along the V_G axis. Although such modulation is desirable and is the primary function of chemical sensors,[1] it would be considered to be a major nuisance in the operation of OFETs intended for signal or information processing. The effect of the ambient atmosphere on the performance of OFET has been reported.[19] The platform described in this report should enhance research in organic semiconductors, specifically, the definition of their correct place in electronics.[20]

Acknowledgment. The design of the platform was supported by NSF grant no. CHE-9816017, and its fabrication was supported by NSF grant no. ENG-95874. We thank David Collard for useful comments on and editing of the manuscript.

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