High-performance non-volatile CdS nanobelt-based floating nanodot gate memory

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High-performance, non-volatile, floating nanodot gate memories (FNGMs) based on single CdS nanobelts (NBs) are reported. Their structure consists of a CdS NB field-effect transistor and Au nanodots embedded in high-κ HfO_2 top-gate dielectrics. Direct tunnelling of charges between the CdS NB and the Au nanodots causes a shift of the threshold. A simple thermal evaporation method was employed to fabricate high-density, uniformly distributed Au nanodots ($\sim 3 \times 10^{12}$ cm^{-2}) in between a 5 nm HfO_2 tunnelling layer and a 15 nm HfO_2 control oxide layer. Under a low operation voltage of 5 V, a typical as-fabricated FNGM has a large memory window of 3.2 V, long retention time of up to 10^5 s, and good stress endurance of more than 10^4 write/erase cycles. The working principle of the CdS nanobelt-based FNGM is discussed in detail in this paper.

Introduction

Floating nanodot (ND) gate memory (FNGM) devices based on metal-oxide-semiconductor (MOS) structure have been widely studied due to their superior characteristics, such as lower operation voltage, faster write/erase speed, longer retention and better endurance, compared to conventional flash memories.[1–6] The FNGM devices usually introduce semiconductor or metal nanodots in between the tunnelling and control oxide layers as charge storage elements. Compared to their semiconductor counterparts, metal nanodots have the advantages of higher density of state around the Fermi level, a wide range of available work functions, stronger coupling with the conduction channel and smaller energy perturbation, due to carrier confinement.[7,8] In order to obtain high-performance FNGM devices, high-density, uniformly distributed metal nanodots are highly desired. In some earlier reported work, metal nanodots were first synthesized by colloidal methods, then spin-coated on the tunnelling oxide deposited on semiconductor channels.[9] A bio-mineralized method was also used to obtain high-density and homogeneous nanodots.[10] However, these methods will introduce extra organic materials, which should be thoroughly removed by additional cleaning processes. Radio frequency magnetron sputtering was another commonly used method to fabricate metal nanodots.[11] In this method, the power of sputtering should be precisely controlled in order to prevent destruction of the tunnelling layer, and an extra annealing process is required. Based on the above consideration, exploring simple ways to fabricate high quality metal nanodots in FNGMs has practical meaning. On the other hand, the semiconductor channels also play an important role in the FNGM devices. As one of the most important semiconductor materials, CdS nanowires/nanobelts (NWs/NBs) have demonstrated excellent performance in a wide range of prototype devices, such as laser devices,[12,13] logic gates,[14] piezoelectric nanogenerators,[15] photoconductors,[16] *etc.* However, to the best of our knowledge, there is no report on CdS NWs/NBs-based memory devices so far.

In this work, we report high-performance FNGMs based on single *n*-CdS NBs for the first time. A simple thermal evaporation method was employed to fabricate the high-density uniformly distributed Au NDs ($\sim 3 \times 10^{12}$ cm^{-2}, 4–6 nm in size) in between a 5 nm HfO_2 tunnelling layer and a 15 nm HfO_2 control oxide layer. No later treatment, such as cleaning, annealing *etc.* was employed. The typical CdS NB-based FNGM shows a large memory window of 3.2 V under a low operation voltage of 5 V, long retention time of up to 10^5 s, and a good stress endurance of more than 10^4 write/erase cycles.

Experiments

The CdS NBs used in the FNGMs were synthesized *via* an improved atmospheric vapor-liquid-solid (VLS) method.[14] The as-synthesized CdS NBs have excellent electrical properties.[17] The fabrication procedure for the FNGMs is as follows: first, CdS NB suspension was dropped on oxidized Si substrates, each with a 400 nm thick SiO_2 film on the top. Second, UV lithography followed by thermal evaporation and a lift-off process was used to fabricate two ohmic contact In/Au (40/80 nm) source and drain electrodes on an individual *n*-CdS NB (Fig. 1a). Third, a thin HfO_2 tunnelling layer (5 nm) was deposited to clad the NB by an atomic layer deposition (ALD) method. Next, a thin layer of Au film (~1 nm) was thermally evaporated, which would self-assemble into high-density discrete Au NDs on the tunnelling layer (Fig. 1b). Fifth, another HfO_2 film (15 nm) was deposited by ALD as the control oxide layer. Finally, an Au top gate electrode (120 nm thick) was made on the control layer in between the source and drain electrodes by a similar process as mentioned in step two (Fig. 1c). The high resolution transmission electron microscopy (HRTEM) image (Fig. 2a) shows that the as-fabricated Au NDs have sizes of 4–6 nm, and are uniformly distributed. The density of the NDs can be estimated to be as high as 3×10^{12} cm^{-2}. Fig. 2b is the

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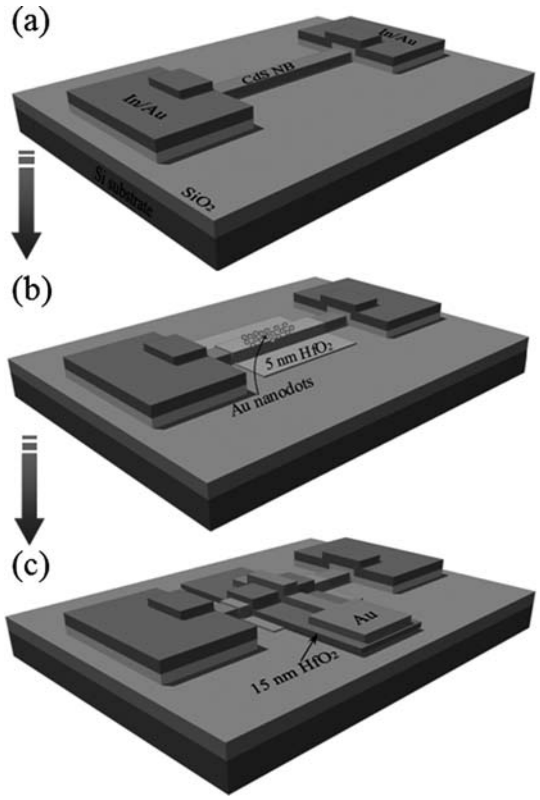

Fig. 1 A schematic illustration of the CdS NB-based FNGM fabrication process. (a) First, two ohmic contact source and drain electrodes were fabricated on a single *n*-CdS NB lying on a SiO_2/Si substrate. (b) Then, a 5 nm thick HfO_2 film was deposited by an ALD method as the tunnelling layer, followed by thermal evaporation of Au NDs; (c) a 15 nm thick HfO_2 film was deposited by ALD as the control oxide layer. Finally, a Au top gate electrode was made across the HfO_2/NB in between the source and drain.

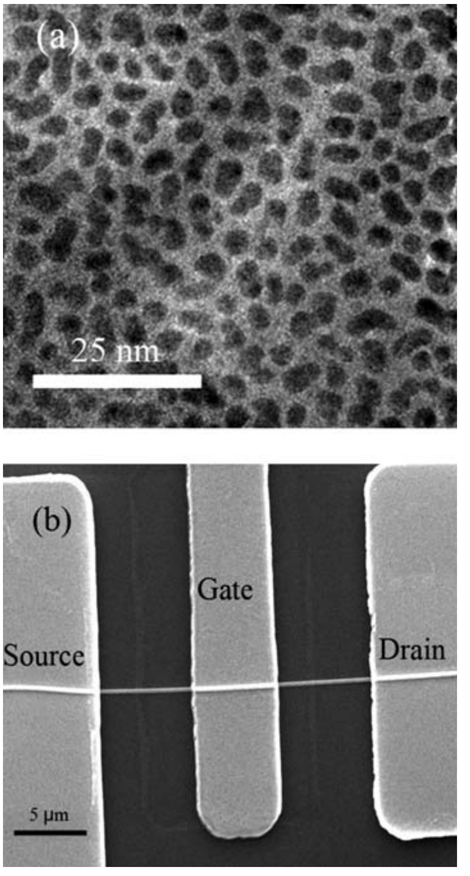

Fig. 2 (a) A HRTEM image of the thermally deposited discrete Au NDs with sizes of 4–6 nm distributed on the 5 nm HfO_2-coated CdS NB. (b) Top-view of a FESEM image of a CdS NB-based FNGM. The width and thickness of the CdS NB used in this FNGM are about 270 and 65 nm, respectively. The lengths of the channel and gate are about 18 and 6 μm, respectively.

top-view field-emission scanning electron microscopy (FESEM) image of a CdS NB-based FNGM. The lengths of the channel and gate are about 18 and 6 μm, respectively. The width and thickness of the CdS NB used in this FNGM are about 270 and 65 nm, respectively. The control devices with similar structure, but without the embedded Au NDs (the HfO_2 film is 20 nm) were also fabricated for comparison. Room-temperature electrical transport measurements on these devices were done with a semiconductor characterization system (Keithley 4200) and an arbitrary waveform generator (Tektronix AFG3000).

Results and discussion

Fig. 3a shows the gate transfer characteristic curves (I_{DS}–V_{GS} curves) for a typical control device in a gate voltage (V_{GS}) sweep range of ±5 V (V_{DS} = 0.5 V). The arrows indicate the sweeping directions. We can clearly see that the threshold voltage hysteresis is only about 0.1 V. This indicates that the influence of the charges within the insulator layer and/or at the insulator/semiconductor interface is negligible. The inset shows the source–drain current (I_{DS}) *versus* source–drain voltage (V_{DS}) relations at various V_{GS}. Fig. 3b shows the I_{DS}–V_{GS} curves of a typical CdS NB-based FNGM in three different sweep ranges (V_{DS} = 0.5 V). The memory windows (*i.e.* the threshold voltage shift ΔV_{th}) under ±1, ±3 and ±5 V double sweep range are about 0, 1.1 and 3.2 V, respectively. The neutral threshold voltage of the FNGM, defined as the V_{th} without any charges trapped in the Au NDs,[18] is about −1 V. This value is read from the I_{DS}–V_{GS} curve in the ±1 V sweep range, where the memory window is near-zero. As the gate voltage sweep range increases, obvious memory characteristics are observed, which originate from the tunnelling of the charges between the *n*-CdS NB channel and the Au NDs. It is worth noting that this type of FNGM can work under low operation voltages (≤ 5 V). Thus it may have practical applications, since, at present, the standard CMOS in semiconductor integrated circuits uses 5 V as the operation voltage.

The working principle of the CdS nanobelt-based FNGM can be understood by plotting the schematic energy band diagrams. Fig. 3c shows the schematic energy band diagram of the CdS NB-based FNGM prior to contacting the power supply. Fig. 3d (upper) shows the writing process of the FNGM. Under a V_{GS} of −5 V, electrons will flow from Au NDs *via* direct tunnelling through the 5 nm HfO_2 layer. The positive charges left in the Au NDs after the writing process will help to accumulate the electrons in CdS NB channels at gate voltages within ±1 V (*e.g.* V_{GS} = 0) (Fig. 3d (lower)), resulting in a higher I_{DS} (logic 1)

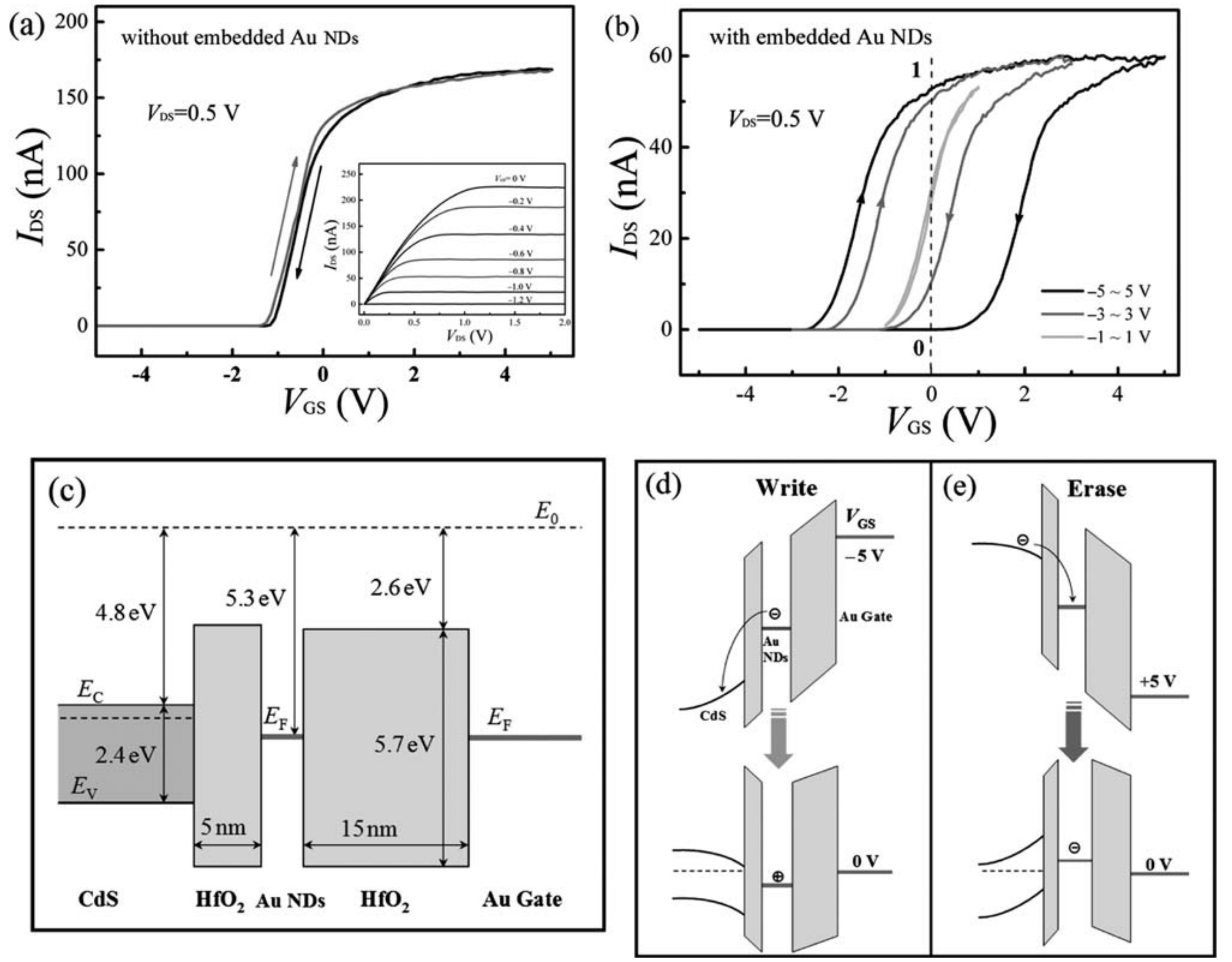

Fig. 3 (a) The gate transfer characteristic curves at $V_{DS} = 0.5$ V of a typical control device (without Au NDs embedded in gate dielectrics) for the double sweep of V_{GS} between ±5 V. The arrows indicate the sweeping directions. The inset shows the I_{DS}–V_{DS} relations at different V_{GS}. (b) I_{DS}–V_{GS} curves in three different double sweep ranges of a CdS NB-based FNGM. The memory windows under ±1, ±3 and ±5 V V_{GS} double sweeps are about 0, 1.1 and 3.2 V, respectively. (c) A schematic energy band diagram of the CdS NB-based FNGM prior to contacting the power supply. (d)/(e) Energy band diagrams of the writing/erasing process (upper) and retention mode after writing/erasing (lower), respectively.

(see Fig. 3(b)). Fig. 3e (upper) shows the erasing process of the FNGM. Under a V_{GS} of +5 V, electrons will flow into Au NDs by direct tunnelling. The negative charges left in the Au NDs after the erasing process will help to deplete the electrons in the CdS NB channel (Fig. 3e (lower)), resulting in a lower I_{DS} (logic 0) (see Fig. 3(b)). From the memory window (ΔV_{th} = 3.2 V) obtained under the ±5 V of V_{GS}, we can estimate the total number of charges stored in each Au ND by the following equation:[19,20]

$$\Delta V_{th} = \frac{Q}{\varepsilon_{OX}}\left(t_G + \frac{1}{2}\frac{\varepsilon_{OX}}{\varepsilon_{ND}}D_{ND}\right)$$

where Q is the charge density (C cm^{-2}) in the nanodot, t_G is the thickness of the control oxide layer (15 nm), and D_{ND} is the size of the Au ND (~5 nm). ε_{ox} (~$17\varepsilon_0$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F cm^{-1}) and ε_{ND} are the permittivities of HfO_2 and Au ND, respectively. Since the permittivity of metal ND is very high (>$10^5\varepsilon_0$),[21] the second term of the equation above can be ignored. From this equation, Q is calculated to be 3.2×10^{-6} C cm^{-2}. Therefore, one Au ND stored about 6.7 charges using the density of the Au NDs (~3×10^{12} cm^{-2}). The size of the Au NDs mainly determines the number of charges trapped within them, and hence affects the memory windows and retention time.[22] Generally speaking, larger NDs tend to trap more charges due to the smaller Coulomb charging energy gap.[9,23] On the other hand, too large metal dots can lead to faster charge loss.[8] We think the sizes of our Au NDs (4–6 nm) here are proper, which can trap enough charges to cause enough of an on-off ratio between the logic 1 and logic 0 states, and can also avoid fast charge loss.

Fig. 4a shows the retention characteristics of a typical as-fabricated FNGM. The device was first written for 2 s at $V_{GS} = -5$ V. Then, the time dependences of the I_{DS} (gray curves) at V_{GS} = −1 V (△) and at V_{GS} = 0 (⊙) were measured, respectively. Next the device was erased for 2 s at V_{GS} = +5 V, and the time dependences of the I_{DS} (black curves) at V_{GS} = 0 (⊙) and at V_{GS} = −1 V (△) were measured, respectively.

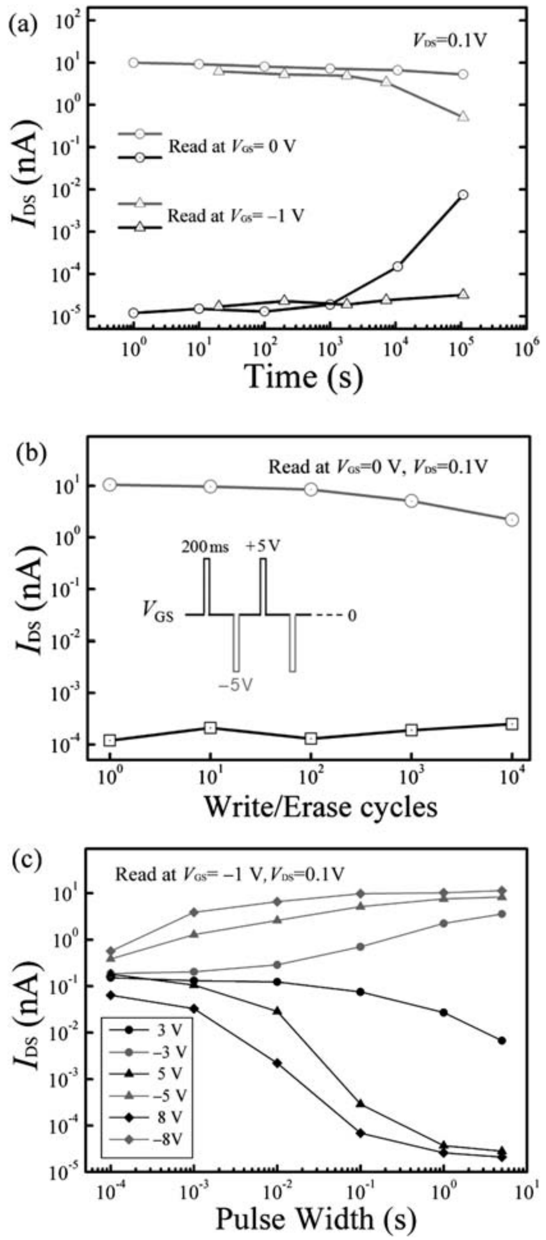

Fig. 4 (a) The retention characteristics of the CdS NB-based FNGM were carried out by measuring the I_{DS} change after the device was charged for 2 s under a V_{GS} of 5 V and −5 V (V_{DS} = 0.1 V). (b) Stressing characteristics of the FNGM was performed by applying a ±5 V erase/write pulses with 200 ms duration and a period of 2 s. (c) The speed characteristics of the FNGM, which were investigated by measuring I_{DS} *versus* the switching time relation at various pulse amplitudes.

We can clearly see that the on-off ratio between the logic 1 and logic 0 states are still up to about 10^3 and 10^4, respectively, at V_{GS} = 0 and −1 V after up to 10^5 s. This indicates that the CdS NB-based FNGM is non-volatile. We think the long retention time results from the higher charge storage ability of the Au NDs, due to its high work function. Besides the work function of Au was reported to increase when in contact with Hf-based high-κ materials, due to the Fermi level pinning effect.[11,24] Moreover, the separation of the Au NDs limits the lateral flow of charge.[1] Basically, there are two possible processes for the long-term loss of the trapped charges. One is the charge tunnelling from the trap states to the states at the HfO_2/CdS NB interface. The other is the charge tunnelling from the trap states to CdS NB.[25] As in our case, the states at the HfO_2/CdS NB interface are much less, as demonstrated by the control device (see Fig. 3a), we think the latter process dominates the long-term loss of the trapped charges.

The stress endurance (see Fig. 4b) of the FNGM was studied by applying ±5 V erase/write pulses with 200 ms duration and a period of 2 s. In the meantime, the I_{DS} values (V_{GS} = 0 V and V_{DS} = 0.1 V) were measured, with the gray and black curves for the logic 1 and logic 0 states, respectively. We can see that there is little change in the on-off ratio for up to 10^4 write/erase cycles. This indicates that the as-fabricated FNGMs have good stress endurance characteristics. We have also investigated the device speed of the CdS NB-based FNGM, since speed is an important parameter to evaluate the performance of memory devices. Because the neutral threshold voltage of our FNGM is around −1 V, we characterize the device speed at V_{GS} = −1 V by measuring the I_{DS} *versus* the voltage pulse relations. Fig. 4c shows the I_{DS} *versus* the pulse width (switching time) relation at various pulse amplitudes. We can see that the device has higher speed at higher pulse amplitude, as expected. That is, at higher voltage amplitude, shorter pulse widths are needed to obtain a rational on-off ratio. An on-off ratio of ∼10 between the logic 1 and logic 0 states can be obtained in 0.1 ms at ±8 V pulse amplitudes. To obtain higher speeds, larger tunnelling currents are needed. The tunnelling current is very sensitive to the thickness of the tunnelling oxide.[19] We think that the speed of our CdS NB-based FNGMs could be further improved by optimizing the tunnelling oxide.

Conclusions

In summary, high-performance, non-volatile CdS NB-based FNGMs were fabricated for the first time. A simple thermal evaporation method was used to fabricate high-density (∼3 × 10^{12} cm^{-2}), uniformly distributed Au nanodots with sizes of 4–6 nm. At a low operation voltage of 5 V, a typical as-fabricated FNGM has a large memory window of 3.2 V, a long retention time of up to 10^5 s, and good stress endurance of more than 10^4 write/erase cycles. These merits make the CdS NB-based FNGM an attractive alternative to current non-volatile memory devices.

Acknowledgements

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