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Growth and Performance of Yttrium Oxide as an Ideal High- κ Gate Dielectric for Carbon-Based Electronics

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ABSTRACT High-quality yttrium oxide (Y_2O_3) is investigated as an ideal high- κ gate dielectric for carbon-based electronics through a simple and cheap process. Utilizing the excellent wetting behavior of yttrium on sp^2 carbon framework, ultrathin (about few nm) and uniform Y_2O_3 layers have been directly grown on the surfaces of carbon nanotube (CNT) and graphene without using noncovalent functionalization layers or introducing large structural distortion and damage. A top-gate CNT field-effect transistor (FET) adopting 5 nm Y_2O_3 layer as its top-gate dielectric shows excellent device characteristics, including an ideal subthreshold swing of 60 mV/decade (up to the theoretical limit of an ideal FET at room temperature). The high electrical quality Y_2O_3 dielectric layer has also been integrated into a graphene FET as its top-gate dielectric with a capacitance of up to 1200 nF/cm², showing an improvement on the gate efficiency and on state transconductance of over 100 times when compared with that of its back-gate counterpart.

KEYWORDS Yttrium Oxide, high- κ , field-effect transistor, carbon nanotube, graphene, carbon-based electronics

The International Technology Roadmap for Semiconductors (ITRS) reveals that the silicon-based technology would reach its performance limits by 2020s, meanwhile carbon-based nanoelectronics including carbon nanotubes (CNTs) and graphene is regarded as one of the promising alternatives for extending Moore's law.^{1–3} The CNT based field-effect transistors (FETs) have been shown to have many advantages when compared with the silicon-based FETs.^{4–15} The graphene FET (G-FET) also exhibits ballistic electron transport and excellent FET properties similar to CNT FETs.^{14–17} But in addition the G-FET can provide the required large on-state current I_{on} that is especially important for high-frequency applications simply by increasing the graphene channel width of the transistor which is impossible for CNT FETs.^{18,19} For all high-performance FETs, high quality gate dielectric with high- κ (dielectric constant) is highly desirable. This is because high- κ dielectric can be utilized to improve the gate capacitance and thus the controlling efficiency of the gate. The two most important gate-related performance metrics of a FET are transconductance (g_m) for the on state and subthreshold swing (SS) for the off state. Although various high- κ dielectrics have been demonstrated to be technically compatible with carbon-based devices,^{8–13,18,20} it is proved to be very difficult to grow uniform thin high- κ film directly on the surface of CNTs or graphene via a general method, for example, atomic layer deposition (ALD). This

is because for a good quality CNT or graphene there exists only delocalized π -bond on the surface of sp^2 hybridization plane, but not many nucleation sites, for example, defects or dangling bonds.^{21,22} Growing thick gate dielectric layer via ALD to bury CNTs is one of the utilities to achieve top-gate high- κ dielectric in CNT FETs.^{8–13} This method is simple to realize but simultaneously limits the ultimate scaling-down on the thickness of the gate dielectric. For example, ALD grown HfO_2 film thicker than 8 nm is needed to fully cover a CNT and to avoid gate leakage.²¹ As a result the corresponding SS value of the CNT FET fabricated this way remains considerably higher than its theoretical value, that is, 60 mV/dec.²¹ The situation is worse for a high quality graphene sheet on which the ALD film can be grown only at the edges or defect sites.^{22,23} To realize direct nucleation on the surface of CNTs or graphene and consequently to grow uniform high- κ film, several methods have been developed that build nucleation sites via surface treatments before ALD growth. These methods include perylene tetracarboxylic acid (PTCA), DNA molecule, NO_2 , and O_3 functionalizations.^{18,21–26} The introduction of the noncovalent functionalization layers (NCFLs) or pretreatments not only adds technical complexity, but also affects the transport properties of the fabricated CNT and graphene FETs, leading to electric field variation and extra scattering brought by the functionalization molecules,^{18,19} and sometimes even damage to the sp^2 carbon framework.²⁷ A well-designed buffered dielectric for a G-FET does not significantly degrade its carrier mobility, but it lowers its gate efficiency due to the reduced effective κ value and added gate thickness.^{19,20} Ideally, we would like

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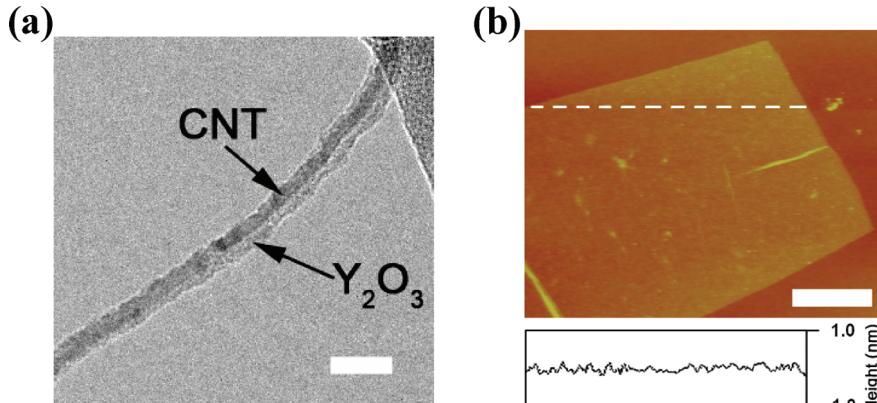


FIGURE 1. Microstructure characterization of the Y_2O_3 coating on CNT and graphene. (a) TEM image of a single CNT coated with about 5 nm thick Y_2O_3 . The image was taken in an under focus condition and the contrast was enhanced by the Fresnel interference effect. Scale bar is 20 nm. (b) AFM image of graphene covered with about 5 nm Y_2O_3 thin film. Scale bar is 1 μm . The height profile through the dashed line is shown below the image with a height scale from −1.0 to 1.0 nm, indicating a smooth morphology of the Y_2O_3 thin film on graphene.

to have a simple, clean, and harmless method to grow ultrathin high-quality high- κ gate dielectric for the further development of carbon-based electronics, and it is the aim of this letter to show that ultrathin yttrium oxide (Y_2O_3) film can be readily grown on CNTs and graphene providing an ideal gate dielectric for carbon-based FETs. We demonstrate that a top-gate CNT FET adopting Y_2O_3 as its top gate dielectric can deliver an ideal SS of 60 mV/dec, which is the theoretical limit for an ideal FET at room temperature. When integrated into a G-FET, the ultrathin Y_2O_3 gate dielectric is shown to have improved the gate efficiency for more than 100 times when compared with that of a back-gate G-FET.

The IIIB subgroup metal oxide Y_2O_3 is one of the most investigated high- κ dielectrics with a dielectric constant κ of about 15.^{28,29} High quality Y_2O_3 thin film can be grown through depositing Y thin film followed by thermal oxidation.²⁹ While Y_2O_3 has been extensively studied for Si-based electronics, it has not yet been explored for carbon-based electronics. In an earlier work, we found that Y shows excellent wetting with CNT³⁰ which is similar to Ti, Ni, and Pd.³¹ But Ti, Ni, and Pd oxides all have a band gap of less than 5 eV and are thus unsuitable for being used as gate dielectrics.²⁸ On the other hand, Y_2O_3 has an energy gap of about 6 eV and therefore a very low leakage current and high breakdown field. Because of the good wetting of Y with the sp^2 carbon framework, the Y film deposited on the CNT or graphene appears continuous and uniform. When the uniform Y thin film is oxidized, a continuous Y_2O_3 film is then formed. In this work, we evaporate Y film with a nominal thickness of about 3 nm by a high vacuum e-beam deposition system, followed by 10 min thermal oxidization at 180 °C in air to transfer Y into Y_2O_3 . The resulting ultrathin Y_2O_3 film (with a thickness of about 5 nm, measured by AFM and confirmed by ellipsometry analysis) showed very low leakage current (see Figure S1a in Supporting Information), a dielectric constant of about 8 (obtained by standard C–V measurement) and very good smooth morphology [for CNT,

referring to the transmission electron microscope (TEM) image shown in Figure 1a]. Unlike the previously reported direct ALD grown high- κ film on CNTs,²¹ the 5 nm Y_2O_3 thin film coated on the CNT seems to be continuous having a relatively smooth morphology. The good wetting behavior of Y on CNT is expected to be extendable to graphene, since the latter is also consisted of sp^2 carbon framework. This is indeed what we observed in the AFM image of the SiO_2 /graphene/ Y_2O_3 (5 nm) structure shown in Figure 1b. It is shown in height profile that the mean roughness of the Y_2O_3 thin film is ~0.2 nm. The 5 nm thick Y_2O_3 film prepared by evaporation of metal Y followed by oxidization in air therefore provides an excellent high- κ gate dielectric for fabricating top-gate carbon-based electronic devices and in what follows we will discuss the performance of these devices.

We first consider using the thin Y_2O_3 film as the top-gate dielectric for CNT FETs. Single-walled CNTs used in this work were grown via catalytic chemical vapor deposition (CVD) method on a p-doped silicon wafer,³² which was covered with a 500 nm SiO_2 layer. Source (S) and drain (D) electrodes of the CNT FET were defined via e-beam lithography (EBL), and a 60 nm scandium (Sc) film was then evaporated followed by a standard lift-off process. Gate oxide layer was also defined by EBL which covered the whole channel region, and the Y_2O_3 film with a thickness of 5 nm was formed by evaporating Y followed by thermal oxidization as just discussed. The gate electrode was formed by evaporation of 10 nm titanium (Ti) thin film. The as-made device structure is shown in Figure 2a, and its scanning electron microscope (SEM) image is shown in Figure 2b. The diameter d of the CNT used in this device is 1.2 nm. The source and drain electrodes are connected by a CNT channel of 2 μm , and in the middle of the channel a gate electrode (with a width of 1 μm) is fabricated. Electrical measurements were carried out in a vacuum chamber under a base pressure of 1×10^{-6} Torr at room temperature. The gate leakage current I_{gs} is smaller than 20 pA for V_{gs} up to 2 V, suggesting that

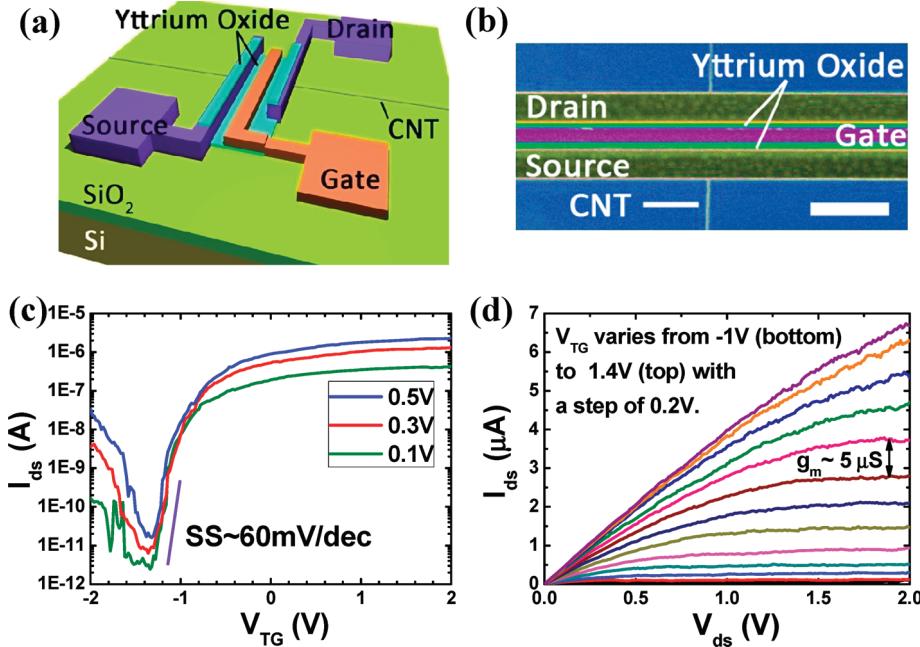


FIGURE 2. Device geometry and performance of a top-gate CNT FET with a thin layer of Y_2O_3 as the top gate dielectric. (a) Schematic diagram of the device structure. (b) SEM image of an as-made CNT FET device with the scale bar denoting $5 \mu\text{m}$. This CNT device is based on a SWCNT with a diameter of 1.2 nm , the channel length of the device is $2 \mu\text{m}$ and the top-gated length is $1 \mu\text{m}$. (c) Transfer characteristics of the device for $V_{\text{ds}} = 0.1, 0.3, 0.5 \text{ V}$ respectively from bottom to top. A SS of 60 mV/decade is shown. (d) Output characteristics of the device for V_{tg} varying from -1 (bottom, black) to 1.4 V (top, purple) with a step of 0.2 V . In all the measurements, the back-gate is kept at $V_{\text{bg}} = 40 \text{ V}$ to electrostatically n-dope the ungated nanotubes segments near the contact regions. The arrow indicates a maximum transconductance of $5 \mu\text{S}$, being 4200 S/m after normalized by the diameter of the nanotube ($d \sim 1.2 \text{ nm}$).

the thin Y_2O_3 gate dielectric is of very high dielectrical quality (see Figure S1b in Supporting Information).

A typical transfer and output characteristics of the CNT FET are shown in Figure 2c,d. Perfect n-type transfer characteristics (Figure 2c) are expected for a Sc-contacted FET since the Sc electrode forms an ohmic contact to the conduction band of the CNT providing a barrier-free electron injection into the FET.⁷ For the two ungated CNT segments between the top-gate finger and the source and drain electrodes, we can apply a moderately large back-gate bias (with $V_{\text{bg}} = 40 \text{ V}$) to electrostatically n-dope these region. This large V_{bg} keeps the “un-gated” (by the top-gate) CNT channels in their on-state, while the top-gate is used to switch off the CNT channel beneath the gate from its constant on state. The $I_{\text{on}}/I_{\text{off}}$ ratio of the CNT device can reach more than 5 orders of magnitude even for $V_{\text{ds}} = 0.5 \text{ V}$, and the normalized (by d) saturation current of the CNT FET is as high as $6 \text{ mA}/\mu\text{m}$ for $V_{\text{ds}} = 2 \text{ V}$ and $V_{\text{tg}} = 1.4 \text{ V}$ (Figure 2d). The switching property of a FET can be characterized by its transconductance g_m and subthreshold swing SS.³³ The normalized (by d) transconductance of our n-type FET of up to 4200 S/m is almost as high as the best value achieved by p-type FET with a similar structure and dimension,²¹ suggesting an excellent top-gate modulation to the on-state current of our device. The SS of 60 mV/decade (Figure 2c) presents a perfect (up to the theoretical limit for an ideal FET at room temperature) transition between the on and off

states,³³ and this is the first time such a perfection has been realized for n-type CNT FETs. The SS of 60 mV/decade was reported for p-type CNT FETs fabricated by ALD deposition of $2\text{--}3 \text{ nm}$ HfO_2 film on CNT, which was functionalized with DNA.²¹ Although the gate electrostatic capacitance [estimated using $C_{\text{ox}} = 2\pi\epsilon_0\kappa/\ln(2 + 4t/d)$] for the Y_2O_3 gate dielectric (with a larger thickness $t \sim 5 \text{ nm}$ and lower dielectric constant $\kappa \sim 8$) in our n-type FET is only about 1.5 pF/cm , the perfect SS value shows that perfect gate control is still realized. This is mainly benefitted from the fact that the Y_2O_3 thin film is directly coated to the CNT surface without the use of any NCFL, and the latter may introduce a small gap of molecular scale between the gate oxide and the CNT reducing the effective gate efficiency.

We now consider the use of Y_2O_3 as the gate dielectric in graphene-based FETs. A single-layer graphene was deposited by mechanical exfoliation on an n-doped silicon substrate ($\rho \sim 2 \Omega \cdot \text{cm}$) that was covered with a 300 nm thick SiO_2 . The layer number of the graphene was characterized by AFM and micro-Raman spectroscopy. Reactive ion etching (RIE) was employed to shape the graphene ribbon via oxygen plasma. The lithography processes were accomplished via EBL, followed by thin film growth and a standard lift-off process, which are basically the same as that for fabricating CNT FETs. The source and drain electrodes were made up of 60 nm Sc, and the top-gate stack was composed of 5 nm Y_2O_3 gate dielectric and 10 nm Ti. The G-FET devices were

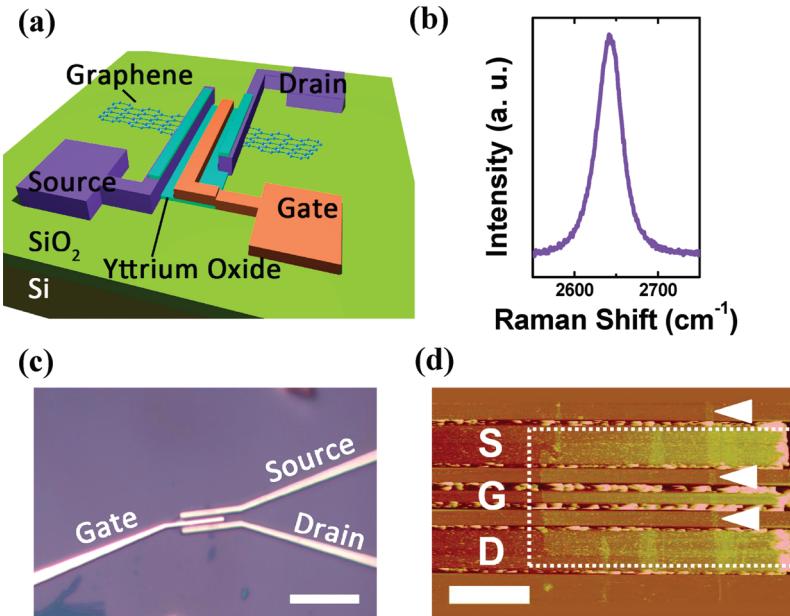


FIGURE 3. Structure and characterization of a top-gate G-FET with a thin layer of Y_2O_3 as the top gate dielectric. (a) Schematic diagram illustrating the device geometry. (b) Raman spectrum taken from the graphene used for fabricating the G-FET, suggesting a single layer graphene. The spectrum was excited by a laser of 633 nm wavelength. (c) Optical microscope image showing a low-magnification view of the G-FET. The scale bar denotes 10 μm . (d) AFM image showing a magnified view of the device shown in (c). The scale bar denotes 2 μm . The arrow tips point to a graphene nanoribbon with a width of 200 nm. The electrodes are source (S), gate (G), and drain (D), respectively, from top to bottom. The channel length is 1.5 μm and the top-gate length is 0.6 μm . The dotted block indicates the area covered with Y_2O_3 .

also tested at room temperature in vacuum with a base pressure of 1×10^{-6} Torr. The device structure of the top-gate G-FET is shown in Figure 3a, and a typical Raman spectrum obtained from the graphene ribbon used in the G-FET is shown in Figure 3b, suggesting that the graphene is a single layer graphene.³⁴ The optical microscope and AFM images of the device are shown in Figure 3c,d respectively, and the region covered by the Y_2O_3 gate dielectric is marked in Figure 3d with the dotted line.

Figure 4 contrasts the transfer characteristics of a back-gate G-FET before and after the growth of the top-gate Y_2O_3 dielectric. Both transfer characteristics show a suppressed hole current in the p-region (for $V_{\text{BG}} < 0$). Before the growth of the top Y_2O_3 gate dielectric, this conductance asymmetry is caused by the use of the Sc contact, which has a work function of 3.3 eV that is far above the Fermi level of the graphene.⁷ The Sc contact injects electrons more effectively into the G-FET than holes, and it is this imbalanced carrier injection that results in the conduction asymmetry observed in the green curve of Figure 4a.³⁵ The transfer characteristic obtained after the growth of the top Y_2O_3 dielectric (red curve in Figure 4a) shows a much more suppressed hole current. This is because the measurement was made under the condition that the top gate was biased with $V_{\text{TG}} = 2$ V (to avoid unwanted interference effects), and this top-gate bias electrostatically doped the graphene channel into n-type leading to even more severe imbalanced carrier injection. It should be noted that for top-gate G-FETs, significant degradation of current, transconductance, and carrier mo-

bility usually occurred after the fabrication of the top-gate due to the additional charged impurity and interface phonon scattering introduced by the top-gate oxide.^{18,36} However in our case the top-gate G-FET shows only limited degradation of electron current and transconductance (see Figure 4a–c). The current under $V_{\text{BG}} = 40$ V and peak transconductance are respectively 14.2 μA and 0.28 μS for a plain back-gate device, and these values reduced slightly to 13.4 μA and 0.25 μS after the growth of the top Y_2O_3 dielectric layer. This represents a 6% degradation of electron current and 11% degradation of transconductance, suggesting that the electrical quality of the Y_2O_3 /graphene interface is very high and only few additional scattering centers were introduced.

We now consider how the electron mobility of our n-type G-FET is affected by the presence of the top-gate dielectric. From the transfer characteristic of the G-FET (Figure 4c), the field-effect mobility μ_{FE} can be retrieved through fitting the transfer characteristic to the equation

$$R_{\text{total}} = R_c + \frac{1}{e\mu_{\text{FE}}\sqrt{n_0^2 + n^2}W} L \quad (1)$$

where $R_{\text{total}} = V_{\text{ds}}/I_{\text{ds}}$ is the total resistance of the device including the channel resistance and contact resistance R_c , e is the electron charge, L and W are the length and width of the graphene ribbon, respectively, and n_0 and n are the

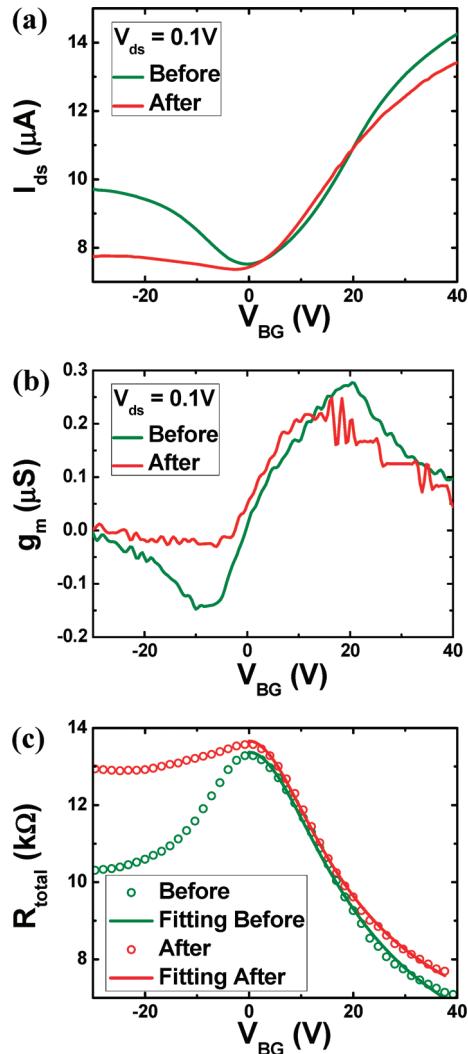


FIGURE 4. Performance and characteristics of a back-gate G-FET, with a graphene channel length of $1.5\text{ }\mu\text{m}$ and a channel width of $0.8\text{ }\mu\text{m}$. Back-gate (a) transfer characteristics, (b) transconductance (g_m) characteristics, and (c) total resistance characteristics of the G-FET before and after the deposition of Y_2O_3 with $V_{\text{ds}} = 0.1\text{ V}$. When measuring transfer curve after oxide, the top-gate is fixed at $V_{\text{TG}} = 2\text{ V}$ to avoid unwanted interference effects. In (c), the circles represent experimental data points, and solid lines denote that of fitting using eq 1 for extracting electron mobility from the experimental data.

carrier density due to residual impurities and back-gate modulation, respectively.^{19,20} The capacitive carrier density n is related to the gate voltage via the equation

$$V_{\text{BG}} - V_{\text{Dirac}} = \frac{ne}{C_{\text{ox}}} + \frac{\hbar v_F \sqrt{\pi} n}{e} \quad (2)$$

where the first term on the right-hand side of eq 2 describe the carrier density induced by the back gate via C_{ox} (with C_{ox} being the back-gate electrostatic capacitance, \hbar being the Planck constant and $v_F \approx 10^6\text{ m/s}$ being the Fermi velocity

in graphene), and the second term describes the effect of quantum capacitance in graphene.^{19,20} The extracted electron mobility μ_{FE} is about $1200\text{ cm}^2/\text{V}\cdot\text{s}$ and $1000\text{ cm}^2/\text{V}\cdot\text{s}$ before and after the growth of top Y_2O_3 dielectric layer respectively. The experimental data and numerical fitting using eq 1 are both given in Figure 4c, showing clearly that the thin Y_2O_3 dielectric layer is of rather high electrical quality bringing in little additional scattering and mobility degradation. But we now show that this little sacrifice will bring significant improvement in gate efficiency and therefore overall device performance.

The electrical characteristics of the top-gate G-FET are shown in Figure 5. The top-gate transfer characteristics (Figure 5a) and transconductance curves (Figure 5b) suggest an excellent top gate control on the conductance of the graphene channel. In this top gate G-FET, the back-gate was utilized to electrostatically dope the ungated (by the top-gate) graphene segments between the top gate and S/D electrodes. Therefore when the back-gate was biased at 40 V , the graphene segments between the top-gate and S/D were n-doped, and the p-branch of the top-gate transfer characteristic (or hole current) was suppressed. On the other hand, when the back gate was reversed from 40 to -40 V , the n-branch or electron current is suppressed as a result of the imbalanced carrier injection. It should be noted that the global back-gate also affects the total carrier density along the whole graphene channel and thus the charge neutral or the Dirac point in the top-gate transfer characteristic, and the shift of the Dirac point as a function of V_{BG} is shown in Figure 5c. Near the Dirac point we have the charge neutrality condition

$$\Delta V_{\text{BG}} C_{\text{BG}} + \Delta V_{\text{TG,Dirac}} C_{\text{TG}} = 0 \quad (3)$$

A linear dependence of the Dirac point shift $\Delta V_{\text{TG,Dirac}}$ on V_{BG} is then expected, and this is indeed what we observe in Figure 5c. The slope of the $V_{\text{TG,Dirac}} - V_{\text{BG}}$ line is determined by the ratio between the back-gate capacitance and top-gate capacitance of unit area, that is, $C_{\text{BG}}/C_{\text{TG}}$. Figure 5c shows that the ratio $C_{\text{TG}}/C_{\text{BG}}$ is about 100 , and this ratio is much larger than that of previously demonstrated devices,^{18–20,36,37} suggesting a significant improvement in the gate efficiency. Using the back-gate capacitance value (for a SiO_2 dielectric of 300 nm) of $C_{\text{BG}} = 12\text{ nF/cm}^2$, the top-gate capacitance is estimated to be $C_{\text{TG}} = 1200\text{ nF/cm}^2$, which is larger than all published gate capacitance of G-FETs.^{18–20,36,37}

The improvement of gate efficiency is also manifested in the transconductance characteristics shown in Figure 5b. The peak transconductance of the top-gate G-FET is about $12\text{ }\mu\text{S}$ (for $V_{\text{ds}} = 0.1\text{ V}$), which compared with $0.09\text{ }\mu\text{S}$ for the back-gate G-FET (Figure 5c), representing more than 130 times improvement on the device on-state performance when measured using the g_m metrics. The output characteristics (Figure 5d) also demonstrate an

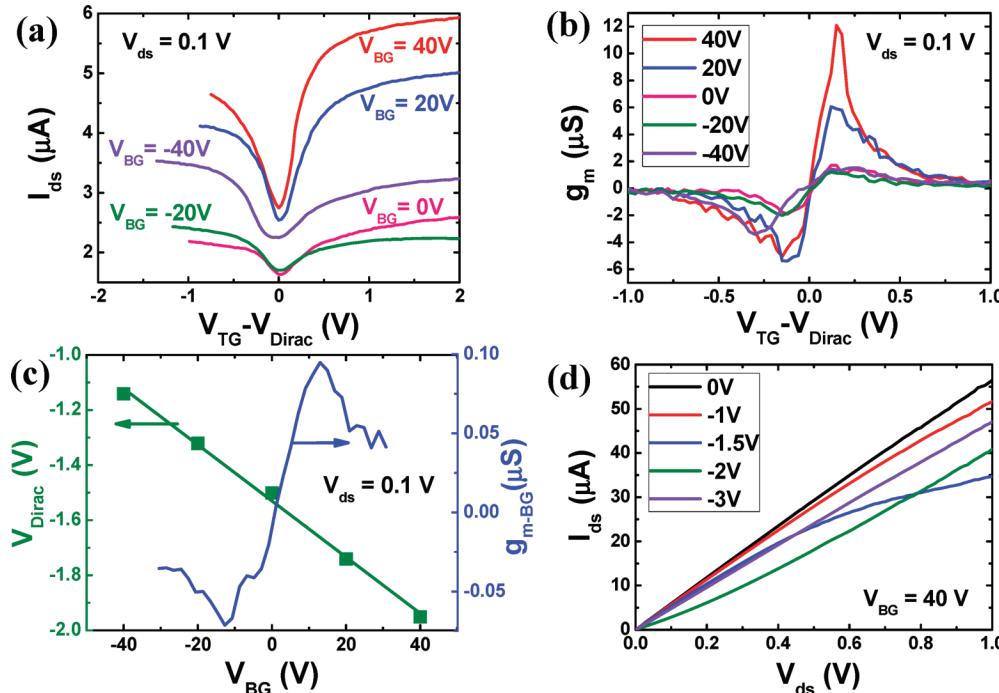


FIGURE 5. Performance and characteristics of a top-gate G-FET with a geometry specified in Figure 3. (a) Room temperature top-gate transfer characteristics of the device for $V_{ds} = 0.1$ V in vacuum with a back-gate V_{BG} equals 40, 20, 0, -20, and -40, V respectively. All the curves are shifted so that their Dirac points are all located at the origin. (b) The corresponding transconductance characteristics of the device at $V_{ds} = 0.1$ V. The back-gate voltages are indicated in the inset legend. (c) Top-gate Dirac point position and back-gate transconductance versus back-gate voltage. The square points are the experimental data and the straight line is the linear fitting of the data, indicating a linear modulation on the Dirac point via back-gate voltage. (d) Top-gate output characteristics of the device. The drain voltage sweeps from 0 to 1 V with V_{TG} equals 0, -1, -1.5, -2, and -3 V, respectively.

excellent top-gate modulation of the graphene channel current. An anomaly output characteristic was observed while the top-gate voltage was biased at -1.5 V, and this may be attributed to the carrier type transition from electron to hole.³⁷

Since the method of growing Y_2O_3 film used in this work is not optimized, the quality of the grown film is thus far from perfect. First the low dielectric constant of about 8 (much lower than the standard value of 15) indicates that the Y_2O_3 film is very loose in structure. Second the large hysteresis of about 0.3 V observed in the transport property of the G-FET using Y_2O_3 as the top gate dielectric (see Figure 2S of Supporting Information) indicates that there exist plenty of charge traps in the interface between Y_2O_3 and graphene. It is well-known that the quality of the dielectric can be improved significantly by optimizing grown conditions via such processes as annealing in Ar at high temperature.²⁶ We expect that the performance of carbon-based devices will be improved further by optimizing the quality of the Y_2O_3 gate dielectric layer.

In conclusion, we demonstrated that high electrical quality and ultrathin yttrium oxide layer of 5 nm can be directly grown on sp² carbon framework, including carbon nanotube and graphene and be utilized as the top-gate dielectric for CNT and graphene FETs. While for the top-gate CNT FET an ideal subthreshold swing SS of 60 mV/decade is realized and for the top-gate graphene FET an top-gate capacitance of

about 1200 nF/cm² is realized, representing an over 100 times gate efficiency improvement when compared with that of the back-gate G-FET.

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Supporting Information Available. Leakage current through Y_2O_3 thin film, and a typical leakage current curve through the top-gate of the CNT FET. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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