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Charge Injection in High-κ Gate Dielectrics of Single-Walled Carbon Nanotube Thin-Film Transistors

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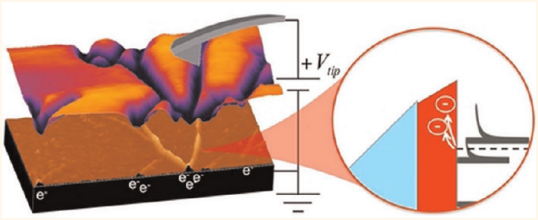
ABSTRACT



We investigate charge injection into the gate dielectric of single-walled carbon nanotube thin-film transistors (SWCNT-TFTs) having Al_2O_3 and HfO_2 gate dielectrics. We demonstrate the use of electric field gradient microscopy (EFM) to identify the sign and approximate the magnitude of the injected charge carriers. Charge injection rates and saturation levels are found to differ between electrons and holes and also vary according to gate dielectric material. Electrically, Al_2O_3 gated devices demonstrate smaller average hysteresis and notably higher average on-state current and p-type mobility than those gated by HfO_2. These differences in transfer characteristics are attributed to the charge injection, observed *via* EFM, and correlate well with differences in tunneling barrier height for electrons and holes formed in the conduction and valence at the SWCNT/dielectric interface, respectively. This work emphasizes the need to understand the SWCNT/dielectric interface to overcome charge injection that occurs in the focused field region adjacent to SWCNTs and indicates that large barrier heights are key to minimizing the effect.

KEYWORDS: charge injection · high-κ dielectric · hafnia · alumina · HfO_2 · Al_2O_3 · atomic layer deposition · carbon nanotube · field effect transistor · thin film transistor

Single-walled carbon nanotubes (SWCNTs) have attracted significant attention as a nanoelectronic material because of their high thermal conductivity, aspect ratio, charge carrier mobility, and maximum current density.[1] Improvements in performance-related factors such as chiral polydispersity,[2−5] environmental sensitivity,[6] and large scale integrability,[7,8] have incrementally advanced SWCNT based electronics toward commercial applications. Despite this, their transition from the laboratory to a commercially viable product has yet to be realized on a large scale. Primary among the challenges impeding the adoption of SWCNTs in commercial nanoelectronics is a prominent gate hysteretic response.[9−12] The associated instability of threshold voltage and inconsistent performance during repeated testing bring into question the stability and ultimate utility of SWCNTs as an electronic channel material. The understanding and mitigation of this gate transfer hysteresis are essential to the viability of SWCNTs as a nanoelectronic transport material.

Hysteresis in SWCNT thin-film transistors (SWCNT-TFTs) has been attributed to a variety of mechanisms. Atmospheric adsorbates, mobile ions in the gate dielectric or in the TFT channel, and charge injection from the SWCNT channel into the gate dielectric have all been studied as possible mechanisms giving rise to hysteresis. The role of atmospheric adsorbates on the observed SWCNT-TFT hysteresis response is well studied,[6,11,13−15] and significantly reduced hysteretic behavior is commonly reported in studies where electrical measurements are performed under vacuum. Aguirre *et al*. propose that water and its associated redox couples provide molecular levels well-matched with the SWCNT conduction and valence band mediating electronic transfer from the SWCNT into its surroundings.[15] For SWCNTs on SiO_2, hysteresis can persist under UHV and at low temperature,[9] although complete subsidence is observed in devices with suspended SWCNTs[11] and greatly reduced when the SiO_2 is treated with hydrophobic passivants including parylene[15] and hexamethyldisilazane.[16] Therefore, atmospheric adsorbates play a strong role, but hysteresis is observed in their absence indicating that a mechanism associated with the gate dielectric must also contribute.[10]

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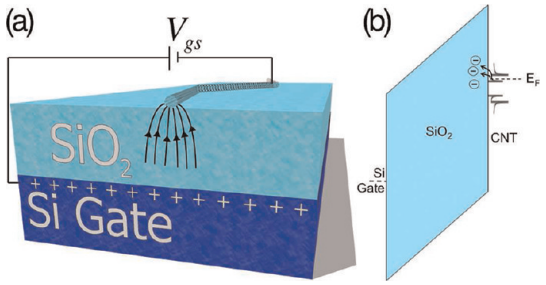

Figure 1. (a) Schematic diagram depicting the electric field in the gate dielectric that results from forward biasing the back gate in reference to a SWCNT. (b) Band structure diagram of the device in panel a again under high forward bias taken at one point along the SWCNT channel. The arrows now indicate electrons tunneling into the resulting triangular barrier region, which may transmit through or become trapped in surface states and deep levels in the oxide.

Mobile ionic impurities, namely Na^+, may have a role in the hysteretic response in SWCNT-TFTs, especially considering the prevalence of Na^+ containing surfactants (including sodium dodecylsulfate, sodium cholate, sodium deoxycholate) used to form stable SWCNT dispersions for electronic type separations and thin-film deposition.[3,5] Hysteresis in SWCNT-TFTs may be caused by the deposition and removal of Na^+ from the SWCNT surface or by Na^+ within the gate dielectric migrating toward or away from the SWCNT channel as the gate is swept between positive and negative bias levels. In both instances, Na^+ causes electron doping of the SWCNT either through direct charge transfer or capacitive coupling, and under typical biasing conditions (see Methods) manifests in electrical characterization as a shift toward *negative gate bias* in the p-channel. In contrast, most reported hysteresis in p-channel SWCNT-TFTs exhibits a threshold voltage shift toward *positive gate bias* during the reverse sweep.[14,17] Furthermore, this behavior has been observed at low temperatures (~20 K) where ionic transport is impeded, further supporting that indeed another mechanism plays a role.[9]

Charge injection at the SWCNT/dielectric interface is a result of the high electric field localized near the SWCNT under application of a high gate bias.[17,18] Classically, this is illustrated by the convergence of electric field lines adjoining at the SWCNT, as in Figure 1a. Under typical biasing conditions, this can give rise to a local electric field that is greater than the breakdown field of the bulk dielectric. Viewed quantum mechanically, the conduction (valence) band offset of the gate dielectric with respect to the SWCNT forms a triangular potential barrier through which tunneling may occur,[18] as in Figure 1b. In both views, the biasing conditions and focused field at the SWCNT interface lead to the reversible injection of charge into the gate dielectric material. In SWCNT-TFTs having SiO_2 gate dielectrics, adsorbed H_2O plays a role in the mediation of this charge injection mechanism *via* electron charge injection into the solvated oxygen redox couple.[15] Various scanning probe techniques have been utilized to provide visual evidence of the charge injected near the SWCNT/SiO_2 interface[19−21] and studies of the charge injection in SiO_2 estimate that the injected charges remain trapped <10 nm from the SWCNT/dielectric interface.[22] Charge injected at the SWCNT/dielectric interface dynamically screens the applied gate bias and affects $I-V$ transfer characteristics, resulting in hysteresis if the trapped charge lifetime is comparable to the time scale of the measurement. The positive (negative) charge of trapped holes (electrons) leads to a threshold voltage shift toward negative (positive) gate bias.

High-κ dielectrics have emerged as materials of significant interest in carbon nanoelectronic applications.[23−26] Common high-κ materials are synthesized *via* atomic layer deposition (ALD), which is performed at moderate temperatures (90−400 °C) and may be deposited directly onto SWCNTs without affecting their atomic structure, thus enabling top-gate architectures. The comparably higher dielectric constant over that of SiO_2 (κ = 3.9, 9.8, and 25 for SiO_2, Al_2O_3, and HfO_2, respectively) allows device designers to simultaneously reduce gate leakage current and maintain or increase the gate capacitance by varying the layer thickness. For instance, the thickness of an Al_2O_3 gate-dielectric layer may be scaled to 2.5 times that of a SiO_2 gate-dielectric while maintaining the same capacitance and channel control. The dielectric constant of ALD-grown thin films is usually less than the bulk value. To account for this, and for dielectric stacks comprising two or more dielectric layers, high-κ films are often characterized by their effective dielectric constant κ_{eff} or effective SiO_2 thickness t_{eff}. Recently, ALD grown high-κ dielectric layers were integrated with SWCNTs to form n-channel SWCNT-FETs for logic,[25] and to fabricate charge-trap memory devices.[27] These uses imply large charge trap densities in ALD-grown high-κ dielectrics, and therefore characterization of charge injection mechanisms at the SWCNT/high-κ dielectric interface is key to mitigating or enhancing the effect for various device applications.

In the first part of this study, SWCNT-TFTs having Al_2O_3/SiO_2 (23 nm/100 nm) and HfO_2/SiO_2 (23 nm/100 nm) gate dielectrics are characterized by electric force gradient microscopy (EFM). This technique is utilized to image and quantify the charge injected at the SWCNT/dielectric interface. These results reveal a clear difference between Al_2O_3 and HfO_2 in terms of their charge injection behavior. The second part of this study consists of a compilation of electrical characterization, including drain current−gate voltage transfer characteristics and the associated extracted parameters, of 78 SWCNT TFTs with Al_2O_3 gate dielectrics and 78 SWCNT-TFTs with HfO_2. Both device structures

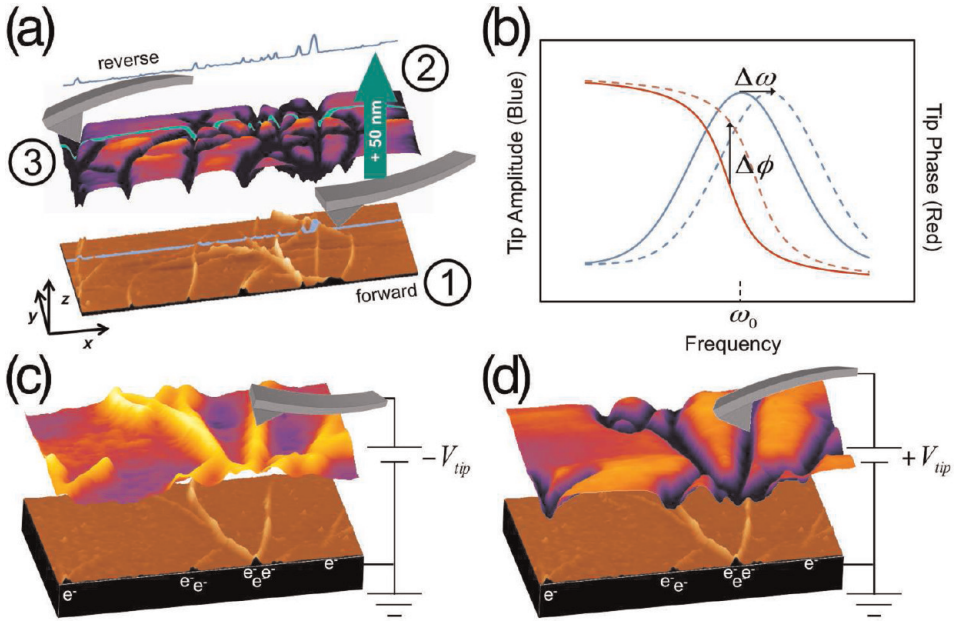

Figure 2. (a) 3-D schematic depicting the EFM measurement technique. (1) Forward scan. A height profile of the sample is recorded; (2) the tip is lifted to a fixed height from the surface (50 nm) and the constant distance is maintained by the AFM feedback mechanism. (3) Reverse scan. In this lifted position, the electric force gradient experienced by the tip due to charge distributed on the surface produces an EFM phase map. (b) Graph depicting the relationship between the change in resonant frequency (blue) of the AFM cantilever from equilibrium (solid) due to an electric force gradient and the change in phase of the AFM tip relative to the AFM feedback mechanism; in this case, this phase shift (red) reflects an attractive force gradient. (c) 3-D surface view depicting the measured EFM phase map overlaid with its associated height profile; the EFM contrast indicates a repulsive force gradient. (d) 3-D surface views depicting the measured EFM phase map and its associated attractive force gradient. In panels c and d, the repulsive and attractive force gradients are obtained on the same sample by applying a positive or negative tip bias, respectively.

exhibit comparable effective oxide thicknesses and were fabricated from the same SWCNT thin-film with identical metallization, allowing a systematic, direct comparison of SWCNT-TFT performance based on gate dielectric material. Devices with a Al_2O_3 gate dielectric demonstrate less average hysteresis and notably higher average on-state drain current and hole mobility than those with a HfO_2 gate dielectric. Comparisons of tunneling rates of electrons and holes are consistent with experimental data and point to strategies for enhancing or mitigating the charge injection effect. In the Supporting Information, we provide derivations for relevant equations, a discussion of the EFM technique and data interpretation, a comparison of SWCNT-TFT gate transfer characteristics measured in air and in vacuum, and capacitance voltage characteristics of the high-κ dielectrics on SiO_2.

RESULTS

Theory. Electric field gradient microscopy (EFM) is a specialized mode of atomic force microscopy (AFM) that facilitates the detection of variations in localized charge on a surface.[20,21,28] EFM is a dual-scan technique performed alongside standard AFM tapping mode measurements, meaning each scan line displayed is the compilation of a tapping-mode topography scan and a lifted-scan where the tip oscillates freely. Tip oscillation in tapping and lift mode is mechanically driven by a piezoelectric transducer in the tip holder.

In the forward scan, labeled 1 in Figure 2a, the probe-tip measures a surface topography profile. In the reverse scan, the cantilever is lifted and the topographical data from the forward scan is used to hold the tip at a prescribed distance from the surface (2 in Figure 2a). In this lifted position, and in the absence of fixed charge on the sample's surface, the probe tip oscillates freely at its resonant frequency and set amplitude. In the presence of fixed surface charge, the probe tip experiences an electrostatic force $F(z)$ (3 in Figure 2a) causing a measurable deviation in the oscillation frequency ω_0 of the tip, given by

$$\Delta\omega \cong -\frac{\omega_0}{2k}\frac{\partial F}{\partial z} \quad (1)$$

where k is the spring constant of the probe cantilever. EFM data measured during the lifted scan is recorded as $\Delta\phi$, the change in phase lag of the cantilever response to the drive voltage applied to the piezoelectric transducer. For small values of $\partial F/\partial z$, $\Delta\phi$ is related to the electrostatic force by

$$\tan(\Delta\phi) \cong -\frac{Q}{k}\frac{\partial F}{\partial z} \quad (2)$$

A derivation of this relationship is provided in the Supporting Information. Figure 2b illustrates the relationship

between $\Delta\omega$ and $\Delta\phi$ as it would be observed for a force gradient yielding $\Delta\omega > 0$.

The magnitude and direction of the electrostatic force experienced by the tip is a function of the surface charge, q_s and the bias applied to the tip relative to the sample stage, V_{tip}. For our instrument (Digital Instruments NanoScope IIIa), regions exhibiting an attractive force gradient result in $\Delta\omega < 0$ and $\Delta\phi < 0$. Such regions appear dark in contrast on the EFM micrograph. Conversely, regions exhibiting repulsive force gradients appear bright in contrast. This contrast inversion can be observed by reversing the polarity of the applied tip bias in the presence of surface charge, as shown in Figure 2c,d. In both cases, surface electrons are illustrated and larger contrast differences are interpreted as force gradients with larger magnitude.

To relate $\Delta\phi$ to the charge density on the surface of the sample, we examine the force, F, experienced by the tip during the lifted scan. We take $z = 0$ to represent the sample's surface and positive z to be above the surface. With this orientation, F is given by

$$F(z, V_{tip}, q_s) = \frac{1}{2}\frac{dC}{dz}V_{tip}^2 + \frac{Cq_s}{4\pi\varepsilon_0 z^2}V_{tip} - \frac{q_s^2}{4\pi\varepsilon_0 z^2} \quad (3)$$

where C is the capacitance of the tip−sample system and ε_0 is the permittivity of free space. The first term is a force arising from the energy stored in the tip−sample capacitor system. The second term is the force due to the charge induced on the tip by the applied bias V_{tip}. The third term is independent of V_{tip} and is a result of the surface charge q_s and its mirror charge in the tip. In the discussion that follows, we will take q_s to be the charge injected at the SWCNT/dielectric interface.

We model the tip−sample capacitor as a sphere, of radius R, at a distance, z, from a plane. For $(z/R) > 1$, the capacitance of the system can be approximated by

$$C = \frac{2\pi\varepsilon_0 R^2}{z} \quad (4)$$

The use of the sphere-to-plane capacitor to model the tip-to-surface capacitance is ultimately an incomplete description of the system and a discussion of this approximation is given in the Supporting Information. However, the use of this model allows the identification of the sign of the surface charge q_s. Combining eq 2−4 and differentiating, we find

$$\tan(\Delta\phi) \cong \frac{Q}{kz^3}\left[-2\pi\varepsilon_0 R^2 V_{tip}^2 + \frac{3q_s R^2}{2z}V_{tip} - \frac{q_s^2}{2\pi\varepsilon_0}\right] \quad (5)$$

With this relation, we can relate the data obtained *via* EFM to the static charge present on the surface of a sample.

Device Architecture. SWCNT-TFTs having different gate dielectrics are investigated. To prepare the substrates, 23 nm of Al_2O_3 (bulk $\kappa = 9.8$) and HfO_2 (bulk $\kappa = 25$) are deposited *via* ALD atop 100 nm thermal SiO_2 on a p-type Si wafer.[29] The substrates are then treated by rapid thermal annealing (RTA), the details of which are included in the Methods section. A random network thin film of 98% pure semiconducting SWCNTs are deposited on the separate dielectric substrates. The resulting devices are globally back gated and unpassivated to ambient conditions. The fabrication process provides high device yield to allow a statistical approach to compare data between devices having different gate dielectrics. A device schematic is provided in Figure 3.

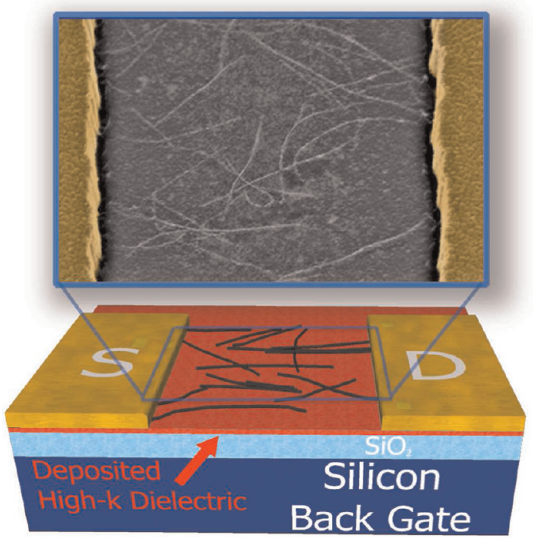

Figure 3. Device schematic of SWCNT/ALD/SiO_2/Si gate stack with false colored scanning electron microscope image illustrating typical SWCNT thin-film density. The source drain electrode separation in the SEM image is 2 μm.

The focus of the investigation is the SWCNT/dielectric interface. The chosen device architecture allows the gate dielectric material to be RTA treated independently of the carbon nanotube device metallization, which is otherwise incompatible with the high temperatures involved. ALD films are known to form charge traps when interfaced with Si[30] and so the chosen architecture features an intermediate SiO_2 layer to reduce interface charge traps. In addition, the thick SiO_2 layer results in both dielectric stacks having comparable total capacitance. RTA treatment is performed to remove charge traps at the dielectric interfaces and reduce the occurrence of mobile ions and capacitance−voltage (C−V) measurements performed before and after RTA treatment indicate a removal of interface trapped charges and a reduction of C−V hysteresis (see Figure S2 of the Supporting Information). Extracted values of κ are found to be 4.8 and 17.1 for the Al_2O_3 and HfO_2 films, respectively.

EFM Measurements. In this section, we apply the EFM technique to image the charge injected at the SWCNT/dielectric interface. For simplicity, we assume that charge observed *via* EFM is entirely surface charge. Note that eq 5 is quadratic in V_{tip}, and plotting $\tan(\Delta\phi)$ against V_{tip} yields a parabola that is concave down with

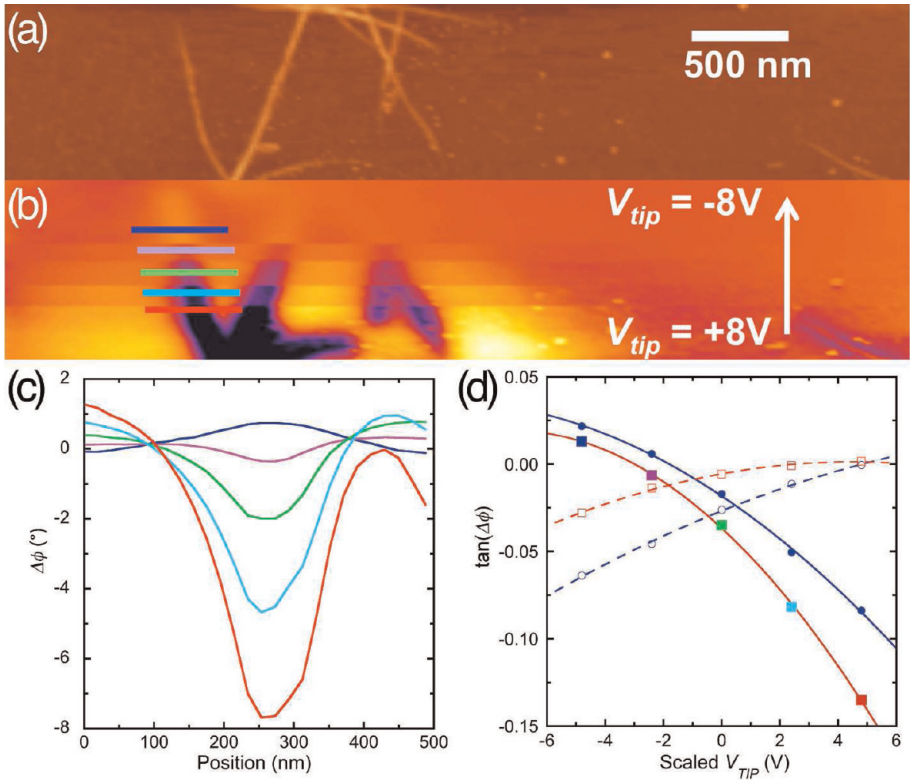

Figure 4. (a) AFM micrograph depicting height profile taken during EFM measurement of Al_2O_3 device biased at $V_{gs} = +15$ V for 60 s and (b) the associated EFM phase response with varying values of V_{tip}. (c) EFM phase profiles as a function of V_{tip}; profile colors correspond to the profile lines indicated in panel b. (d) Tangent of peak height *versus* V_{tip} for Al_2O_3 (red) and HfO_2 (blue) devices biased at $V_{gs} = -15$ V (open) and $+15$ V (filled); for Al_2O_3 at $V_{gs} = +15$ V, colored data points correspond to peak heights of colored profiles from panels b and c; the lines correspond with quadratic fits, and parabolas having a vertex with $V_{tip} < 0$ correspond to injected electrons, while parabolas having a vertex with $V_{tip} > 0$ correspond to injected holes.

negative *y*-intercept. Moreover, a parabola of the form $y = ax^2 + bx + c$ has a vertex with *x* coordinate $x = -(b/2a)$. Thus, the graph of tan ($\Delta\phi$) *versus* V_{tip} has its vertex at

$$V_{tip} = \frac{3q_s}{8\pi\varepsilon_0 z} \qquad (6)$$

The sign of this quantity depends only on the sign of q_s. As a result, plotting tan($\Delta\phi$) *versus* V_{tip} and noting the V_{tip} coordinate of the vertex allows us to determine the sign of the surface charge q_s. In the absence of surface charge (*i.e.*, $q_s = 0$) the resulting parabola would have its vertex at $V_{tip} = 0$ and would thus be symmetric about the *y*-axis. The presence of negative charge ($q_s < 0$) causes the resulting parabola vertex to have $V_{tip} < 0$, and the opposite is observed for positive charge.

In a typical experiment, we inject charge into a sample under predetermined biasing conditions, and then measure the peak $\Delta\phi$ as a function of V_{tip}. Plotting tan($\Delta\phi$) *versus* V_{tip} allows the determination of the sign of the injected charge as discussed above. Devices are biased at a constant gate voltage V_{gs} with the source grounded and drain floating, under a continuous flow of dry N_2 to reduce adsorption of surface contaminants. After biasing, samples are transferred to the AFM, and EFM measurements are performed. Figure 4 panels a and b give an example of the AFM height profile and the EFM $\Delta\phi$ data for an Al_2O_3 device biased at $V_{gs} = -15$ V for 1 min. For reference, the drain electrode is adjacent to the lower left region image and contacts the SWCNTs just out side the field of view; it is electrically floating during scanning probe measurements. Note that V_{tip} is varied during a single image capture to reduce time between measurements. Figure 4c is a compilation of $\Delta\phi$ profiles corresponding to the colored horizontal lines in Figure 4b and markers in Figure 4d. In addition, Figure 4d contains plots corresponding to Al_2O_3 and HfO_2 biased at $V_{gs} = +15$ V and -15 V for 1 min. Parabolas having vertices with $V_{tip} < 0$ correspond to injected electrons, and parabolas having vertices with $V_{tip} > 0$ correspond to injected holes. We observe that for both dielectric materials, $V_{gs} = -15$ V resulted in injected holes while electrons are injected when $V_{gs} = +15$ V. Note the SWCNT bundle in the lower right corner of the AFM micrograph and the difference in its EFM contrast relative to the SWCNTs measured on the left. The lone SWCNT bundle lacks an EFM response because it is electrically isolated from the metal contact and as a result does not contribute to current in the channel or charge injection into the dielectric. Additionally, we note that V_{tip} is the total potential drop from the tip to the sample stage,

which is in electrical contact with the sample's silicon substrate. The capacitance of the sphere-to-plane capacitor assumes a conductive plane (sample) and the presence of the gate dielectric reduces the potential drop from the probe tip to the sample surface. Values of V_{tip} in Figure 4d are reduced by a factor of $C_{air}/(C_{air} + C_{ox})$, where C_{air} and C_{ox} are the capacitance of the air and dielectric layers, respectively. Finally, the signs of the charges present at the dielectric surface after biasing are opposite of what would be expected if the migration of mobile ions were the primary mechanism contributing to the accumulation of charge near the SWCNT. Instead, the injected charge signs correspond to the charge carrier doping in the SWCNTs at the respective bias conditions.

We use EFM to measure the relative amounts of charge injected during different biasing conditions and in the different dielectrics. For $V_{tip} = 0$, eq 5 simplifies to a single electrostatic term that is independent of the capacitance of the system. Therefore, further EFM measurements are performed with $V_{tip} = 0$. Devices are biased at $V_{gs} = \pm 15$ V for 10, 20, and 30 s, and measured following each biasing, giving total bias times of 10, 30, and 60 s. The sphere-to-plane capacitor model features an effective area of $2\pi R^2$. We use this to estimate the injected charge per unit area, which we plot as a function of total bias time in Figure 5a. We observe that most combinations of substrate and injected carrier saturate at a level that is in the mid 10^{12} carriers/cm^2 range, the notable exception being holes in Al_2O_3, which saturate at a lower charge density. Moreover, the charge saturation generally occurs at or before 10 s, which is consistent with the observation that a "hold time" of 5 s at high bias before performing a gate sweep saturates the charge injected in SiO_2 devices.[9]

Figure 5b illustrates relaxation (*via* thermionic emission, recombination, etc.) of injected electrons in an Al_2O_3 device. The device was biased at $V_{gs} = +15$ V for 30 s and time $t = 0$ corresponds to the end of biasing. The first EFM measurement is taken ~8.5 min after biasing and indicates the time required to transfer the sample to the AFM, navigate to the device, and bring the tip into contact. The graph features two exponential fitting curves indicating fast ($<10^3$ s, $\tau = 1.4 \times 10^3$ s) and slow ($>10^3$ s, $\tau = 9.7 \times 10^3$ s) carrier relaxation processes involved in the dissipation of injected charge near the SWCNTs. Extrapolating to $t = 0$ s, the short-term curve indicates a 1.5× greater charge density at the cessation of biasing than is measured ~8.5 min later. This serves as a lower-bound for the level of injected charge since additional fast processes ($\tau \ll 10^3$ s) may contribute to carrier relaxation but have relaxed at the time of the first measurement. With this result, we revisit the data included in Figure 5a and estimate that electrons in Al_2O_3 and holes and electrons in HfO_2 saturate at the high 10^{12} carriers/cm^2 range. For comparison, a parallel-plate capacitor with the high-κ dielectric stacks used here and biased at 10 V would yield a surface carrier density of $\sim 2 \times 10^{12}$ carriers/cm^2, consistent in magnitude with the injected charge carrier densities reported here.

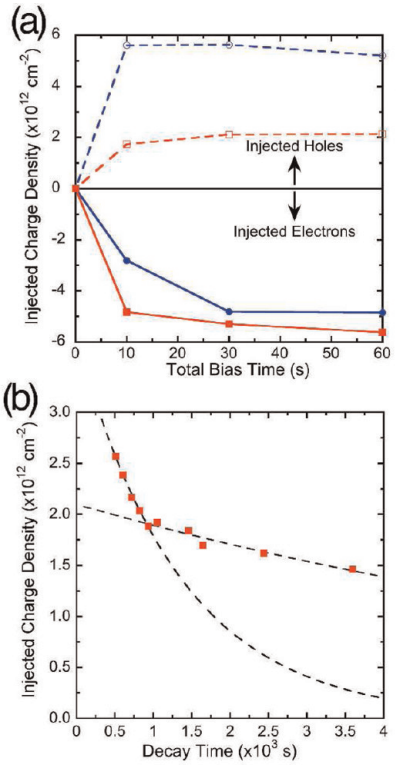

Figure 5. (a) Density of injected charge versus bias time for Al_2O_3 (red) and HfO_2 (blue) biased at $V_{gs} = -15$ V (open) and +15 V (filled); sign of charge given by quadratic fits in Figure 4d. (b) Time decay of injected electron charge density in Al_2O_3 device; two exponential fits indicate fast and slow mechanisms involved in self-discharge process; extrapolation of short-term exponential indicates ~1.5× higher charger density at $t = 0$ compared to time of first measurement.

At the above estimated injected charge densities, it is reasonable to expect the injected charges to screen the bias applied by the gate. If charge injection is in fact the mechanism that leads to $I-V$ hysteresis in SWCNT FETs, then the devices should exhibit a significant hysteresis response when tested electrically. Moreover, the disparity in injected charges in the different dielectrics (namely the lower levels of hole injection in Al_2O_3) should lead to differences in transfer characteristics between devices having an Al_2O_3 gate dielectric and those having HfO_2. We look to electrical characterization of these devices to determine if indeed these predicted device characteristics are observed.

Electrical Measurements. Devices studied in the previous section were characterized electrically to quantify the effect of injected charge on current−voltage transfer characteristics. All electrical measurements are performed under vacuum to reduce the effect of atmospheric adsorbates during testing. We observe differences between tests performed under ambient

TABLE 1. Primary Differences Observed in *I*−*V* Transfer Characteristics for Al_2O_3 Devices Compared to HfO_2 Devices; Standard Deviation Values Are Given in Parentheses

	value	
parameter	Al_2O_3	HfO_2
forward μ_p (cm^2/(V s))	0.8 (0.9)	0.3 (0.4)
forward V_T (V)	−1.3 (5.6)	−4.5 (4.0)
p-channel $(L/W) \cdot I_{D,max}$ (nA)	17.4 (17.7)	7.8 (7.8)
ΔV_H (V)	9.7 (2.8)	10.4 (4.2)

and vacuum conditions which are consistent with those typically observed with SWCNT-TFTs having SiO_2 gate dielectrics; in particular, hysteresis in these devices persists even after extended desorption and heating in vacuum (see Supporting Information). A total of 156 devices are tested—78 Al_2O_3 and 78 HfO_2. The large sample size is taken to reduce the effects of irregularities in SWCNT deposition density and bundling, both of which are proposed to contribute to widely varying transfer characteristics,[8] and are likely the source of the large standard deviation in the summary of mean electrical parameters listed in Table 1. Though not strictly statistically significant, the mean values reported in Table 1 are appropriate for highlighting a number of qualitative differences observed between Al_2O_3 and HfO_2 devices. In particular, devices on Al_2O_3 have higher hole mobilites, threshold voltages, V_T, that are more consistent with theoretical values based on work function differences between SWCNTs and the p-type Si gate, 2× greater maximum drain current $I_{D,max}$, and a slightly lower hysteresis. These differences in performance parameters cannot be attributed to irregularities in depositing the SWCNT thin film on the different substrates, as both films are from the same solution/filter paper and were fabricated at the same time (see Methods). Moreover, AFM measurements indicate no qualitative difference in SWCNT thin films on the different substrates.

These differences are readily explained by the charge injection mechanism established in the previous section. In the following discussion, we progress through an *I*−*V* gate sweep for these devices and examine the band diagrams at key steps, the illustrations of which are provided with representative gate sweeps in Figure 6a.

(I) A typical gate sweep begins at high reverse bias, in our case at $V_{gs} = -15$ V. Observe that the dielectric bands have bent and the Fermi level of the SWCNTs has shifted to lower energy, favoring hole doping. The band bending results in a triangular potential barrier through which hole injection into the dielectric can occur. Upon sweeping V_{gs} in the positive direction, it is energetically favorable for holes injected during this step to remain fixed until V_{gs} is increased to a point where the slope of the band bending is reversed. The trapped holes screen the applied reverse gate bias, resulting in a less negative effective bias experienced by the SWCNTs, and therefore, lower channel charge density and conductance. EFM results indicate a lower level of hole injection in Al_2O_3 than in HfO_2, as illustrated in schematics 1 and 2 of Figure 6b. The exemplary electrical results shown in Figure 6a are consistent with these results since the increased hole traps in HfO_2 result in a more negative V_T and lower conductance.

(II) As we approach the high forward bias end of the gate sweep, the conduction band diagram appears in an analogous state to the high reverse bias state and is illustrated in schematics 3 and 4 of Figure 6b. The bands have shifted so the SWCNTs are now electron doped and the biasing conditions now favor electron injection at the SWCNT/dielectric interface. EFM measurements indicate comparable levels of electrons injected in both Al_2O_3 and HfO_2. In addition, the holes that had been injected during step I may be released. Once injected, the trapped electrons screen the applied forward gate bias, resulting in a less positive effective bias experienced by the SWCNTs. As the reverse sweep begins, these electrons remain fixed until the polarity of V_{gs} is reversed.

(III) As we return to the high reverse bias end of the gate sweep, the band diagrams again favor hole injection. In addition to the injection of holes, previously injected electrons may be released.

Recall that fixed charge has the effect of shifting transfer characteristics toward forward or reverse bias, depending on the sign of the charge carriers. Thus, the holes injected in HfO_2 during step I dynamically shift the threshold voltage toward more negative gate bias, while the effect is reduced in Al_2O_3 due to its lower level of hole injection. This accounts for the observed difference in threshold voltage for the different gate dielectrics. Moreover, the electrons injected in both materials during step II will dynamically shift V_T toward higher forward bias during the reverse sweep. A comparable shift in V_T toward the right in the reverse sweeps and an unequal shift in V_T toward the left in the forward sweeps may in part explain the slightly larger hysteresis ($\Delta V_H = V_{T,r} - V_{T,f}$) for HfO_2 devices than for Al_2O_3. Maximum sheet conductance is directly proportional to the carrier concentration in the SWCNT and results from electrostatic doping by the gate electrode at high bias (reverse or forward, for p-type or n-type devices, respectively). The devices under study exhibit greater p-type conduction than n-type. As a result, the maximum drain currents occur at high reverse bias. Thus, the screening of the applied bias by the holes injected in HfO_2 devices result in a lower maximum drain current compared to devices having an Al_2O_3 substrate.

To examine the effect of charge injection on measured mobility, we consider the difference between increasing $|V_{gs}|$ ($V_{gs} = 0 \rightarrow \pm 15$) *versus* decreasing ($V_{gs} = \pm 15 \rightarrow 0$). In both the forward and reverse sweep, when $|V_{gs}|$ is increasing, charge is being released, and

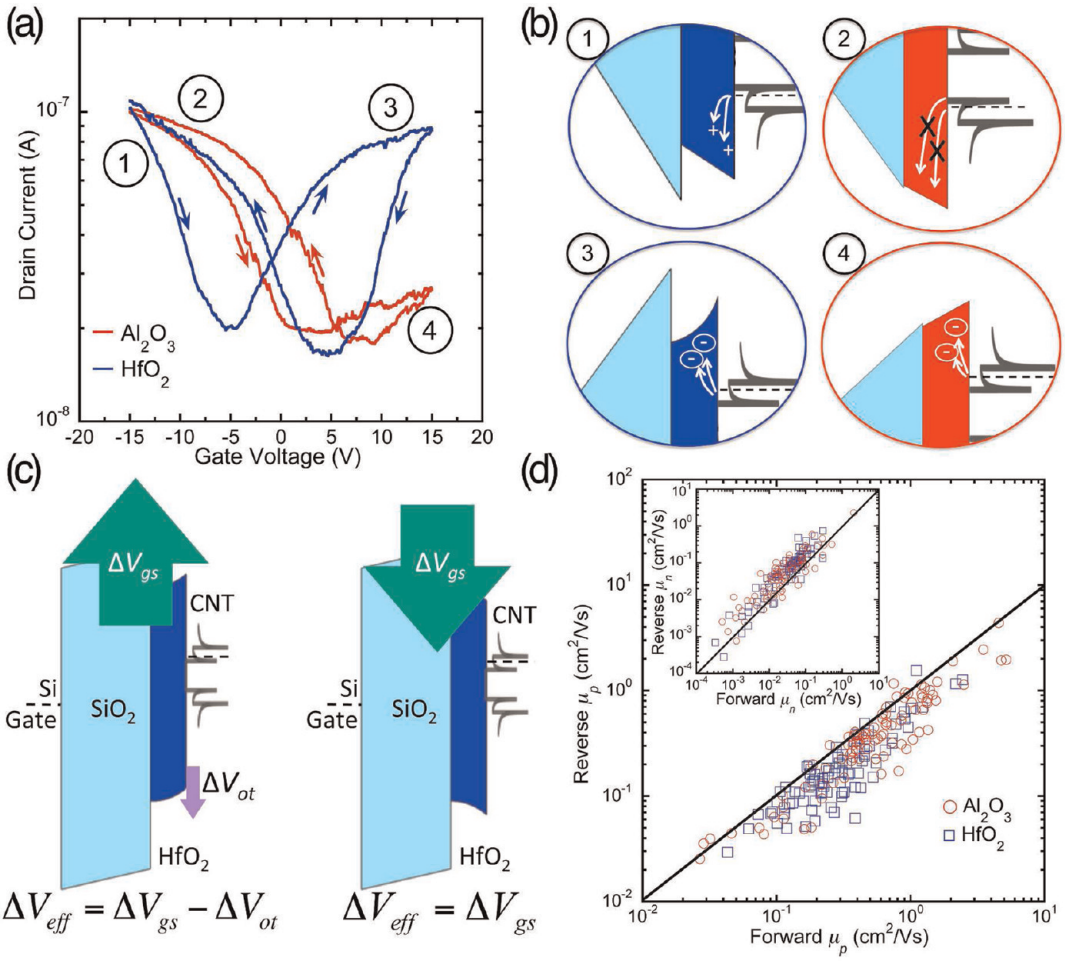

Figure 6. (a) Representative gate sweeps of an Al_2O_3 (red) device and a HfO_2 (blue) device; (b) diagrams of charge injection at high reverse and high forward bias corresponding to the numbered positions in panel a. Position 2 indicates a lack of hole injection into Al_2O_3. (c) Band diagrams of HfO_2 device when $|V_{gs}|$ is increasing (left) and when $|V_{gs}|$ is decreasing (right); nonzero ΔV_{ot} caused by dynamic screening by injected charges leads to reduced gate control when $|V_{gs}|$ is increasing. (d) Hole mobility in the reverse sweep versus the forward sweep for every device in the study with Al_2O_3 in red and HfO_2 in blue; position of data points below "equal mobility" line indicates higher hole mobility in forward sweep than reverse sweep, illustrating the effect shown in panel c; inset provides same plot for electrons, with opposite results.

the opposite charge carrier is being injected. The result of this dynamic charge screening is a reduced ability for the applied gate voltage to modulate the charge carrier concentration in the SWCNT channel. In contrast, when $|V_{gs}|$ is decreasing, the injected charges are fixed and no loss of gate control occurs. A comparison of these processes is included in Figure 6c, where ΔV_{eff} is the effective change in gate bias and ΔV_{ot} is the fraction of the ΔV_{gs} dropped across the dielectric layer resulting from oxide trapped charges injected during the sweep. The loss of gate control with increasing $|V_{gs}|$ causes a reduction in the measured mobility of holes in the reverse sweep compared to the forward sweep, while the opposite is true for electrons. In Figure 6d and its inset, these values are plotted against each other for every device in the study. For either charge carrier, if the mobilities were the same in both the forward and reverse direction, the markers would fall on the "equal mobility" line, where $y = x$. Instead, we find that nearly every device in the study performs in a way that is consistent with the dynamic charge injection mechanism. We must note that dynamic charge screening is time dependent and differences in forward and reverse mobilities are likely to depend on sweep rate. If measurements could be performed sufficiently fast to eliminate all charge injection, or sufficiently slow to allow for charge equilibration at every gate bias level, the difference in mobility between forward and reverse sweeps is expected to vanish. This time-dependence associated with the charge injection mechanism is consistent with recent studies of SWCNTs-TFTs with SiO_2 gate dielectrics that illustrate a sweep-rate dependent hysteresis[22] and use ambipolar pulsed gating techniques to eliminate hysteresis entirely.[31]

DISCUSSION

The preceding sections have established a correlation between the charge injection at the SWCNT/dielectric interface and illustrated its effect on $I-V$ transfer characteristics. Presently, we discuss the mechanisms that give rise to the observed disparities in injected

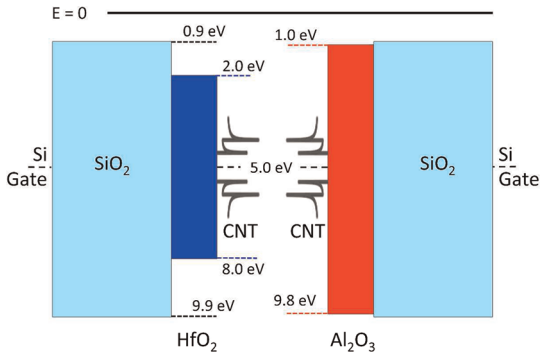

Figure 7. Band alignment for HfO_2 devices (left) and Al_2O_3 devices (right); height of potential barriers in high-κ layer strongly affect charge injection.

charge in the different dielectric materials. We examine the devices' approximate equilibrium band alignment taken at one point along the channel, penetrating through the dielectric layer from gate to the SWCNT (Figure 7). Specifically, we note the differences in electron affinity (1.0 eV for Al_2O_3, 2.0 eV for HfO_2) and ionization potential (9.8 eV for Al_2O_3, 8.0 for HfO_2)[29,32] for the two dielectric materials, and the resulting conduction and valence band offsets relative to the SWCNT. The conduction band offsets are similar for both high-κ dielectrics (*ca.* 2.75−3.75 eV). In contrast, the valence band offset is considerably larger (~4.75 V) for Al_2O_3 than it is for HfO_2 (~2.75 V). From this data we approximate the *relative* Fowler−Nordheim tunneling currents that lead to electron and hole charge injection in the two high-κ dielectric materials under bias. The tunneling current density is given by[33]

$$J_{FN} \propto \varepsilon^2 \exp\left(-B\sqrt{m^*}\frac{\phi^{3/2}}{\varepsilon} \right) \quad (7)$$

where A and B are constants, ε is the magnitude of the electric field at the SWCNT surface, m^* is the effective mass of the charge carrier in the dielectric material, and ϕ is the electric potential barrier height. The electric field term ε is given by[17]

$$\varepsilon = \frac{V_{gs}}{\kappa R_{CNT} \ln\left(\frac{t_{ox}}{R_{CNT}}\right)} \quad (8)$$

and is nearly equal for the two dielectric materials because the overall capacitance of the SiO_2/high-κ stack is dominated by the capacitance of the thick SiO_2. Therefore, differences in tunneling current are believed to be a result of differences in m^* and ϕ for the different charge carriers and different dielectric materials. Nominal values for the barrier heights are readily available from the band structure but there is ambiguity in the literature regarding m^* for holes and electrons in Al_2O_3 and HfO_2. Holes in Al_2O_3 and both charge carriers in HfO_2 exhibit a strong dependence on the crystalline phase of the material and a physical anisotropy based on the direction of migration through a crystalline unit cell.[34] In light of these limitations, inserting nominal values for the hole and electron effective masses into eq 8 does indeed produce relative theoretical values for the tunneling current density that are consistent with our EFM results. Specifically, these calculations predict far smaller injection of holes into Al_2O_3 than in HfO_2, which are the primary cause of the disparity in transfer characteristics in devices having the two different substrates.

The Fowler−Nordheim tunneling current is related to the probability of carriers tunneling through the entire triangular barrier, a process that would not directly lead to the population of trapped charges. If instead, we consider the tunneling probability through a triangular barrier into shallow levels near the conduction or valence band, the analysis remains essentially the same with a few minor differences. The effective tunneling length reduces and the tunneling probability becomes more resonant-like having the highest probability for energies near the trap level, yet accounting for these differences does not change the critical result that predicts lower hole injection rates in Al_2O_3. As we alluded to previously, once the states are populated and bias is removed, the bands will flatten making it more difficult for these trapped charges to be emitted. Frenkel−Poole emission is likely the dominant mechanism for their subsequent transport out of the layer; application of an opposite polarity bias lowers the thermal emission barrier and thus increases the rate of this process.[30] While the definition of an interface and the physical origin of interface states is still largely ambiguous for 1-dimensional nanostructures,[35] the charge injection mechanism we discuss here is phenomenologically similar to charge trapping by interface states distributed throughout the gap of the high-κ dielectric. Large forward or reverse bias allows for a greater range (in energy) of interface state filling, which subsequently relax when the bias is removed. Application of an opposite polarity bias would speed-up this relaxation process and could lead to the depopulation of interface states shifting the threshold voltage in opposite direction beyond the initial shift consistent with our results. Depending on the distribution of energies and their trapping tendencies, donating or accepting, a high density of interfaces states can potentially lead to Fermi level pinning in the SWCNT. We propose this as a possible mechanism that suppresses the electron concentration and subsequently the electron conduction in the $I-V$ transfer characteristics of SWCNT-TFTs on Al_2O_3 even at high forward bias.

The difference between bulk high-κ dielectric trap states and interface states is subtle, the latter having faster decay dynamics and displaying a stronger gate dependence, while the former has a greater dependence on biasing time and more persistent effects. Ultimately, we expect both mechanisms to

contribute to hysteresis in SWCNT-TFTs, and mitigation of these effects requires a means by which charge transfer between the SWCNT and high-κ dielectric is blocked. Our results, consistent with typical Si MOSFETs, point to increased barrier heights as a means to mitigate charge injection. Marked hysteresis reduction has been observed in SWCNT and graphene transistors with passivated (*via* hexamethyldisilazane or parylene) SiO_2 gate oxides.[15,16,36−38] In addition to increased hydrophobicity, these coatings increase the effective tunneling distance into the oxides and may also reduce the concentration of surface states thereby mitigating the effects of Fermi level pinning. Ultimately, a dielectric material with a high injection barrier, high dielectric constant, and very low density of surface (interface) states is necessary to overcome the hysteresis challenge in SWCNT-TFTs.

CONCLUSIONS

The injection of charge at the SWCNT/dielectric interface in SWCNT-TFTs having Al_2O_3 and HfO_2 gate dielectrics has been observed and correlated to $I-V$ transfer characteristics. Electric field gradient microscopy (EFM) was used to image and quantify the charge injected at the SWCNT/dielectric interface. It was found that high reverse bias yielded injected holes, while high forward bias yielded injected electrons. Moreover, the relative magnitudes of the injected charges as a function of time reveal significantly fewer holes injected in Al_2O_3 than in HfO_2. Transfer characteristics for these devices were found to vary dramatically in correlation with the relative levels of charges injected in the different dielectric materials. An analysis of the expected tunneling current density reveals theoretical values for the relative amounts of injected charge that agree with observation. This work emphasizes the need to carefully consider the SWCNT/dielectric interface of a SWCNT thin-film transistor. Specially engineered dielectric materials may mitigate charge injection and the resulting deleterious effects on transfer characteristics.

METHODS

Gate dielectric substrates are 100 nm thermal SiO_2 on p-type Si having resistivity 1−10 ohm-cm. Al_2O_3 is deposited *via* plasma ALD at 300 °C and HfO_2 is deposited *via* plasma ALD at 250 °C. RTA is conducted at 1000 °C under N_2 for 1 min. Film thickness is measured before and after ALD using an n&k analyzer by n&k Technology, Inc. For C−V measurements, metal circles (5 nm Ti, 50 nm Au) are deposited *via* shadow mask on a control sample. We prepare SWCNT-TFTs following a previously reported procedure with slight modification.[39,40] In short, 98% pure semiconducting SWCNT samples are purchased from NanoIntegris. An appropriate amount of SWCNTs are horn sonicated (at 0 °C) in a 1% w/v SDS stock solution to form a 100 μg/mL suspension, which is subsequently centrifuged and diluted with the stock solution 2× to form a 1 μg/mL suspension. From this suspension, 250 μL is vacuum filtered through a mixed cellulose esters filter paper (pore size 0.2 μm) over an area of 1.77 cm^2. To ensure the same thin film on both substrates, the filter is cut in half and each half is transferred onto a separate substrate. The filter papers are pressed, SWCNT side down, on the substrate of choice and dissolved in a heated acetone bath, thrice refreshed, followed by a methanol bath and dried with flowing N_2. The samples are annealed in air overnight at 300 °C and rinsed with acetone/isopropyl alcohol to remove nonvolatilized carbonaceous impurities. Metal contacts are patterned photolithographically and deposited in a stack of 5 nm Ti, 50 nm Au. Device channels are patterned photolithographically and devices are isolated *via* O_2 reactive ion etch.

Electrical measurements are performed under vacuum ($<10^{-5}$ Torr) using a Keithley 4200-SCS semiconductor parametric analyzer. Prior to measurement, devices are heated under vacuum at 325 K for at least 12 h to aid in removing pre-existing adsorbates. $I-V$ gate sweeps were performed with constant V_{ds} = 0.1 V. EFM measurements are performed on a Digital Instruments NanoScope IIIa atomic force microscope. AFM tips are NSG10, reflective side Au-coated conductive silicon tips from NT-MDT. Tips have a nominal radius of curvature of 6 nm (maximum 10 nm), spring constant 11.8 N/m and resonant frequency 240 kHz. Quality factor $Q = f_0/\Delta f$ ranges from 300 to 450 for the various tips used in the study. V_{gs} is applied under flowing dry N_2 at a rate of 2 scfh air.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Derivation of eq 3; discussion regarding physical applicability of EFM model; capacitance−voltage plots of atomic-layer deposited high-κ material; current−voltage plot illustrating effect of vacuum on electrical measurements. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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