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Letter

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Integrated Circuits Based on Bilayer MoS_2 Transistors

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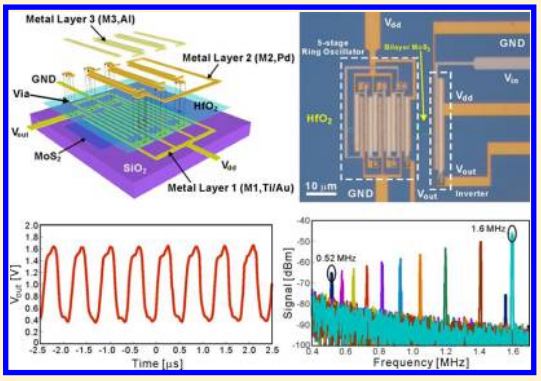
Supporting Information

ABSTRACT: Two-dimensional (2D) materials, such as molybdenum disulfide (MoS_2), have been shown to exhibit excellent electrical and optical properties. The semiconducting nature of MoS_2 allows it to overcome the shortcomings of zero-bandgap graphene, while still sharing many of graphene's advantages for electronic and optoelectronic applications. Discrete electronic and optoelectronic components, such as field-effect transistors, sensors, and photodetectors made from few-layer MoS_2 show promising performance as potential substitute of Si in conventional electronics and of organic and amorphous Si semiconductors in ubiquitous systems and display applications. An important next step is the fabrication of fully integrated multistage circuits and logic building blocks on MoS_2 to demonstrate its capability for complex digital logic and high-frequency ac applications. This paper demonstrates an inverter, a NAND gate, a static random access memory, and a five-stage ring oscillator based on a direct-coupled transistor logic technology. The circuits comprise between 2 to 12 transistors seamlessly integrated side-by-side on a single sheet of bilayer MoS_2. Both enhancement-mode and depletion-mode transistors were fabricated thanks to the use of gate metals with different work functions.



KEYWORDS: *Molybdenum disulfide (MoS_2), transition metal dichalcogenides (TMD), two-dimensional (2D) electronics, integrated circuits, ring oscillator*

Two-dimensional (2D) materials, such as molybdenum disulfide (MoS_2)[1] and other members of the transition metal dichalcogenides family, represents the ultimate scaling of material dimension in the vertical direction. Nanoelectronic devices built on 2D materials offer many benefits for further miniaturization beyond Moore's Law[2,3] and as a high-mobility option in the emerging field of large-area and low-cost electronics that is currently dominated by low-mobility amorphous silicon[4] and organic semiconductors.[5,6] MoS_2, a 2D semiconductor material, is also attractive as a potential complement to graphene[7−9] for constructing digital circuits on flexible and transparent substrates, while its 1.8 eV bandgap[10,11] is advantageous over silicon for suppressing the source-to-drain tunneling at the scaling limit of transistors.[12] Recently, various basic electronic components have been demonstrated based on few-layer MoS_2, such as field-effect transistors (FETs),[13−15] sensors,[16] and phototransistors.[17] However, until now only primitive circuits involving one or two discrete MoS_2 transistors connected through external wiring have been reported.[18] These devices also have mismatched input and output logic levels, making them unsuitable for cascading multiple logic stages. This paper addresses the next challenge in the development of 2D nanoelectronics and optoelectronics on MoS_2, that is the construction of fully integrated multistage logic circuits based on this material to demonstrate its capability for complex digital logic. These circuits were fabricated entirely on the same chip for the first time thanks to the seamless integration of both depletion-mode (D-mode) and enhancement-mode (E-mode) MoS_2 transistors. The transistors show multiple state-of-the-art characteristics, such as current saturation, high on/off ratio ($>10^7$), and record on-state current density (>23 μA/μm). This demonstration of integrated logic gates, memory elements, and a ring oscillator operating at 1.6 MHz represents an important step toward developing 2D electronics for both conventional and ubiquitous applications, offering materials that can combine silicon-like performance with the mechanical flexibility and integration versatility of organic semiconductors.

Molybdenum disulfide (MoS_2) is a layered semiconductor from the transition metal dichalcogenides material family (TMD), MX_2 (M = Mo, W; X = S, Se, Te).[10,11,19,20] A single molecular layer of MoS_2 consists of a layer of Mo atoms sandwiched between two layers of sulfur atoms by covalent

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bonds.[10] The strong intralayer covalent bonds confer MoS_2 crystals excellent mechanical strength, thermal stability up to 1090 °C in inert environment,[21] and a surface free of dangling bonds. On the other hand, the weak interlayer Van der Waal's force allows single- or few-layer MoS_2 thin films to be created through micromechanical cleavage technique[22] and through anisotropic 2D growth by chemical vapor deposition.[23,24] This unique property of MoS_2, and 2D materials in general, enables the creation of atomically smooth material sheets and the precise control on its number of molecular layers. Field-effect transistors (FETs) built on the ultrathin few-layer 2D crystals, hence, are effectively the optimal form of ultrathin body FETs,[25] a transistor structure ideal for suppressing the short-channel effects at its scaling limit. This benefit of 2D FETs has been demonstrated in ref 14 that shows a high on/off current ratio of 10^8 in a single-layer MoS_2 FET.

The planar nature and mechanical flexibility of 2D materials also make them excellent candidates for fabricating lightweight and rollable or foldable electronic systems on common commodities like paper, plastics, and textiles, as well as for constructing low-cost driving circuits for flat-panel display applications.[26] The incumbent technology for such applications is based on amorphous Si and polycrystalline Si, with organic semiconductors being the other potential option. Thin film transistors based on amorphous Si, for example, often have mobility below 1 $cm^2\ V^{-1}\ s^{-1}$, the on−off ratio in excess of 10^6, and the device switches from on to off within about 5−8 V, making it barely fit within the requirements of display applications.[4] The organic semiconductors offer ease of fabrication but exhibit similar or even lower mobility than amorphous Si due to its intrinsically disordered nature and quantum-mechanical-tunneling based transport.[27] In contrast, the covalently bonded, highly ordered crystalline 2D materials have carrier mobility that is orders of magnitude higher than in amorphous Si and organic semiconductors. 2D materials are thus promising for improving the performance and enable new functionality of ubiquitous electronics and display technology, such as flexible radio frequency identification tags and enhanced integration of drivers and logic circuits into display backplanes.

In this Letter, we address the next key challenge in the development of 2D nanoelectronics by demonstrating the first fully integrated multistage circuits entirely assembled on few-layer MoS_2. These circuits are based on the development of a direct-coupled FET logic (DCFL)[28] in this material system for which both enhancement-mode and depletion-mode devices with excellent pinch-off and current saturation are necessary. All the circuits were fabricated on bilayer MoS_2 obtained from micromechanical cleavage. Bilayer MoS_2 offers an excellent trade-off between the off-state and on-state current levels (see Supporting Information). The number of MoS_2 layers can be confirmed by atomic force microscopy (AFM) (Figure 1A) based on its thickness and by Raman spectroscopy based on the peak spacing between the E_{2g} mode and the A_{1g} mode,[29] respectively (Figure 1B and Supporting Information Figure S1). The lateral size of the exfoliated bilayer MoS_2 thin films, which are 13 Å thick, can reach up to 40 μm (Inset of Figure 1A).

The DCFL technology is a popular architecture for constructing high-speed circuit with low power dissipation, where an excellent trade-off between speed and power loss may be achieved[30,31] and is suitable for application in low-power flexible electronics. The DCFL circuits used in this Letter integrates both negative (D-mode) and positive (E-mode) threshold voltage transistors on the same chip (Figure 2A,B).

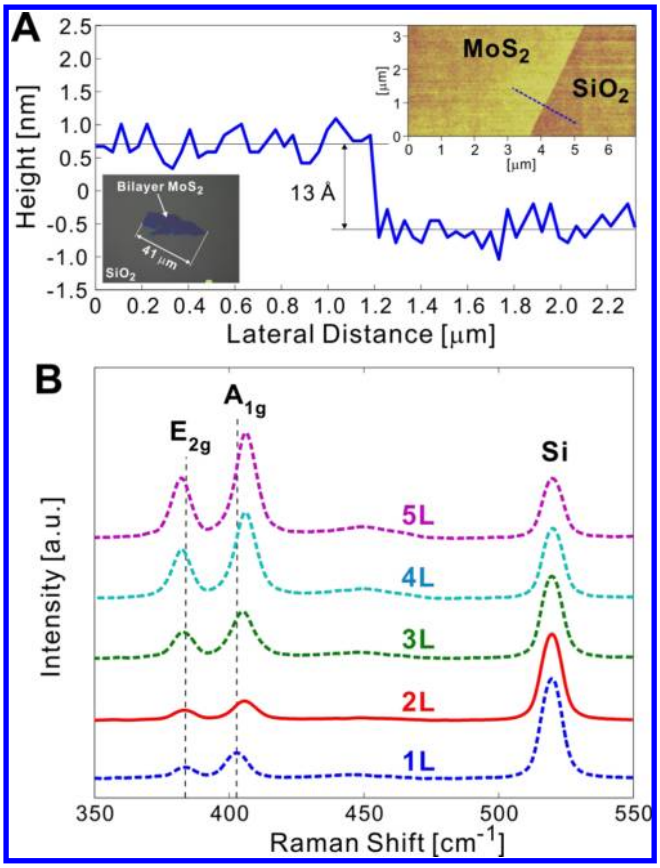

Figure 1. Optical micrograph, AFM and Raman spectroscopy of bilayer MoS_2. (A) Optical micrograph and AFM data of a bilayer MoS_2 thin film. The flake is 13 Å thick, which is equal to twice the thickness of single-layer MoS_2, confirming the flake being bilayer. (B) The number of layers in the MoS_2 thin film can also be confirmed from its Raman spectroscopy based on the peak spacing between the E_{2g} mode and the A_{1g} mode.[29] The red shift of E_{2g} peak and blue shift of A_{1g} peak lead to increasing peak spacing between E_{2g} and A_{1g} modes as the number of layers in the MoS_2 thin film increases.

This can be achieved through engineering the gate metal work functions of the MoS_2 FETs (see Supporting Information). Figure 2C,D shows the device characteristics of two MoS_2 FETs with Al (w_M = 4.08 eV) and Pd (w_M = 5.12−5.60 eV)[32] gates, respectively, fabricated side-by-side on the same bilayer MoS_2 thin film (see Supporting Information for fabrication). The difference in the work functions of these two metals effectively shifts the threshold voltages of the MoS_2 FET characteristics by about 0.76 V to form a D/E-FET pair (Figure 2C,D). The shift in the threshold voltage is lower than the metal work function difference in vacuum (~1.04 eV) (see Supporting Information).

Both the *D*-mode and *E*-mode FETs have a high on/off current ratio in excess of 10^7 (Figure 2D), which is very close to that in single-layer MoS_2 FETs.[14] On the other hand, at the on-state these devices based on bilayer MoS_2 have much higher on-state current density (exceeding 23 $\mu A/\mu m$ at V_{ds} = 1.0 V and V_{tg} = 2.0 V for the depletion mode FET, Figure 2C) than that reported for single-layer MoS_2 FETs.[14,18] The corresponding maximum transconductance of the bilayer FETs exceeds 12 $\mu S/\mu m$ at V_{ds} = 1.0 V. These bilayer MoS_2 FETs can hence offer superior on-state performance than single-layer devices with only a small degradation in terms of on/off current ratio. The high-field transport of both FETs shows saturation behavior

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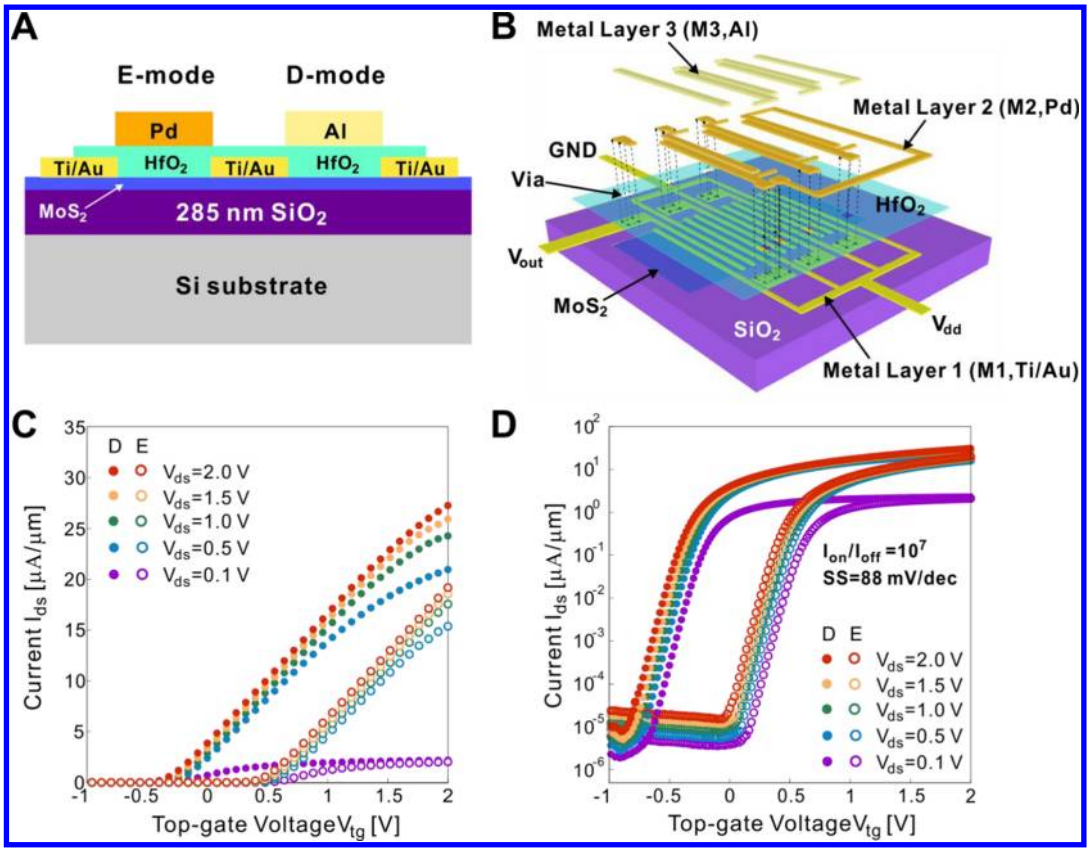

Figure 2. (A) Schematic representation of an E-mode and a D-mode device. (B) Schematic illustration of an integrated five-stage ring oscillator circuit on MoS_2 thin films, which is constructed by integrating 12 MoS_2 FETs. Three distinct metal layers of the MoS_2 IC are represented by M1, M2, and M3. M1 is directly in contact with the bilayer MoS_2 thin film while M2 and M3 are the Pd and Al gate layers, respectively. Via holes are etched through the HfO_2 dielectric layer to allow connections from M2 and M3 to M1. The fabricated ring oscillator circuit corresponding to the design above is shown in Figure 5. The general aspects of the fabrication process apply to all the devices and logic circuits presented in this Letter. (C) The transfer characteristics of depletion (*D*) mode and enhancement (*E*) mode bilayer MoS_2 FETs. The depletion mode FET has Al as the gate metal while the enhancement FET has Pd as the gate metal. The on-state current and transconductance of a device are its key dc performance metrics, critical for circuit application. In these bilayer MoS_2 FETs, the on-state current density exceeds 23 μA/μm at V_{ds} = 1 V and the transconductance is above 12 μS/μm, both being the highest values reported for MoS_2 FETs so far. The difference between the work functions of Al and Pd (~1.04 V in vacuum) gates results in a 0.76 V shift in the threshold voltage. The discrepancy between the work function difference in vacuum and in HfO_2 can be attributed to the dipoles at the metal/HfO_2 interface, resulting from charge transfer across this boundary.[38] (D) The transfer characteristics in logarithmic scale of *D*-mode and *E*-mode bilayer MoS_2 FETs. The I_{on}/I_{off} ratio exceeds 10^7 for V_{ds} above 0.5 V and is about 10^6 at V_{ds} = 0.1 V. The subthreshold slope (SS) is 88 mV/dec. Device dimension: L_g = 1 μm and L_{ds} = 1 μm. The substrate is grounded.

(Figure 3A), a critical feature for both logic and analog circuits, for the first time in top-gate MoS_2 FETs. The excellent match between the on-set of saturation and the gate overdrive (i.e., $V_{sat} = V_{tg} - V_t$, where V_{sat} is the saturation voltage and V_t is the threshold voltage of the FETs) indicates that the current saturation is due to the classic channel pinch-off mechanism, as is typical for long channel MOSFETs.[33] The field-effect mobility at V_{ds} = 1 V is extracted to be 10−15 $cm^2\ V^{-1}\ s^{-1}$ before depositing the halfnium oxide (HfO_2). After the MoS_2 thin film was passivated by a 20 nm thick HfO_2 layer, a conservative estimate based on back-gated characteristics shows a field effect mobility exceeding 300 $cm^2\ V^{-1}\ s^{-1}$ (see Supporting Information).

Using the technology described above, we built four different integrated logic circuits entirely assembled on bilayer MoS_2: a logic inverter, a NAND gate, a static random access memory (SRAM) cell, and a five-stage ring oscillator, all constructed with DCFL technology.[28] For each of the four logic circuits, all active and passive elements are integrated on the same piece of bilayer MoS_2. It is found that a supply voltage of V_{dd} = 2 V is suitable for operating the fabricated circuits. Hence, in this Letter a voltage level close to 2 V represents the logic state 1 while a voltage level close to 0 V represents the logic state 0.

An inverter circuit is a basic logic element that outputs a voltage representing the opposite logic-level to its input. Our inverter was constructed from an enhancement-mode MoS_2 transistor, and a depletion-mode resistor that was formed by connecting the gate of a depletion-mode transistor directly to its source electrode (Figures 3B inset and 5A). The quality of a logic inverter is often evaluated using its voltage transfer curve (Figure 3B), which is a plot of input versus output voltage. When the input voltage is V_{in} = 2 V (logic state 1), the *E*-mode MoS_2 FET is much more conductive than the depletion-mode FET, setting the output voltage to below 0.2 V (logic state 0). When V_{in} is 0 V (logic state 0), the MoS_2 FET is nonconducting and the output is close to 2 V (logic state 1). The slope of the transition region in the middle provides a measure of the gain, or the quality of switching. In the circuit of Figure 3B, a voltage gain close to 5 is achieved. Figure 3B also shows the mirror reflection of the V_{in}−V_{out} characteristics, which highlights the robustness of the inverter toward noise for multistage operations. When multiple inverter stages are

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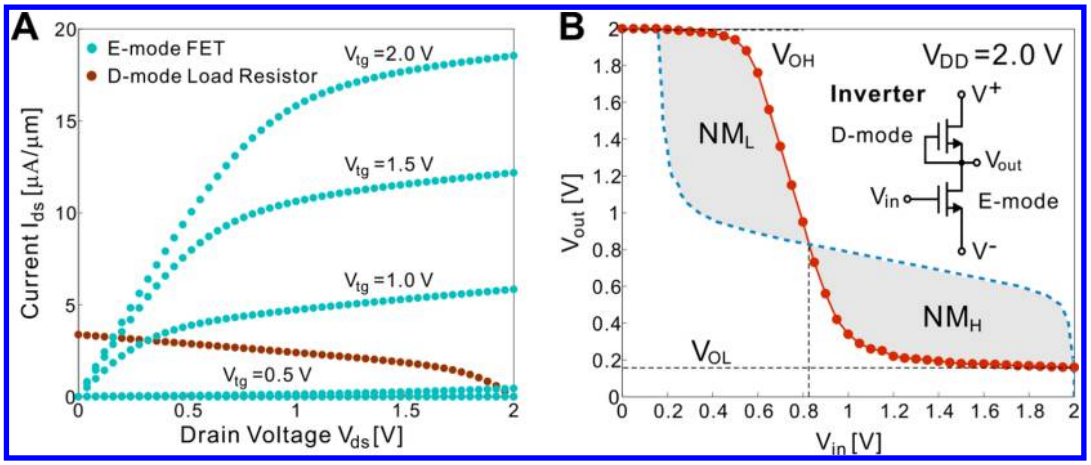

Figure 3. Demonstration of an integrated logic inverter on bilayer MoS_2. (A) Output characteristics (I_{ds}−V_{ds}) of the *E*-mode FET and *D*-mode load for the inverter shown in Figure 5A. L_g = 1 μm and L_{ds} = 1 μm. For the *E*-mode FET, in the linear regime at small source−drain voltages, the current is proportional to V_{ds}, indicating that the source and drain electrodes made of Ti/Au metal stack forms ohmic contact with MoS_2. The current saturates at higher drain bias ($V_{ds} > V_g - V_t$) due to the formation of depletion region on the drain side of the gate, as is typical of long channel MOSFETs. (B) Output voltage as a function of the input voltage, and its mirror reflection, for a bilayer MoS_2 logic inverter. The shaded area indicates its noise margins (NM_L and NM_H) for logic operation. The gain of the inverter is close to 5. (Inset) Schematic of the electronic circuit for a logic inverter.

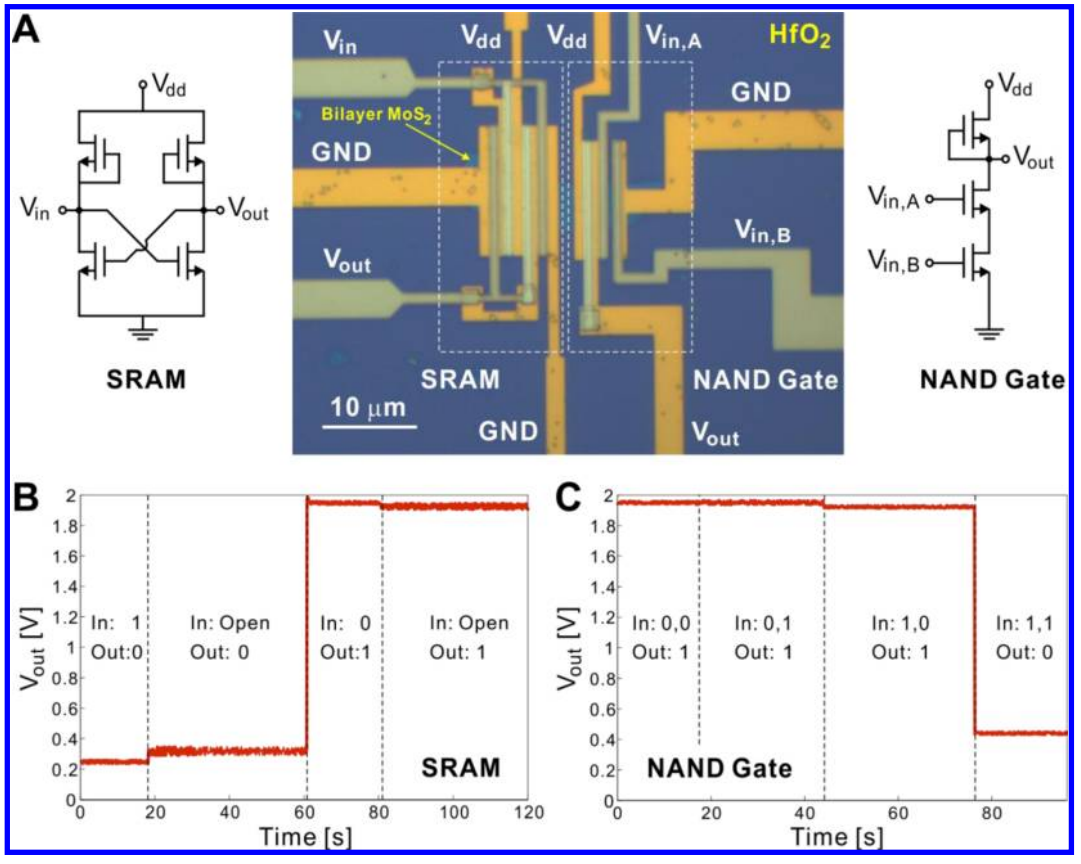

Figure 4. Demonstration of an integrated NAND logic gate and a static random-access memory (SRAM) cell on bilayer MoS_2. (A) Optical micrograph of the NAND gate and the SRAM fabricated on the same bilayer MoS_2 thin film. The corresponding schematics of the electronic circuits for the NAND gate and SRAM are also shown. (B) Output voltage of the flip-flop memory cell (SRAM). A logic state 1 (or 0) at the input voltage can set the output voltage to logic state 0 (or 1). In addition, the output logic state stays at 0 or 1 after the switch to the input has been opened. (C) Output voltage of the NAND gate for four different input states: (0,0), (0,1), (1,0), and (1,1). A low voltage below 0.5 V represents a logic state 0 and a voltage close to 2 V represents a logic state 1.

cascaded together, the output signal from the previous stage becomes the input signal to the next stage. Hence, the shaded area (NM_L and NM_H) represents the noise margin that can be tolerated by the inverter for multistage operations, which is particularly important for the demonstration of the ring oscillator.

The schematic design and the optical micrograph of an NAND gate circuit fabricated on a sheet of bilayer MoS_2 are

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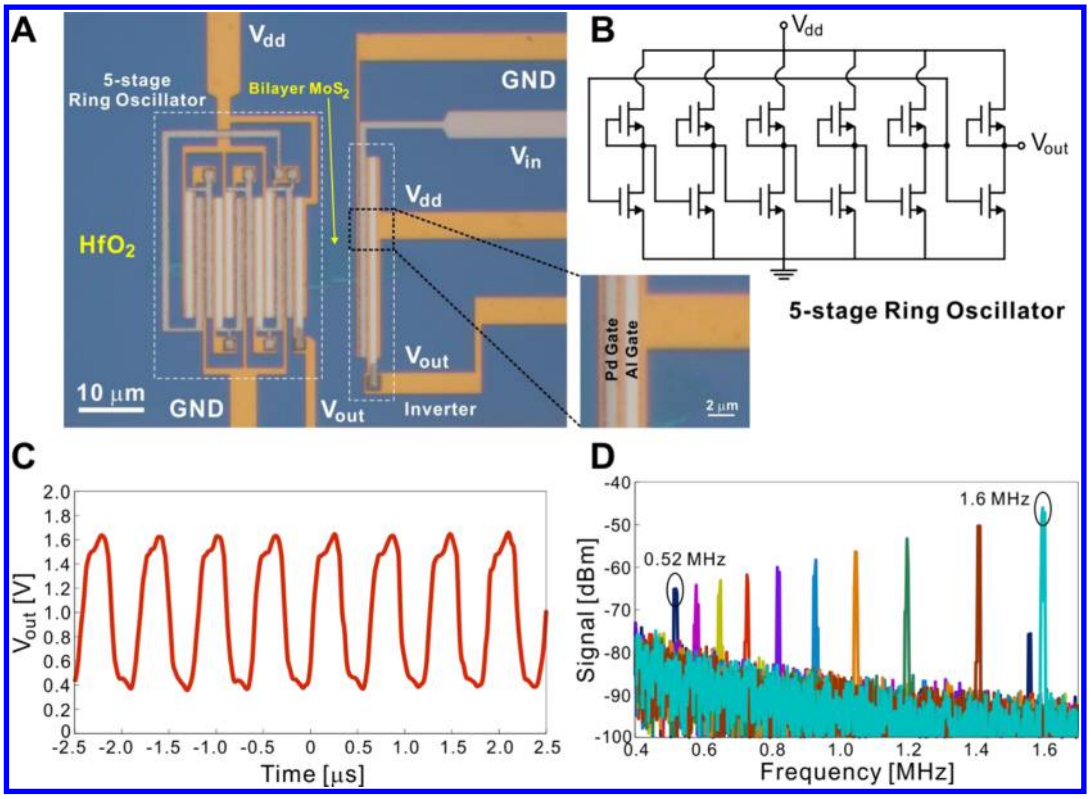

Figure 5. A five-stage ring oscillator based on bilayer MoS_2. (A) Optical micrograph of the ring oscillator constructed on a bilayer MoS_2 thin film. (B) Schematic of the electronic circuit of the five-stage ring oscillator. The first five inverter stages form the positive feedback loop, which leads to the oscillation in the circuit. The last inverter serves as the synthesis stage. (C) Output voltage as a function of time for the ring oscillator at V_{dd} = 2 V. The fundamental oscillation frequency is at 1.6 MHz. The corresponding propagation delay per stage is 62.5 ns. (D) The power spectrum of the output signal as a function of V_{dd}. From left to right, V_{dd} = 1.15 V and 1.2 to 2.0 V in step of 0.1 V. The corresponding fundamental oscillation frequency increases from 0.52 to 1.6 MHz.

shown in Figure 4A. The output of the circuit is close to 2 V (logic state 1) when either or both of the inputs are at logic state 0 (V_{in} <0.5 V). Under this state, at least one of the MoS_2 FETs is nonconducting and the output voltage is clamped to the supply voltage V_{dd}. The output is at logic state 0 only when both inputs are at logic state 1, so that both MoS_2 FETs are conducting. In Figure 4C, the output voltage is measured as a function of time while the two input voltage states vary across all four possible logic combinations (0,0), (0,1), (1,0), and (1,1). This data demonstrates the stable NAND gate functions of this two-transistor bilayer MoS_2 circuit. A NAND gate is one of the two basic logic gates (the other being NOR gate) with universal functionality. Any other type of logic gates (AND, OR, NOR, XOR, etc.) can then be constructed with a combination of NAND gates. Hence, this first demonstration of a NAND gate shows that it is possible to fabricate any kind of digital integrated circuit with MoS_2 thin film layers.

A flip-flop memory element (SRAM) has also been constructed from a pair of cross-coupled inverters (Figure 4A). This storage cell has two stable states at the output, which are denoted as 0 and 1. The flip-flop cell can be set to logic state 1 (or 0) by applying a low (or high) voltage to the input. To verify the functionality of this flip-flop cell, a voltage source is applied to the input to set V_{in} to 2 V at time T = 0 s. This drives V_{out} into logic state 0 (Figure 4B). Then at T = 20 s, the switch at V_{in} is opened and the output of the SRAM cell V_{out} remains at logic state 0. At time T = 60 s, we apply V_{in} = 0 V at the input to write a logic state 1 into V_{out}. As the switch is opened again at T = 80 s, the output of the SRAM cell remains in the logic state 1. This data demonstrates that the flip-flop SRAM circuit fabricated on the bilayer MoS_2 thin film indeed functions as a stable memory cell.

Finally, a five-stage ring oscillator was constructed to assess the high frequency switching capability of MoS_2 and for evaluating the material's ultimate compatibility with conventional circuit architecture[28,34−36] (Figure 5A). The ring oscillator, which integrates 12 bilayer MoS_2 FETs together, was realized by cascading five inverter stages in a close loop chain (Figure 5B). An extra inverter stage was used to synthesize the output signal by isolating the oscillator operation from the measurement setup to prevent the interference between them. The output of the circuit was connected to either an oscilloscope or a spectrum analyzer for evaluation. The voltage transfer curve of the test inverter circuit fabricated side-by-side on the same piece of bilayer MoS_2 thin film (Figures 3B and 5A) as the ring oscillator, shows that the gain in each inverter stage is close to 5. For robust ring oscillator performance, it is imperative to have stable operations in all five inverter stages throughout the oscillation cycles, and its tolerance toward noise can be determined from the noise margins for both low and high logic levels, that is, the shaded regions in Figure 3B. The positive feedback loop in the ring oscillator results in a statically unstable system, and the voltage at the output of each inverter stage oscillates as a function of time (Figure 5C). At V_{dd} = 2 V, the fundamental oscillation frequency is at 1.6 MHz, corresponding to a propagation delay of $\tau_{pd} = 1/(2nf)$ = 62.5 ns per stage, where n is the number of stages and f is the fundamental oscillation frequency. The

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frequency performance of this ring oscillator, while operating at a much lower $V_{dd,}$ is at least an order of magnitude better than the fastest integrated organic semiconductor ring oscillators.[35] It also rivals the speed of ring oscillators constructed from the printed ribbons of single-crystalline silicon reported in the literature.[37] The output voltage swing measured by the oscilloscope (input impedance 1 MΩ)) is about 1.2 V.

The output signal of the ring oscillator can also be measured in terms of its frequency power spectrum. Figure 5D shows the spectrum of the output signal from the ring oscillator as a function of the drain bias voltage V_{dd} (Figure 5D). The resonance frequency is at 0.52 MHz for V_{dd} = 1.15 V. The corresponding fundamental resonance frequency reaches 1.6 MHz as V_{dd} increases to 2 V. The improvement in frequency performance with increasing V_{dd} can be attributed to the enhancement in the current driving capability of the ring oscillator due to the rise in the drain current I_{ds} in each individual MoS_2 FET with increasing drain and gate voltages. The fundamental frequency of oscillation is currently limited by the parasitic capacitances in various parts of the circuit rather than the intrinsic performance of the MoS_2 devices (see Supporting Information). The signal peaks measured by the spectrum analyzer increases from −65 to −46 dBm as V_{dd} raises from 1.15 to 2 V. This is again a result of the I_{ds} dependence on V_{dd}.

To summarize, the realization of fully integrated multistage logic circuits based on few-layer MoS_2 DCFL represents the first demonstration of integrated multistage systems on any 2D materials, including graphene. It is an important step toward realizing 2D nanoelectronics for high-performance low-power applications. Further optimization is underway to increase operating speed and toward realizing complementary logic circuits to decrease the power dissipation. With the rapid progress in large-scale growth of MoS_2 by chemical vapor deposition,[23,24] these 2D crystals are extremely promising new materials for both conventional and ubiquitous electronics.

■ ASSOCIATED CONTENT

Supporting Information

Additional information and figures. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interests.

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