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Nanosheet thickness-modulated MoS_2 dielectric property evidenced by field-effect transistor performance†

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We report on the nanosheet-thickness effects on the performance of top-gate MoS_2 field-effect transistors (FETs), which is directly related to the MoS_2 dielectric constant. Our top-gate nanosheet FETs with 40 nm thin Al_2O_3 displayed at least an order of magnitude higher mobility than those of bottom-gate nanosheet FETs with 285 nm thick SiO_2, benefiting from the dielectric screening by high-*k* Al_2O_3. Among the top-gate devices, the single-layered FET demonstrated the highest mobility of ~170 $cm^2\ V^{-1}\ s^{-1}$ with 90 mV dec^{-1} as the smallest subthreshold swing (SS) but the double- and triple-layered FETs showed only ~25 and ~15 $cm^2\ V^{-1}\ s^{-1}$ respectively with the large SS of 0.5 and 1.1 V dec^{-1}. Such property degradation with MoS_2 thickness is attributed to its dielectric constant increase, which could rather reduce the benefits from the top-gate high-*k* dielectric.

Graphene and related two-dimensional (2D) nanosheet materials have been studied with much attention in view of their applications to future nanoelectronics.[1,2] These 2D materials have initially been prepared by the exfoliation method.[2,3] Graphene has its high carrier mobility (μ) over 100 000 $cm^2\ V^{-1}\ s^{-1}$ but also reveals intrinsic limitations caused by its rather small bandgap (E_g).[4–6] Even though significant efforts to open up the bandgap of graphene were made modifying its form into a nano-ribbon, the gap turned out to be only around 200 meV while the intrinsic mobility was seriously reduced to ~200 $cm^2\ V^{-1}\ s^{-1}$.[7,8] Very recently, molybdenum disulfide (MoS_2) layers appeared to overcome the dilemma of graphene as an alternative nanosheet material.[9–15] Although E_g of bulk MoS_2 is known to be ~1.2 eV of indirect type, a few angstrom-thin single-layered MoS_2 has recently been reported to exhibit a direct bandgap of 1.8 eV, a high mobility of 200–350 $cm^2\ V^{-1}\ s^{-1}$, and a high on/off current ratio of 10^6–10^8 along with a very low subthreshold swing (SS) when used as the channel of a top-gate transistor with thin high-*k* oxide, which provides dielectric engineering for mobility enhancement.[15–21] However, as the nanosheet thickness increases, the mobility appears to decrease and the detailed mechanisms for mobility change due to the MoS_2 thickness still remain unclear.[16] In the present work, we demonstrated top-gate field-effect transistors (FETs) with single- to triple-layered MoS_2 nanosheets adopting a 40 nm thin atomic layer deposited (ALD) Al_2O_3, and also clarified the nanosheet thickness-involved issues: mobility and SS changes. Our nanosheet FET with a single-layered MoS_2 channel exhibited a maximum mobility of 170 $cm^2\ V^{-1}\ s^{-1}$, which systematically decreases to 25 and 15 $cm^2\ V^{-1}\ s^{-1}$ with double- and triple-layered MoS_2 as respective channels.

Surface-cleaned 285 nm thick SiO_2/p^{++}-Si wafer was chosen as the substrate for our n-type MoS_2 nanosheet transistor with Au source/drain (S/D) electrodes, since 285 nm was reported as an optimal thickness to identify few-layered dichalcogenide.[22,23] Indeed, each exfoliated MoS_2 flake showed a distinctive optical contrast with thinner flakes exhibiting less optical density, which enabled fast screening of few layered-flakes under the optical microscope. Fig. 1(a) and (b) display a MoS_2 flake which was caught *via* photolithography to contact with patterned Au for S/D. Since the flake size was as long as ~10 μm, a 5 μm long channel was available for our device (W/L ratio was ~1). Fig. 1(c) illustrates a 3D scheme of our FET with a MoS_2 nanosheet and a 40 nm thin Al_2O_3 dielectric, which was obtained by atomic layer deposition (ALD) at 200 °C. Fig. 1(d) shows Raman spectra obtained from many nanosheets assigned to single- to 6-layered MoS_2 flakes spanning ~5 × 5 μm^2. As shown by the previous report,[24] the frequency difference between E_{2g}^1 and A_{1g}, the two prominent Raman-active modes of 2H-MoS_2 crystals, increases stepwise with the number of layers. The inter-peak separation or frequency difference for the thinnest flake in Fig. 1(d) was ~18.0 cm^{-1} which is in excellent agreement with that for single-layered MoS_2.[24] Our results are also consistent with theoretical calculations based on the density functional perturbation theory.[25] Confirming the layer number of exfoliated flakes by Raman spectra,

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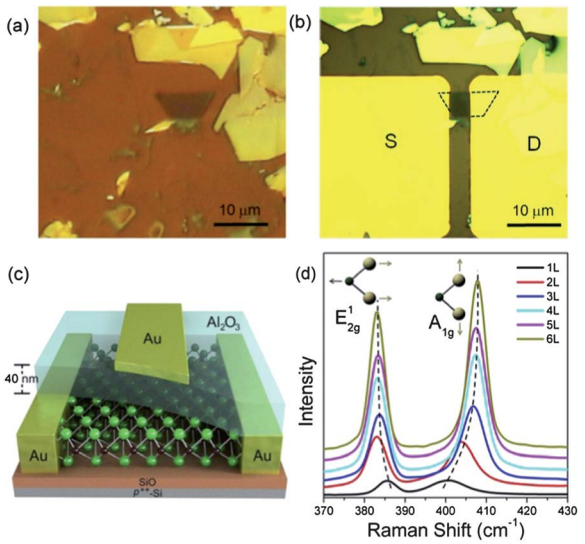

Fig. 1 Optical microscopy images of (a) a few-layered MoS_2 flake on 285 nm thick SiO_2 and (b) the flake contacted with Au for S/D electrodes. (c) Three-dimensional schematic view of a transistor with a single-layered MoS_2 nanosheet. (d) Raman spectra of 1–6 layered MoS_2 flakes, along with inset figures for two representative Raman-active modes, $E_{2g}{}^1$ and A_{1g}.

we selected single- to triple-layered MoS_2 as the channel for our nanosheet transistor. (The thickness of monolayer MoS_2 was measured by previous researchers to be ~0.65 nm.)[15]

Fig. 2(a) and (b) respectively show the drain current–gate voltage (I_D–V_G) transfer curves and linear mobility (μ_{lin}) plots of bottom-gate FETs with a 285 nm thick SiO_2 dielectric (Fig. 2(b), inset) with the three different MoS_2 nanosheet channels: single, double, and triple layered MoS_2. With the increase of the layer number, the drain current (I_D) and linear mobility (μ_{lin}) apparently decrease as shown in the figures. According to the mobility plots, the highest maximum mobility of the nanosheet FET was obtained from single layered MoS_2 to be ~13 $cm^2\,V^{-1}\,s^{-1}$ but the mobility appears to be only ~1 $cm^2\,V^{-1}\,s^{-1}$ with the triple layered MoS_2 channel, primarily because the inter-layer scattering of electrons reduces the mobility in the source-to-drain transport while such scattering would be subdued in the single-layered channel.[26] However, according to previous reports, these bottom-gate mobility results may not always be depending on the MoS_2 thickness but more sensitively depending on the density of local states between MoS_2 and SiO_2, even though one tries to fabricate the bottom-gate MoS_2 FETs using the same experimental conditions; so a broad range of linear mobility has been reported for bottom-gate MoS_2 FETs.[27–29] The μ_{lin} was estimated and plotted as a function of gate voltage (V_G), based on the following equations: $g_m(V_G) = dI_D/dV_G$ (transconductance) and $\mu_{lin} = (g_m/C_{ox}V_D) \times (L/W)$, where C_{ox} is the dielectric capacitance. Fig. 2(c) and (d) show that our single- to triple-layered MoS_2 channels have good ohmic contacts with Au S/D electrodes.

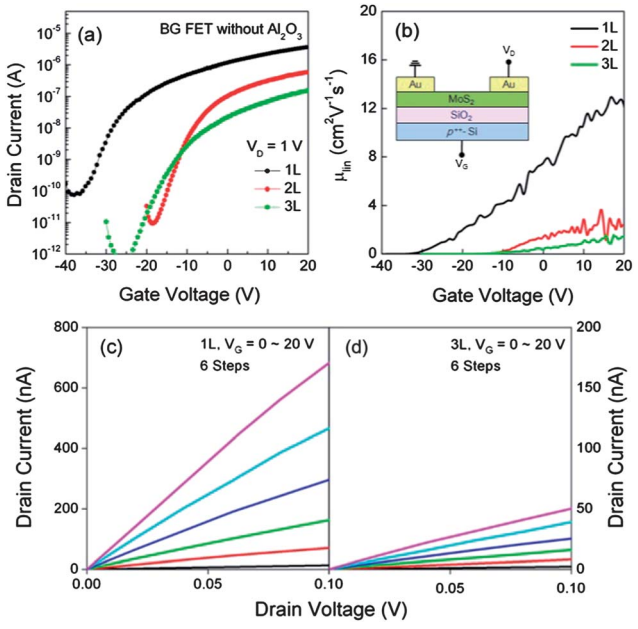

Fig. 2 (a) The transfer and (b) linear mobility curves of bottom gate-controlled FETs with 1, 2, and 3 layered MoS_2. The inset shows a 2D schematic of the devices. Output curves of bottom gate FETs of (c) single- and (d) triple-layered MoS_2 channel with Au S/D electrodes.

The linear mobility of the MoS_2 nanosheet FETs suddenly increases by at least an order of magnitude if equipped with our 40 nm thin Al_2O_3 top-gate dielectric (see the inset of Fig. 3(b) for the top-gate FET scheme). According to the transfer curves of Fig. 3(a), the top-gate controlled nanosheet FETs display 12, 5, and 1.5 μA of on-current I_D respectively with single, double, and triple layered MoS_2 under $V_D = 0.5$ V. The mobility plots in Fig. 3(b) display 170, 25, and 15 $cm^2\,V^{-1}\,s^{-1}$ as the respective maximum linear mobilities of single, double, and triple layered MoS_2 FETs. Such highly enhanced mobilities and I_D current, which are at least an order of magnitude higher than those of bottom-gate devices, can only be explained by dielectric screening effects from the high-k top-dielectric overlayer ($k \sim 7$ in ALD Al_2O_3).[21] The on/off I_D ratio was 5×10^5 to 10^6 for all cases. The high-k overlayer effects were again confirmed by bottom-gate controlled FETs with double layered MoS_2 as respectively shown in the transfer curves and mobility plots of Fig. 4(a) and (b). According to the transfer curves in Fig. 4(a), the bottom-gate FET with an Al_2O_3 overlayer displays apparently higher I_D by an order of magnitude than that of the other bottom-gate device without the top layer. The linear mobility of the bottom-gate controlled FET with the overlayer appeared almost similar to that of the top-gate control device to be 25–30 $cm^2\,V^{-1}\,s^{-1}$ (Fig. 4(b)), even though the SS values of top- and bottom-gate FETs are very different from each other.

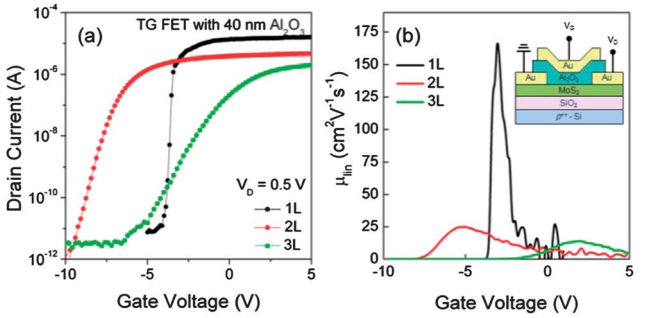

Fig. 3 (a) The transfer and (b) linear mobility curves of 1, 2, and 3 layered MoS_2 top gate FETs with a 40 nm thin Al_2O_3 dielectric. The inset shows the 2D schematic of our top gate devices.

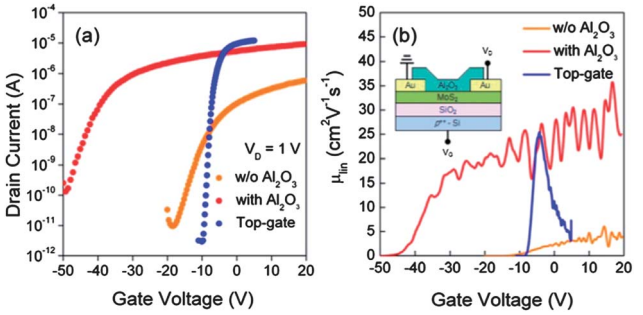

Fig. 4 (a) The transfer and (b) linear mobility curves of double-layered MoS_2 bottom gate FETs with and without Al_2O_3 overlayer as compared to the top gate FET with an Al_2O_3 dielectric. The inset shows the 2D schematic of this bottom gate FET with an Al_2O_3 overlayer.

As shown above, we could initially notice that the mobility of MoS_2 nanosheets is enhanced with the high-k overlayer due to the dielectric screening, whether the high-k overlayer plays as a gate dielectric or just an overlayer. Besides, the mobility of our FETs appears modulated and actually reduced with the MoS_2 nanosheet thickness whether the device is bottom-gate- or top-gate-controlled; it was primarily attributed to the thickness-induced (inter-layer) carrier scattering.[26] However, there exists another noticeable phenomenon which is also thickness-related: SS degradation with the nanosheet thickness. The thickness-induced SS degradation is particularly apparent with the top-gate MoS_2 FETs (Fig. 3(a)) and this should be properly explained along with the mobility reduction. According to a well-known theory, the SS value of FETs originates from an equation below:[30,31]

$$SS = (\ln 10)(kT/q)\left[1 + qx_{ox}\left(\sqrt{q^2\varepsilon_{ch}N_{bt}/kT} + qD_{it}\right)\Big/\varepsilon_{ox}\right], \quad (1)$$

where kT = 0.026 eV at room temperature, ε_{ch} and ε_{ox} are the respective dielectric constants of the channel semiconductor and oxide dielectric, x_{ox} is the dielectric oxide thickness, N_{bt} and D_{it} are respectively the near-interface-bulk trap density and the interface trap density-of-states (DOS) at the channel/dielectric interface trap as energy-independent average values; their units are cm^{-3} and cm^{-2} eV^{-1}, respectively. If we assume that the single-, double-, and triple-layered MoS_2–Al_2O_3 interfaces have almost the same and negligible interface trap DOS, D_{it}, above eqn (1) becomes mostly dependent on the following four factors: $\sqrt{\varepsilon_{ch}}$, $\sqrt{N_{bt}}$, x_{ox}, and ε_{ox}. (Since we prepared the different-layered MoS_2 flake samples in the same way, the process-contamination-induced D_{it} would be almost the same for all FETs.)

According to our Fig. 3(a), the SS of the top-gate FET with single-layered MoS_2 was as small as 90 mV dec^{-1} while the SS decreases with the layer thickness or layer number (0.5 and 1.1 V dec^{-1} for double and triple layers). It is very likely that ε_{ch} is closely related to the MoS_2 thickness as the band gap does; larger the MoS_2 thickness, so its ε_{ch} does become larger until the thickness reaches the bulk state. N_{bt} may also be dependent on the nanosheet thickness, possibly existing at the MoS_2 inter-layer locations. If ε_{ch} and N_{bt} are irrelevant to the MoS_2 thickness and rather identical for all the MoS_2 nanosheets, the SS must be almost the same, which is, however, not matched to our experimental results at all. Interestingly, very recent theoretical study supports the thickness-dependent ε_{ch} which increases with MoS_2 layer thickness.[25,32] According to the theoretical results, dielectric constants of MoS_2 increase with the nanosheet thickness, which is opposite to the band gap behavior.[16,20] Unless the surface roughness of the single-, double-, and triple MoS_2 layers or the trap densities at the three MoS_2–Al_2O_3 interfaces are much different from one another, the thickness-dependent change of the nanosheet dielectric constant would be the main contribution able to explain the SS degradation.

Intrigued with the thickness-induced ε_{ch} change, we have fabricated another set of top-gate nanosheet FETs with a high-k organic gate-dielectric, which used to be a 200 nm thick ferroelectric organic polymer [P(VDF-TrFE); $k \sim 7$], to observe the MoS_2 thickness-dependent SS changes. According to the transfer curves of ferroelectric memory FETs with MoS_2 nanosheets (ESI, Fig. S1†), the SS of the ferroelectric memory FET with single-layered MoS_2 again appears to be smallest along with the largest memory window while it degrades with the nanosheet thickness that causes memory window decrease.[33] Unlike the cases of top-gate FETs, our bottom-gate nanosheet FETs in Fig. 2(a) and (b) did hardly show clear signs of such SS difference for single-, double-, and triple-layered MoS_2 FETs. It is probably because their SS values are already too large to show visible SS differences in view of eqn (1), according to which large SS values for all FETs are expected from low-k gate oxide ($\varepsilon_{SiO_2} = 3.9\ \varepsilon_o$) thickness ($x_{ox}$ = 285 nm). In spite of the bottom-gate structure, a very small SS value is achievable if we use high-k thin oxide as a gate dielectric, since that approach again meets the conditions for a small SS in eqn (1).[27]

As a final point, it could be worthwhile to understand that the mobility decrease of our top-gate MoS_2 nanosheet FETs in Fig. 3(b) is closely related to the dielectric constant increase with the MoS_2 thickness. Although the inter-layer scattering is already expected to be a generally known source of mobility loss in a low dimension channel, the dielectric constant increase with 2D nanosheet thickness could be another impelling one. If the increased ε_{ch} competes with (high-k) ε_{ox}, the source-to-drain electric field could not be confined to the channel thickness, and as a result, the high mobility-enabling mechanism by top-gate high-k dielectric engineering possibly becomes invalidated. Hence, the channel mobility is so closely related to the thickness of the MoS_2 nanosheet in the two aspects: inter-layer scattering and degradation of dielectric engineering (or degradation of SS).

Conclusions

In summary, the nanosheet-thickness effects on the performance of MoS_2 FETs were studied. Our top-gate nanosheet FETs with 40 nm thin Al_2O_3 displayed at least an order of magnitude higher mobility and smaller SS than those of bottom-gate nanosheet FETs with 285 nm thick SiO_2, benefiting from the dielectric screening by high-k Al_2O_3. Among the top-gate devices, the single-layer FET demonstrated the highest mobility of ~170 cm^2 V^{-1} s^{-1} with 90 mV dec^{-1} as the smallest SS but the double- and triple-layered FETs showed only ~25 and ~15 cm^2 V^{-1} s^{-1} respectively with the large SS of 0.5 and 1.1 V dec^{-1}. Such property degradations with MoS_2 thickness are actually attributed to the dielectric constant increase. The most superior device performance would be expected from a top-gate

single layered MoS_2 FET with a high-k dielectric, and the double- and triple-layered FETs could be promising only under a very high-k top-gate dielectric, of which the constant is even higher than that of thick MoS_2.

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