AIP | Applied Physics Letters

Electronic properties of metal-semiconductor and metal-oxide-semiconductor structures composed of carbon nanotube film on silicon

Ashkan Behnam, Nischal Arkali Radhakrishna, Zhuangchun Wu, and Ant Ural

Citation: Applied Physics Letters **97**, 233105 (2010); doi: 10.1063/1.3524194
View online: http://dx.doi.org/10.1063/1.3524194
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/97/23?ver=pdfcov
Published by the AIP Publishing

Electronic properties of metal-semiconductor and metal-oxide-semiconductor structures composed of carbon nanotube film on silicon

Ashkan Behnam,[1,a)] Nischal Arkali Radhakrishna,[1] Zhuangchun Wu,[2,b)] and Ant Ural[1,a)]
[1]*Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida 32611, USA*
[2]*Department of Physics, University of Florida, Gainesville, Florida 32611, USA*

(Received 7 September 2010; accepted 9 November 2010; published online 7 December 2010)

We fabricate and experimentally characterize the electrical properties of metal-semiconductor (MS) and metal-oxide-semiconductor (MOS) structures where the metal is single-walled carbon nanotube (CNT) film and the semiconductor is a Si substrate. Our results suggest that for the MS devices thermionic emission is the main high-temperature current transport mechanism, while tunneling becomes the dominant mechanism for MOS devices with thermally grown thin oxide layers between the CNT film and Si. In addition, the CNT film workfunction, a key parameter for the performance of CNT film-based devices, is obtained from the capacitance-voltage measurements on the MOS structures. © *2010 American Institute of Physics*. [doi:10.1063/1.3524194]

Single-walled carbon nanotube (CNT) film is a transparent, conductive, and flexible material that exhibits uniform physical and electronic properties.[1] Due to these favorable properties, several promising device applications of these films have recently been demonstrated.[2–7] Specifically, CNT film can be used as a transparent and conductive electrode in optoelectronic and photovoltaic devices.[4–6] For these applications, the interface between the CNT film and its adjacent layer plays a significant role in the charge transport mechanisms. The focus of most of the research so far, however, has been more on the overall performance of the devices fabricated rather than on the properties of the junction between the CNT film and the active material.[4–6] In a few recent studies, the electrical properties of the interface between individual nanotubes and GaAs substrates[7,8] and that between vertical forest of nanotubes and Si substrates,[9] and metal-semiconductor-metal structures[5] have been investigated. However, a careful study of the electrical properties of the junction between CNT films and Si substrates as well as CNT film-SiO_2–Si structures has not been performed previously. Such metal-oxide-semiconductor (MOS) structures could have applications in electronic and optoelectronic devices.[10,11]

In this letter, we experimentally characterize the electronic properties of metal-semiconductor (MS) and MOS devices in which the CNT film acts as the metal and Si is the semiconductor. We demonstrate the rectifying behavior of the MS junctions on both *p*-type and *n*-type Si substrates at various temperatures, discuss the transport mechanisms, and extract important junction parameters. Then, by analyzing the MOS structures, we show that the presence of the oxide changes the dominant transport mechanism at room temperature. Our results encourage further work in order to develop process steps that would allow precise control and fine-tuning of the CNT film-Si interface properties.

Figure 1(a) shows an optical microscope image of a fabricated CNT film-Si MS structure. In order to fabricate the MS and MOS structures, first CNT films were prepared using vacuum filtration, as explained in detail before.[1,12] An atomic force microscope (AFM) image of an ~50 nm thick CNT film is shown in Fig. 1(b). Next, $\sim 10^{16}$ cm^{-3} doped *n*- and *p*-type Si substrates with thermally grown SiO_2 layers (~400 nm thickness) were cleaned [Fig. 1(c)] and windows were opened in the oxide layer by photolithography and HF wet etching [Fig. 1(d) and the circular area in Fig. 1(a)]. For MOS samples, a thin oxide layer (with a thickness of 5, 10, 15, and 20 nm) was then thermally grown on the exposed Si areas [Fig. 1(d2)], while for MS devices, no oxide growth was performed. Next, CNT films were deposited on both the MS and MOS samples [Fig. 1(d)] and then patterned by O_2 plasma etching[12] to form individual devices [Fig. 1(e) and the large square area in Fig. 1(a)]. Finally, Cr/Pd (10/90 nm) metallic rings were patterned on the films using photolithography, e-beam evaporation, and lift-off for electrical probing [Fig. 1(e) and the square-shaped ring in Fig. 1(a)].

Figure 2(a) shows the *I-V* characteristics for a CNT film-*n*-type Si (CNT-*n*Si) MS structure measured over a tem-

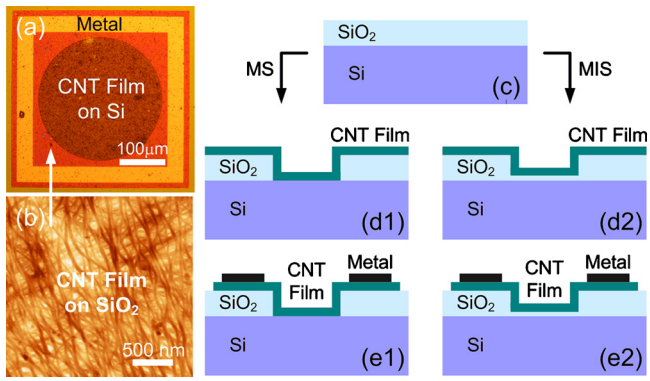

FIG. 1. (Color online) (a) Optical microscope image (top view) of a CNT film-Si MS structure. (b) AFM image of an ~50 nm thick CNT film. [(c)–(e)] Cross-sectional schematic of the fabrication process for MS [(c)–(e1)] and MOS [(c)–(e2)] structures. (c) *p*-type and *n*-type Si substrates with a 400 nm thermally grown SiO_2 are cleaned. [(d1) and (d2)] Oxide is etched in the active region [circular area in (a)] and CNT film is deposited. In (d2), a thin thermal oxide is grown before CNT film deposition. [(e1) and (e2)] CNT film is patterned and a Cr/Pd metal contact (10/90 nm) is evaporated on the film [the outer square ring in (a)].

a)Authors to whom correspondence should be addressed. Electronic addresses: abehnam@ufl.edu and antural@ufl.edu.
b)Present address: National Renewable Energy Lab, Golden, Colorado 80401.

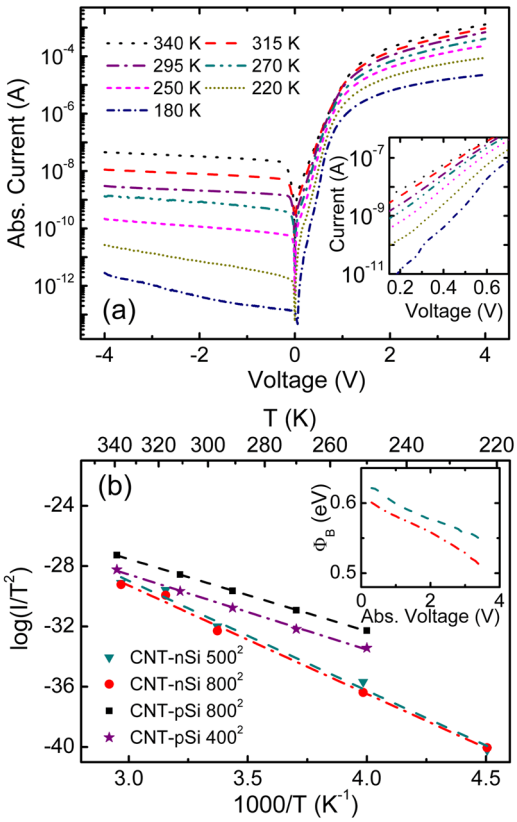

FIG. 2. (Color online) (a) *I-V* characteristics for a CNT-*n*Si MS structure with an area of 800^2 μm^2 at various temperatures in the range of 180–340 K. The inset depicts the same *I-V* characteristics magnified in the small forward-bias region. (b) Log I/T^2 vs $1000/T$ at a reverse bias of $|V|=0.5$ V for two CNT-*n*Si (with areas of 500^2 and 800^2 μm^2) and two CNT-*p*Si (with areas of 400^2 and 800^2 μm^2) MS devices as labeled. The inset shows the barrier height vs reverse bias voltage for the CNT-*n*Si devices in the main panel.

perature (T) range of 180–340 K. All the *I-V* curves depict strong rectification behavior with an exponential slope in the small forward-bias region and a small saturation current in the reverse-bias region that are both temperature-dependent. The inset of Fig. 2(a), which is a magnified view of the small forward bias region, better depicts the temperature-dependence of the current slope. Similar results are obtained for CNT film-*p*-type Si (CNT-*p*Si) devices. Based on these observations, thermionic emission (TE) transport can explain the results for $T>180$ K, which is expressed by[13]

$$I = AA^{**}T^2 \exp\left(-\frac{\Phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right], \tag{1}$$

where A is the effective device area, A^{**} is the reduced effective Richardson constant, k is the Boltzmann constant, q is the electronic charge, and Φ_B is the Schottky barrier height between the CNT film and Si. Below 180 K, however, current levels were found to weakly depend on T, an indication of the dominance of tunneling transport.

In the TE regime, based on Eq. (1), Φ_B can be extracted from the slope of the log I/T^2 versus $1/T$ plot in reverse bias,[14] as shown for two *p*-type and two *n*-type devices in Fig. 2(b) at a reverse bias of $|V|=0.5$ V. The obtained values from the slopes of the curves in Fig. 2(b) are 0.41 ± 0.01 and 0.63 ± 0.03 eV for CNT-*p*Si and CNT-*n*Si devices, respectively.

However, the extracted Φ_B values depend on the reverse bias voltage, as shown for two CNT-*n*Si devices in the inset of Fig. 2(b). The reverse bias dependence of the barrier height due to image-force lowering for CNT-*n*Si devices can be approximated as[15]

$$\Phi_B(V) = \Phi_B^{\text{hom}} - \delta\Phi_{\text{if}}^0 + (1-1/n_{\text{if}})qV, \tag{2}$$

where Φ_B^{hom} is the zero-bias Schottky barrier height if the zero-bias image-force lowering $\delta\Phi_{\text{if}}^0$ is neglected, and n_{if} is the ideality factor. First, n_{if} can be obtained from the slope of a linear fit to the Φ_B versus reverse bias voltage according to Eq. (2). Then, by calculating the band-bending ($|V_i^0|$) at zero-bias, $\delta\Phi_{\text{if}}^0$ is obtained from $\delta\Phi_{\text{if}}^0=4q|V_i^0|\times(1-1/n_{\text{if}})$.[15] Extracted n_{if} and $\delta\Phi_{\text{if}}^0$ values are 1.01 ± 0.006 and 24 ± 7 meV for CNT-*p*Si and 1.025 ± 0.008 and 16 ± 2.5 meV for CNT-*n*Si devices, respectively. Furthermore, the extracted values of Φ_B^{hom} [i.e., $\Phi_B(V=0)+\delta\Phi_{\text{if}}^0$] for *p*- and *n*-type devices sum up to a value close to the bandgap of Si [extracted $\Phi_B(V=0)$ values are 0.435 ± 0.015 and 0.635 ± 0.03 eV for *p*- and *n*-type devices, respectively].

Another interesting observation is that in Fig. 2(a), experimentally measured reverse current levels are three to five orders of magnitude lower than the values calculated based on Eq. (1). This difference can be related to the presence of a very thin native oxide (due to the air-exposed Si surface during and after the CNT film deposition), the porousness of the CNT film (which reduces the effective MS contact area), and the curvature of the nanotubes at the contacts (which increases the effective tunneling distance). The effect of tunneling through the very thin oxide can be modeled in Eq. (1) as an exponential prefactor in the form $\exp(-\chi^{0.5}\delta)$ (obtained by calculating the probability of tunneling using the WKB approximation), where δ is the native oxide thickness and χ is the effective barrier height of the oxide which depends on δ.[16] If we ignore the effect of the film porousness and the nanotube contact curviness, we obtain $\chi^{0.5}\delta>6.5$ $\text{eV}^{1/2}$ Å for both CNT-*p*Si and CNT-*n*Si devices, which in turn corresponds to a native oxide thickness of $\delta>1.8$ nm.[16] However, in addition to the native oxide, the porousness of the CNT film could also contribute to the low current level observed, since it results in incomplete coverage of the substrate surface. A simple geometrical calculation suggests that the actual contact area due to this incomplete surface coverage can be two orders of magnitude lower than the nominal area. Similarly, the curvature of the nanotubes at the contacts can increase the effective oxide thickness, and hence result in an exponential decrease in the tunneling current. Due to these two effects, the above estimation for δ only provides an upper limit for the minimum native oxide thickness in these devices.

Figure 3(a) compares the *I-V* characteristics of a CNT-*p*Si MS structure with those of three CNT film-SiO_2-*p*Si MOS structures with different oxide thicknesses. *I-V* characteristics of the MOS structures are exponential, but both their magnitudes (at a fixed voltage) and slopes are significantly smaller than those of the MS *I-V*s, an indication of tunneling transport.[14] The slopes of the electric-field (E) renormalized currents [I/E^2 versus $1/E$ plot in the inset of Fig. 3(a)] suggest that for oxide thicknesses of 10 nm and above, the Fowler–Nordheim tunneling is the main transport mechanism (the slopes are very similar for 10 and

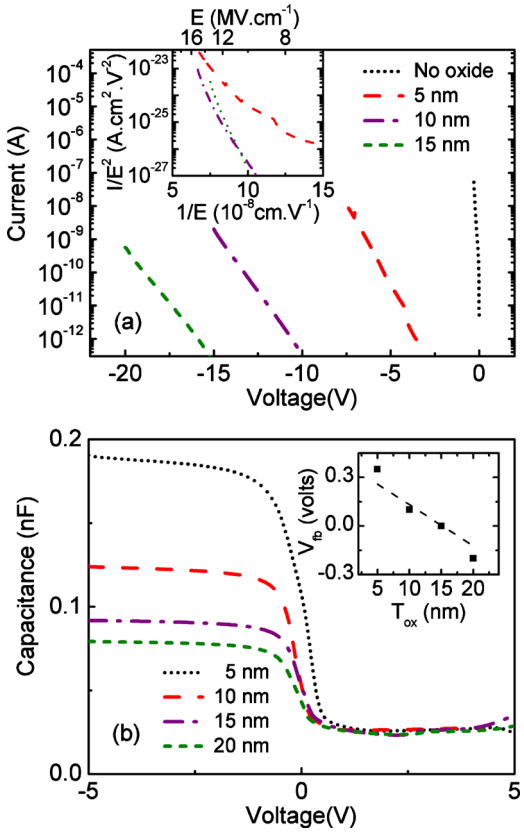

FIG. 3. (Color online) (a) *I-V* characteristics of one CNT-*p*Si MS structure and three CNT film-oxide-*p*Si MOS structures with various oxide thicknesses as labeled, all with an area of 400^2 μm^2. The inset compares I/E^2 vs $1/E$ for the three MOS structures. (b) *C-V* characteristics of four CNT film-oxide-*p*Si MOS structures with oxide thicknesses ranging from 5 to 20 nm, but with the same area of 200^2 μm^2. The inset shows the flat-band voltage extracted from the *C-V* curves as a function of oxide thickness for the same devices.

15 nm curves in the inset), while for the 5 nm oxide, direct tunneling could play a significant role as well.[14]

We have also performed high-frequency capacitance-voltage (*C-V*) measurements on CNT film-SiO_2-*p*Si MOS structures, as presented in Fig. 3(b), for various oxide thicknesses. Measured *C-V* curves agree well with the analytical expectations based on the oxide thicknesses and Si doping density. However, the effective device areas seem to be smaller than the nominal areas due to the porousness of the CNT film, which affects the capacitance values more as the oxide thickness is reduced. The effect of porousness on capacitance is not as pronounced as that on MS tunneling currents, since almost all the tunneling current is injected by nanotubes that are lying directly on the substrate surface, whereas nanotubes that are above the surface can still contribute to the total capacitance. The inset of Fig. 3(b) shows the plot of the flat-band voltage (V_{fb}) versus oxide thickness (T_{ox}). V_{fb} values were found by first calculating the flat-band capacitance C_{fb} from $C_{fb}=C_{ox}C_s/C_{ox}+C_s$, where C_{ox} is the oxide capacitance and C_s is the depletion region capacitance at the Debye length,[13] and then reading the corresponding V_{fb} value from the *C-V* curves. Finally, using $V_{fb}=\phi_{MS}-Q/C_{ox}$, where Q is the total oxide and interface charge and ϕ_{MS} is the CNT film-Si workfunction difference, a workfunction of ~5.2 eV is extracted from the *y*-intercept of the linear fit in the inset of Fig. 3(b) for the CNT film, which is in the same range as the values reported for individual nanotubes and nanotube bundles.[17–19] Oxygen-doped nanotubes or nanotube bundles have higher workfunctions compared to intrinsic individual tubes,[17,18] and the presence of these materials in our CNT films can explain the obtained workfunction.

In conclusion, we have characterized MS and MOS structures with CNT film as the metal and the Si substrate as the semiconductor. We have found that at temperatures above ~180 K, thermionic emission is the dominant transport mechanism in CNT-*p*Si and CNT-*n*Si MS junctions. Schottky barrier heights were extracted as a function of bias, with values of 0.41 and 0.63 eV at a reverse bias of $|V|=0.5$ V for CNT-*p*Si and CNT-*n*Si devices, respectively. We have also found that for oxide thicknesses of 10 nm and above, the Fowler–Nordheim tunneling is the main transport mechanism in CNT film-SiO_2-*p*Si MOS structures, as expected. Furthermore, from MOS *C-V* curves, a CNT film workfunction of ~5.2 eV is extracted. These results provide fundamental insights into the electronic properties of the CNT film-Si and CNT film-oxide-Si structures, which is important for device applications using CNT film transparent and conductive electrodes.

This work was funded in part by the UF Seed Fund. The authors thank Professor A. G. Rinzler for providing CNT films, Dr. P. Kapur for fruitful discussions, Dr. E. Perozziello for help with microfabrication, and Professor S. Thompson for access to characterization equipment.

[1]Z. Wu, Z. Chen, X. Du, J. Logan, J. Sippel, M. Nikolou, K. Kamaras, J. Reynolds, D. Tanner, A. Hebard, and A. Rinzler, Science **305**, 1273 (2004).
[2]C. Kocabas, N. Pimparkar, O. Yesilyurt, S. J. Kang, M. A. Alam, and J. A. Rogers, Nano Lett. **7**, 1195 (2007).
[3]E. S. Snow, F. K. Perkins, E. J. Houser, S. C. Badescu, and T. L. Reinecke, Science **307**, 1942 (2005).
[4]J. Li, L. Hu, L. Wang, Y. Zhou, G. Gruner, and T. J. Marks, Nano Lett. **6**, 2472 (2006).
[5]A. Behnam, J. Johnson, Y. Choi, M. G. Ertosun, A. Okyay, P. Kapur, K. C. Saraswat, and A. Ural, Appl. Phys. Lett. **92**, 243116 (2008).
[6]Z. Li, V. P. Kunets, V. Saini, Y. Xu, E. Dervishi, G. J. Salamo, A. R. Biris, and A. S. Biris, ACS Nano **3**, 1407 (2009).
[7]C.-W. Liang and S. Roth, Nano Lett. **8**, 1809 (2008).
[8]H. Li, W. K. Loke, Q. Zhang, and S. F. Yoon, Appl. Phys. Lett. **96**, 043501 (2010).
[9]T.-F. Kuo, M. B. Tzolov, D. A. Straus, and J. Xu, Appl. Phys. Lett. **92**, 212107 (2008).
[10]T. Yang, Y. Liu, P. D. Ye, Y. Xuan, H. Pal, and M. S. Lundstrom, Appl. Phys. Lett. **92**, 252105 (2008).
[11]J. Bae, H. Kim, X. M. Zhang, C. H. Dang, Y. Zhang, Y. J. Choi, A. Nurmikko, and Z. L. Wang, Nanotechnology **21**, 095502 (2010).
[12]A. Behnam, L. Noriega, Y. Choi, Z. Wu, A. G. Rinzler, and A. Ural, Appl. Phys. Lett. **89**, 093107 (2006).
[13]D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (Wiley, New Jersey, 2006), Chap. 6.
[14]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, New Jersey, 2007), Chaps. 2 and 4.
[15]W. Mönch, *Electronic Properties of Semiconductor Interfaces* (Springer, Berlin, 2004), Chaps. 2 and 3.
[16]H. C. Card and E. H. Rhoderick, J. Phys. D **4**, 1589 (1971).
[17]C. W. Chen and M. H. Lee, Diamond Relat. Mater. **12**, 565 (2003).
[18]J. Zhao, J. Han, and J. P. Lu, Phys. Rev. B **65**, 193401 (2002).
[19]M. Shiraishi and M. Ata, Carbon **39**, 1913 (2001).