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Instability in threshold voltage and subthreshold behavior in Hf-In-Zn-O thin film transistors induced by bias-and light-stress

Khashayar Ghaffarzadeh, ¹ Arokia Nathan, ^{1,a)} John Robertson, ² Sangwook Kim, ³ Sanghun Jeon, ^{3,b)} Changjung Kim, ³ U-In Chung, ³ and Je-Hun Lee⁴

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Electrical bias and light stressing followed by natural recovery of amorphous hafnium-indium-zinc-oxide (HIZO) thin film transistors with a silicon oxide/nitride dielectric stack reveals defect density changes, charge trapping and persistent photoconductivity (PPC). In the absence of light, the polarity of bias stress controls the magnitude and direction of the threshold voltage shift (ΔV_T) , while under light stress, V_T consistently shifts negatively. In all cases, there was no significant change in field-effect mobility. Light stress gives rise to a PPC with wavelength-dependent recovery on time scale of days. We observe that the PPC becomes more pronounced at shorter wavelengths. © 2010 American Institute of Physics. [doi:10.1063/1.3480547]

Metal oxide semiconductors offer an attractive alternative to hydrogenated amorphous silicon (a-Si:H) as the active channel of thin film transistors (TFTs), due to their high field-effect mobility ($\mu_{\rm FE}$) values and optical transparency. One recent candidate is HIZO, in which hafnium (Hf) is introduced to control the carrier concentration and Hall mobility. However, a critical figure of merit in TFTs is the V_T instability during operation as it has a strong bearing on device/circuit lifetime, power consumption and pixel architecture. This paper examines the instability of HIZO TFTs under bias-light stress.

In earlier studies of V_T -instability in a-Si:H systems under electrical stress, two mechanisms were identified: (1) charge trapping inside the dielectric or at the interface and (2) defect state creation within the channel.^{4,5} The former produces rigid and parallel transfer curve shifts while defect creation degrades the subthreshold slope (SS). Although this framework has been applied to several metal oxide based TFTs, it is not clear when one or the other mechanism prevails. Furthermore, in spite of the relatively wide band gap, reports indicate that visible light also contributes to electrical instability. For example, Gorrn et al. showed that visible illumination induces a negative ΔV_T , which was attributed to persistent photoconductivity (PPC) induced by surface effects. Similarly, Gosain et al. reported a negative ΔV_T under exposure to wavelengths (λ) < 420 nm, although this was argued to be due to hole trapping at light-created sites at the interface. Lee et al. also observed a negative ΔV_T under a negative bias-light stress, which was also explained by light-enhanced hole trapping. In this letter, we demonstrate that the polarity of bias stress controls both the magnitude and direction of ΔV_T , while light stress, regardless of bias, causes a negative ΔV_T (despite being passivated) for wavelengths as long as green. We attribute this to PPC, which is observed to be wavelength-dependent with recovery

on a time-scale of days. Its origin in these passivated devices is believed to stem from oxygen vacancies (V_o) .

A schematic cross-section of the TFTs examined here is depicted in Fig. 1. Details of the device fabrication have been reported elsewhere.³ The TFTs have the following geometrical and physical parameters: channel aspect ratio 400 μ m/4 μ m, μ_{FE} 1.4 cm²/V s, SS 0.2 V/dec, V_T 3.5 V hysteresis 0.5 V, gate capacitance (C_i) 1.53×10⁻¹² F/cm², ON/OFF ratio 10⁸, and approximate interface defect density (N_{it}) 2×10¹² cm⁻². Light stressing was carried out using a microscope focused on the top side of the device through the passivation layer. The intensity and spectrum were measured using an S 2387-66R silicon photodiode and an HR200 Ocean Optic spectrometer, respectively (Fig. 1). Rises in substrate temperature under illumination are less than 1 °C. All measurements were performed at room temperature. The samples were annealed before each measurement at 130 °C for 4–5 h and naturally cooled to restore V_T to within 0.7 V of its original value. The devices were stressed using a Kei-

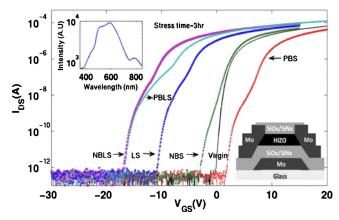


FIG. 1. (Color online) Transfer characteristics of HIZO TFTs subjected to PBS, NBS, LS, NBLS, and PBLS. The upper inset depicts the spectrum of the illumination source on a semilogarithmic scale and the lower inset the schematic cross-section of the TFTs examined. The front- and back-channel interfaces of the TFT are formed by the HIZO/SiO_x layers.

¹London Center for Nanotechnology, University College London, London WC1H 0AH, United Kingdom

²Department of Engineering, Cambridge University, Cambridge CB2 1PZ, United Kingdom

³Semiconductor Device Laboratory, Samsung Advanced Institute of Technology, Yongin-Si, Gyeonggi-Do 449-712, Republic of Korea

⁴Samsung Electronics, Yongin-Si, Gyeonggi-Do 449-712, Republic of Korea

a)Electronic mail: anathan@ucl.ac.uk.

b) Electronic mail: sanghun1.jeon@samsung.com.

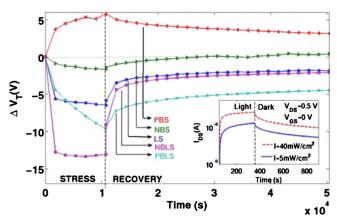


FIG. 2. (Color online) The shift in threshold voltage as a function of time during 3 h of bias and light stress followed by 11 h of natural recovery. Stretched-exponential fits to the recovery curves yield the following values of (τ, β) : $(1.14 \times 10^5 \text{ s}, 0.48)$ for PBS, $(2.1 \times 10^4 \text{ s}, 0.22)$ for LS, $(6 \times 10^3 \text{ s}, 0.21)$ for NBLS, and $(1 \times 10^5 \text{ s}, 0.3)$ for PBLS. The inset demonstrates that illumination gives rise to a PPC. The OFF-current is 10^{-12} A.

thley 4200 Semiconductor Measurement Unit. Stressing was interrupted at 30-min intervals to sample transfer characteristics at V_{DS} =0.5 V. Illumination was turned off 10 s before each sampling operation to allow meaningful comparisons with the dark transfer characteristics. The V_T was extracted using the commonly-used extrapolation technique for a TFT biased in the linear $(V_{GS} \gg V_{DS})$ regime. ¹⁰

Figure 1 compares transfer characteristics of devices subjected to negative bias stress (NBS), positive bias stress (PBS), light stress (LS), and negative/positive bias-light stress (N/PBLS). The light intensity was 40 mW/cm² and the bias stress conditions were $V_{\rm GS}$ =+/-20 V and $V_{\rm DS}$ =0 V. The PBS and NBS shift the transfer characteristics in the positive and negative directions, respectively, and LS causes a large negative ΔV_T , the magnitude of which is enhanced by adding bias to LS.

Stressing the devices causes a humplike shape to appear in the subthreshold region. Full natural recovery of the hump (i.e., in the absence of bias or illumination) follows a stretched-exponential behavior of the form $\exp[-(t/\tau)^{\beta}]$, where t is measurement time (s), τ the relaxation time (s) and β the exponent. Following 3 h of NBS, LS, NBLS, PBS, and PBLS, the extrapolated recovery times are 3 h, 13 h, 24 h, 36 h, and 355 h, respectively. The appearance of the humps is believed to be due to multiple conduction paths with non-identical thresholds. ¹¹

Figure 2 shows ΔV_T as a function of time under various bias stress conditions. Before discussing each stress-recovery behavior, we note that $\mu_{\rm FE}$ variation under light-bias stress is less than 3%, suggesting that the density of conduction band tail states remains unaltered. PBS increases ΔV_T by 5.8 V and $\Delta {\rm SS}$ by ~ 0.21 V/dec, which are reduced to 3 V and ~ 0.12 V/dec, respectively, after 13 h of subsequent natural recovery. Assuming that the stress-induced $\Delta {\rm SS}$ is entirely due to defect creation at or near the interface, the total number of new defect sites ($\Delta {\rm N}_{\rm defect}$) and the maximum $\Delta {\rm SS}$ -induced ΔV_T can be estimated from the following:

$$\Delta N_{\text{defect}} = (C_i/q)[q \log(e)\Delta SS/(KT) - 1], \tag{1}$$

$$\Delta V_T = q \Delta N_{\text{defect}} / C_i. \tag{2}$$

Here, q is the elementary charge, K the Boltzmann constant, and T the temperature (K). The resulting estimates of $\Delta N_{\rm defect}$ and ΔV_T are $1.56\times 10^{12}~{\rm cm}^{-2}$ and $2.6~{\rm V}$, respectively, suggesting that in the worst case, charge trapping could be an equal contributor to ΔV_T under PBS. Realistically, however, ΔSS may not be entirely due defect state creation since (a) stress-induced ΔSS recovers at room temperature and (b) the original device characteristics can be restored by annealing at a moderately low temperature ($\sim 130~{\rm ^{\circ}C}$) and time (3–4 h). Another possible cause of ΔSS could be related to the presence of multiple conduction paths in the channel.

The recovery of V_T follows a stretched-exponential with $\tau \sim 1.14 \times 10^5$ s, $\beta \sim 0.48$ and a recovery time of ~ 8.4 days, identifying the $\mathrm{SiO_x}$ as the primary location of trap sites. Using the method described by Wright *et al.*, and following similar assumptions, the characteristic penetration depth (d) in the $\mathrm{SiO_x}$

$$d \cong 1.15\Delta V_T / (K_0 r_0), \tag{3}$$

can be estimated as 3 Å, which implies that trapping takes place at the vicinity of the interface. ¹² In Eq. (3), K_0 is the tunneling probability constant ($\sim 10^{10}$ m⁻¹) and r_0 the discharge rate given by $[\Delta V_T/\Delta \log_{10}(t)]$.

NBS leads to a reduction in V_T , which can be attributed to a de-population of donorlike traps (which are neutral when occupied and positive when empty) near the HIZO/SiO_x interface. Its plausibility is based on the observation that V_T recovers after only 2 h of stress release and that there is no hole conduction in n-type metal oxides. Indeed NBS causes a Δ SS of 0.44 V/dec, which then recovers to 0.16 V/dec in 13 h, alluding to a depopulation of existing traps sites. ¹³

Illumination gives rise to a PPC (Fig. 2). Here, the channel conductivity is raised by several orders of magnitude after exposure to white light with intensities of 40 and 5 mW/cm². The current during subsequent relaxation in the dark follows a stretched-exponential with $\tau \sim 85$ s and $\beta \sim 0.36$, giving a recovery time of 1.5 days. Similarly, LS results in PPC causing the active channel to behave as though it was n-doped, thus lowering the V_T . On release from LS, it is the photocurrent decay that governs the recovery process, which also follows a stretched-exponential decay with $\tau \sim 2.1 \times 10^4$ s, $\beta \sim 0.22$, and recovery time of around 18.4 days. The slower recovery (relative to that observed in the inset) is believed to be due to the longer stress time (3 h) and/or sampling intervals (30 min).

A negative bias during LS (i.e., NBLS) physically separates photogenerated e-h pairs as schematically depicted in Fig. 4, thus reducing recombination, leading to a larger ΔV_T . Contributions from trapping of photogenerated holes inside the dielectric are expected to be small because the valence band is mainly composed of 2p oxygen orbitals, causing the localization of holes. Recovery from NBLS can be parameterized using a stretched-exponential with $\tau \sim 6 \times 10^3$ s and $\beta \sim 0.21$, yielding a time period of around 11 days. A positive bias during LS (i.e., PBLS) also physically separates the photogenerated e-h pairs while increasing the electron concentration thus reducing the initial negative ΔV_T , as compared to NBLS. At the same time, PBLS leads to greater electron trapping in the dielectric due bias- and lighting during the interaction in the abstract in clusters.

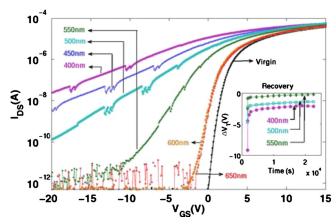


FIG. 3. (Color online) Transfer characteristics of TFTs subjected to 30 min of illumination at different wavelengths and sampled under light. Inset shows that the PPC becomes more pronounced at shorter wavelengths.

This progressively reduces the gate drive $(V_G - V_T)$ thus increasing ΔV_T with stress time. The subsequent recovery process is governed by a combination of photocurrent decay, under an effective negative V_{GS} induced by trapped electrons, and charge de-trapping from the SiO_x . Consequently, the recovery in this case can be parameterized by $\tau \sim 1 \times 10^5$ s and $\beta \sim 0.3$, giving a recovery time of around 38 days.

To gain insight into origin of PPC, the light was passed through optical band pass filters centred at λ =400, 450, 500, 550, 600, and 650 nm with spectral width of 40 nm. The corresponding intensities were measured to be 0.5, 2.7, 6.7, 8.1, 8.7, and 9.2 mW/cm². The devices were subjected to 30 min of illumination and sampled under light. The OFF-current begins to rise with exposure to λ <550 nm. Due to enhanced absorption, the magnitude of OFF-current rises and the negative ΔV_T increases despite the decrease in incident light intensity with decreasing λ . The inset of Fig. 3 shows the recovery of ΔV_T after exposure to 550, 500, and 400 nm illumination, demonstrating that PPC effects become more pronounced as the λ decreases.

The PPC in ZnO thin films and nanostructures is generally attributed to surface and ambient effects However, device passivation rules this out here. ^{16,17} Furthermore, we note that while defect state creation reduces the conductivity of a-Si:H, V_o generation can in fact increase it in metal oxides. ¹⁸ Here, LS causes a Δ SS and ΔN_{defect} of 0.53 V/dec and 4.8×10^{12} cm⁻², respectively, which subsequently recovers to 0.43 V/dec and 4.8×10^{12} cm⁻², respectively, in 17 h. This, however, cannot account for the PPC because approximately 1.1×10^6 cm⁻³ of V_0 sites must be generated in 1-2 s to reproduce the current behavior shown in Fig. 2. Thus we attribute the PPC to V_o 's becoming singly (V_o^+) or doubly ionized (Vo++) under illumination. Here, holes are physically localized at V_o sites, which sit at $\sim\!2.3\,$ eV in ZnO as shown in Fig. 4. $^{19-21}$ Therefore, the photoinstability is controlled by the V_o concentration, which is affected by the composition of the channel as well as gate/channel and channel/passivation interfaces. Although a crude comparison of the photoinstability of HIZO and IGZO shows the latter to have faster recovery times, a more accurate assessment needs to consider a variety of other factors including, TFT bias, and, the nature of the interfaces.

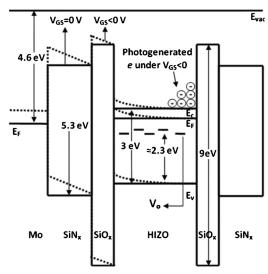


FIG. 4. Approximate energy band diagrams of TFT system examined here. Ionized V₀ sites are suggested as the origin of the PPC. Negative gate bias bends the energy bands upwards and separates photogenerated e-h pairs.

In summary, charge trapping in SiO_{x} and depopulating donorlike traps near the interface are suggested as the primary instability mechanisms in the dark under PBS and NBS, respectively. Light stress, with and without bias stress of either polarity, is shown to give rise to PPC, resulting in reduction in the V_{T} . Localization of holes at vacancy sites is suggested as the origin of the PPC.

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