Influence of Surface States on Electron Transport through Intrinsic Ge Nanowires

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Received: December 3, 2004; In Final Form: January 22, 2005

Solution-grown single-crystal Ge nanowires were used as conductive channels in field effect transistor devices to study the influence of surface states on their electron transport properties. Nanowires contacted with Pt electrodes using focused ion beam metal deposition exhibited linear current−voltage (*IV*) curves at room temperature with apparent resistivities ranging from 10^1 to 10^{-1} Ω cm. In all cases, the nanowire conductance decreased with positive external electric fields applied perpendicular to the nanowire surface by a gate electrode, characteristic of p-type carrier accumulation at the nanowire surface. The field-induced change in conductance exhibited a time-dependent relaxation, with response time and magnitude of current decrease that depended on the nanowire surface chemistry. Nanowires treated with an organic passivation layer using a thermally initiated hydrogermylation reaction exhibited 2 orders of magnitude slower current relaxation and a smaller decrease in current relative to "bare" nanowires with oxidized surfaces.

Introduction

Chemically grown semiconductor nanowires have been explored for use as building blocks to construct various electronic and optical devices, including logic gates,[1] address decoders,[2] memory components,[3] light emitting diodes,[4] photodetectors,[5] lasers,[6,7] and chemical sensors.[8,9] Given this range of potential applications, it is exciting to consider how colloidal semiconductor nanowires could potentially be merged with plastic materials for cheap disposable flexible electronics and photonics to dramatically reduce unit cost without significant sacrifices in performance. Germanium (Ge) nanowires are particularly interesting for electronic applications, as Ge has higher electron and hole mobilities than silicon (Si), which will be advantageous for higher performance in transistors with nanoscale gate lengths.[10] Recently, our group[11] and others[12−15] have fabricated prototype electrical device structures from chemically grown Ge nanowires. In these devices, interfaces are extremely important; for example, the metal/semiconductor contacts and the gate metal/dielectric/nanowire layer depend in large part on the interfacial chemistry. In two previous papers, we addressed metal/Ge nanowire contact fabrication and studied Ge nanowire surface chemistry in detail with the development of effective synthetic schemes for chemically passivating Ge nanowires.[11,16] Here, we examine the field effect (i.e., changes in conductance with external applied electric fields) on intrinsic nanowires, finding that they exhibit p-type behavior. This field effect decays over the course of many seconds to minutes, which is a characteristic of slow surface states. We find that the lifetimes of these slow surface states depend on the nanowire interface chemistry, with covalent surface termination with hydrocarbon ligands extending the lifetimes by 2 orders of magnitude relative to "bare" nanowires.

Experimental Details

Ge Nanowire Synthesis. Single-crystal Ge nanowires with diameters ranging from 5 to 30 nm were synthesized by the gold nanocrystal-seeded supercritical fluid−liquid−solid (SFLS) method using a continuous flow reactor.[17] The nanowires were produced by continuously feeding hexane with 10 mM diphenylgermane (DPG, Geleste) and 3 nm diameter dodecanethiol-coated Au nanocrystals at a molar Ge/Au ratio of 1000:1 into a 1 mL Ti steel reactor at 380 °C and 7 MPa and a reactor residence time of approximately 90 s. Approximately 30 mg of Ge nanowires are produced in ∼2 h. In some cases, the nanowires are chemically treated with either isoprene or hexene to yield organic passivation layers: the Ge nanowire surfaces react with the unsaturated carbon bonds of the diene or alkene through a thermally initiated hydrogermylation reaction to render a covalently bonded organic monolayer.[16] Untreated nanowires readily oxidize upon exposure to ambient conditions to form a 1−2 nm thick GeO_{2-x} shell, which continues to grow to reach a self-limited thickness of ∼4 nm over the course of ∼24 h.[16] Isoprene and hexene passivation yields chemically stable nanowires exposed to wet or dry oxidative conditions, as confirmed by chemical stability tests, X-ray photoelectron spectroscopy (XPS), and Fourier transform infrared (FTIR) spectroscopy.[16]

Nanowire Field Effect Transistor (FET) Fabrication. Single nanowire device test structures were fabricated on ∼10 × 10 mm sections of highly doped p-type Si substrates (1−10 Ω cm) coated with 100 nm of SiO_2, which serves as the gate dielectric. First, contact pads and reference marks are defined by electron beam lithography (EBL) patterning (Raith 50) of PMMA (poly(methyl methacrylate)) photoresist, followed by thermal evaporation of 3 nm Cr and 40 nm Au (Denton Thermal Evaporator). Nanowires are deposited onto these prefabricated substrates by submersing the substrate in a dilute (∼10 μg/mL) toluene or isopropyl alcohol suspension of Ge nanowires for 10−15 min to achieve a nanowire surface density of 500−1000 mm^{-2}. Nanowires with "untreated" surfaces have a 2−4 nm thick oxide layer. Some nanowires were briefly etched for 30 s in 5% HCl. The isoprene- and hexene-treated nanowires were not etched in acid.

Electrical contact to the nanowires was made by writing 100 nm wide Pt lines in a dual-beam scanning electron

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10.1021/jp044491b CCC: $30.25
Published on Web 02/26/2005

microscope/focused ion beam (SEM/FIB) system (FEI Strata DB 235) to connect the gold contact pads with the nanowires. EBL, which is a widely used technique for defining electrical contacts to nanowires, requires multiple processing steps, such as resist deposition, pre-and postbake, development and lift-off, which expose the nanowires to various chemical species that can modify the surface. In contrast, "direct-write" processes using focused ion- or electron-beam-assisted chemical vapor deposition (CVD) of metal contact electrodes can preserve the nanowire surface chemistry. The SEM/FIB system enables both imaging and metal deposition, so that the nanowires can be located on the substrate by SEM and then Pt lines can be deposited using the focused ion beam, which degrades the precursor trimethyl-methylcyclopentadienyl-platinum.[11] Our recent detailed studies of the effect of EBL and focused electron- and ion-beam-assisted CVD on the contact resistance in single Ge nanowire devices showed that Pt electrodes deposited by FIB-assisted Pt CVD offer a low resistance, chemically non-intrusive approach for electrically contacting the Ge nanowires.[11] The Pt electrodes were written with a 30 keV Ga^+-beam at 10 pA beam current. These deposition conditions yield Pt lines with a cross-sectional area of $\sim 0.35\ \mu m^2$ and a total resistance of less than $\sim 5\ k\Omega$ between the nanowire and the gold contact pads. All Ge nanowire devices made with Pt contacts by FIB-assisted CVD exhibited ohmic *IV* curves with resistivities ranging from 10^1 to $10^{-1}\ \Omega$ cm.

Electrical Measurements. Electrical measurements were performed immediately after device fabrication on a Karl Suss PM5 probe station connected to a Keithley 4200 digital parameter analyzer. Prolonged exposure to oxygen and ambient moisture was avoided, and the device properties were measured in a home-built nitrogen chamber. Field effect measurements were performed either using the heavily doped Si substrate as a global gate or using a Pt metal gate electrode deposited on the substrate surface near that nanowire, positioned between the two contact electrodes. The nanowire resistivity, ρ, is calculated from the measured resistance R with no applied gate voltage, the electrode spacing L, and the nanowire diameter d, determined from the nanowire height profile measured by atomic force microscopy (AFM, Dimension 3100): $\rho = R(\pi d^2/4L)$. The contact resistance determined for a few devices using four point probe measurements was an order of magnitude smaller than the nanowire resistance, as discussed elsewhere.[11] Nonetheless, the ρ values reported here represent upper limits.

Results

p-Type Field Effect in SFLS-Grown Ge Nanowires. Figure 1 shows room-temperature current−voltage (*IV*) curves for a hexene-treated Ge nanowire as a function of gate voltage. The curves are linear. The conductance decreases with positive gate potential and increases with negative gate potential. Although the nanowires are not intentionally doped, they exhibit this field effect response characteristic of a p-type semiconductor. It is actually well-known that Ge tends to accumulate holes at the semiconductor surface as a result of trapped negative surface charge related to the Ge surface.[18] Figure 2 shows a schematic illustration of how negative surface charges can arise from the presence of trap levels located below the Fermi level, which then bend the valence and conduction bands up near the surface. The Ge surface layer is known to have a significant concentration of electron traps located ~ 0.15 eV below the middle of the band gap.[19,20] The trap level is filled with an electron when the semiconductor Fermi level is higher than the trap level. The resulting surface charge promotes hole accumulation, or upward

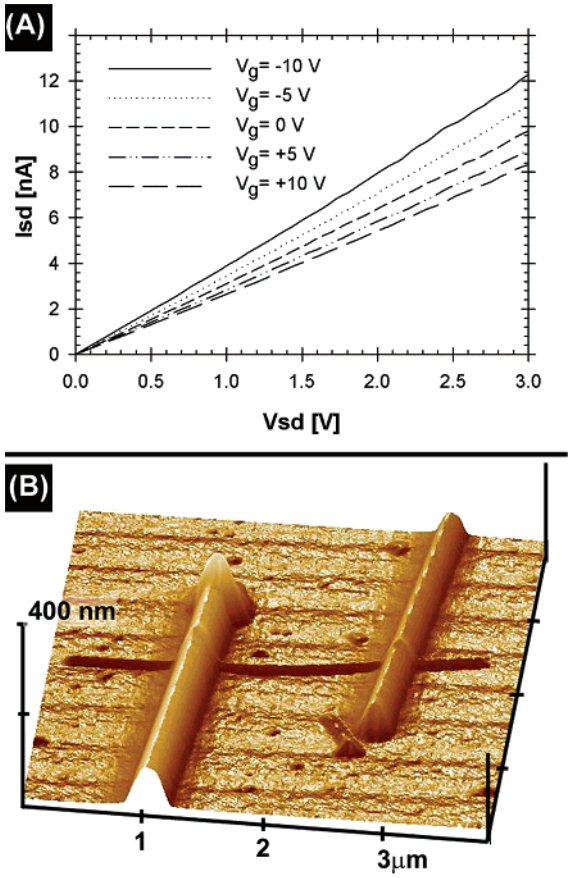

Figure 1. (A) Room-temperature *IV* curves as a function of gate voltage applied using the p-doped Si substrate as a back gate. The nanowire conductance decreases with positive gate voltage, characteristic of p-doping. (B) AFM image of the device measured in panel A showing the 24 nm diameter hexene-passivated Ge nanowire contacted by two Pt contact electrodes.

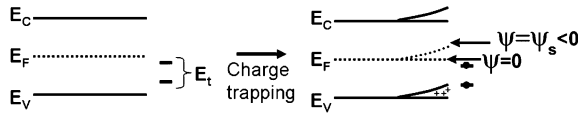

Figure 2. (Left) Band structure and Fermi level E_F of intrinsic Ge with available trap levels E_t at the semiconductor surface. If E_t is lower than E_F, the trap level will be filled with electrons. The charge trapping results in a negative field at the surface that bends the band upward, which results in hole accumulation, as shown on the right. The schematic representation of the trap levels is only a crude illustration of how the available trap levels may be spread within the band gap.

band bending, to maintain charge neutrality in the nanowire. Another way to think about this is that the negative surface charge makes the flat band potential more negative. This surface-induced hole accumulation gives rise to the p-type semiconductor field effect observed in these nanowires.

Field Effect Hysteresis and Time-Dependent Field Effect Decay. Gate voltage sweeps (at ~ 0.5 V/s) in single Ge nanowire FETs exhibit significant hysteresis for nanowires with "bare" oxidized surfaces (Figure 3A). The amount of hysteresis increases with larger ranges of applied gate voltage. Hexene-treated nanowires also exhibit hysteresis in gate voltage sweeps; however, the amount of hysteresis is only about half as much as in the nanowires without surface treatment (Figure 3B). Hysteresis indicates that some degree of irreversibility is occurring in the system and that there is a kinetic factor in the field effect that is important. Dai and co-workers[15] also recently reported field effect hysteresis in CVD-VLS grown Ge nano-

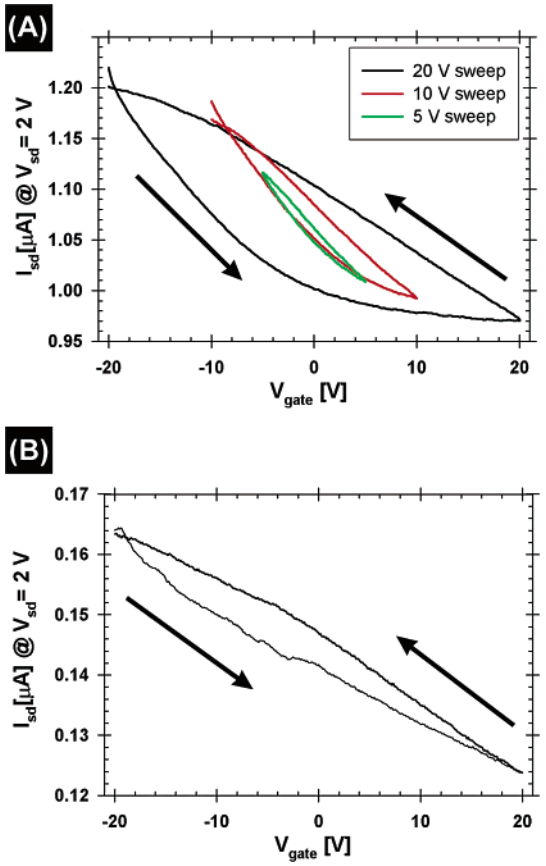

Figure 3. Current vs gate voltage for (A) an untreated oxidized Ge nanowire and (B) a C_6 hydrocarbon monolayer coated Ge nanowire. The gate voltage was swept at 0.5 V/s.

wires and attributed the hysteresis to the surface oxide species, consistent with previous studies of the field effect on bulk Ge substrates.[18] Since the hysteresis results from a kinetic effect, most likely related to charge trapping on the surface, one would expect to see a time-dependence in the source−drain current after the gate potential has been applied. In fact, as shown in Figure 4, this is what is observed.

The source−drain current relaxes over the course of several seconds to minutes after a step change in gate voltage, as shown in Figure 4. For untreated Ge nanowires with a surface oxide, the source−drain current returns to a steady-state value within ~500 s after applying a +20 V gate potential. With a negative applied gate potential (−20 V), the current decreases much more rapidly, relaxing to a steady-state value within ~120 s. Similar current relaxation profiles are observed when positive and negative gate voltages are applied in the opposite order (i.e., −20 V followed by +20 V).

Field Effect Relaxation Kinetics. The surface states that give rise to the p-type field effect and source−drain current decay have characteristic lifetimes greater than a millisecond, which have been characterized as "slow" surface states by Kingston and others.[18,21−23] The "fast" surface states reside at the Ge/GeO_x interface and are primarily responsible for recombination processes. The slow surface states in Ge are very sensitive to both the surface structure and the ambient environment and can exhibit densities as high as 10^{15} cm^{-2}.[18] Therefore, it is no surprise that hexene-terminated Ge nanowires exhibit less hysteresis in the gate sweeps and a different field effect time-dependence since the surface passivation reduces the amount of surface oxidation and limits the amount of environmental exposure to water and other surface adsorbates.[16]

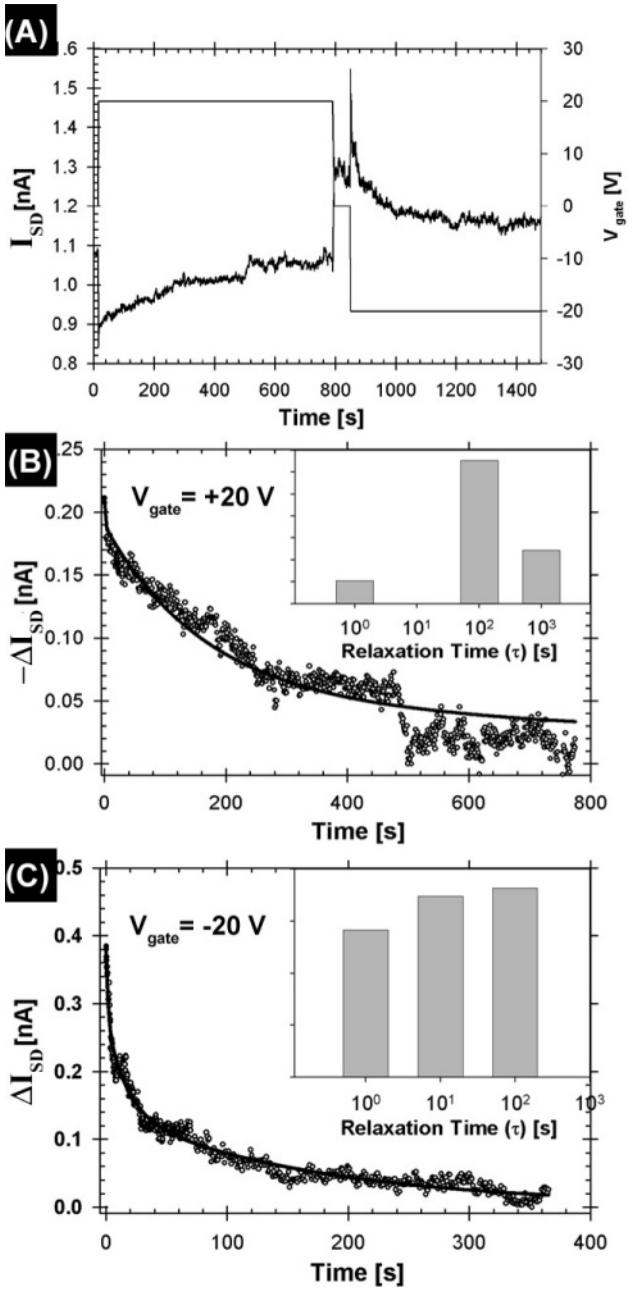

Figure 4. (A) Change in source−drain current for 1 V source−drain voltage with time and applied gate voltage for an untreated Ge nanowire under a bias of 1 V. The gate voltage was applied as a step function with a delay time of 0.5 s to account for possible displacement currents. (B,C) Detailed views of the field effect decay during positive and negative applied gate voltage. The histograms in the inset show the relaxation time distributions obtained from a fit of eq 1 to the experimental data.

The current relaxation results from the slow redistribution of charge on the nanowire surface after applying the gate potential. This redistribution shifts the value of ψ_s, which therefore shifts the "effective" applied gate potential, which is $V_g^{eff} = \psi_s + V_g$. Immediately after applying V_g, the bands shift relative to the initial surface potential. However, as shown in Figure 5, the band shift that occurs as a result of the applied field leads to the filling of higher trap levels, as in the case of $V_g < 0$, or the discharging of lower trap levels when $V_g > 0$. This charging or discharging of the surface with applied field changes the value of ψ_s, which in turn shifts V_g^{eff}. The charging and discharging of trapped surface charge is a relatively slow

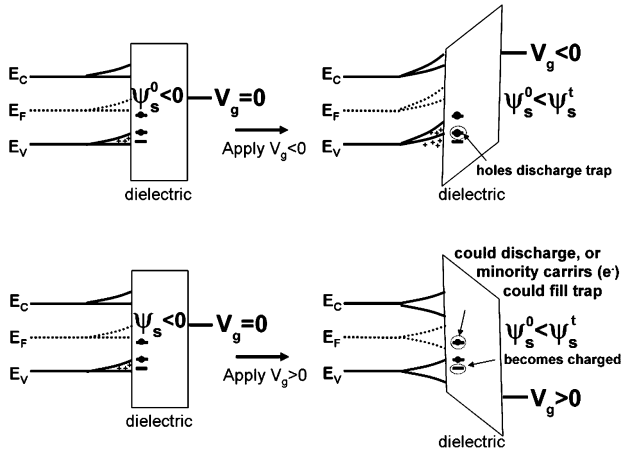

Figure 5. Proposed mechanism for decaying field effect with $V_g < 0$ or $V_g > 0$. In both cases, charge redistribution at the nanowire surface, a kinetically limited process, will shift ψ_s away from its initial equilibrium value, thus changing the effective V_g over time. The applied field from the gate electrode shifts the bands up ($V_g < 0$) or down ($V_g > 0$). With $V_g < 0$, lower-lying charge trap levels will be neutralized as holes accumulate at the surface with energies lying above E_t. The neutralization process will be slow, but as these trapped charges are lost, ψ_s will shift down, decreasing the effective applied gate potential. With $V_g > 0$, lower-lying trap levels that may have been neutralized by accumulated holes will become charged, thus shifting ψ_s up in energy, decreasing the effective applied gate potential. Again, this is a kinetically limited process.

process, kinetically limited by either a diffusion barrier or a tunnel barrier at the nanowire surface. In fact, the current relaxation exhibits a multiexponential time-dependence, indicating there is a significant spread in the spatial and energy distribution of the surface trap states and associated rate processes.

The multiple relaxation processes that can occur in parallel to relax the current can be accounted for using a convolution of an empirical equation developed by Koc[23] that takes into account multiple characteristic times and their differing relative contributions to the overall measured current relaxation:

$$\Delta\sigma = \Delta\sigma_0 \sum_i (\exp(-t/\tau_i)^{0.6}) \qquad (1)$$

where $\Delta\sigma$ and $\Delta\sigma_0$ are the instantaneous and initial change in conductance, t is the elapsed time after applying the gate potential, and τ_i is the characteristic relaxation time of each process i. Kingston and McWhorter proposed that slow surface relaxation derives from mobile carrier tunneling into nonconducting surface states and that the relaxation kinetics reflects the carrier transfer rate from bulk to surface states.[21] Their model was consistent with temperature-independent surface relaxation, as measured by Kingston.[24] Similar experiments by Morrison,[22] however, revealed an exponential temperature dependence and an influence of other external factors such as illumination and oxygen partial pressure. Morrison proposed a model in which the rate-determining step is carrier transport over a surface potential barrier that is related to the amount of surface charge. Koc[23] explained the slow relaxations in terms of induced charge diffusion into trapping levels in the surface oxide. We have expanded upon Koc's empirical model to account for multiple relaxation times as shown in eq 1.

Figure 4B,C shows the distribution of the multiple characteristic relaxation times involved in the decay of the current after applying the external field on bare nanowires. The distributions were determined by fitting eq 1 to the data in Figure 4A. The characteristic relaxation times range from seconds to hundreds of seconds, and the distributions depend on the polarity of the applied gate potential, suggesting an uneven spread of surface state levels across the band gap. For $V_g = -20$ V, the values of τ_i are spread evenly from 1 to 100 s. For $V_g = +20$ V, τ_i is spread unevenly from 1 to 1000 s, with the primary rate process exhibiting a characteristic time of ~100 s. The energy level diagram in Figure 6A shows qualitatively the corresponding distribution of surface trapping levels expected on the oxide surface layer based on the relaxation data in Figure 4. Since Ge nanowires with untreated surfaces exhibit pronounced relaxation effects for both positive and negative applied gate voltages, the energy levels of the capturing surface states appear to be spread across the entire band gap.

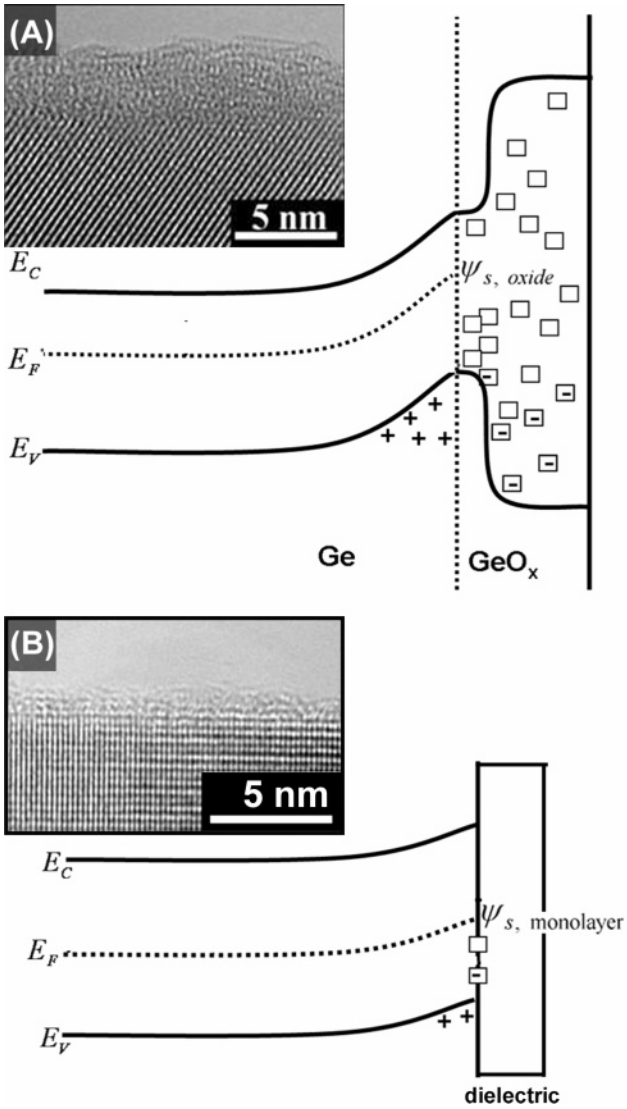

Figure 6. Schematic representation of the energy diagram near the surface of (A) oxidized and (B) organic-monolayer-passivated Ge nanowires. The insets show HRTEM images of oxidized and isoprene-passivated surfaces, respectively.

Effects of Etching and Surface Passivation on Slow Surface States. Figure 6B shows the energy diagram expected for a nanowire with a lower concentration of surface trap levels, as would be expected for organic-monolayer-coated nanowires with little surface oxidation. The high-resolution transmission electron microscopy (HRTEM) image in Figure 6B of a nanowire with an isoprene-passivated surface shows the characteristic absence of native surface oxide that forms on bare

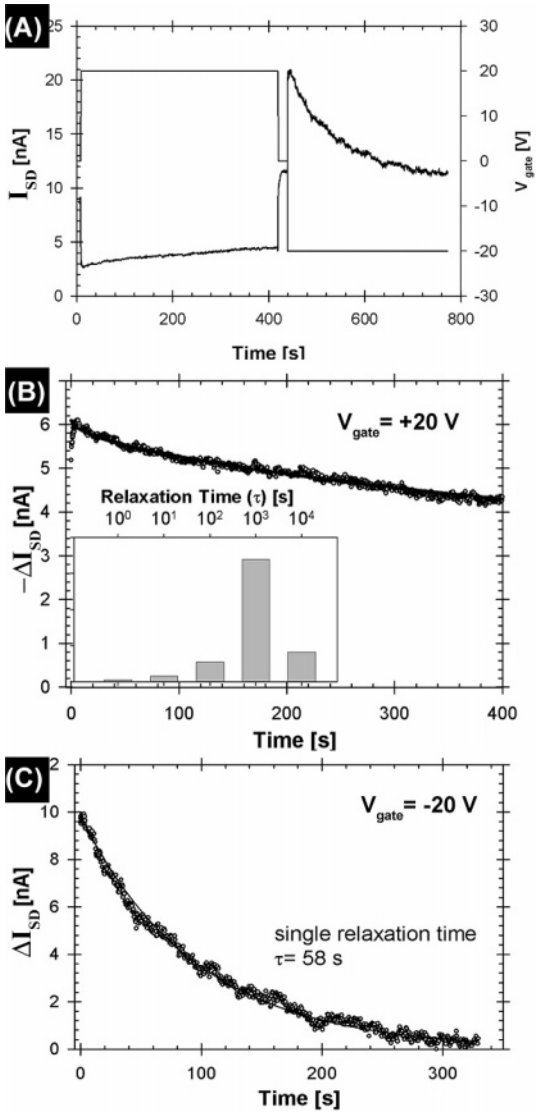

Figure 7. (A) Change in current vs time plots for step changes in applied gate voltage for a Ge nanowire with a freshly etched surface. (B,C) Detailed view of the field effect decay under positive and negative applied gate voltage. The source−drain voltage was 1 V. The histograms (inset) show the relaxation time distributions obtained by fitting eq 1 to the experimental data.

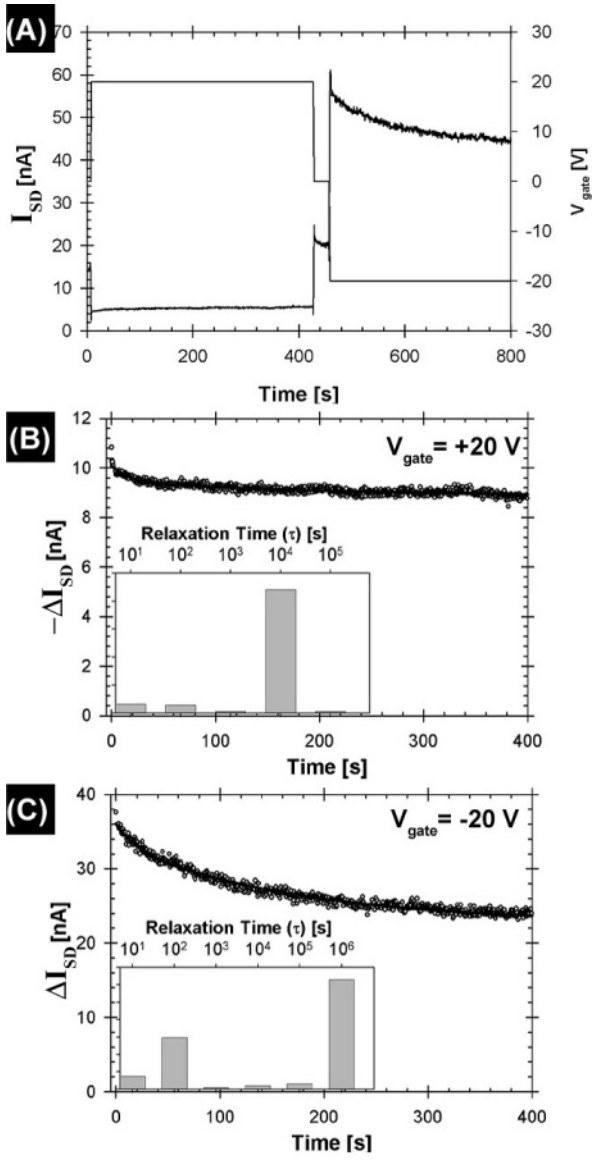

Figure 8. (A) Change in current vs time plots for step changes in applied gate voltage (right axis) measured on a device prepared from isoprene-passivated Ge nanowires. (B,C) Detailed view of the field effect decay after applying positive and negative gate voltages. The histograms in the inset show the relaxation time distributions obtained from a fit of eq 1 to the experimental data.

nanowires (for example, compare the TEM images in panels A and B of Figure 6). Although organic-monolayer-terminated nanowires still exhibit a p-type gate effect, the characteristic time-dependence of the field effect relaxation is qualitatively different than for bare nanowires with much longer values of τ_i. This is most likely due to a significant reduction in surface state density, as the primary source of surface trap levels appears to be the GeO_{2-x} species on the nanowire surface. Consider, for example, field effect relaxation measurements of Ge nanowires with etched surfaces. These nanowires showed a significantly slower decay in the positive field-induced conductivity (see Figure 7), with $\tau_i \approx 10^3$ s at $V_g = +20$ V, compared to nanowires with oxidized surfaces. The most distinct difference was that there was very little current relaxation with $V_g > 0$ compared to the unetched nanowires. These results suggest that the surface trap levels that may exist near the valence band edge for unetched Ge nanowires do not appear to be present in etched nanowires. Also quite distinct from the unetched nanowires is the decay in the field-induced conductivity after applying $V_g = -20$ V, which is well represented by a single relaxation time of 58 s. Carriers induced with $V_g < 0$ exhibited much faster trapping, resulting in nearly complete current relaxation to steady state within ~200 s. It appears that the relaxation of the gate effect with $V_g < 0$ relates primarily to the rate of hole transport from the nanowire surface to the charged trap states upon increased hole accumulation (i.e., upward band bending) with applied negative gate voltage. As holes neutralize the charged traps, ψ_s becomes more positive and shifts V_g^{eff} down, thus reducing the net applied field and the gate-enhanced conductance. Perhaps in the untreated nanowires, the trap states are located closer to the surface than in the oxidized wires, therefore leading to faster decay and carrier trapping.

Isoprene-treated Ge nanowires exhibit even less surface charge relaxation with $V_g > 0$ than the etched nanowires. As shown in Figure 8, the current decreases by only ~10% after applying the positive gate potential, relative to ~1/3 for etched nanowires and ~90% for unetched nanowires. With $V_g = 20$

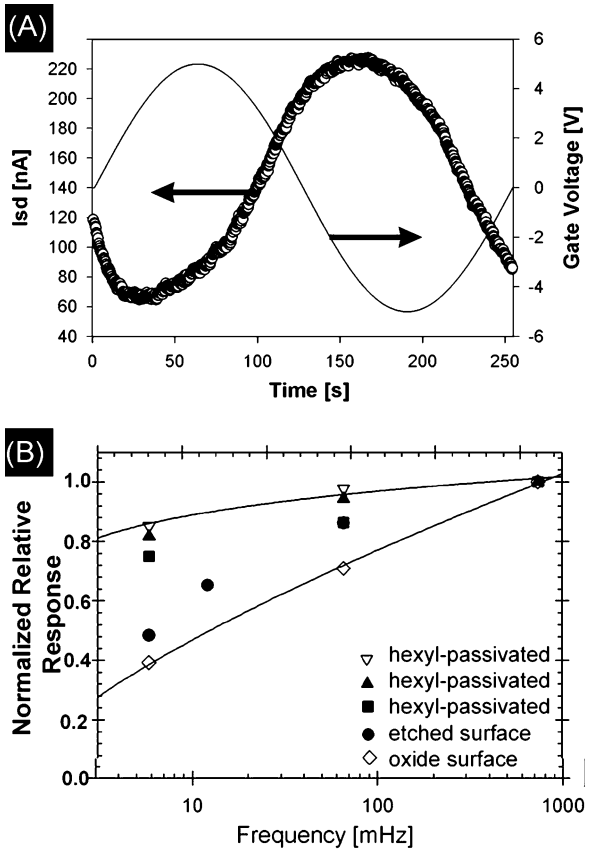

Figure 9. (A) Conductance vs time for a gate voltage applied as a sinusoidal wave with 25 mHz. (B) Normalized relative response of Ge nanowire devices with different surface treatment as a function of frequency (ω). The solid lines refer to the fit of the form $R(\omega) = a(\ln(\omega))^b + c$, where a, b, and c are fitting parameters.

V, the current relaxation that does occur takes place very slowly, with exceedingly long relaxation times of $\tau \cong 10^4$ s. With $V_g = -20$ V, the current relaxation is also very slow, with a significant fraction of the relaxation processes exhibiting very long values of $\tau_i \cong 10^6$ s. Although there is a contribution of faster relaxation processes, with τ_i on the order of 10 and 100 s, the slower relaxation times indicate a significant kinetic barrier to hole transport from the nanowire core to the negatively charged surface states that is much higher than what is found on both etched and unetched nanowires. It is also possible that some of the surface states associated with the Ge nanowires are actually located in the underlying SiO_2 interface, as has been observed in some carbon nanotube field effect devices.[25] In such a situation, the organic passivation layer provides a tunnel barrier isolating carriers in the nanowire from the traps in the gate oxide, which would also result in reduced current relaxation kinetics.

Field Effect Decay Kinetics Determined by Sinusoidal Gate Voltage Sweeps with Varying Frequency. By comparing τ_i measured in Figures 4, 7, and 8 for the unetched, etched, and monolayer-treated nanowires, the characteristic relaxation times increase ($V_g > 0$) with reduced surface oxidation. Another approach for characterizing relaxation time distributions of slow surface states introduced by Kingston and McWhorter[21] employs sweeping the gate voltage as a sinusoidal wave with variable frequency. Figure 9A shows the source−drain current of a Ge nanowire device with constant source−drain voltage (1 V) in response to a ±4 V amplitude gate voltage applied at a frequency of $\omega = 25$ mHz. The data in Figure 9B compare the maximum change in source−drain current versus the frequency of the sinusoidal gate potential sweep, over the frequency range

TABLE 1: Average Carrier Mobilities, Resistivities, and Carrier Concentrations Determined from *IV* Measurements of Several Devices with Nanowires with Different Surface Treatment

surface	g_m (nS)[b]	μ_s (cm^2/Vs)	ρ (Ω cm)	n_{h^+} (10^{19} cm^{-3})[a]
oxidized	0.016	0.01	17	3.6
etched	0.46	0.67	1.54	0.6
isoprene	1.4	2.01	0.23	1.4

[a] n_{h^+} was estimated assuming that $n_{h^+} > n_{e^-}$, using the relationship $\rho \approx (q\mu_s n_{h^+})$. [b] Transconductance, $g_m = dI_{SD}/dV_{GS}$, measured at $V_{GS} = 1$ V.

from 1 to 1000 mHz, for devices prepared from nanowires with different surface chemistry. The data are plotted as the relative response $R(\omega)$, which is the peak-to-peak conductance change at the frequency ω normalized to the peak-to-peak conductance change measured at $\omega = 1000$ mHz. Surface traps with slow capture times cannot respond to the applied gate at high frequency; i.e., if the sweep rate is faster than $\sim\tau_i$ then the current will not decay and $R(\omega) \approx 1$. Oxidized nanowires exhibit a pronounced reduction in peak-to-peak source−drain current change ($R(\omega) < 1$) at the lower frequencies compared to etched nanowires and monolayer-coated nanowires. This trend follows expectations based on the relaxation time distribution data in Figures 4, 7, and 8, indicating that the monolayer-passivated nanowires exhibit the longest τ_i. The data in Figure 9B furthermore illustrate the reproducibility in surface passivation with different wires with hexyl surface termination showing the same long relaxation times relative to the unetched and etched nanowires. Although the range of gate voltage frequencies investigated here is relatively narrow due to experimental limitations, the observed frequency dependence agrees with measurements on bulk Ge samples by Kingston and McWhorter, who observed a more pronounced reduction in $R(\omega)$ at lower frequencies for oxidized surfaces in a wet environment compared to "clean" surfaces.[21]

Discussion

The electrical data indicate that organic monolayer passivation has a large influence on the electrical transport properties. As summarized in Table 1, the transconductance ($g_m = dI_{SD}/dV_{GS}$) increases significantly with passivation, from 0.016 nS for unpassivated nanowires to 1.4 nS. Using the measured values of g_m, the carrier mobility μ_s can be estimated:[26]

$$\mu_s = \left(\frac{dI_{sd}}{dV_G}\right)\left(\frac{L^2}{C}\right)\left(\frac{1}{V_{sd}}\right) \tag{2}$$

where V_{sd} is the applied source−drain voltage and L is the electrode spacing. Neglecting the influence of surface states, the capacitance C for a nanowire device gated from the bottom of the substrate is[13,27]

$$C = 2\pi\epsilon\epsilon_0 L\left(\cosh^{-1}\left(\frac{d+2h}{d}\right)\right)^{-1} \tag{3}$$

with ϵ as the dielectric constant of the SiO_2 layer of thickness h, and d, the nanowire diameter. For $h = 100$ nm and $d = 30$ nm, the Ge nanowire device capacitance is ~0.4 fF. As shown in Table 1, the carrier mobilities calculated from the measured values of dI_{sd}/dV_G ranged from 0.01 cm^2/Vs for unetched oxidized nanowires to 4.0 cm^2/Vs for isoprene-passivated nanowires.

The mobility values in Table 1 for passivated nanowires are nearly 2 orders of magnitude greater than those of nanowires

with untreated oxide-coated surfaces. However, the estimated carrier mobilities in the Ge nanowires are orders of magnitude lower than the "ideal" hole mobility in bulk Ge (1820 cm^2/V s), and furthermore, the calculated mobilities are much lower even than those theoretically predicted based on diffuse scattering at the surface.[28] This is consistent with the observation that the surface trap levels are not completely eliminated from the nanowire devices upon monolayer passivation (i.e., the passivated nanowires still exhibit hysteresis and time-dependent relaxation of the field enhanced (and reduced) source−drain currents). Nonetheless, it should be noted that the calculated mobility values represent *lower bounds* to the actual mobilities. Surface states on the nanowire, as well as in the underlying SiO_2 dielectric layer, decrease the electrical coupling between the gate and the nanowire and give rise to a series capacitance that is lower than the value calculated using eq 3.

We have not discussed possible effects of the finite size of the nanowires on their transport properties. Negative surface charge gives rise to the p-type field effect on bulk Ge as a result of upward band bending and hole accumulation at the semiconductor surface. A nanowire, however, is very small compared to the typical space charge region in a bulk semiconductor (∼100 nm), and band bending from the nanowire core to the surface is unlikely. Nonetheless, a negative surface charge will shift the Fermi level down across the entire nanowire with respect to the conduction band and valence band levels, thus increasing the number of holes available for transport. These holes will be delocalized through the entire nanowire core, even though the hole accumulation would be considered a "surface"-related phenomenon in bulk semiconductors. The nanoscale size of the nanowires could also have a more fundamental influence on the electrical transport by inducing new surface conductance channels for carrier transport. A recent semiclassical theoretical investigation by Sundaram and Mitzel[29] of surface scattering effects on nanowire transport showed significant departure from bulk values for nanowires as large as 100−300 nm in diameter, an order of magnitude larger than the Ge nanowires of interest in our work. Recently, Kobayashi[30] presented a more explicit illustration of the significance of surface effects in a theoretical treatment of conductance in Si nanowires with diameters ranging from 3−4 nm. The nanowire model in his work was based on a hexagonal nanowire cross section which exhibited highly inhomogeneous current distributions with localized conductance channels at the edges of the nanowire cross section. Although the nanowires used to fabricate field effect devices studied in this work have slightly larger diameters than the dimensions considered by Kobayashi, his theoretical work nevertheless underlines the potential importance of finite size and surface effects on electron transport through semiconductor nanowires.

Conclusions

Chemically grown intrinsic Ge nanowires exhibit a p-type field effect, which apparently results from negative surface charges that accumulate on the nanowire surface in interband trap levels associated with surface oxide species. The surface traps give rise to gate sweep hysteresis in the source−drain current and time-dependent relaxation of the field effect. Field effect relaxation measured from oxidized nanowires occurs over the course of hundred of seconds, whereas monolayer-passivated surfaces exhibit much longer relaxation times on the order of 10^4 s. Furthermore, the magnitude of the current relaxation is much greater for unpassivated nanowires than those coated with organic monolayers. Monolayer passivation reduces the number of slow surface states on the nanowires, ultimately resulting in transconductance values that are 2 orders of magnitude higher than those of bare oxidized nanowires. Nonetheless, slow surface states were not entirely eliminated with monolayer passivation, possibly due to the additional presence of surface traps in the underlying gate oxide layer. Surface states will most certainly play an influential role in the device performance of future nanowire electronics.

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