# Temperature Dependence of the Field Effect Mobility of Solution-Grown Germanium Nanowires

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The temperature dependence of the field effect mobility was measured for solution-grown single-crystal Ge nanowires. The nanowires were synthesized in hexane from diphenylgermane by the supercritical fluid−liquid−solid process using gold nanocrystals as seeds. The nanowires were chemically treated with isoprene to passivate their surfaces. The electrical properties of individual nanowires were then measured by depositing them on a Si substrate, followed by electrical connection with Pt wires using focused ion beam assisted chemical vapor deposition. The nanowires were positioned over TaN or Au electrodes covered with $ZrO_2$ dielectric that were used as gates to apply external potentials to modulate the conductance. Negative gate potentials increased the Ge nanowire conductance, characteristic of a p-type semiconductor. The temperature-dependent source/drain current−voltage measurements under applied gate potential revealed that the field effect mobility increased with increasing temperature, indicating that the carrier mobility through the nanowire is probably dominated either by a hopping mechanism or by trapped charges in fast surface states.

## Introduction

Semiconductor nanowires have been explored as a technology platform for a variety of nanodevices such as field effect transistors (FETs),[1,2] p−n diodes,[3,4] memory elements,[5] logic gates,[6] and chemical sensors.[7] Their solution-processability, high surface area-to-volume ratios, and the potential for cheap large-scale production and integration with silicon microelectronics or organic electronic materials on alternative plastic and glass substrates makes them particularly interesting new materials. However, despite a few demonstrated devices with the expected performance characteristics,[1,2,8,9] there are many questions about the fundamental electrical transport properties of chemically grown semiconductor nanowires: for example, what is the nature of electrical transport through the nanowire and how is it influenced by the nanowire surface chemistry? In the case of Ge nanowires, the transport properties have been very sensitive to surface chemistry, with hysteresis in gate potential scans along with time-dependent decay in gate response due to the presence of slow surface states.[10−12]

Here, we study the temperature dependence of the electrical conductivity of individual Ge nanowires synthesized in organic solvents and the influence of applied external fields (i.e., electrical gating). The nanowires are passivated with an organic monolayer and are not intentionally doped during or after the synthesis. For electrical measurements, the nanowires were deposited on substrates prepatterned with TaN or Au gate electrodes covered with $ZrO_2$ as a gate dielectric. Individual nanowires were electrically connected by depositing Pt (source/drain) contacts using focused ion beam (FIB) assisted chemical vapor deposition. The nanowires exhibited a gate response in their conductivity; however, the nanowires behave like gated resistors as opposed to transistors. There was no saturation observed in the source/drain IV curves, and the currents could only be modulated by about a factor of 2 under reasonable gate bias (<3 V). This behavior is consistent with the fact that the source/drains are not doped and the Pt/Ge contacts are ohmic—there is no potential barrier across the nanowire that can be modulated by the gate electrode. Typical (field effect) carrier mobilities measured at room temperature were on the order of ~1 $cm^2/V$ s, but were observed to be an order of magnitude or two lower than this in some wires produced in the same synthetic batch. The carrier mobility increased with increasing temperature, indicating that electrical transport is probably dominated by either hopping or charge trapping in fast surface states.

## Experimental Details

**Ge Nanowire Synthesis.** Crystalline Ge nanowires were synthesized using a supercritical fluid−liquid−solid (SFLS) process[10,11,13−15] in a continuously stirred 250 mL PARR reactor. This procedure yields ~1 g of crystalline Ge nanowires in a single reaction, with very little particulate byproduct. Briefly, anhydrous hexane with 34.8 mM diphenylgermane (DPG, Geleste) and 3 nm diameter dodecanethiol-coated gold nanocrystals were continuously fed into the reactor at the molar ratio of Au/Ge 1:1200 at 380 °C and 800 psi. The Au nanocrystals were prepared by arrested precipitation as described in the literature.[16,17] The flow rate for the reaction was 7 mL/min, giving a residence time of 35 min. The total volume of hexane, DPG, and Au nanocrystals used were 500 mL, 3.25 mL, and 1.25 mL, respectively. Before removing the nanowires from the reactor, the Ge nanowires were passivated with isoprene: The reactor was cooled to 250 °C and the pressure was increased to 1100 psi with the addition of hexane; then 25 mL of isoprene was added to the reactor, which increased the pressure to 2300 psi while the temperature was maintained at 250 °C. The reactor was then cooled to 145 °C, flushed with hexane at 5 mL/min

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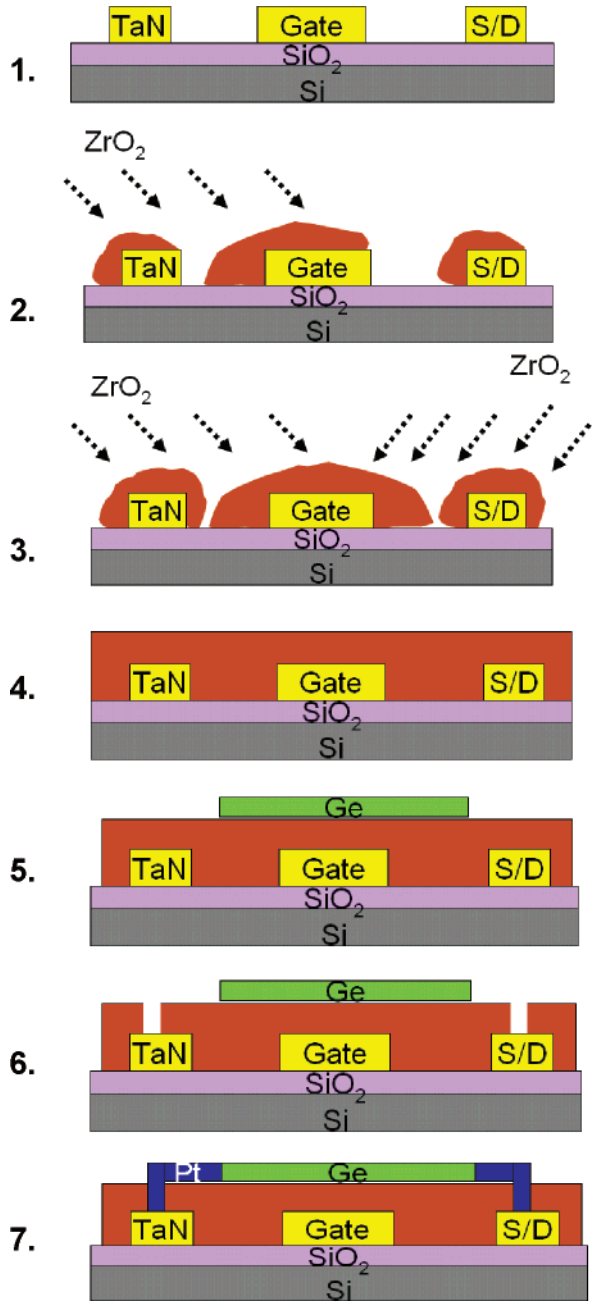
**SCHEME 1: TaN/$ZrO_2$-Gated Ge Nanowire FET Fabrication**[a]

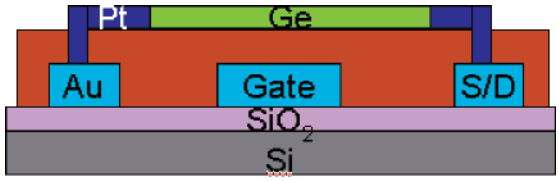



[a] 1. Photolithographically defined TaN source-drain and gate. 2, 3, 4. $ZrO_2$ ebeam deposition at +30°, −30°, and normal to the target. 5. Drop cast nanowires onto substrate. 6. Ion mill/etch hole in the $ZrO_2$ to the TaN source-drain. 7. Deposit Pt by FIB to connect TaN source-drain to the Ge nanowire.

for 25 min, and then further cooled to 75 °C and flushed again with hexane at 5 mL/min for 10 min. The reactor was finally cooled to room temperature, and the wires were removed from the reactor. The Ge nanowires ranged in diameter from 10 to 60 nm with predominantly a ⟨110⟩ growth direction[18] and exhibited very few extended defects.

**Nanowire FET Fabrication.** Two different device configurations were fabricated and tested. In one configuration, TaN was used as a metal gate, and in another Au was used as the gate metal. Zirconia ($ZrO_2$) was applied as the gate dielectric in each case. Ge nanowires were then drop cast from a toluene dispersion onto the substrate and electrically connected to the underlying metal source/drain contacts by a "dig-depo" process

**SCHEME 2: Au/$ZrO_2$-Gated Ge Nanowire FET**[a]




[a] The device is made using the same fabrication steps as the TaN-gated device, except that the Au gate and source-drain structures are defined using electron beam lithography and the Au was deposited by thermal evaporation.

using an FEI dual FIB/SEM tool. The fabrication procedure is illustrated in Scheme 1.

**TaN-Gated Device.** A 310−350 nm layer of tantalum nitride (TaN) was deposited using a DC magnetron sputtering tool (Kurt J. Lesker) onto a silicon substrate with a 300 nm thick oxide. The process pressure was 10 mTorr, and the sputtering time was 5 min. A 1.5 $\mu$m layer of AZ5209 photoresist was then spun onto the TaN surface followed by a 90 °C, 90 s post bake. The substrate was patterned using a Karl Suss MA4 mask aligner photolithography system and then etched using a batch-top reactive ion etcher (Plasma therm, 6" RIE MF) for 1 min using a $CF_4$ etch at 50 sccm followed by a 4 min $Cl_2$ etch at 10 sccm. The etch conditions were 150 W and 50 mTorr total pressure. The remaining photoresist was removed with acetone.

**Au-Gated Device (Scheme 2).** A 400 nm layer of Zep 520 positive resist was spun on a silicon substrate with a 165 nm thick oxide and patterned in a JEOL JBX-6000FS/E electron beam lithography system. The patterned substrate was developed using ZED N-50 developer and then metallized by evaporating 30 nm Au on top of a 3 nm Cr adhesion layer using a Denton DV502 vacuum chamber evaporator. The excess metal covering the resist was lifted off by sonicating in acetone followed by an isopropyl alcohol rinse.

**Dielectric Deposition and Ge Nanowire/Pt Contact Fabrication.** The dielectric deposition and contact patterning processes were the same for both TaN and Au gate device configurations. $ZrO_2$ was used as the gate dielectric. The source-drain bond pads were protected with nail polish (Revlon clear top coat). $ZrO_2$ was deposited using a three-step shadow evaporation technique on an Edwards Auto 500 Magnetron Sputtering System. A total of 30−40 nm of $ZrO_2$ (Cerac Inc.) was deposited at three different angles (+30°, −30°, and normal to the target) for a total dielectric thickness of 120∼160 nm. After the $ZrO_2$ was deposited, the nail polish was removed with acetone to expose the bond pads.

Germanium nanowires were then drop cast from toluene onto the substrate. The substrate coverage was about 2 nanowires per 100 $\mu m^2$. If the nanowire deposition step did not yield nanowires with the appropriate orientation relative to the TaN pattern, the chip was sonicated in toluene and then acetone for 2−3 min to remove the nanowires. Nanowires were then redeposited on the substrate. The source and drain contact pad structures were located below the $ZrO_2$ layer on the same plane as the gate electrode, making it necessary to etch a hole (1∼2 $\mu$m square) through the dielectric to reach the source-drain metal. This was done using the ion milling function on the FIB tool, which removed the $ZrO_2$ dielectric by $Ga^+$ bombardment. A 1.5 $\mu$m by 1.5 $\mu$m hole was etched into the oxide to expose the source-drain metal electrode. The hole was then filled with Pt by ion beam assisted chemical vapor deposition (CVD) on the FEI xPDB (Dual Beam) FIB/SEM tool. The ion beam was held at 30 kV for both the etching/milling and Pt deposition, with Pt write currents of 30−35 pA for the Au structures and

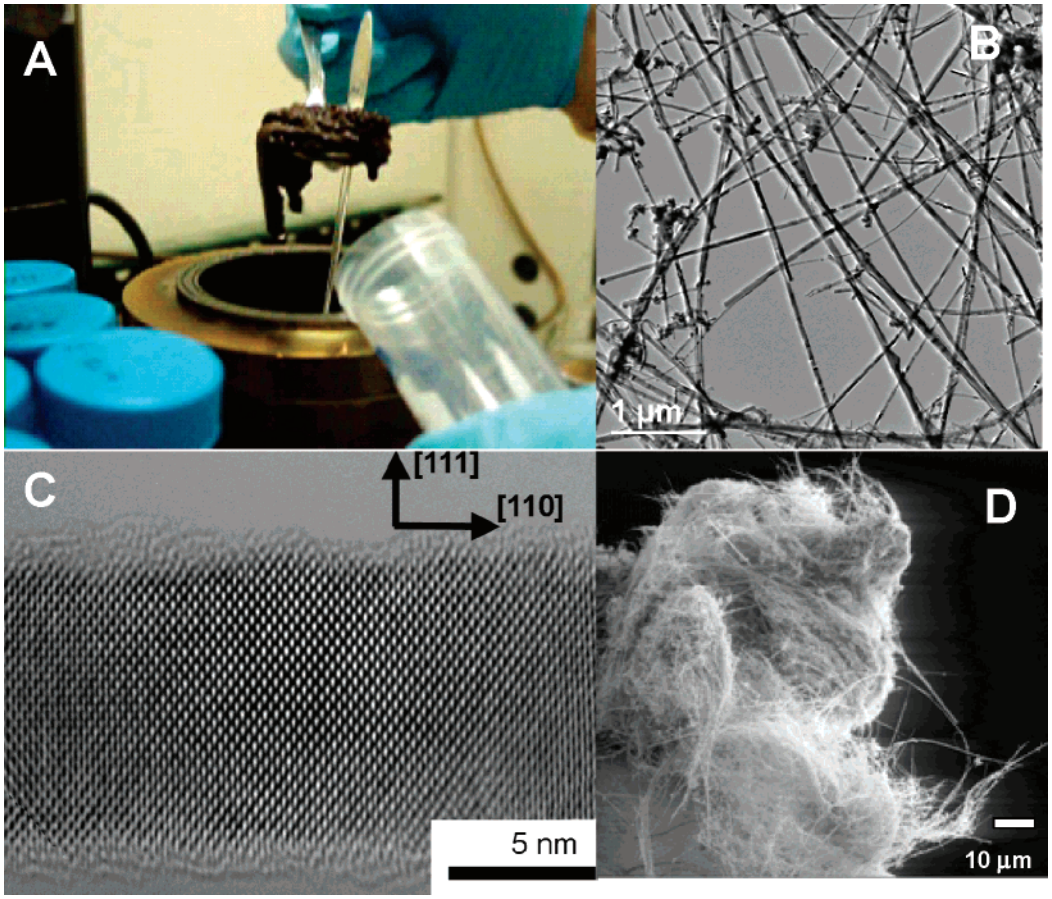



**Figure 1.** SFLS-grown Ge nanowires synthesized in a 250 mL Parr reactor. (A) Photograph of ~500 mg of isoprene-treated Ge nanowires extracted by a spoon from the reactor. (B) TEM image of the nanowire product as-produced from the reactor without further purification. (C) TEM image of a nanowire showing the internal crystallinity and the [110] growth direction. (D) SEM image of the Ge nanowire product, as extracted from the reactor, revealing a wool-like morphology.

50−55 pA for the TaN structures. A line of Pt was deposited to link the Pt contact to the Ge nanowire as shown in Scheme 1.

**Characterization and Testing.** Transmission electron microscopy (TEM) images were obtained using a JEOL 2010F equipped with a field emission gun operated at 200 kV. Nanowires were drop cast onto lacey carbon-coated copper TEM grids for imaging. Devices were imaged by scanning electron microscopy (SEM) on a LEO 1530 SEM equipped with a GEMINI field emission gun operated at 3 kV. $ZrO_2$ film thicknesses were measured using a Dektak 6M Stylus Profiler (Veeco Instruments).

Current−voltage (IV) measurements were obtained at temperatures ranging from 297 to 493 K using an Agilent femtoammeter semiconductor analyzer in a light-shielded, nitrogen-purged chamber with a temperature-controlled sample chuck. Nanowire photoconductivity was measured with light excitation from an unfiltered Novacure 2100 UV light source with spectral illumination across the visible wavelengths with peak excitation wavelengths at 250, 365, 410, 440, 550, and 580 nm. The light intensity was measured using a Newport Optical Power Meter (Model 1830C).

## Results and Discussion

Figure 1 shows the Ge nanowire product obtained by the SFLS process from a 250 mL Parr reactor. The nanowires were synthesized using diphenylgermane as the Ge reactant, dodecanethiol-capped Au nanocrystals as the crystallization seeds, and hexane as the solvent. By pressurizing the reactor above the critical point of hexane, reaction temperatures exceeding the Au:Ge eutectic at ~360°C can be reached in a solution-phase reaction environment. The SFLS process has the advantage of scalability over gas-phase processes such as CVD. Unlike CVD, which is a batch synthetic process with very low production rates since it is limited to growth off substrate surfaces, SFLS (and solution methods in general) is a homogeneous reaction process with very high precursor and seed metal concentrations and the potential for kg/day reactions in scaled reactors. The nanowires are of very high quality. The reaction produces very little particulate byproduct, as revealed by TEM and SEM imaging of the product obtained from the reactor (Figure 1B,D). The nanowires have extremely high aspect ratios, greater than 1000, and reach over 10 $\mu$m in length. They are crystalline and grow primarily in the ⟨110⟩ direction, although some wires in the reaction (~10%) exhibit the ⟨111⟩ or ⟨211⟩ growth directions. Unlike many semiconductor nanowires grown by CVD-VLS, the SFLS-grown nanowires do not exhibit significant changes in thickness along their length, as sidewall Ge deposition does not occur in the SFLS process. The nanowires exhibit nanometer-scale surface roughness, but almost no surface oxidation with isoprene surface treatment.[11] The isoprene treatment is necessary to minimize the influence of slow surface states on the transport properties, as described previously by our group.[10,11] Figure 2a shows another TEM image of a Ge nanowire with the ⟨110⟩ growth direction.

The Ge nanowires are relatively easy to disperse in organic solvents with mild, brief sonication. The nanowires can then be electrically contacted individually by drop-casting on sub-

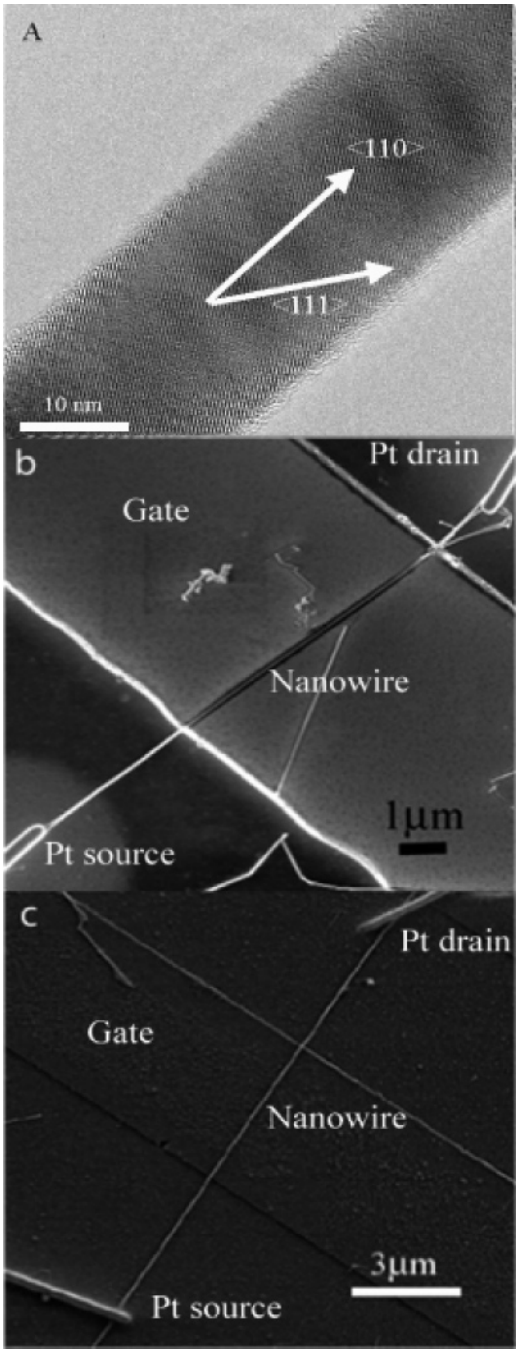



**Figure 2.** (a) TEM image of a Ge nanowire with ⟨110⟩-growth direction and SEM images of Ge nanowires gated with (b) TaN and (c) Au. Both devices have a $ZrO_2$ dielectric layer separating the nanowire from the metal gates. The nanowire diameters are (b) 80 nm and (c) 64 nm. The nanowires are contacted with Pt lines with source-drain separations of (b) 12.3 $\mu$m and (c) 14.6 $\mu$m. The active channel length of the wire spanning the gate electrodes are (b) 7.2 $\mu$m and (c) 5.0 $\mu$m.

strates pre-patterned with Au or TaN contact pad and gate electrodes. After drop-casting the Ge nanowires, Pt "local contacts" were deposited using a dual-beam FIB/SEM tool and a "dig-depo" process to connect the nanowires to the Au or TaN electrodes as described above. Figures 2b and 2c show SEM images of a TaN-gated wire and a Au-gated nanowire. In both configurations, the gate electrodes do not overlap with the Pt source/drain metal contacts.

**Ge Nanowire Field Effect Response.** Figure 3a shows room temperature IV curves for a TaN-gated Ge nanowire with Pt source and drain contacts. The Pt-contacted nanowires exhibit

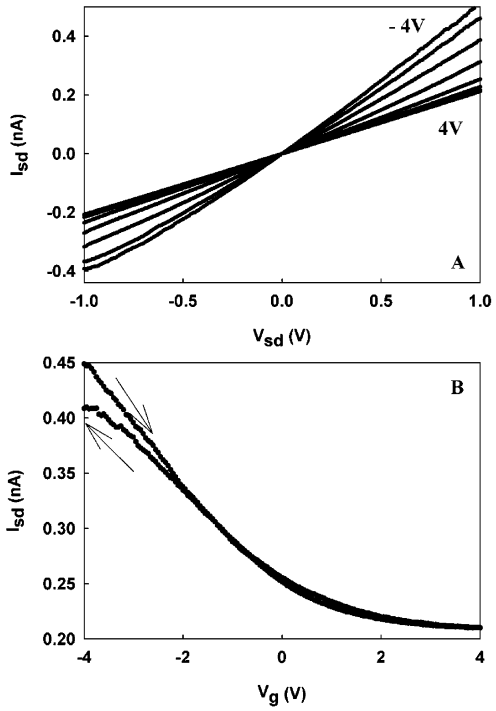



**Figure 3.** Room temperature (A) source-drain IV curves and (B) source-drain current as a function of gate potential ($V_{sd}$ = 1 V) for a TaN/$ZrO_2$-gated Ge nanowire. The curves in part A correspond to source-drain IV measurements as the gate potential was scanned from −4 to 4 V in 1 V increments. The curves in part B correspond to forward (→) and reverse (←) gate potential scans (0.5 V/s) of the source-drain current. The Pt contacts were separated by 11.4 $\mu$m, the nanowire diameter was 56 nm, the $ZrO_2$ dielectric thickness was 116 nm, and the active channel length was 8.3 $\mu$m.

ohmic IV curves with low contact resistance relative to the nanowire resistance as studied in detail in ref 19. The nanowire was gated with an "inline" TaN gate covered by 116 nm of $ZrO_2$ as shown in Figure 2b. The nanowire conductance increased when negative gate voltages were applied. Positive gate potentials decreased the conductivity until reaching a positive threshold voltage where the gate potential had little effect on the source-drain current. This kind of gate response is characteristic of a p-type semiconductor, as previously reported by our group for isoprene-treated SFLS-grown Ge nanowires gated by a Pt/$SiO_2$ gate stack.[10,11] Note that there was very little hysteresis in the gate sweeps, indicating that the nanowires are reasonably well-passivated with isoprene and that slow surface states are minimized on these nanowires.[10] The metal/dielectric/nanowire interface can also be a source for surface states, and it should be noted that the TaN/$ZrO_2$-gated Ge nanowires exhibited less hysteresis than previously observed by our group[10] from Pt/$SiO_2$-gated Ge nanowires, indicating an overall lower surface state concentration in the TaN/$ZrO_2$-gated isoprene-treated Ge nanowire structures.

In Figure 3A, the source-drain IV curves do not saturate at high source-drain bias and the IV curves are nearly linear under the entire ±4 V range of source-drain potential. (Higher source-drain potentials were avoided due to device degradation.) The ohmic Pt/Ge nanowire contacts are consistent with the alignment of the Pt Fermi level with the Ge conduction and valence bands. The work function of Pt is 5.6 eV, and the Ge electron affinity is 4.0 eV (which corresponds to the conduction band energy). Given that the band gap of Ge is 0.67 eV, the Pt Fermi level is well below the valence band edge of the Ge nanowire, which means there is no energetic barrier to hole transport from the

contact into the p-type nanowire. The Pt-contacted Ge nanowire is behaving as a gated resistor as opposed to a true field effect transistor.

The "threshold voltage", $V_{th}$, of the gate required to turn "off" the current is positive. By a linear extrapolation of $I_{sd}$ versus $V_g$ from the region of "high" current (at negative gate potentials) to regions of "low" currents (~210 pA at $V_g = 3$ V), $V_{th}$ was found to be approximately 0.66 V. The subthreshold swing ($\{-dV_g\}/\{d \log I_{sd}\}$ in the linear "high" current range) determined for the nanowire in Figure 3B is 6.7 V per decade, about 2 orders of magnitude worse than the theoretical limit for a Si CMOS transistor (60 mV/decade),[20] which indicates that the nanowire is relatively unresponsive to the gate. The relatively poor gate response of the device is due in part to the fact that there is no potential barrier across the length of the nanowire that can be modulated by the gate potential.

**Ge Nanowire Field Effect Mobility.** The field effect mobility $\mu$ of the carriers in the Ge nanowires was estimated from gate sweeps of the source-drain current at a fixed source-drain bias. Using a conventional model, $\mu$ relates to the transconductance ($g_m$) as[10]

$$g_m = \frac{dI_{sd}}{dV_g} = \frac{\mu C}{L^2} V_{sd} \quad (1)$$

$L$ is the channel length. Assuming the nanowire to be a cylinder, the capacitance between the gate and the nanowire, $C$, depends on the dielectric constant of the gate material ($\epsilon_{ZrO_2}$), the dielectric thickness ($h$), and the nanowire diameter $d$:[1]

$$C = \frac{2\pi\epsilon_0\epsilon_{ZrO_2} L}{\ln(4h/d)} \quad (2)$$

$\epsilon_0$ is the vacuum permittivity ($8.85 \times 10^{-14}$ F/cm). Plugging $\epsilon_{ZrO_2} = 23$ into eq 2, and the appropriate device dimensions, the nanowire structure measured in Figure 3 has $C = 5$ fF. $\mu$ estimated from $g_m$ of the "on" state in Figure 3 ($g_m = 0.056$ nS) is 0.008 cm$^2$/V s, which is several orders of magnitude lower than the bulk hole mobility in Ge. Also note that this value of $\mu$ is significantly lower than the hole mobilities measured for isoprene-treated Ge nanowires in ref 10. However, the mobility was found to vary significantly from wire to wire, even when produced in the same synthetic batch, and was found to be a couple orders of magnitude higher for most devices. Figure 4 shows the IV curves and transconductance plots for a different Ge nanowire, which shows p-type behavior with a room temperature resistivity ($V_g = 0$) of 0.59 Ω cm and $\mu = 1.47$ cm$^2$/V s. The highest mobilities measured for individual Ge nanowires were on the order of ~2 cm$^2$/V s, which is consistent with previous measurements.[10]

Figure 5 shows transconductance plots at a fixed $V_{sd}$ of 1 V as a function of temperature from 293 to 493K. The current through the nanowire (i.e., $I_{sd}$ ($V_g = 0$)) and the transconductance (i.e., the slope of $I_{sd}$ versus $V_g$ (at $V_g < 0$)) both increased with increasing temperature. Figure 6A shows the temperature dependence of the nanowire resistivity $\rho$, measured with $V_g = 0$. ln $\rho$ increased linearly with $1/T$, characteristic of an activated process, where $\rho = \rho_o \exp(E_a/kT)$. The activation energy $E_a$, determined from Figure 6A, was 0.19 eV. The resistivity of a p-type semiconductor depends on both the active carrier concentration $p$ (#/cm$^3$), and the carrier mobility $\mu$ (cm$^2$/V s)

$$\rho = \frac{1}{pe\mu} \quad (3)$$

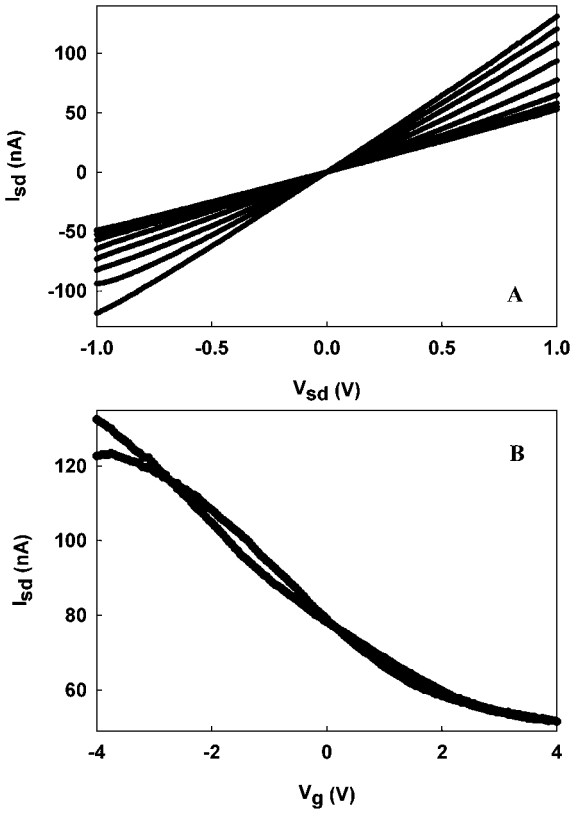



**Figure 4.** A TaN/$ZrO_2$-gated Ge nanowire: room temperature (A) source-drain IV curves with the gate potential scanned from −4 to 4 V gate in 1 V increments, (B) source-drain current at constant source-drain bias of 1 V as the gate potential was scanned from −4 to 4 V back to −4 V ($V_g$ scan rate of ~0.5 V/s). The contacts were separated by 12.3 $\mu$m, the nanowire diameter was 80 nm, and the active channel length was 7.15 $\mu$m.

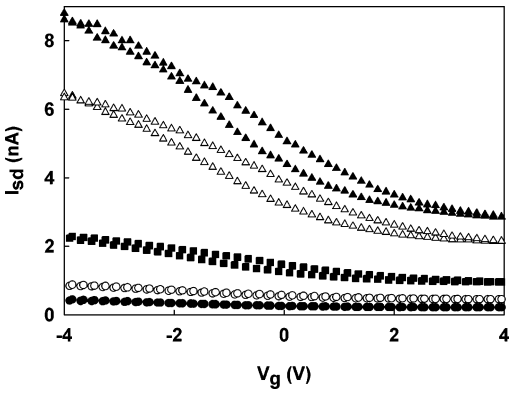



**Figure 5.** Source-drain current plotted as a function of gate voltage for a TaN/$ZrO_2$-gated Ge nanowire measured at different temperatures: (●) 295, (○) 333, (■) 393, (△) 453, (▲) 473 K. In this device, the Pt contacts were separated by 11.4 $\mu$m, the nanowire diameter was 56 nm, the $ZrO_2$ dielectric thickness was 116 nm, and the active channel length was 8.3 mm.

where $e$ is the electron charge ($1.6 \times 10^{-19}$ C). When carrier concentration is determined by dopants and not traps, impurities, or defects, the resistivity should decrease at higher temperatures, as is indeed observed. $\mu$ (calculated from $g_m$ in Figure 5 using eqs 1 and 2), however, increased with increasing temperature, which is unexpected for band conduction through a semiconductor, as increased phonon scattering of carriers at higher temperature generally decreases $\mu$. ln $\mu$ versus $T^{-1}$ plotted in Figure 6B shows an Arrhenius dependence of the form $\mu = \mu_0 \exp(-E_{a,\mu}/kT)$, which gives an activation energy $E_{a,\mu} = 0.21$

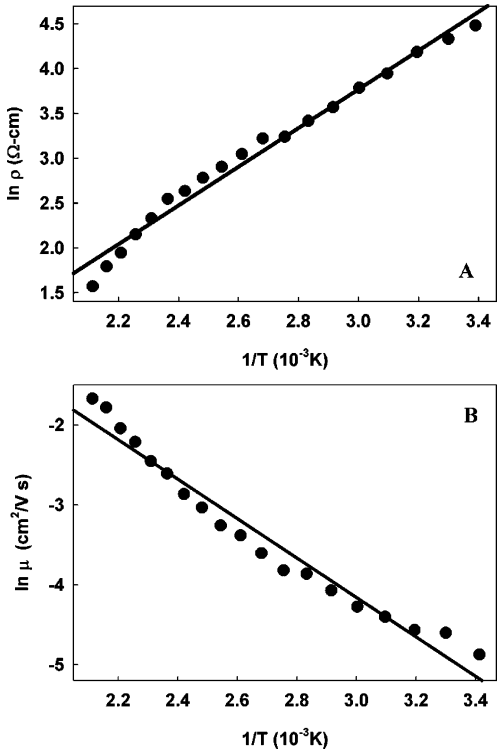



**Figure 6.** (A) $\rho$ and (B) $\mu$ plotted as a function of temperature for a TaN/$ZrO_2$-gated Ge nanowire. $\rho$ was determined from source-drain IV curves with $V_g = 0$. $\mu$ was calculated using eqs 1 and 2 from the data in Figure 3 as described in the text. The nanowire was 56 nm in diameter with an 11.4 $\mu$m separation between Pt contacts, an active channel length of 8.3 $\mu$m, and an 116 nm thick $ZrO_2$ layer. From the slopes of the plots in parts A and B, $E_a = 0.19$ eV and $\rho_o = 0.066$ Ω cm, and $E_{a,\mu} = 0.21$ eV and $\mu_o = 25.6$ $cm^2$/V s.

eV (and the prefactor, $\mu_o = 25.6$ $cm^2$/V s) which is very close in value to $E_a$. This is a strong indication that conductivity through the nanowire is either dominated by a hopping mechanism or by trapped charge in fast surface states that screens the gate potential from the wire.

The nanowire is crystalline, so it is somewhat surprising that the nanowire exhibits a low mobility that increases with temperature. The observed temperature dependence of the mobility could be due to a hopping mechanism for electrical transport. Another explanation for the observed increase in mobility with increased temperature is related to the nanowire surface and the presence of *fast* surface states.[21−23] $\mu$ is actually a "field effect" mobility, which may be different than the carrier mobility in a bulk crystal.[23] The field effect mobility calculated from the transconductance using eqs 1 and 2 do not take into account that the coupling between the electric field and the nanowire can be significantly affected by charges trapped in fast surface states that may influence the actual gate potential applied to the nanowire. These trapped charges could screen the gate potential and reduce the field effect mobility from the actual carrier mobility in the nanowire. It is possible that as the temperature is raised, the surface states might be thermally depopulated, giving rise to the *appearance* of an increased mobility with increased temperature.

**Photoconductivity.** Figure 7 shows the photoresponse of a TaN/$ZrO_2$-gated Ge nanowire illuminated with light with energies greater than the band gap energy. The total current increases by 18% at $V_g = 0$. The transconductance does not change upon illumination, indicating that the carrier mobility is relatively insensitive to light exposure. The photoinduced change in conductivity, $\Delta\sigma$, relates to the rate of optical

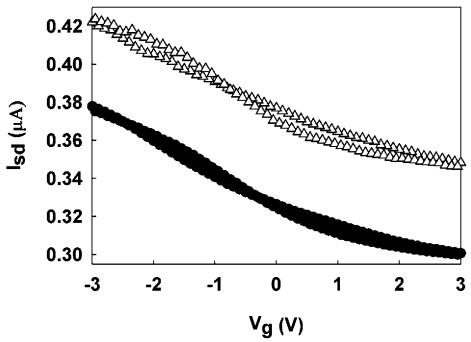



**Figure 7.** Source-drain current ($I_{sd}$) plotted versus gate voltage ($V_g$) for a TaN/$ZrO_2$-gated Ge nanowire under a constant source-drain bias of 1 V before (●) and after (△) exposure to 4.6 $\mu$W of UV and visible light. The active channel length, nanowire diameter, contact separation, and $ZrO_2$ dielectric thickness were 8.4 $\mu$m, 69 nm, 19 $\mu$m, and 340 nm, respectively.

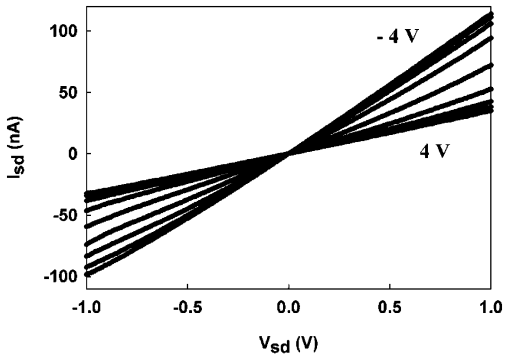



**Figure 8.** Room temperature IV curves for a Au/$ZrO_2$-gated Ge nanowire scanned from −4 to 4 V gate in 1 V increments. For this device, the contacts were separated by 14.6 $\mu$m, the nanowire diameter was 64 nm, the $ZrO_2$ layer was 160 nm thick, and the active channel length was 5.0 $\mu$m.

excitations, $g_{opt}$, and the carrier lifetime $\tau$ (the subscripts n and p refer respectively to electrons and holes):

$$\Delta\sigma = eg_{opt}(\tau_n\mu_n + \tau_p\mu_p) \quad (4)$$

The light absorption event creates an electron and hole that contribute to electrical conduction and increases the conductivity, while not affecting the mobility.

**Dual Gating of Ge Nanowires.** One approach to achieving higher transconductance, which has been applied recently to carbon nanotube devices,[24] has been the use of a dual gate structure consisting of an inline gate and a back gate (silicon substrate). This approach was explored for gated Ge nanowires. Figure 8 shows room temperature source-drain IV curves for a Au/$ZrO_2$-gated Ge nanowire at different Au gate potentials. The Ge nanowire exhibits a p-type gate response with increased currents at more negative $V_g$. From eq 2, with $\epsilon_{ZrO_2} = 23$, $C =$ 2.8 fF, which when using eq 1 and the transconductance extracted from the data in Figure 8 gives a carrier mobility of 1.6 $cm^2$/V s.

Figure 9 shows room temperature Au/$ZrO_2$ gate sweeps of the Ge nanowire source-drain current with an additional applied potential of 5 V, 0 V, or −6 V to the Si substrate. The Si back gate operates not only across the same $ZrO_2$ layer separating the Au electrode from the wire but also the additional thick layer of $SiO_2$. The Au/$ZrO_2$-gated Ge nanowire exhibits more pronounced hysteresis in the transconductance plots than the TaN/$ZrO_2$-gated nanowires. An additional positive potential from the Si substrate did not affect the Au gate response of the

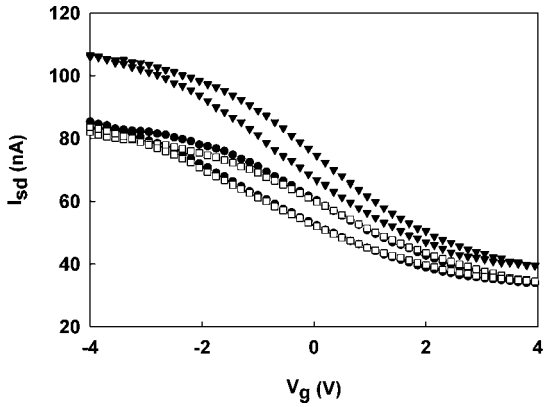



**Figure 9.** Room temperature forward and reverse gate scans of a Au/$ZrO_2$-gated Ge nanowire with a 1 V source-drain bias and an additional gate potential applied from the Si substrate of (●) 5 V, (□) 0 V, and (▼) −6 V. For this device, the contacts were separated by 14.6 $\mu$m, the nanowire diameter was 64 nm, the active channel length was 5 $\mu$m, the $ZrO_2$ thickness was 160 nm, and the $SiO_2$ thickness was 100 nm.

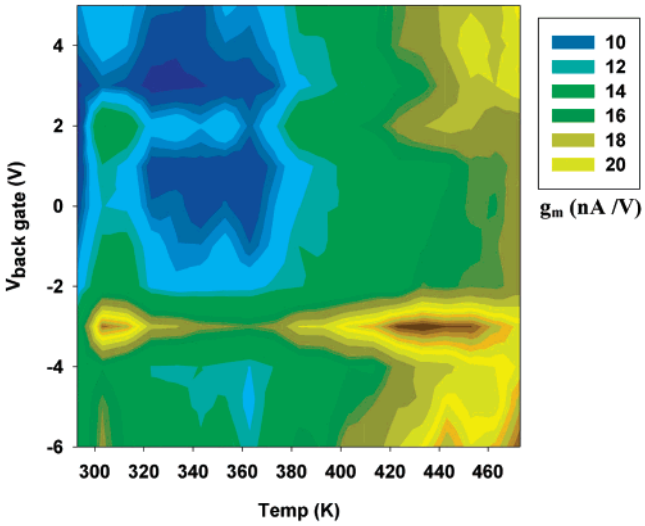



**Figure 10.** Contour plot of the transconductance ($g_m$) of a Au/$ZrO_2$-gated Ge nanowire measured as a function temperature and added Si back gate bias. $g_m$ was determined from gate sweeps of the source-drain current with a fixed $V_{sd} = 1$ V by taking the slope of $I_{sd}$ versus $V_g$ at negative $V_g$.

device; however, an additional negative applied potential increased the transconductance and the conductivity significantly. Figure 10 shows a contour plot of the transconductance of a Au/$ZrO_2$-gated Ge nanowire measured as a function of both temperature and Si back gate potential. The transconductance increased with increasing temperature and increasingly negative Si substrate potential. From eq 1, $g_m \propto \mu C$. Since $C$ does not depend on the temperature, the temperature dependence of $g_m$—i.e., increasing with increasing temperature—most likely is a result of hopping transport or fast surface states. From the contour plot, the transconductance, $g_m$, ranged from $8.3 \times 10^{-9}$ to $2.2 \times 10^{-8}$ A/V and the estimated mobilities ranged from 0.73 to 1.92 $cm^2$/V s. The increase in $g_m$ with increasingly negative Si substrate potentials relates to the relative increase in gate capacitance $C$ due to the thicker dielectric layer.

## Conclusions

The electrical properties of solution-grown single-crystal Ge nanowires that were not intentionally doped were studied. The Pt-contacted Ge nanowires exhibited ohmic IV curves with a p-type gate response. The field effect mobility determined from transconductance measurements were relatively low, ranging from ~2 $cm^2$/V s down to as low as 0.008 $cm^2$/V s for some devices. The temperature dependence of the transconductance revealed an increase in field effect mobility with increasing temperature, which could be consistent with a hopping mechanism for transport or screening of the gate potential by charge trapped in fast surface states. It should be noted that the *slow* surface states identified and studied by us in ref 10 were mostly eliminated in these devices by isoprene surface treatment of the nanowires. The Ge nanowires exhibited photoconductivity with increased conductivity under light excitation, and the nanowire transconductance could be increased by about 75% by applying an additional negative gate potential to the Si substrate.

The low mobility values are really not too surprising considering that the nanowire has a very large surface-to-volume ratio that can provide many scattering and trapping sites for the carriers.[11,13] It is actually well-known that the "surface mobility" of carriers in Ge is significantly less than the bulk carrier mobility.[21,25] Ge as a material is also notorious for having a high concentration of surface states, due to its electrically poor oxide, which can provide additional sources of surface defects, although $ZrO_2$ passivation in some cases has been shown to help eliminate these.[10,11,21] Certainly in the case of Ge nanowires, the surface chemistry and the elimination of *both* fast and slow surface states is critical to good device performance, as it is in Si CMOS devices.

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