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Metallic Single-Crystal CoSi Nanowires via Chemical Vapor Deposition of Single-Source Precursor

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We report the synthesis, structural characterization, and electrical transport properties of free-standing single-crystal CoSi nanowires synthesized via a single-source precursor route. Nanowires with diameters of 10−150 nm and lengths of greater than 10 μm were synthesized through the chemical vapor deposition of $Co(SiCl_3)(CO)_4$ onto silicon substrates that were covered with 1−2 nm thick SiO_2. Transmission electron microscopy confirms the single-crystal structure of the cubic CoSi. X-ray absorption and emission spectroscopy confirm the chemical identity and show the expected metallic nature of CoSi, which is further verified by room-temperature and low-temperature electrical transport measurements of nanowire devices. The average resistivity of CoSi nanowires is found to be about 510 $\mu\Omega$ cm. Our general and rational nanowire synthesis approach will lead to a broad class of silicide nanowires, including those metallic materials that serve as high-quality building blocks for nanoelectronics and magnetic semiconducting $Fe_{1-x}Co_xSi$ suitable for silicon-based spintronics.

Recently, $Fe_{1-x}Co_xSi$ alloys were found to be magnetic semiconductors.[1] These magnetic semiconductor materials are crucial for the realization of spintronics, a growing field which seeks to exploit the spin properties instead of or in addition to charge degrees of freedom in solid-state electronic and photonic devices.[2] Although diluted magnetic semiconductors such as GaMnAs are gaining more attention,[3] less developed spintronics based on silicon and metal silicides[4] would have the advantage of long spin coherence lifetimes in silicon[5] and well developed materials and processing from several decades of silicon microelectronics research. A particularly fruitful approach to nanospintronics is to use single-crystalline one-dimensional (1-D) nanoscale materials with precisely controlled structures and properties[6,7] as high-quality nanoscale building blocks[8−10] following the bottom-up paradigm.[11] Successful synthesis of CoSi nanowires, together with our success in FeSi nanowires,[12] will pave the way for CMOS compatible magnetic semiconducting $Fe_{1-x}Co_xSi$ alloy nanowires toward the exploration of silicon-based nanospintronics.

Moreover, CoSi belongs to a broad class of low-resistivity metallic transition metal silicides that have found great applications as the Ohmic contacts, interconnects, and gates in VLSI and ULSI CMOS processes.[13,14] These "novel" silicide materials enable the contact resistance reduction[15] and gate work function tuning[16] that are crucial to the scaling of MOSFETs down to the nanoelectronic regimes of the 65 and 45 nm technological nodes. For instance, CoSi was exploited as Ohmic contact to *p*-type MOSFETs to show reduced contact resistance[17] compared to other more popular silicides (NiSi and $CoSi_2$) due to the suppression of B dopant diffusion[18] and ternary phase formation.[17,18] Therefore, single-crystal CoSi nanowires are already useful as high-quality metallic nanoscale building blocks for bottom-up assembled nanoelectronics, as integrated Ohmic contacts,[19] interconnects, or cross nanowire gates. Herein, we report the direct chemical synthesis and the structural and physical property investigation of single-crystal free-standing CoSi nanowires prepared through the chemical vapor deposition of the single-source precursor $Co(SiCl_3)(CO)_4$. This represents a general approach to a broad family of transition metal silicide nanowires that are potentially very useful for nanoelectronics and nanospintronics.

Rational synthesis of nanowires usually has two main challenges: the delivery of source materials and the anisotropic crystal growth to form 1-D nanostructures.[8−10,20] For the former, we chose to use chemical vapor deposition (CVD) of single-source precursors (SSPs),[21,22] which are organometallic molecules that comprise all of the elements to be delivered and deposited. Recently, Park and co-workers reported an interesting method of forming the analogous FeSi nanowires by evaporating $FeCl_3$ onto silicon substrates at high temperature (1100 °C).[23] We are attracted by this simple and inexpensive method, but we are concerned that the fact that silicon needs to come from the substrate might mean inflexible control of stoichiometry and inhomogeneous composition along the nanowires. This could pose difficulties for long term exploration of well-controlled nanostructures for nanoelectronics and nanospintronics. SSPs would enable low-temperature delivery of *both the silicon and the metal elements in precise stoichiometries* to the substrate using simple and safe experimental setups,[21,22] giving us better

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control of the reaction and higher quality material growth.[24] We synthesized the organometallic precursor $Co(SiCl_3)(CO)_4$ from commercially available $Co_2(CO)_8$ and $SiHCl_3$ (see eq 1) following a procedure modified from the literature[25,26] and confirmed the identity of the compound.[27]

$$Co_2(CO)_8 + 2SiHCl_3 \rightarrow 2Co(SiCl_3)(CO)_4 + H_2 \quad (1)$$

$Co(SiCl_3)(CO)_4$ is a modestly air- and moisture-stable compound with a reported melting point of 65 °C and thus can be easily sublimed and delivered as a vapor phase CVD precursor. In fact, it was recently employed for successful CVD of cobalt silicide thin films by thermally decomposing this SSP at temperatures between 250 and 450 °C.[28] Our experiments show this SSP readily allows precisely controlled vapor phase delivery of Co and Si in a 1:1 ratio to acquire nanomaterials of CoSi out of the five possible phases[29] of cobalt silicides—Co_3Si (high temperature), α-Co_2Si, β-Co_2Si (high temperature), CoSi, and $CoSi_2$—through the following reaction:[28]

$$2Co(SiCl_3)(CO)_4(g) \rightarrow 2CoSi(s) + 8CO(g) + 3Cl_2(g) \quad (2)$$

For the anisotropic nanowire crystal growth, we have found the simple nanowire growth methods identified in our previous synthesis of FeSi nanowires[12] to be generally applicable to the formation of CoSi nanowires as well. By simply using silicon substrates covered by a thin SiO_2 layer of about 1−2 nm thickness without the intentional use of any metal catalysts, the CVD of the $Co(SiCl_3)(CO)_4$ SSP[30] produced dense nanowires of CoSi in high yields covering entire substrates as revealed by representative scanning electron microscopy (SEM) images[31] (Figure 1a). Nanowires synthesized under our optimized conditions typically have diameters of 20−50 nm and lengths of 10−15 μm. When optimized conditions were not followed, different diameter size regimes (10−150 nm) were observed. The nanowires were never terminated with catalyst caps (Figure 1a, inset). In some experiments, square facets and enlargement of the nanowire diameters were observed at the tips of the nanowires (Figure 1b).

We want to emphasize that no metal catalyst was intentionally employed and observed for the synthesis of CoSi nanowires. The growth mechanism is likely not the traditional vapor liquid solid (VLS) nanowire growth.[8,9,32] Instead, a thin SiO_2 layer on silicon appears to be the key for the formation of nanowires, which is very similar to the growth of FeSi nanowires[12] we discovered. Although using nearly identical procedures for FeSi nanowire synthesis led to CoSi nanowire formation, we performed a thorough investigation of synthesis conditions that included silicon oxide thickness, SSP sublimation temperature, carrier gas flow rate, pressure, and reaction temperature. We found 1−2 nm thick SiO_2 formed by controlled oxidation of freshly HF cleaned silicon substrate using an oxidative "metal etching solution" (30% H_2O_2/37% HCl/H_2O = 1:1:5 v/v) at 70 °C for 20 min led to the most consistent production of straight and smooth nanowires in high yields. This oxide thickness was confirmed by ellipsometry measurements and is in agreement with the general expectation of silicon surface oxidation. Nanowire density, diameter distribution, and morphology suffer when thicker oxides are used. Thin film growth accompanied with sparse nanorods of large diameter dominates when thinner oxides are used. Controlling the delivery rate of SSP to the substrates is also very important to successful CoSi nanowire growth, which is mainly dictated by the SSP sublimation temperature and carrier gas flow rate, and somewhat by the total pressure. We found that the longest, densest, and most uniform

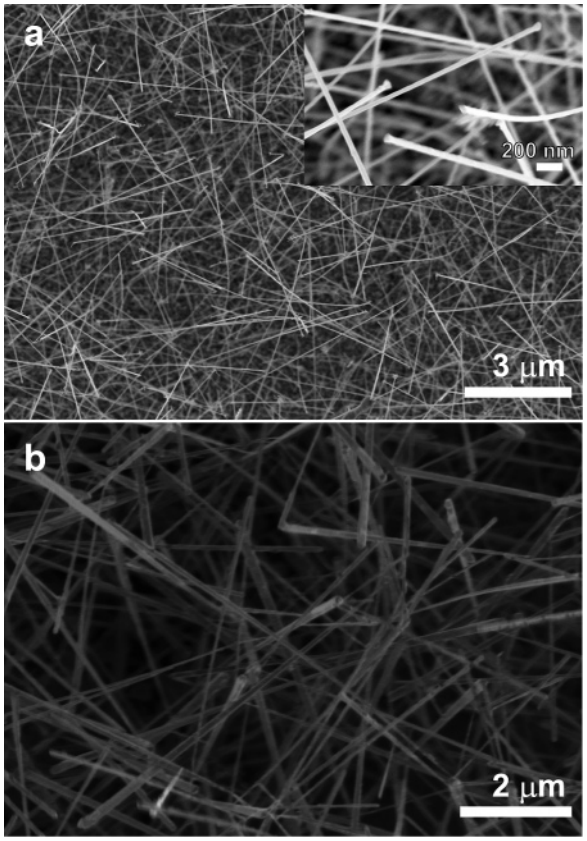

Figure 1. Representative SEM images of CoSi nanowires grown by chemical vapor deposition of the single-source precursor $Co(SiCl_3)(CO)_4$: (a) thin nanowires prepared under optimal conditions and highlight of several tips of these nanowires at higher magnification (inset); (b) thicker nanowires with enlarged faceted wires at the tips.

nanowires were produced when $Co(SiCl_3)(CO)_4$ was sublimed at lower temperatures (~100 °C) and carried by lower flow rates (100 sccm) of the inert Ar gas, both in comparison with the FeSi nanowire synthesis. The reason for this difference is attributed to the higher volatility of the CoSi SSP $Co(SiCl_3)(CO)_4$ (mp 65 °C) as compared to FeSi SSP $Fe(SiCl_3)_2(CO)_4$ (mp 93−96 °C).[25] For example, if identical conditions for FeSi nanowire synthesis are employed, the $Co(SiCl_3)(CO)_4$ precursor will be consumed in 3−5 min to produce dominantly thin films accompanied with a very low yield of low-aspect-ratio nanowires. A lower total pressure (<100 Torr) than the optimal pressure of 200 Torr results primarily in thin film growth. The ability to finely control the silicon oxide thickness on silicon and the SSP delivery rate consistently is crucial to obtaining uniform nanowire diameters and reproducible morphology, which can be obtained with our optimized experimental conditions. We are working on further improving the oxide thickness control by UV irradiation assisted surface oxidation of freshly HF etched Si surfaces.

The chemical structure and the single-crystalline nature of the resulting nanowires were confirmed using powder X-ray diffraction (PXRD) (Figure 2a) and high-resolution transmission electron microscopy (HRTEM)[31] (Figure 2b). All major diffraction peaks that are not from the growth silicon substrate are indexed to the cubic CoSi structure (JCPDS PDF00-008-362), which belongs to the FeSi structure type (space group $P2_13$, Person symbol $cP8$, $Z = 4$)[33] with a lattice constant of 4.43 Å. The two minor unidentified diffraction peaks that are marked with an asterisk do not match any other phases of cobalt silicides or any phases consisting of any combination of cobalt,

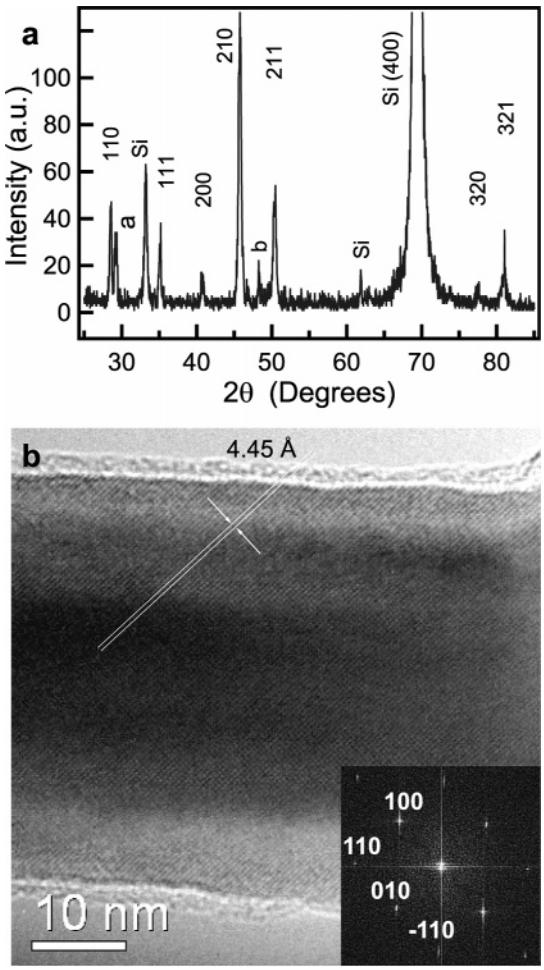

Figure 2. (a) Powder X-ray diffraction pattern from a sample of CoSi nanowires covering the growth substrate. Peaks from CoSi and from silicon substrate are indexed by comparing with standard diffractograms, and two unidentified minor peaks are marked with an asterisk. (b) Representative HRTEM image with the adjacent (100) planes and spacing marked along with the two-dimensional FFT (inset) of CoSi nanowires.

silicon, and oxygen. HRTEM images reveal cubic CoSi lattice fringes for a representative CoSi nanowire along the [100] zone axis (Figure 2b), and the corresponding fast Fourier transformation (FFT) (Figure 2b, inset) can be successfully indexed to a simple cubic lattice. The observed lattice spacing of 4.45 Å for CoSi nanowires matches well with the reported value of 4.43 Å. All nanowires observed under TEM were single-crystalline CoSi structures. This exemplifies the precise and consistent control of nanowire stoichiometry enabled by the SSP approach. All nanowire axes observed using TEM were parallel to the ⟨110⟩ crystal directions. This is the same crystallization habit seen for the FeSi nanowires made using the SSP approach[12] but different from the FeSi nanowires prepared by Park and co-workers.[23] The smooth nanowire surface is covered with a thin (2−3 nm) amorphous silicon oxide layer resulting from surface oxidation of silicides.[34]

The electronic properties of CoSi nanowires were probed by X-ray absorption spectroscopy (XAS) and X-ray emission spectroscopy (XES) (Figure 3).[35] X-ray spectroscopy was collected for CoSi nanowires dispersed on a germanium substrate using the undulator Beamline 8 at the Advanced Light Source (ALS) at Lawrence Berkeley National Laboratory. The XAS spectrum shows the L_3 and L_2 edges of Co at 775 and 790 eV, respectively, in agreement with X-ray spectroscopy

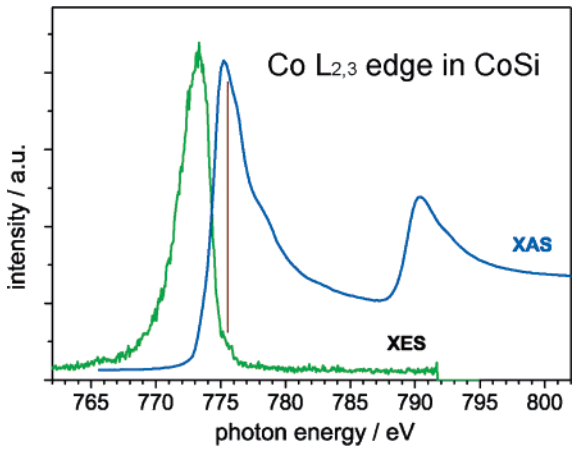

Figure 3. Spectroscopic characterization of CoSi nanowires by X-ray absorption spectroscopy (XAS) and X-ray emission spectroscopy (XES) at the Co $L_{2,3}$ edge. The solid vertical line points to the excitation energy for XES.

results reported for bulk cobalt silicide.[34] The spectrum represents a rather unstructured absorption band which is due to excitations from Co $2p_{3/2,1/2}$ core levels into the empty Co 3d valence-band states. CoSi is a nonmagnetic, metallic material, and the broad absorption band reflects the width of the empty Co 3d states. The somewhat narrower XAS peaks in CoSi, compared with FeSi,[12] qualitatively reflect the smaller hole density in CoSi (higher filling of the 3d shell). The emission spectrum (XES) shown in Figure 3 was excited with the photon energy set at the maximum absorption band (solid vertical line in Figure 3) and stems from transitions out of the Co 3d valence states into the Co $2p_{3/2}$ core holes. As such, the emission spectrum reflects the distribution of occupied Co 3d states below the Fermi energy. Since the upper cutoff of the emission spectrum coincides with the lower cutoff of the absorption spectrum (roughly speaking the half-height points at 774 eV), CoSi is clearly metallic. The Fermi level (E_F), which can be defined as the crossing point of the two spectra, intersects the metallic Co 3d band with a high density of states (DOS). This spectroscopic study also lays the foundation for future element-specific X-ray spectroscopic investigation of nanowires consisting of the alloy $Fe_{1-x}Co_xSi$, a magnetic semiconductor in bulk form.

To investigate the electrical transport properties of the CoSi nanowires produced, we fabricated four (two) terminal devices of CoSi nanowires using e-beam lithography (photolithography) techniques followed by evaporation of Ti/Au electrode.[36] Representative room-temperature electrical transport measurements of a typical CoSi nanowire device show linear current versus voltage (V_{sd}) behavior (Figure 4a) with a resistance of 3.29 kΩ, as determined with the two-probe $I-V$ curve (Figure 4a, red circles). Four-probe measurements allow us to better estimate the resistivity of our nanowires by eliminating contact resistance from the measurement. By comparing the four-probe $I-V$ (Figure 4a, blue crosses) with the two-probe $I-V$ for the same nanowire segment, we determine the additional resistance added by contact to the wires and that imposed by the measurement setup to this representative CoSi nanowire device to be 1.8 kΩ. Through the measurements of several four-probe devices, we found noticeable but not dominating contact resistances ranging from 1 to 5 kΩ. Measurements of resistance (R) as a function of temperature in the range 10−300 K using selected nanowire devices shows that the resistivity decreases monotonically as the temperature decreases, clearly confirming the classical metallic behavior as expected for CoSi (Figure 4b).

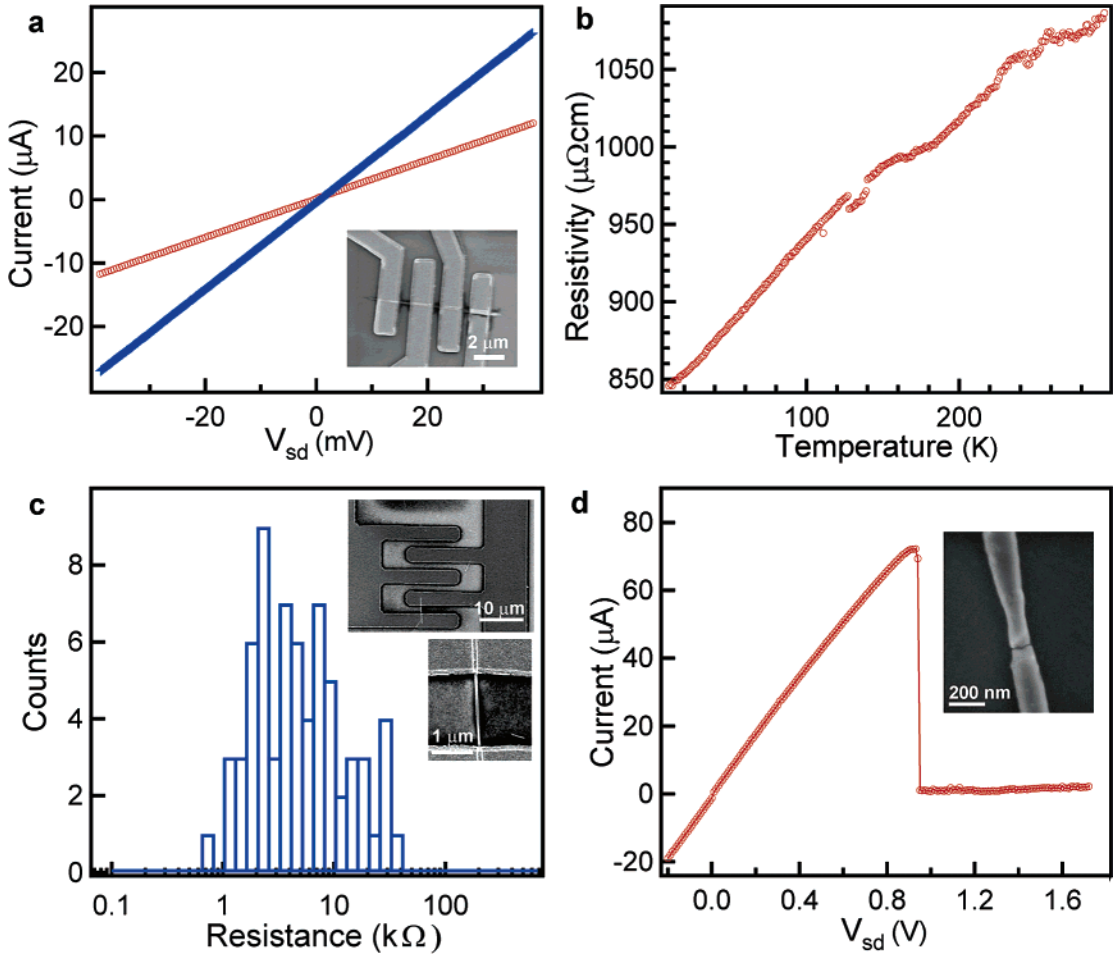

Figure 4. Electrical transport properties of CoSi nanowires: (a) two-probe (red circles) and four-probe (blue crosses) current vs V_{sd} measurements across the middle segment of a typical four-terminal CoSi nanowire device shown in the inset SEM image; (b) resistivity vs temperature for a typical two-terminal device; (c) histogram of the observed resistance for 68 CoSi nanowire devices; (d) current vs V_{sd} recorded for a typical CoSi nanowire device that breaks down at higher voltage and current. (inset) SEM image of the broken nanowire in this particular device after failure.

The nearly linear increase of resistivity up to about 120 K and the slight downward curvature above that is similar in trend to reported bulk CoSi behavior,[37,38] though the saturation at lower T is not as pronounced for our samples.

To acquire a better statistical survey of the transport properties of CoSi nanowires, we employed photolithography methods[39] to produce a large number of addressable devices. The calculated resistance values for a collection of 68 of these two-terminal devices are displayed in a logarithmic histogram (Figure 4c). Deviation from peak resistance is due to the range of nanowire diameters grown, differences in channel lengths from the random orientation of nanowires across the fixed electrode gaps, and a certain probability of multiple wire devices, which is consistent with our large scale device fabrication scheme.[39] We determined the average resistivity of our CoSi nanowires to be 510 $\mu\Omega$ cm using data from 35 single nanowire devices for which diameter, channel length, and single connectivity were established by SEM. This value is within the (surprisingly large) range of room-temperature resistivity values reported for CoSi: 180 $\mu\Omega$ cm for single-crystal CoSi[37] and 2200 $\mu\Omega$ cm for polycrystalline CoSi.[40] When current densities exceed what is allowed for by the heat dissipation through the electrodes, typically under an applied voltage of between 1 and 2 V, the devices burn out as shown by the sudden loss of current in the $I-V$ curve (Figure 4d). Post burnout SEM examination of the failed devices (Figure 4d, inset) shows the evident meltdown mechanism by resistive self-heating. Our nanowire devices are capable of conducting currents between 60 and 100 μA, reaching maximum current densities (J_{max}) typically on the order of 5×10^6 A cm^{-2}, which is comparable to the lithographically defined metal lines currently employed in CMOS processes.[41] This demonstrates the high-quality nature the of single-crystalline metallic CoSi nanowires, making them attractive building blocks for nanoelectronics.

In summary, we have synthesized single-crystalline free-standing CoSi nanowires from single-source precursor Co(SiCl$_3$)(CO)$_4$ using a simple CVD method with no intentional metal catalyst. Physical characterization using X-ray spectroscopy and electrical transport measurements verifies the anticipated metallic properties of the CoSi nanowires and demonstrates the promise of this new CMOS compatible nanoscale building block for nanoelectronics. Our single-source precursor approach utilizing thin SiO_2 on Si for preparing nanowires has now been extended to two transition metal silicides, FeSi and CoSi, which are the basis for synthesizing nanowires of magnetic semiconducting $Fe_{1-x}Co_xSi$ alloys via simultaneous delivery of both SSPs.

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(26) In a typical preparation of $Co(SiCl_3)(CO)_4$, approximately 15 mL of $SiHCl_3$ was added to 3.04 g of dry $Co_2(CO)_8$ placed in a Carius tube and cooled to −40 °C in an acetonitrile/dry ice slurry. The reaction tube was pumped down to 0.5 Torr, sealed, and stirred at −40 °C for 2 h before warming to room temperature. The reaction mixture was transferred to a sublimation apparatus in a glovebox, and the remaining $SiHCl_3$ was removed with dynamic vacuum before sublimation at 40 °C and 0.1 Torr was carried out for 2 h. The final product of yellow crystals collected on the coldfinger weighed 3.65 g (a 68% yield). Sublimed crystals were suitable for single-crystal X-ray diffraction study, which revealed identical cell parameters to those previously reported (ref 27); therefore, full crystallographic data collection was not carried out.

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(30) All nanowire synthesis experiments were carried out in a home-built CVD setup comprising a quartz tube heated by a tube furnace and equipped with pressure and gas flow controls. The Si/SiO_2 substrates used were prepared by exposing a HF etched silicon substrate to an oxidizing solution often used to etch metals (30% H_2O_2/37% HCl/H_2O = 1:1:5 v/v) at 70 °C for 20 min and were placed in the hot center zone of the furnace. About 150 mg of the SSP in a small alumina boat was placed 2 cm upstream from the entrance to the furnace at about 100 °C, evaporated, and carried downstream by a flow of 100 sccm of argon. Optimal nanowire growth was carried out at a furnace set temperature of 750 °C and a total pressure of 200 Torr for 20−25 min in which time the SSP was usually consumed.

(31) SEM images were taken with a LEO Supra field-emission electron microscope or a Zeiss Crossbeam microscope. PXRD was collected using a Siemens STOE X-ray diffractometer. HRTEM images were collected using a Philips CM200 UT transmission electron microscope with an accelerating voltage of 200 kV on nanowires that were sonicated and suspended in ethanol, dispersed onto lacey carbon film TEM grids.

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(36) For device fabrication, CoSi nanowires were first suspended in ethanol via sonication and deposited onto degenerately doped Si(100) coated with 600 nm of thermally grown oxide. Electrodes were then defined using either standard contact photolithography or e-beam lithography. Contacts to nanowires were made using thermally or e-beam deposited 40 nm Au atop 40 nm Ti after a 5 s 5% HF etch. Room-temperature measurements were performed using a Cascade probe station and a home-built transport setup. Low-*T* measurement was performed on Al wire-bonded device chips using a Quantum Design Physical Property Measurement System (PPMS) and a Keithley 2400 sourcemeter.

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