High Density Germanium Nanowire Assemblies: Contact Challenges and Electrical Characterization

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The conductive properties of vertically aligned germanium nanowires, with mean diameters of 50 and 100 nm, within anodized aluminum oxide (AAO) templates have been characterized by conductive atomic force microscopy (C-AFM) and macrocontact measurements. C-AFM was used to determine the electrical transport properties of individual nanowires within the arrays, while macrocontacts were used to measure the mean current−voltage characteristics of groups of nanowires. Contact resistance between the nanowires and metal macrocontacts was minimized by polishing and gradual etching of the AAO surface, to expose the nanowires, prior to deposition of the contacts. Impedance measurements were used to analyze the importance of defects on the charge transport properties of the germanium nanowire arrays. Conductivity data from C-AFM and macrocontact measurements were found to be comparable suggesting that both methods are inherently suitable for evaluating the electrical transport properties of encapsulated nanowires within a matrix. These results are significant as the ability to make good ohmic contacts to nanowires, within well-defined arrays, is key for the future "bottom-up" fabrication of multilayered device architectures for future electronic and optoelectronic devices.

Introduction

As microelectronic devices are being scaled below the sub-100 nm regime, with currently over 400 million transistors incorporated on a single integrated chip,[1] there has been renewed interest in using germanium as an alternative to silicon due to its superior electron and hole mobilities.[2] Additionally, Lieber, Samuelson, and others have demonstrated on a small scale that sub-100 nm semiconductor nanowires can be exploited for nanoscale applications such as chemical sensors,[3] high-speed FETs,[4] light emitting devices,[5] and single electron memory devices[6] with very low power consumption.

Ultimately, the successful incorporation of nanowires into optical and electronic devices will require their assembly into electrically addressable high-density architectures so that their unique transport properties, either individually or collectively, can be utilized. To date, the bulk of electrical transport measurements reported in the literature has focused on individual nanowires.[4,7−15] In particular, Heath and co-workers prepared functional devices and measured the transport properties of individual Si nanowires,[8] while recently Shan et al. [9] have developed a "grow in place" method for producing self-assembled, electrically contacted, crystalline Si nanowires. Dai and co-workers have successfully demonstrated the significance of surface states in the construction and operation of Ge nanowire-based FETs.[14,15] Great strides have been made in this area by Lieber and co-workers[16,17] who have demonstrated that carrier type (electrons, n-type; holes, p-type) and carrier concentrations in single-crystal silicon nanowires can be controlled during growth using phosphorus and boron dopants. Korgel and co-workers have also been extremely successful in synthesizing[18] and electrically contacting[11] Ge nanowires grown using a supercritical fluid−liquid−solid mechanism. An inherent problem associated with many of these approaches, however, is the formation of entangled meshes of nanowires. Considerable effort has been expended to manipulate a number of these nanowire meshes into useful configurations for nanoscale electronic devices.[4,19] In particular, Lieber and Dai pioneered the use of Langmuir−Blodgett films to align large amounts of surfactant stabilized nanowires[20,21] for use in nanolithography. However, methods based on the assembly of nanowire devices based on flow techniques are unlikely to facilitate the assembly of nanowires into high-density nanochip architectures, which are predicted to contain in excess of 1×10^{10} components per chip before the end of this decade.[1]

Encapsulation of semiconductor nanowires within an ordered template offers the possibility of manipulating nanowires into useful configurations as well as allowing their aspect ratios and hence their electrical properties to be tailored. Several groups have reported the synthesis of ordered arrays of semiconducting nanowires within the pores of ordered templates.[12,22,23] However thus far, little progress has been made on the characterization of their electrical properties. Mohney et al. recently described the fabrication of cobalt silicide contacts to Si nanowires within anodized aluminum oxide (AAO) arrays.[24] However this method

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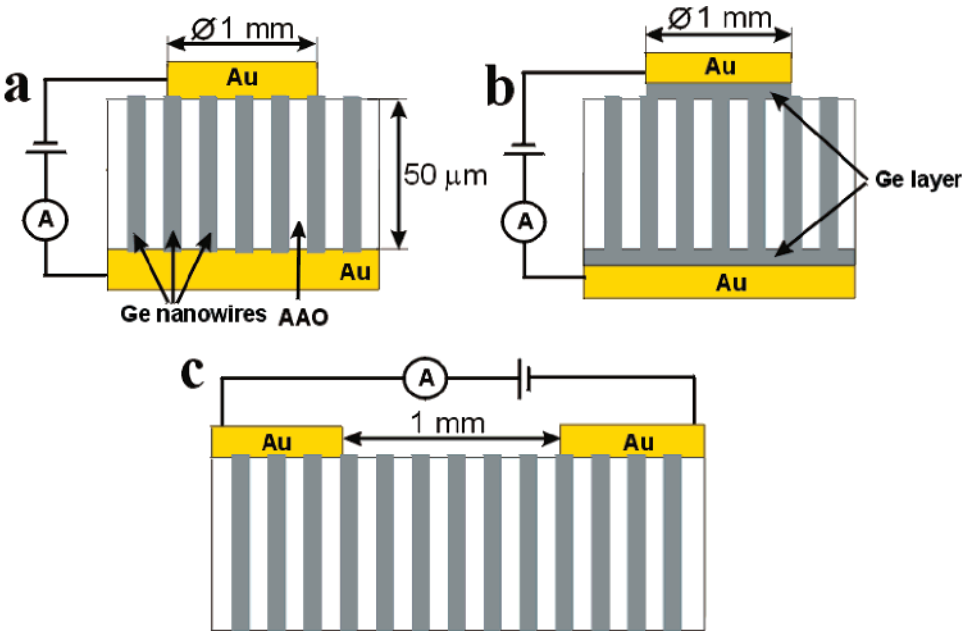

Figure 1. Representation of the macrocontact setup: (a) averaged conductivity through nanowires with Au−Ge nanowire contact interface; (b) same as (a) but with a Ge−Ge nanowire interface; (c) surface conductivity measurement.

may lead to doping of the Si nanowire with Au. With respect to semiconductor arrays, research has been focused primarily on ZnO nanowires[25] and our own initial investigations of Ge nanowire arrays.[26] Ohmic contacts to semiconductor nanowires are essential for future nanoelectronic devices, and the elimination of contact resistance between the contacts and the nanowires is vital to ensure ohmic contact. This problem was recently investigated by Mohney et al. who developed equations for extracting specific contact resistivity from several different Si test structures.[27]

In this paper we describe the electrical characteristics of Ge nanowires synthesized within the pores of AAO templates. Ohmic contacts, with minimum contact resistance, between the Ge nanowires and the macrocontacts were obtained using polishing and selective etching techniques. Conductive atomic force microscopy (C-AFM) was used to measure the conductivity of individual nanowires within the array while macrocontacts were developed to probe the mean conductivities of large numbers of nanowires within the array.

Experimental Section

Porous AAO membranes with a mean pore diameter of 100 nm were purchased from Anodisc filters, SPI Supplies, West Chester, PA. Porous AAO membranes with a pore diameter 50 nm were synthesized in-house using a well-known procedure described previously.[28,29] Ge nanowires were synthesized in AAO pores using a supercritical fluid (SCF) deposition technique described previously.[30] Briefly, Ge nanowires within the AAO porous membranes were synthesized in a 25 mL high-pressure cell. An appropriate amount of diphenyl germane was placed adjacent to the membranes inside an open top quartz glass boat. The cell was attached via a three-way valve, to a stainless steel reservoir (~48 mL). A high-pressure pump (Isco Instruments, Lincoln, NE) was used to pump CO_2 through the reservoir into the reaction cell. The cell was placed in a furnace and heated to 873 K and pressurized to 37.5 MPa simultaneously using a platinum resistance thermometer and temperature controller. The reaction proceeded at these conditions for 30 min. After the synthesis, Ge nanowires within the AAO membranes were cooled and removed from the reaction cell.

Warning: The high pressures and temperatures used in these experiments and the volatile nature of the chemicals could potentially lead to fire or explosion. Suitable safety precautions should be taken into consideration including the use of a blast screen.

The surface of the Ge nanowire-filled AAO membranes (GeNW-AAO) was mechanically polished using diamond suspensions with grain sizes of 6, 1, and 0.25 μm. The samples were polished until nanowires could be observed protruding from the surface of the AAO by atomic force microscopy (AFM). After being polished, the membranes were washed with acetone. To increase the contact area between the nanowires and the deposited macrocontacts, the top layer of the AAO surface was etched with 9 wt % H_3PO_4 for 5−90 min.

Individual germanium nanowires were released from the AAO membranes by dissolving the GeNW-AAO composite material with 6 M NaOH at 150 °C. The liberated nanowires were washed with distilled water and filtered on a 0.02 μm Anodisc filter (SPI Supplies). The filter was suspended in methanol and immersed in an ultrasonic bath for 20 min. The released nanowires were adsorbed onto glass slides and carbon-coated Cu grids from ethanol for AFM and transmission electron microscopy (TEM) (JEOL 2000) measurements.

Au or Pd/Au contacts were deposited on the AAO membrane using a precision etching coating system (Gatan). Firstly the system was used to remove the oxide layer from the Ge nanowire surfaces, and possible surface contamination, by cleaning with Ar ions at an energy of 5 keV at a current of 250 mA for 20 s. The metal electrodes of film thickness 50−100 nm were then coated on the surface of the AAO in the same chamber without breaking the vacuum at 10^{-4} Torr and at a coating speed of 1−1.5 Å s^{-1}. Different contact configurations were deposited as shown in Figures 1 and 2. For conductivity measurements on groups of nanowires, a large electrode was deposited on one side of the AAO membrane and a contact, of diameter between 1 and 2 mm, was formed by sputtering metal onto the opposite surface of the AAO nanowire membrane through a mask (Figure 1a,b). For C-AFM measurements only one surface was coated with a metal electrode (Figure 2).

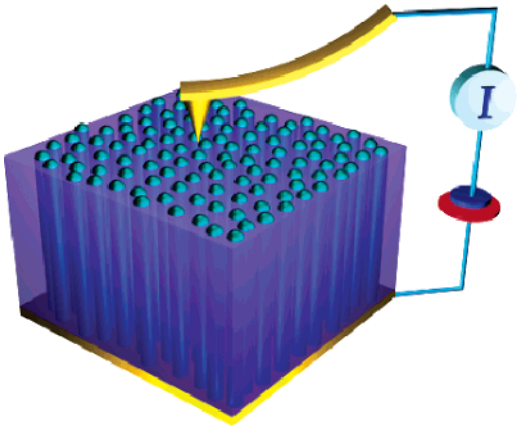

Figure 2. Representation of the C-AFM setup used to measure conductivities in individual wires.

To investigate the significance of the metal contact to the Ge nanowires, a Ge contact was also interfaced to the nanowires. A 1 mm electrode was deposited directly on top of the adhered surface Ge layer, and the remaining Ge layer on the AAO surface around the 1 mm diameter electrode was removed by Ar ion etching for 45 min (Figure 1b). A metallic contact was also applied to the thin Ge layer on the opposite side of the membrane. Conductivity measurements through the empty AAO membranes were achieved by depositing the gold under a 50° angle to decrease possible Au penetration through the nanopores. Surface conductivity of the filled Ge nanowire arrays was conducted as schematically showed in Figure 1c.

A home-built contact mode AFM was used for topography and current mapping. Conductivity measurements were undertaken by C-AFM as depicted in Figure 2. Conductive Pt-coated ultrasharp silicon AFM tips (Micromasch CSC12/Pt/50), having a radius of curvature less than 35 nm, were used in all experiments. A low-noise preamplifier, SR570 (Stanford Research Systems), was used for current amplification in both C-AFM and macrocontact measurements. Impedance measurements were undertaken using a sweep function frequency generator (Hung Change 8205A).

Activation energy measurements were carried out inside a HelioxAC-V ^{3}He refrigerator (Oxford Instruments) in the temperature interval of 140−300 K (current measurement at lower temperatures was impossible due to limitations of used equipment). An HP 34401A multimeter and preamplifier, SR570 (Stanford Research Systems), was used for conductivity measurements.

X-ray diffraction (XRD) data were collected on a Phillips Xpert PRO diffractometer using Cu Kα_1 radiation, an anode current of 40 mA, and an accelerating voltage of 40 kV. Data were collected in the range of 10−90 2θ deg with a step size of 0.005° and a scan rate of 0.2 s per step used. The AAO samples were polished and etched and then placed on a glass slide that minimized incoherent background scattering contributions, and the amorphous silica background trace was subtracted from the total XRD trace to analyze the contribution from the Ge nanowires.

Results and Discussion

(a) Structural Characterization of Nanowires. Figure 3 illustrates a background subtracted powder X-ray diffraction (PXRD) pattern from a polished and etched GeNW-AAO nanowire array. The mean diameter of the nanowires was 50 nm. Five well-resolved peaks are observed, corresponding to

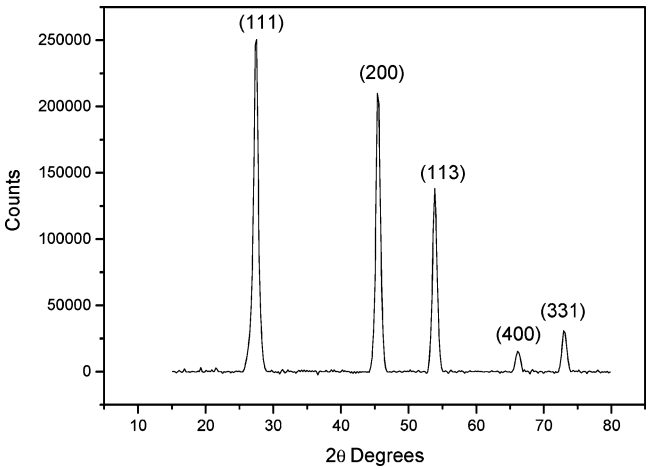

Figure 3. Background-subtracted XRD pattern of GeNW-AAO sample containing nanowires with a mean diameter of 50 nm.

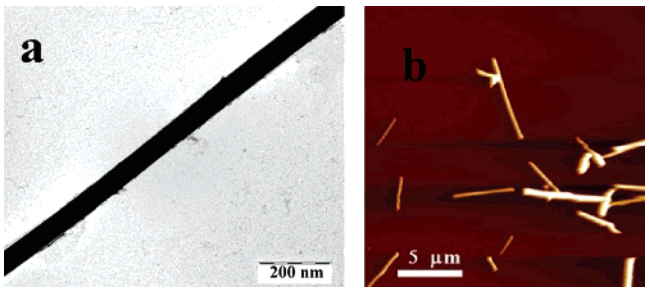

Figure 4. (a) TEM image of a liberated Ge nanowire liberated from an AAO membrane with a mean pore diameter of 50 nm and (b) AFM image of Ge nanowires liberated from an AAO membrane with a mean diameter of 100 nm.

(111), (200), (113), (400), and (331) reflections that can be indexed to the face centered cubic structure of Ge (JCPDS card no. = 03-0486).[31] The XRD pattern indicates a highly crystalline nanowire structure. The diameter of the nanowires after complete dissolution of the AAO templates was determined by AFM and TEM as shown in Figure 4. The mean diameter of the nanowires formed within the commercial and in-house AAO templates was approximately 100 and 50 nm, respectively (parts a and b of Figure 4), which corresponds to the mean pore diameters of the AAO membranes used as templates.

(b) Contacts to the Nanowires. To obtain linear $I(V)$ curves, surface preparation of the nanowire arrays before metallization was necessary. Figure 5a shows an AFM image of the surface of a commercial AAO membrane after Ge nanowire deposition prior to surface polishing or etching. A thin layer of Ge, approximately 1 μm in thickness, adhered to the surface of the membrane, and individual nanowires were not visible on the topography measurements. Large numbers of Ge nanowires are clearly visible extending 1−10 nm from the surface after sample polishing (Figure 5b). Figure 5c highlights the GeNW-AAO surface after chemical etching with 9 wt % H_3PO_4 for 15 min. The acid selectively removes the AAO membrane without etching the nanowires. After being polished and etched, Ge nanowires were observed to protrude from the surface of the etched membrane at a height of approximately 20−50 nm.

Macrocontacts, 1 and 2 mm in diameter (Figure 1a), were used to investigate the mean electrical properties of the Ge nanowires within the templates and determine the activation energy for the region of intrinsic conductivity. For thermally activated processes for intrinsic current carrier activation, the

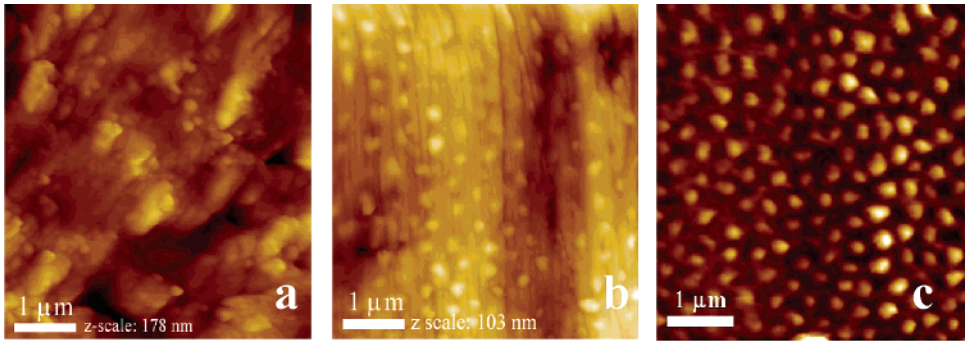

Figure 5. AFM images of AAO surfaces filled with Ge: (a) after Ge inclusion in the pores; (b) after mechanical polishing; (c) after chemical etching of (b) with 9% H_3PO_4.

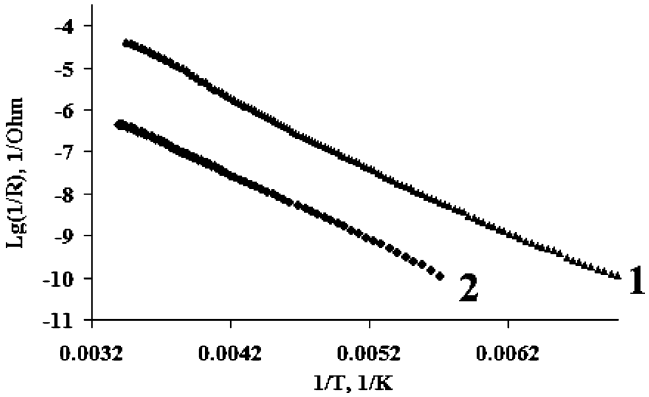

Figure 6. Conductivity dependence on temperature for Ge nanowires with a mean diameter of (1) 100 nm and (2) 50 nm templated inside AAO membranes.

current (I) through a nanowire depends on temperature (T) according to eq 1

$$I = I_0 \exp(-E_a/2kT) \quad (1)$$

where E_a is the activation energy and k is Boltzmann's constant. The activation energy of the Ge nanowires within the arrays was determined from current−temperature dependence in the temperature interval of 140−300 K (Figure 6). The activation energy of the Ge nanowires with mean diameters of 100 and 50 nm was found to be 0.61 and 0.58 eV respectively. These values are close to the band gap value for bulk Ge at 0.66 eV[2]. From the acquired data, we can conclude that conductivity has intrinsic character until at least 140 K with no visible doping impurity ionization impact.

$I(V)$ characteristics for the polished and etched GeNW-AAO samples, as depicted in Figure 1c, measured by the macro-contact method are shown in Figure 7. The conductivity through the empty AAO matrix and surface conductivity of the filled GeNW-AAO matrix (Figure 1c) was found to be 10^3−10^5 times lower than the conductivity through the nanowires and was therefore neglected. Hence, the $I(V)$ data solely reflects the conductivity through the nanowires within the arrays. For contacts deposited on mechanically polished samples, with no etching, both nonlinear (Figure 7a, curve 1) and linear (Figure 7b, curve 1) $I(V)$ curves were obtained for the 100 nm diameter nanowires while $I(V)$ curves obtained for the 50 nm diameter wires exhibited pronounced nonlinearity for all of the samples investigated (Figure 7c, curve 1). The nonlinear $I(V)$ curves in both samples may be due to the presence of a Schottky barrier between the Ge nanowire and the metal contact or an insulating layer, such as an oxide, between the nanowire and the metal contact.

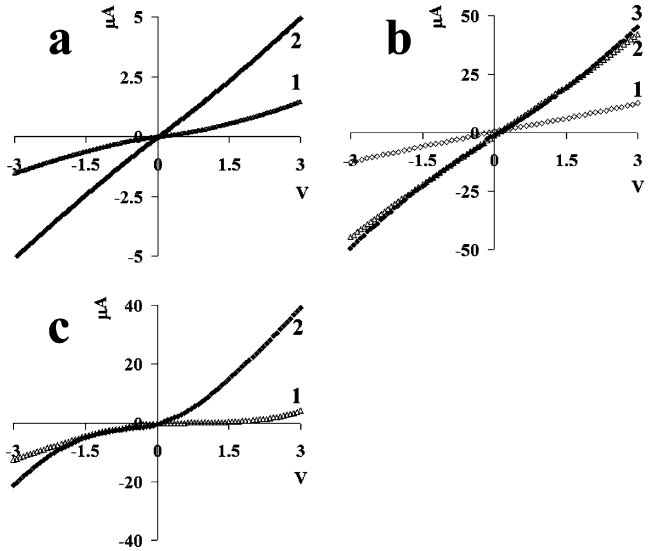

Figure 7. $I(V)$ data for Ge nanowire arrays: (a) with a mean nanowire diameter of 100 nm for (1) nonetched, (2) a sample etched for 15 min; (b) another 100 nm Ge nanowire sample, with a mean nanowire diameter of 100 nm, for (1) nonetched, (2) a sample etched for 90 min, and (3) an unpolished sample with a Ge−Ge contact interface to the nanowire; (c) a Ge nanowire sample, with a mean diameter of 50 nm for (1) a sample etched for 5 min and (2) a sample etched for 10 min.

The $I(V)$ characteristics of the 100 nm diameter Ge nanowires became linear and displayed good ohmic contact characteristics when the mechanically polished surfaces were treated with 9 wt % H_3PO_4 to gradually etch the surface AAO layer (parts a and b of Figure 7, curves 2). This change implies that the nonlinearity observed with the nonetched samples is due to the presence of an insulator layer, i.e., AAO, between the nanowires and the metal electrode. After etching, the resistivities of the samples decreased further for both the 50 and 100 nm diameter nanowires. Resistivities decreased on average by a factor of 4 for the etched samples in comparison to samples that were solely mechanically polished, with some samples showing an improvement of 10 to 20 times. By gradual etching of the AAO layer on top and around the circumference of the nanowires, the contact area to the nanowire increases. A degree of nonlinear behavior was however still observed for the 50 nm diameter nanowires after polishing and etching (Figure 8c, curve 2), which possibly implies that the AAO layer around the 50 nm nanowire was not completely removed.

In the ideal case H_3PO_4 should uniformly remove the AAO layer around the nanowire as shown in parts a and b of Figure 8. In reality etching of the AAO from the nanowires is not uniform. Etching of the GeNW-AAO membrane with NaOH

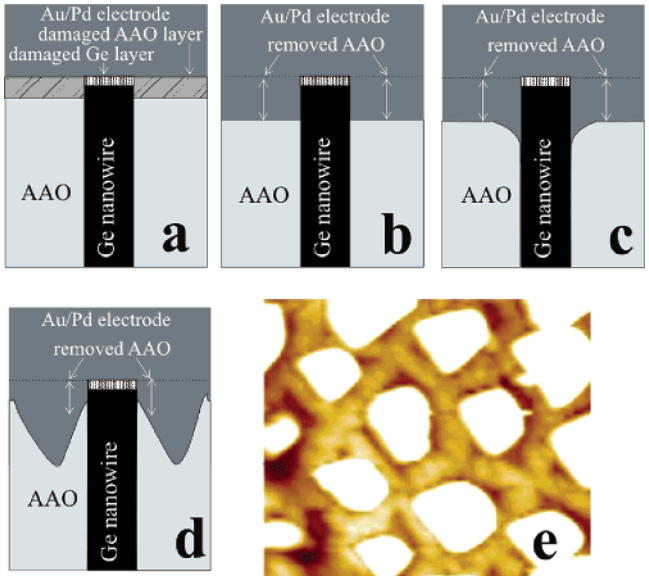

Figure 8. Schematics of (a) contact before etching, (b) assuming homogeneous removal of the AAO matrix during surface etching, (c) assuming more effective AAO matrix etching in close proximity to the nanowire for 100 nm diameter GeNW-AAO samples, (d) assuming more effective etching away from nanowire for the 50 nm diameter GeNW-AAO samples, and (e) AFM topography surface image of 100 nm nanowire array etched for 15 min in 9% H_3PO_4.

solution was attempted.[32] However in our membranes the best results were obtained with 9 wt % H_3PO_4 solution. For 100 nm GeNW-AAO samples, the etching is almost uniform despite the high temperature synthesis of the Ge nanowires. In fact it occurs more efficiently around the edge of the nanowire as shown in Figure 8e. A schematic of this situation is shown in Figure 8c. Dark areas in the AFM topography images around the nanowires (Figure 8e) correspond to effective removal of AAO material in comparison to areas between the nanowires. For the 50 nm GeNW-AAO samples, the presence of nonlinear $I(V)$ characteristics (Figure 7c, curve 2) even after gradual etching of the surface may be due to poorer etching of the alumina in close proximity to the nanowires compared to areas between the wires as shown schematically in Figure 8d. The difference in etching between the commercial GeNW-AAO with a mean diameter of 100 nm and an as-prepared GeNW-AAO, with a mean diameter 50 nm, is possibly due to the presence of different structural defects in each membrane after high temperature treatment. Different confinement and wetting effects between the two membranes could also account for the different etching observations. The resistivity for a single nanowire, based on a mean value obtained for a group of nanowires, was between 80 and 1000 Ω·m for nanowires with a mean diameter of 100 nm and 140−3000 Ω·m for nanowires with a mean diameter of 50 nm, respectively, for 10 different batches of NW samples.

C-AFM measurements were undertaken on polished GeNW-AAO samples. Figure 9a shows the topography of a GeNW-AAO membrane after polishing to remove the surface Ge layer. Due to the highly resistive nature of the nanowires, a voltage of at least 10 V applied across the nanowires was required to achieve a current of at least 1 pA. Current maps from individual nanowires, with mean diameters of 100 nm, measured at 20 and 40 V are shown in Figure 9. The areas of high current density are shown in parts b and c of Figure 9 correspond well with the protrusions in the topographic image of the nanowires displayed in Figure 9a. Some nanowires not observed in the topographic images were also detected in the current maps. From the current maps it can be concluded that practically 100% of the nanowires examined were conductive throughout the entire membrane. The current through the nanowires also increased from a mean value of 2.5 to 12 pA as the voltage was increased, as shown in the histograms of parts d and e of Figure 9. All the nanowires measured showed a mean current distribution within 200%. This tight current distribution indicates that all of the nanowires within the array have similarly conducting characteristics. The density of Ge nanowires within the AAO membranes, as determined by topography and conductivity measurements, with mean pore diameters of 100 and 50 nm was 9×10^8 and 1.4×10^{10} cm^{-2}, respectively.

Figure 10 illustrates a comparison between the C-AFM and macrocontact measurements for GeNW-AAO samples. For both methods, as the voltage is increased above 10 V the $I(V)$ characteristics become nonlinear (Figure 10). At higher voltages (50 V) the resistivities decrease two to three times. The reason for the lower resistivity at higher voltages is possibly due to thermoelectric ionization.[2] The change in resistance through the nanowires as a function of applied voltage is almost identical for both the macrocontact and C-AFM measurements (Figure 10). Resistivity values for a single nanowire for both systems are approximately the same despite the contact area with the macrocontacts being 3 orders of magnitude larger, 8000 nm^2 for the 100 nm diameter nanowires and 2000 nm^2 for the 50 nm diameter nanowires, than the contact area with C-AFM, i.e., 2−4 nm^2. This result suggests that for the polished samples, both the C-AFM and macrocontact methods are inherently suitable for measuring the electrical properties of such nanowire arrays. It should be noted that there may be differences in the nature of the association between the nanowire and the metal contact for the macrocontact and C-AFM methods. In C-AFM measurements a force is applied between the AFM tip and the surface which can improve the quality of the contact. The AFM tip can readily remove or penetrate material which may otherwise be weakly adhered to the surface of the nanowire, e.g., an oxide layer. With the macrocontacts, the contact is deposited directly on top of the nanowires and hence adhered surface layers may act as a barrier between the contact and the metal.

To compare the quality of the metallic macrocontact to our Ge nanowires, the data from the metallic−semiconductor contact interface were compared to data obtained from a semiconductor−semiconductor, i.e., Ge−Ge, contact interface, schematically shown in Figure 1b. The Ge nanowire−Ge contact interface was obtained by overfilling the AAO pores with Ge to form a continuous film on top of the AAO membrane before deposition of the metal electrode. Hence, the nanowires formed within the AAO pores are terminated within this film and are therefore the same material as the contact, in terms of crystallinity, quality, and type. Scattering of electrons at the contact−nanowire interface is therefore minimized because the contact has an identical structure to the nanowires. For these samples where the metallic contact was deposited on the thin Ge layer (Figure 1b), the $I(V)$ characteristics obtained are close to those observed for the etched samples (Figure 7b, curves 2 and 3). Since both the metallic/semiconductor contact and the semiconductor/semiconductor contact give similar resistivity values, this indicates that good ohmic contact to the Ge nanowires has been obtained with the metallic contact.

The Ge nanowires inside the AAO membranes showed higher resistivities than those already reported in the literature, e.g., 1.4×10^{-4}−0.3 Ω·m[10] for Ge nanowires grown on gold nanoparticles by a VLS mechanism and 0.001−0.1 Ω·m[11] for Ge nanowires grown from gold nanocrystal-seeded supercritical

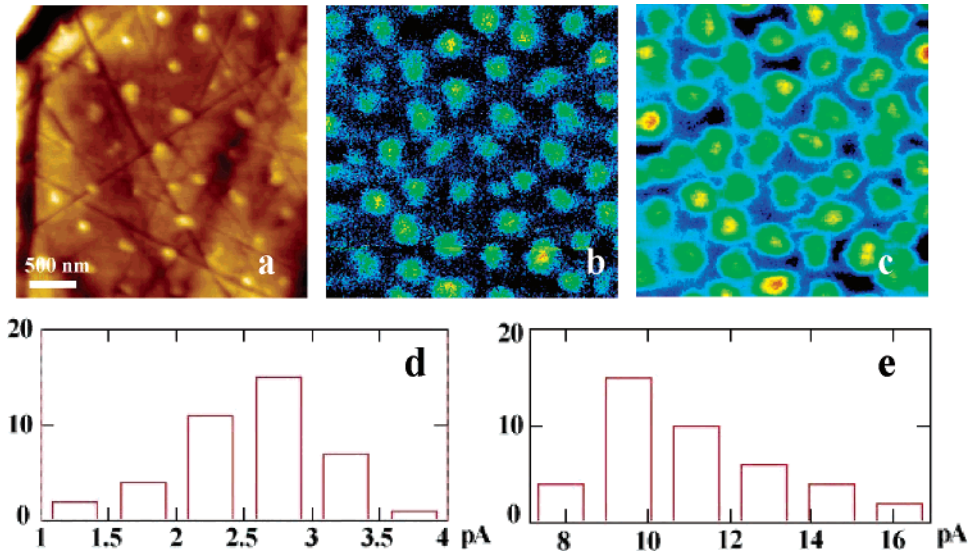

Figure 9. (a) AFM topography of a polished GeNW-AAO surface. (b) C-AFM current map of (a) at 20 V. (c) Current map of (a) at 40 V. (d) Conductivity histogram of current map (b) and (e) conductivity histogram for current map (c).

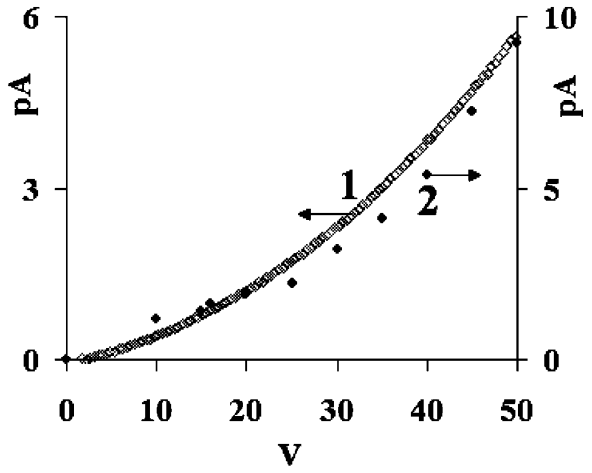

Figure 10. Dependence on the current vs voltage dependence through an individual 100 nm Ge nanowire measured by (1) macrocontact and (2) C-AFM.

fluid−liquid−solid (SFLS) method using a continuous flow reactor. However, our synthesis technique does not involve a gold catalyst, and therefore the nanowires are undoped. Consequently higher resistivities would be expected in comparison to nanowires grown via a gold-catalyzed VLS mechanism. Resistivity values for our nanowires encapsulated inside AAO templates are significantly higher than the resistivity of bulk Ge (0.47 Ω·m)[2]. The higher mean resistivities of the Ge nanowires within the AAO templates compared to bulk Ge are possibly due to the influence of surface states[14] at the nanowire−AAO interface which may increase electron scattering within the nanowires. Hence, as the surface area of the Ge nanowires within the AAO templates increases, i.e., in going from 100 to 50 nm, the mean resistivity of the nanowires also increases due to the growing influence of these surface states. An investigation into the nature of the interface between the nanowires and the templates is currently ongoing.

To investigate the response of the GeNW-AAO systems to fast switching conditions, the impedance of the nanowire arrays, in the frequency range of $1-10^5$ Hz for etched and nonetched samples, was investigated (Figure 11a, curves 1−3). The impedance (Z) of the nonetched, but polished, nanowires with a mean diameter of 100 nm was observed to decay at

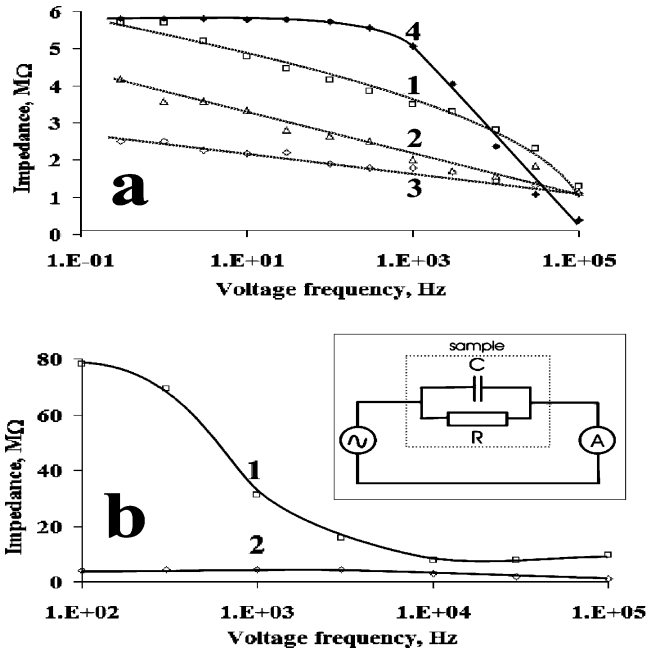

Figure 11. Frequency-dependent impedance measurements for: (a) 100 nm diameter Ge nanowires, (1) polished, (2) polished and etched for 15 min in 9% H_3PO_4, (3) polished and etched for 45 min in 9% H_3PO_4, and (4) equivalent scheme; (b) for 50 nm diameter Ge nanowires, (1) polished and etched for 5 min in 9% H_3PO_4 and (2) polished and etched for 10 min etched in 9% H_3PO_4.

1−10 Hz. Figure 11a, curve 4, shows the impedance of the equivalent scheme (Figure 11b insert) of a real sample relating to eq 2

$$Z = 1/(1/R + \omega C) \qquad (2)$$

where the measured real resistance R and capacitance C of the sample $R = 5.7$ M·Ω and $C = 4$ pF were used. Impedance for the equivalent scheme (Figure 11b insert) starts decaying at frequencies 100−1000 times higher than those for the Ge nanowire arrays (Figure 11a, curve 4) implying that the impedance in the sample is not determined simply by the capacitance and resistance of the AAO/nanowire system but is more complicated. In our opinion such behavior is due to presence of defects in the system. Defects may be created at

the surface of the Ge nanowire and the AAO wall which may influence the conductivity as was observed for oxidized Ge nanowires in air.[11] The relative magnitude of the impedance drop for the gradually etched samples decreased with increasing etching time (Figure 11a). This indicates that charge carriers are trapped or scattered mainly in the Ge layer close to the end of the nanowire. Localized states may be present in a thin damaged layer at the ends of the nanowires due to a high concentration of structural imperfections (Figure 8a). Structural imperfections created by polishing may diffuse into the bulk of the nanowire matrix, but they mostly accumulate in the thin layer close to the top surface of the nanowire. Similar impedance dependences were noticed in amorphous semiconductors.[33]

After the AAO surface layer was chemically removed, the top of the Ge nanowires extend above the surface. The sides of the nanowires, which have not been mechanically treated, are now also exposed to the contact (Figure 8c). Consequently, it is possible that the majority of the current passes through these untreated parts of the nanowires and the impact of the defects on top of the nanowires on the impedance measurements decreases. It was noticed that for the best conductive 100 nm diameter samples, the impedance drop, in the interval $1-10^5$ Hz, almost vanishes for the etched samples. This result indicates that defects are not created at the AAO−nanowire interface but are present in the contact. Similar results were observed for the impedance drop with nonetched and etched 50 nm nanowires samples (Figure 11b, curves 1 and 2).

Conclusions

Semiconductor nanowires have potential applications in future nanoelectronics as nanodevices and as interconnects. While the electrical properties of individual nanowires have been intensely investigated, there are relatively few studies on the conductive properties of ordered arrays of semiconductor nanowires within defined architectures. Macrocontact and C-AFM measurements were shown to be extremely useful techniques for characterizing the electrical properties of nanowires within arrays. Crucially, both methods give approximately the same electrical resistivity results indicating that both methods are intrinsically suitable for electrical characterization of such arrays. Improvements in contact resistance were achieved by mechanically polishing and chemical etching the membranes to a point where the metallic contact to the etched samples does not adversely affect nanowire resistivity. Impedance measurements on the nanowires confirm the presence of defects at the surface of the nanowire which affects charge transport at high frequencies. However, after membrane etching it was found that these defects do not significantly affect electron transport in the Ge nanowires. In summary this paper offers a viable method for the use of Ge nanowire arrays as potential architectures for future nanoelectronic devices as an alternative to current top-down lithography synthesis.

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