FULL PAPER

High-Density Carrier Accumulation in ZnO Field-Effect Transistors Gated by Electric Double Layers of Ionic Liquids

By *Hongtao Yuan,* Hidekazu Shimotani, Atsushi Tsukazaki, Akira Ohtomo, Masashi Kawasaki,* and *Yoshihiro Iwasa*

Very recently, electric-field-induced superconductivity in an insulator was realized by tuning charge carrier to a high density level (1×10^{14} cm^{-2}). To increase the maximum attainable carrier density for electrostatic tuning of electronic states in semiconductor field-effect transistors is a hot issue but a big challenge. Here, ultrahigh density carrier accumulation is reported, in particular at low temperature, in a ZnO field-effect transistor gated by electric double layers of ionic liquid (IL). This transistor, called an electric double layer transistor (EDLT), is found to exhibit very high transconductance and an ultrahigh carrier density in a fast, reversible, and reproducible manner. The room temperature capacitance of EDLTs is found to be as large as 34 μF cm^{-2}, deduced from Hall-effect measurements, and is mainly responsible for the carrier density modulation in a very wide range. Importantly, the IL dielectric, with a supercooling property, is found to have charge-accumulation capability even at low temperatures, reaching an ultrahigh carrier density of 8×10^{14} cm^{-2} at 220 K and maintaining a density of 5.5×10^{14} cm^{-2} at 1.8 K. This high carrier density of EDLTs is of great importance not only in practical device applications but also in fundamental research; for example, in the search for novel electronic phenomena, such as superconductivity, in oxide systems.

1. Introduction

Carrier density is well recognized as a key parameter of the electronic properties of semiconductors and superconductors. The most common method used to control carrier density is chemical doping, either substitutional or interstitial. Less common, but in contrast to chemical doping, which is inherently associated with disorder, is electric-field control of charge carrier density. This is a method completely free of structure disorder, and has attracted much attention because it is remarkably simple to modulate the physical properties of condensed matter and to explore new functionalities in field-effect transistors.[1,2] As early as the 1960s, researchers demonstrated the changeable superconducting critical temperature (T_c) in Sn and In by electrostatic charging.[3] Other known cases in field-effect transistor geometry have involved tuning of T_c of superconductivity in high T_c cuprates[2] and the control of the Currie temperature of a ferromagnetic semiconductor GaMnAs[4]. However, for most dielectric materials in conventional metal–insulator-semiconductor field-effect transistors (MISFETs), owing to the relatively low dielectric constants and the breakdown voltage limitation,[5–8] the maximum accumulated carrier density is extremely low ($<10^{13}$ cm^{-2}) and far from what is expected to induce superconductivity in non-superconducting matters. Thus, the field-effect doping has so far been limited only to the modulation of the critical temperature of oxide superconductors and ferromagnetic semiconductors.[2,4] For realizing the field-effect induced superconducting transition, or some other novel electronic phenomena, further increase in the maximum attainable carrier density in field-effect transistor is of great importance and urgency.

Recently, a new type of field-effect transistors, named electric double layer transistors (EDLTs), have been employed for attaining a high carrier density by using polymer electrolytes or ionic liquids (ILs) as gate dielectrics, in which large capacitances can be achieved in the electric double layer capacitors (EDLCs).[9–20] Figure 1a displays a cross-section of an IL-gated EDLT based on ZnO, a wide bandgap oxide semiconductor. When an electric potential is applied between

[*] Dr. H. T. Yuan, Dr. H. Shimotani, Dr. A. Tsukazaki, Dr. A. Ohtomo, Prof. M. Kawasaki, Prof. Y. Iwasa
Institute for Materials Research, Tohoku University
Sendai 980-8577 (Japan)
E-mail: htyuan@imr.tohoku.ac.jp
Dr. H. T. Yuan, Dr. H. Shimotani, Prof. M. Kawasaki, Prof. Y. Iwasa
Japan Science and Technology Agency (CREST)
Kawaguchi 332-0012, Japan
Prof. M. Kawasaki
WPI Advanced Institute for Materials Research, Tohoku University
Sendai 980-8577 (Japan)
and
Institute for Materials Research, Tohoku University
Sendai 980-8577 (Japan)
and
Japan Science and Technology Agency (CREST)
Kawaguchi 332-0012, Japan.

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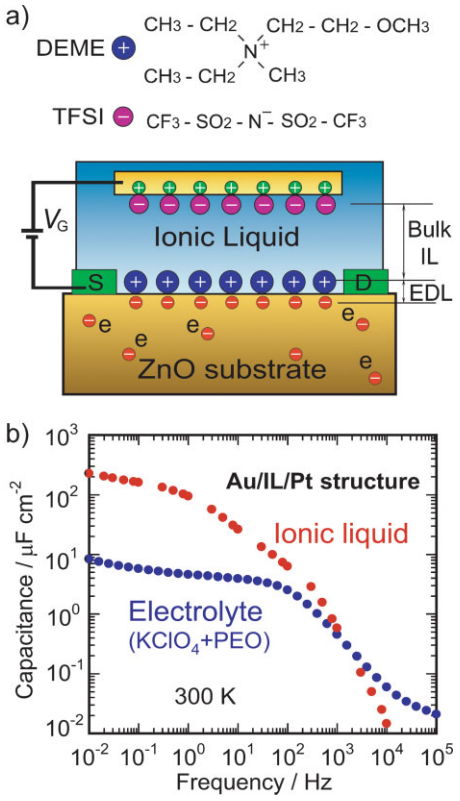

Figure 1. A schematic demonstration of an IL-gated EDLT on ZnO surface. a) Schematic molecular structures of the IL DEME-TFSI (top) and the cross-section of IL/ZnO EDLT (bottom). Blue, pink, green, and red spheres represent the $DEME^+$ cation, $TFSI^-$ anion, hole, and electron. b) The nominal capacitance C_{EDL} of an IL-gated EDLC on a Pt/IL/Au sandwich structure with a channel surface area of 1.0×10^{-3} cm^{-2} obtained by using an impedance spectrum analyzer with the frequency of applied ac voltage of 5 mV from 0.01 Hz to 0.1 MHz.

the gate electrode and transport channel, merging inside IL, the mobile cation and anion of the IL will move towards the oppositely charged electrodes to form EDLs. The EDL at the IL/semiconductor interface, regarded as a nanogap capacitor with a huge capacitance, can accumulate charges in the transport channel to a very high density level that is impossible to reach in conventional FETs with solid gate dielectrics. In such self-organized EDLCs, a large capacitance coupling and high charge densities were achieved in certain organic and oxide semiconductor systems.[9–20] Particularly with oxide semiconductors, an insulator–metal transition was observed in ZnO EDLTs gated by $KClO_4$/polyeltheleneoxide (PEO) electrolytes and also in InO_x EDLTs by using IL. In the case of ZnO, a direct estimate for accumulated carrier density obtained through Hall-effect measurement reached 4×10^{13} cm^{-2},[16] much higher than that for oxide dielectric gated ZnO transistors ($<10^{13}$ cm^{-2}).[21–27] More importantly, by tuning charge carrier to a very high density of 1×10^{14} cm^{-2} on $SrTiO_3$ channel in EDLTs, two dimensional superconductivity was electrostatically induced on the insulating $SrTiO_3$ without the aid of any chemical doping.[1] These achievements indicate the usefulness and importance of EDLTs for high-density charge accumulation in oxide semiconductor field-effect transistors. Because $SrTiO_3$ is a superconductor needing the lowest carrier concentration, further increase in carrier density in the channel is strongly required for the extension of the field-effect-induced insulator–superconductor transition to other potentially interesting materials via this EDL technique. However, owing to the limitation of the electrochemical potential window of electrolytes or ILs (normally within ±3 V), the room-temperature carrier accumulation in EDLTs has its limitations. Meanwhile, with a high gate bias at room temperature, the redistribution of mobile ions in polymer solution and the charge injection from electrodes sometimes result in irreversible chemical reactions on channel surfaces. Therefore, the charge accumulation at low temperatures, where all the electrochemical processes are completely suppressed, shows promise for the extension of maximum attainable high carrier density.

Here, we chose the IL (DEME-TFSI, see Experimental Section) as a gate dielectric for EDLTs and investigated its charge accumulation properties, particularly at low temperature, on a standard oxide semiconductor, ZnO. The molecular structure of DEME-TFSI, which is a highly polar binary salt composed of nitrogen-containing cations and imide anions, is schematized in Figure 1a. It has a higher ionic conductivity and dielectric constant than electrolyte dielectrics.[15] Also, it is solvent-free and compatible with most materials, especially oxide systems, in which it can be exposed to moderate voltages without undergoing redox reactions.[15] In this Full Paper, we report ultra-high-density electron accumulation (up to 4.5×10^{14} cm^{-2} at room temperature) in IL/ZnO EDLT in a fast, reversible, and reproducible operation mode. Furthermore, we found that carriers can be accumulated even at temperatures down to 220 K, allowing us to achieve high carrier density one order of magnitude larger than the previous report.[16] A maximum carrier density of 8×10^{14} cm^{-2} can be achieved at 220 K with a higher applied gate voltage of 5.5 V, and a high density level of 5.5×10^{14} cm^{-2} maintained down to 1.8 K.

2. Results and Discussion

2.1. High Carrier Density and High Transconductance in IL/ZnO EDLTs

The most direct way to measure the large capacitance of EDLCs is through capacitance-frequency measurements. The nominal EDL capacitance C_{EDL} could be measured by impedance spectroscopy on a Pt/IL/Au structure sandwiching IL with a Pt gate and a gold electrode. A ZAHNER-electric-IM6eX impedance analyzer was used to obtain the frequency profiles on an Au surface of 500 μm ×200 μm over a frequency range of 0.01 Hz–100 KHz with the application of an ac voltage amplitude of 5 mV. As shown in Figure 1b, the nominal capacitance C_{EDL} of the Pt/IL/Au EDLC increases to 120 μF cm^{-2} with the frequency decreasing to 0.01 Hz. Compared to the nominal EDL capacitance of 7.4 μF cm^{-2} in Pt/$KClO_4$(PEO)/Au structure, the IL-gated EDLC has a much higher capacitance, implying a better capability for carrier accumulation.

Transfer characteristics and Hall-effect properties were measured on Hall-bar-patterned ZnO EDLTs. Figure 2a shows the transfer curve (I_D–V_G relation) associated with a considerably small leak current (three orders of magnitude smaller than the channel current, which guarantees the device performance will not be affected by the leakage). This leak current, less than 400 nA, is significantly smaller than that in electrolyte/ZnO EDLTs[16] owing to the electrochemical silence of the IL as compared with the electrolyte $KClO_4$/PEO. The nearly hysteresis-free transfer characteristics (Fig. 2a), with a source–drain voltage of $V_D = 100$ mV, show that the maximum current at gate voltage $V_G = 3$ V is as great as 220 μA, even with the small width-to-length ratio of 0.5 in the channel, which is thought to directly result from the large capacitance and the highly-charged behavior of the IL-gated EDLTs. The on-off ratio of the device, ranging from 10^3 to 3, differs from sample to sample because the off-state current is determined by a range of bulk conductivities of ZnO single crystals. Output characteristics (I_D–V_D relation, plotted in Fig. 2b) show the saturation behavior of I_D at larger V_G, which is a clear sign of pinch-off phenomena. The saturation current at $V_G = 3$ V is as large as 1.25 mA, also resulting from the huge capacitance of highly charged EDLTs.

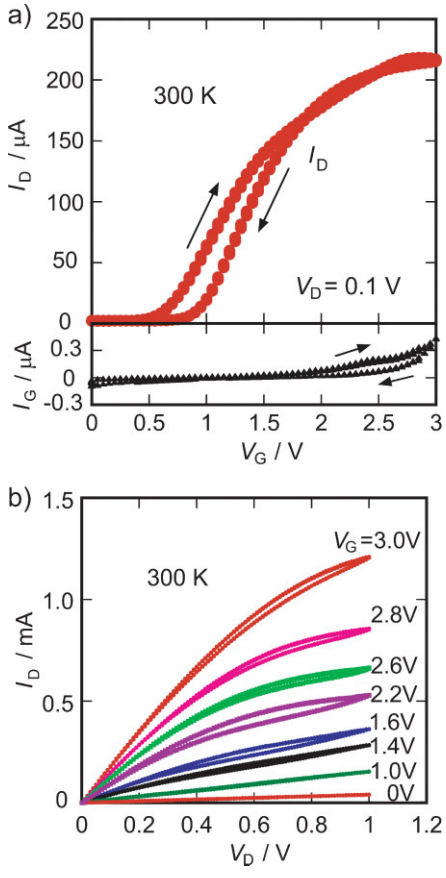

Figure 2. Basic characteristics of an IL/ZnO EDLT at 300 K. a) Transfer characteristics: I_D–V_G (top) and I_G–V_G curves (bottom) at $V_D = 100$ mV. The gate voltage was swept at a rate of 20 mV s^{-1}. b) I_D–V_D output curve with applied V_G from 0 to 3.0 V (scan speed: 30 m V s^{-1}).

For evaluation of transistor performance, the transconductance g_m of the EDLTs was deduced from an I_D–V_G curve by using the following equation:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} C_{in} \mu_{FE} V_D \quad (1)$$

Here, W and L are the width and length of the transport channel, C_{in} is the capacitance of the IL/ZnO interface, and μ_{FE} is the field-effect mobility. A high transconductance g_m of 0.16 mS is obtained in the IL-gated EDLTs with a very small source-drain voltage of 100 mV and a low gate bias of 1.1 V. To make a comparison of the g_m in EDLTs with those in oxide gated transistors, the normalized transconductances (g_n, normalized by the V_D and the W/L ratio) are summarized in Table 1. The value of 4 mS V^{-1} for g_n in IL-gated EDLTs is several orders of magnitude larger than that in ZnO transistors using oxides as gate dielectrics, and also several times larger than that in electrolyte-gated EDLTs. This is mainly attributed to the large capacitance of the nano-gap EDL capacitor. The extremely high g_n with low-voltage operation in the IL/ZnO EDLTs is a great advantage for their practical applications in electronic devices since it could dramatically reduce the operation voltage of the FET devices.

Figure 3a shows the transient response of IL/ZnO EDLTs to a square-shaped V_G with a pulsed amplitude of 2 V. The device exhibits an excellent reproducibility of current response to the repeatedly pulsed V_G. This strongly suggests that no chemical doping or chemical reaction occurs at the IL/ZnO interface when the gate potential is biased, because if chemical doping or a chemical reaction had occurred, I_D would not have returned to its original value after gate scanning.[14] Furthermore, details of the pulsed-V_G response indicates that the stabilized current rose by 85% upon switching on within as little as 0.5 s, and fell by 99% upon switching off within 0.5 s. Generally, in polymer dielectrics, the polarization relaxation time is strongly related to the conductivity of the polymers.[18,28] Low molecular weight and high polarizability make ILs much more conductive than electrolytes, which is responsible for the rapid switching behavior of IL-gated EDLTs. From Figure 3b, one can see that the switching of IL/ZnO EDLTs is much faster than that of electrolyte-gated EDLTs using liquid or solid $KClO_4$/PEO. It is this reversible and rapid polarization relaxation of the mobile ions in highly conductive ILs that leads to the fast response and robust properties of IL/ZnO EDLTs. A similarly quick response has been observed in IL-gated EDLTs on organic semiconductors.[18,19,28]

2.2. High-Density Carrier Accumulation at Room Temperature

As the most direct and reliable way of evaluating carrier density and mobility in semiconductors, Hall-effect measurements were performed on the IL/ZnO EDLTs. Figure 4 shows the sheet carrier density n_s and the Hall mobilities μ_H as a function of V_G at 300 K. The maximum n_s of 4.0×10^{14} cm^{-2} in this device is two orders of magnitude higher than those in oxide-gated ZnO transistors[21–27] and one order of magnitude higher than those in electrolyte-gated EDLTs.[16] Among all the measured IL/ZnO EDLTs in our

Table 1. The normalized transconductance g_n by the V_D and the W/L ratio in IL gated ZnO EDLTs and oxide gated transistors, where the normalized transconductances were derived from $g_n = (g_m/V_D)(L/W) = C_{in}\mu_{FE}$.

Gate dielectrics		V_G (V) for g_m	V_D (V) for g_m	$W \times L$ (μm^2)	g_m (mS)	W/L ratio	g_n (mS V^{-1})	Refs.
EDL	ILs	1.2	0.1	200×500	0.16	0.4	4	This work
	$KClO_4$/PEO	2.6	0.1	60×220	0.03	0.273	1.1	[14]
Oxide	Al_2O_3/ZnMgO	−5	4	100×4	3	25	0.03	[22]
	ZnMgO	−4	3	50×50	0.03	1	0.01	[23]
	$Ba(Sr)TiO_3$	6	6	100×5	0.1	20	0.00083	[24]
	$ScAlMgO_4$	1000	10	60×220	0.00005	0.273	0.0000183	[25]

study, the highest n_s obtained at room temperature so far was 4.5×10^{14} cm^{-2}. We can see in the n_s–V_G plot (Fig. 4) that the carrier density is almost proportional to V_G before the saturation, with the threshold voltage $V_{th} = 0.5$ V. From the equation $C_{in} = e(\partial n_s/\partial V_G)$ and the slope of the n_s–V_G curve, the capacitance C_{in} of the EDLC at the IL/ZnO interface was determined to be 34 μF cm^{-2}, which is five times larger than that of electrolyte/ZnO EDLCs,[16] and comparable to that obtained on organic semiconductor using an ion gel as a gate dielectric.[18] It was found that the μ_H of a bulk ZnO crystal (50 cm^2 V^{-1} s^{-1}) rose sharply to around 100 cm^2 V^{-1} s^{-1} by forming an accumulation channel through the IL gating. μ_H shows a peak at relatively small V_G, followed by a gradual decrease with an increase in V_G. This decrease could be ascribed to the enhanced surface scattering of electrons in the accumulation layer because a higher electric field pushes accumulated carriers in ZnO much closer to the surface, making carriers more susceptible to surface scattering. One more feature to be addressed here is the saturation behavior above $V_G = 2.7$ V in the transfer characteristic (Fig. 2a) and the n_s–V_G curve (Fig. 4). This saturation behavior occurs near the positive voltage end of the electrochemical window of the IL, and indeed the leak current I_G exhibits an upturn above $V_G = 2.7$ V. Thus, the saturation of charge accumulation in the ZnO channel is presumably attributable to the limitation of the room-temperature potential window of IL. The transfer curve is reversible even after the saturation of I_D, excluding the irreversible degradation in the ZnO channel.

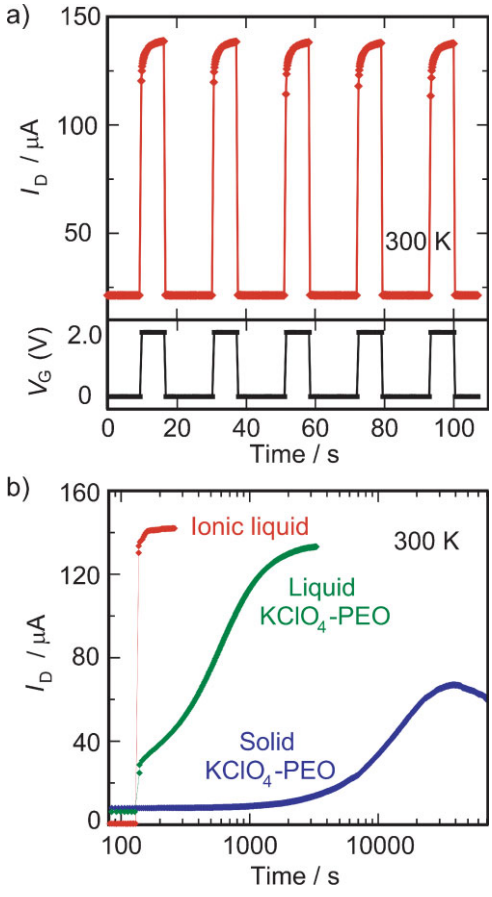

Figure 3. Transient behavior of IL/ZnO EDLTs at 300 K, with $V_D = 100$ mV. a) Time response of IL/ZnO EDLTs to a pulsed square-shaped gate voltage with an amplitude of 2 V, showing a superior reproducibility. b) Comparison of the dynamical response to stepwise pulses of $V_G = 2$ V in EDLTs gated by IL, liquid $KClO_4$/PEO ($M_w = 200$) and solid $KClO_4$/PEO ($M_w = 2000$) electrolytes.

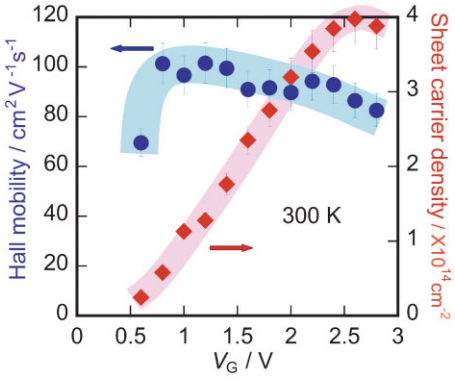

Figure 4. Room temperature carrier accumulation in IL/ZnO EDLTs. Sheet carrier density n_s and Hall mobility μ_H as a function of gate voltage V_G at 300 K, determined by Hall effect measurements.

Compared to the nominal capacitance C_{EDL} of 120 μF cm^{-2} obtained on a Pt/IL/Au sandwiched structure from the capacitance–frequency measurement by using impedance spectroscopy, the capacitance C_{in} of 34 μF cm^{-2} derived from the Hall-effect measurement is relatively small. The variation between the C_{EDL} and the C_{in} probably occurs for the following reasons: i) all the charges, including the trapped charges, at the IL/Au interface were measured in capacitance–frequency measurement, whereas in the Hall-effect measurement, only mobile carriers in the IL/ZnO interface are estimated for the capacitance. ii) The

theoretical investigation on the distribution of concentrated electrons near the ZnO surface has indicated that the carriers are mainly accumulated in a thin layer which is 10 Å from the outmost surface,[29] whereas, on the Au plate, the accumulated carriers are expected to be congregated much closer to the outmost surface due to the small Thomas–Fermi screening length of Au (<0.5 Å).[30,31] Thus, in the IL/ZnO EDL structure, the distance from the electron accumulation layer to the IL/ZnO interface is apparently larger than that in the IL/Au EDL from the accumulation layer to the IL/Au interface, and thus, the capacitance difference between the two cases occurs.

2.3. Low-Temperature Behavior of the Accumulation Layer in IL/ZnO EDLTs

Low-temperature transport properties of the carriers accumulated at room temperature were measured at several values of gate bias V_G. As reported in Ref. [16], V_G was first applied at room temperature and then kept constant during the temperature decrease. An insulator–metal transition can be realized by IL gating in ZnO EDLTs, as in the case of EDLT using a $KClO_4$/PEO electrolyte.[16] Figure 5a summarizes the sheet resistance R_s of room temperature accumulation layer as a function of temperature. The particular device used in this R_s–T measurement showed a relatively high conductivity at $V_G = 0$ V, and thus a low on/off ratio. One can see that the R_s of EDLT at $V_G = 0$ V, where we probed the bulk properties of the ZnO crystal sample, increased dramatically as the temperature decreased, which is typical behavior for an insulator. At V_G values above 1 V, on the other hand, the channel resistance depended only weakly on temperature, indicating that the highly charged ZnO channel formed a metallic state. By electrostatically control, the insulator–metal transition was observed in the accumulation layer, and the highest room temperature sheet conductance of the highly charged channel could reach 5.3 mS for a metallic state.

Hall-effect measurements revealed the low temperature behavior of the room temperature accumulated carriers in a clear manner. In Figures 5b and c, the μ_H and n_s of the accumulation layer at different V_G values are plotted as a function of temperature (V_G applied from 300 K). For $V_G > 1$ V in Figure 5b, the μ_H in conduction channel increases, behaving as typical metals as the temperature is decreased, in sharp contrast to the μ_H reduction at $V_G = 0$ V. Remarkably, μ_H reached 250 cm^2 V^{-1} s^{-1} at 10 K and $V_G = 2$ V. As shown in Figure 5c, within the region from 300 to 1.8 K, the obtained n_s covered a large range from 2.0×10^{10} cm^{-2} ($V_G = 0$ V at 150 K) to 4.5×10^{14} cm^{-2} ($V_G = 2.5$ V at 300 K). The temperature dependence of n_s revealed that n_s decreases on cooling to 200 K. For $V_G = 0$ V, n_s vanishes completely below 200 K, reflecting the freeze-out of the bulk carriers. Even at the metallic state with a higher V_G, the accumulated high n_s still exhibits a substantial decrease as the temperature decreases from 300 to 200 K. The remaining carrier density at lower temperature was sufficient to keep the metallic state of the channel. The maximum remained n_s for the room temperature accumulated carriers is about 1.3×10^{14} cm^{-2} ($V_G = 2.5$ V below 200 K).

This n_s decreasing from 300 to 200 K is partly due to the ordinary insulator behavior of the bulk ZnO substrate as seen from the plot of $V_G = 0$ V. To exclude the contribution from the bulk ZnO crystal, we have estimated the effective capacitance of EDLT from the difference in the n_s at $V_G = 1.5$ V and 2 V, which is plotted in Figure 6 by red triangles. This effective capacitance represents the reduction in the accumulated channel carriers in the EDLT at low temperature. We attribute this decrease in n_s to the reduction of the effective gate potential drop on the EDL. In the equivalent circuit of EDLTs, shown in the inset of Figure 5c, the Pt-gate/IL/ZnO sandwiched structure is regarded as a series of impedance of EDL and bulk IL. At room temperature, the

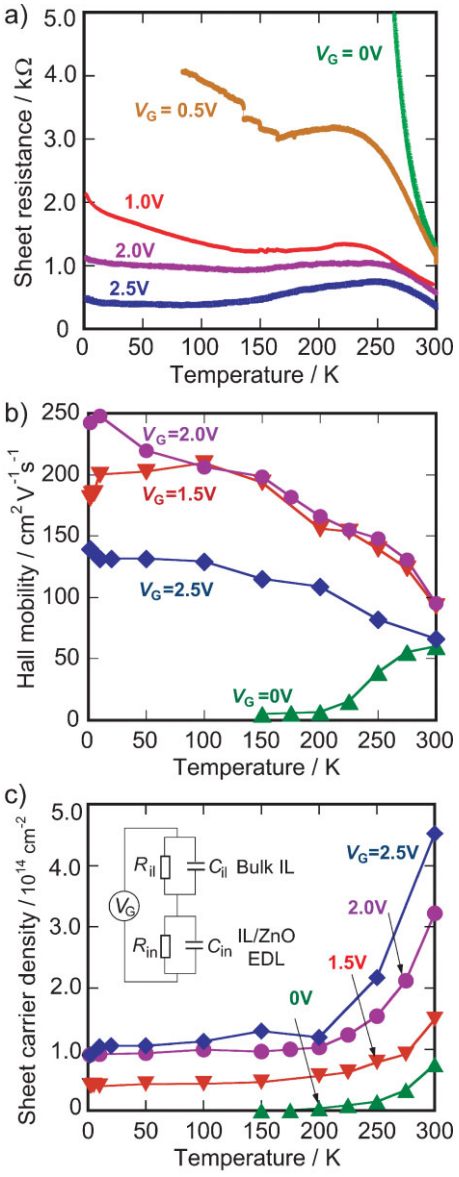

Figure 5. Temperature dependence of resistance and Hall-effect measurements for the IL/ZnO EDLTs. a) sheet resistance R_s, b) Hall mobility μ_H, and c) sheet carrier density n_s at several values of V_G. Here, the gate voltage was applied at room temperature followed by cooling with fixed V_G values. The inset in (c) is the equivalent circuit of IL/ZnO EDLTs. R_{in}, C_{in}, R_{il}, and C_{il} are the resistance and capacitance of the IL/ZnO interface and bulk IL, respectively.

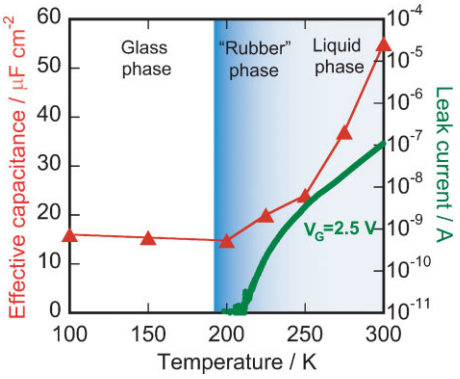

Figure 6. Low-temperature behavior of the accumulation layer in IL/ZnO EDLTs gated at room temperature. The leak current of EDLT between gate and source electrodes at $V_G = 2.5$ V applied from room temperature (the green curve), and the effective capacitance (the red triangles) as a function of temperature. The latter was obtained from the difference in n_s at $V_G = 1.5$ and 2.0 V by $\Delta n_s/0.5$ V, representing the reduction of accumulated charges on cooling.

potential drop between ZnO and the gate electrode is dominated by the EDL because the impedance of bulk IL is negligibly small owing to its high ionic conductivity. However, ionic conductivity is dramatically decreased when the IL is cooled, greatly enhancing its impedance. This is indicated by the exponential decrease in the leak current of EDLT with temperature reduction (shown as green curves in Fig. 6). Consequently, the increase in impedance of bulk IL, which is comparable to or even larger than that of EDL, results in the decreased gate-potential drop at the EDL. This should be the cause of the reduction of effective capacitance, i.e., the reduction of accumulated charge density on cooling from 300 K.

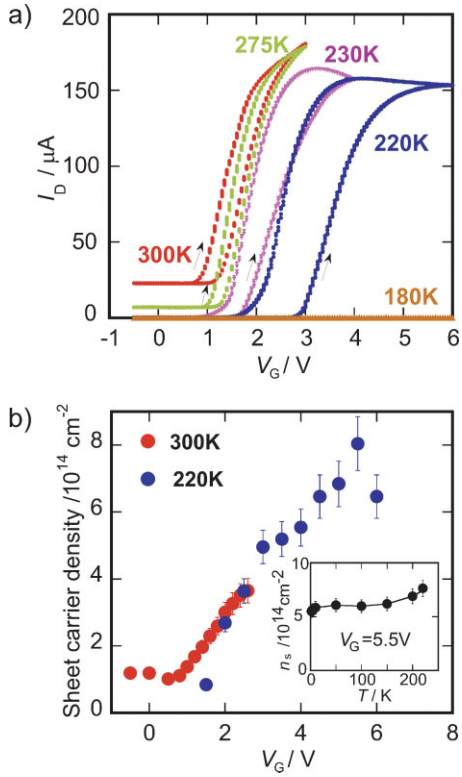

Figure 7. Low-temperature characteristics of supercooling IL-gated ZnO EDLTs, with $V_D = 100$ mV. a) Transfer curves recorded at 300, 275, 230, 220, and 180 K at a V_G scan speed of 20 mV s^{-1}. b) Sheet carrier density n_s as a function of V_G, obtained by Hall effect measurements at 300 and 220 K. The inset is the temperature dependence of n_s in the highly charged layer accumulated at 220 K with $V_G = 5.5$ V.

2.4. Ultra-high-Density Carrier Accumulation at Low Temperature

To achieve high-density carrier accumulation at low temperature is of great importance, where one is interested in investigation of the electronic phase transition phenomena in condensed electron systems.[1,2] As mentioned in previous section, when the gate bias was applied at room temperature for carrier accumulation, there was an unexpected decrease in the carrier density (Fig. 5c). However, we found that the gating capability of supercooled state of IL enabled us to avoid the decrease in carrier density at low temperature. Figure 6 shows the leak current I_G and the effective capacitance of room temperature accumulated EDLTs as a function of temperature. From 300 to 230 K, the monotonous logarithm reduction of I_G suggests that there is not clear liquid-to-solid transition in the IL with a cooling rate of 0.5 K min^{-1}. This may be due to the widely observed supercooling properties of ILs and the low temperature state near 230 K, referred to as the "rubber" state.[32–34] Importantly, the mobile ions in the supercooled (namely, rubber) state of the IL still can electrostatically modulate the carrier accumulation at IL/ZnO interface by the gate bias. Figure 7a shows the I_{DS}–V_G characteristics of EDLTs at varied low temperatures. One can see that the IL-gated field effect in EDLTs could be realized at low temperatures, even down to 220 K. In the rubber phase of the IL, the ion motion and hence the response time of the EDLT is gradually slowed, as seen from the large hysteresis in the EDLT transfer curve at 230 and 220 K in Figure 7a. Further decrease in temperature induced the well-known glass transition from rubber phase to glass state, taking place at $T_g = 190$ K, where the mobile ions in the IL are completely frozen. In the glass phase, the current modulation by electrostatic gating control was not available, shown by the plot of 180 K in Figure 7a. More importantly, the gate bias that can be applied increases with a decrease in temperature. At room temperature, the applied V_G is limited by the electrochemical window of the IL (~2.7 V). In sharp contrast, at low temperatures, we can apply a V_G of as high as 6 V without device degradation and dielectric breakdown, possibly owing to the decreased electrochemical activity of the ILs. The saturation behavior in the I_D–V_G curve in Figure 7a is possibly due to the enhanced surface scattering as well as the scattering by the cation Coulomb potentials of the IL at the EDL.

Since we are now able to apply higher gate biases at lower temperatures, it is intriguing to see how much charge can be accumulated at 220 K with a high V_G. Figure 7b shows the gate bias dependence of n_s at 220 and 300 K by the Hall-effect measurement. A maximum carrier density of 8×10^{14} cm^{-2} was achieved at 220 K with a higher applied V_G of 5.5 V. This carrier

density corresponds to 0.19 electrons per Zn, assuming that the charges are distributed uniformly in the 1-nm-thick accumulation layer of ZnO. One can see that the room-temperature capacitance deduced from the n_s–V_G curve in this device is exactly consistent with that of the IL/ZnO EDLTs shown in Figure 4. The inset of Figure 7b shows the temperature dependence of n_s accumulated at 220 K gated by 5.5 V. The high carrier density was almost temperature independent below T_g, keeping constant above 5.5×10^{14} cm^{-2} even at 1.8 K. Such a high carrier density, available in IL/oxide EDLTs, demonstrates a new capability of the heterogeneous interfaces between oxide semiconductors and IL.

3. Conclusions

In summary, by using an IL as gating dielectric, high-performance IL/ZnO EDL transistors have been demonstrated with a high transconductance and high carrier densities of up to 4.5×10^{14} cm^{-2} at room temperature in a fast, reversible, and reproducible manner. The capacitance of IL/ZnO EDLTs, as large as 34 μF cm^{-2}, determined by Hall-effect measurements, played a crucial role in the high-density carrier accumulation and the insulator–metal transition. Hall-effect measurements revealed that the n_s accumulated at 300 K decreases by a factor of two or three on cooling to 200 K due to the reduction of the voltage drop on the EDL with decrease in temperature; however, in the rubber state of the IL at low temperatures a higher V_G can be applied, giving an effective method to further increase the carrier density up to 8.0×10^{14} cm^{-2} at 220 K, and to keep a very high value of 5.5×10^{14} cm^{-2} down to 1.8 K. These findings provide us with new opportunities for fundamental research on electron correlation phenomena, such as field-effect-induced superconductivity, in condensed electron systems.

4. Experimental

The IL *N*,*N*-diethyl-*N*-(2-methoxyethyl)-*N*-methylammonium bis-trifluoromethylsulfonyl)-imide (DEME-TFSI) used in this study was purchased from Kanto Chemical Co. The electrochemical potential window of this compound was −3 V to +2.7 V, determined using Ag/AgCl as a reference electrode. The capacitance measurement of IL EDLC on Pt/IL/Au sandwich structure with a channel surface area of 1.0×10^{-3} cm^{-2} was carried out by using an impedance spectrum analyzer with the frequency of applied ac voltage of 5 mV from 0.01 Hz to 0.1 MHz. The EDL capacitance C_{EDL} was derived from the equation $C_{EDL} = 1/(2\pi f Z'')$, where f is the frequency and Z'' is the imaginary part of the impedance.

Atomically flat polar ZnO surfaces were obtained by annealing ZnO single crystal substrates (5×5 mm^2, Furuuchi Chemical Co.) at 1000 °C for 1 h. EDLTs on both Zn- and O-polar ZnO surfaces were systematically examined (a detailed report on polarity dependence of ZnO EDLT will be published elsewhere). Here, we focused on EDLTs fabricated on Zn-polar ZnO surfaces. Ti/Au ohmic electrodes with thickness 30 nm/100 nm were evaporated on ZnO as Hall-bar patterns with the dimensions 500×200 μm^2. Au wires were bonded to the pattern by silver paste, and the device surface was passivated with silicone adhesive sealant (TSE397, GE Toshiba Silicones) except for the transport channel. After immersing the channel surface and the Pt gate electrode into an IL, a typical IL/ZnO EDLT was fabricated. Controlling the alignment of the gate electrode and the thickness of IL dielectrics was less important because a nanoscale capacitor spontaneously formed at an IL/ZnO interface as the gate was biased.

The transport characteristics of all IL/ZnO EDLTs were measured by a combination of a Physical Property Measurement System (PPMS, Quantum Design) with an Agilent 5270B semiconductor parameter analyzer. A small source-drain voltage of 100 mV and a fast V_G sweep speed of 20 mV s^{-1} were used to measure the transfer characteristics of EDLTs by the four-probe method. The Hall-effect measurement was carried out in the constant-current mode with a relatively large current of 1 μA to obtain a detectable Hall voltage for the instrument. The temperature dependence of the channel resistivity and Hall effect were measured at a fixed V_G, applied from 300 K or 220 K to accumulate charges before going to lower temperatures. All electrical measurements were performed in a vacuum of about 10^{-1} Torr since the EDLCs were found to be sensitive to both oxygen and humidity. Particularly, oxygen completely killed the charged carriers. Under vacuum, more than 20 measured EDLT devices behaved in a very reproducible manner.

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