Recent Progress in Organic Electronics: Materials, Devices, and Processes

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Research in organic electronics has included advances in materials, devices, and processes. Device architectures, increasingly complex circuitry, reliable fabrication methods, and new semiconductors are enabling the incorporation of organic electronic components in products including OLED displays and flexible electronic paper.

Introduction

Organic electronics as a field of study has come a long way in the past 10 years. From a literature search covering many of the available R&D materials databases, and using the search terms "organic thin film transistor," 12 publications were found for 1993, but well over 300 were found for 2003! If the search is broadened to include organic thin film electronic devices such as memory, photovoltaics, and organic light-emitting diodes (OLEDs), over 40,000 publications are found for the period of 1998−2003. This implies a very active research subject spanning many areas, including materials development, device design, deposition processes, and modeling. More researchers continue to join the field, with few dropping out each year, even though, as a community, we still await the key applications that may drive organic electronics toward mature industrial persistence. Several companies are in the process of bringing the first commercial organic electronic products to market, with Pioneer's OLED car stereo display, launched in 1998, Motorola's Timeport color OLED cell phone, using Pioneer's display,[1] and Kodak's color OLED digital camera.[2] Although all of these devices are OLED with traditional Si-based backplanes and control electronics, they are a tremendous step toward realizing an organic share of the electronics markets. Additional progress is being made in active matrix backplanes using organic semiconductors by Philips[3] and others,[4] and a smattering of articles implies progress in organic sensors,[5] organic memories,[6] and possibly smart textiles.[7] One aspect we should not neglect as a technological community is competition—the downward march in the cost of silicon-based electronics,[8] the emergence of hybrid organic/inorganic systems,[9] and the concept of systems designed to combine the performance of silicon-based electronics and functionality of organic components for sensing, flexibility, and actuation.[10] In addition, recent reports decoupling fabrication of high quality, single-crystal Si semiconductors from lower-temperature processing steps present potential alternative approaches toward the realization of low cost electronics.[11] Since all approaches face similar challenges and address similar markets, organic electronic solutions must provide unique advantages such as cost, flexibility, functionality, or appearance.

In terms of review, we wish to use this space to highlight the areas of recent progress, including some of our own results, which we believe are essential to the continuing development and successful commercialization of organic electronics. Rather than a comprehensive review, we will present some of the highlights of the last several years with a focus on materials, devices, and manufacturing methods.

Semiconductors

Pentacene has continued to be the most widely used small molecule semiconductor primarily due to routinely obtainable thin film transistor hole mobilities in excess of 1 cm^2/Vs. Researchers are beginning to investigate long-term and operational stability in pentacene devices,[4c,12] but pentacene still remains the most reliable benchmark material for vapor-deposited thin film transistors (TFTs). Recent reports have increased awareness that charge carrier mobility is not the only device parameter to consider, and for some applications, may not even be the most important. For RFID applications, mobility and threshold voltage may be critically important, but for display backplanes, threshold voltage stability and off current may be the key parameters.[13] Many reports have been made using pentacene in thin film devices,[9a,14] but several other materials have also shown promise, deposited from either the vapor phase or through solution delivery routes. Notable results include reports on tetracene (naphthacene),[15] rubrene,[16] oligoacenes,[17] modified[18] and precursor pentacenes,[19] oligothiophenes,[20] and polyfluorenes.[21] Researchers have shown that thiophenes can often be made soluble and maintain higher mobilities, typically through the addition of alkyl chains.[22] Xerox Research Centre of Canada in collaboration with PARC reported printable dispersions of a thiophene-based material.[23] Organic n-type materials[24] remain challenging due to rapid degradation in mobility and on/off ratio, although recent reports showing improved oxidative stability and mounting

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mobilities are encouraging.

Pentacene, in one form or another, remains the most widely reported organic semiconductor for thin film transistor development. Early reports[25] of vapor-deposited pentacene TFTs claimed exceptional mobilities of 2−3 cm^2/Vs and more recent results from our group, and separately from Infineon, have claimed mobilities of 3−4 cm^2/Vs, through the use of self-assembled monolayer surface modifications.[26] We recently reported average mobilities of 5 cm^2/Vs, using a polymeric surface treatment.[27] Improved growth in the first molecular layers is a likely cause of the improved performance, and may be due to a combination of effects, including smoothing of the dielectric, the modification of the surface energy resulting in a near match to the pentacene being deposited, or the presentation of a more uniform surface chemistry than is typically found in metal oxide dielectrics. Researchers have also begun to report their efforts to model and explain the nucleation and growth of organic semiconductor thin films.[28] It is interesting to note that the University of Groningen recently reported ultrapure pentacene single crystals with exceptionally high mobilities, in excess of 35 cm^2/Vs, obtained through space charge limited current measurements,[29] possibly setting a new point of reference for comparison with TFTs. In addition, Rutgers University reported elevated field effect mobilities in rubrene single crystals, as well as the behavior of contacts and mobility as a function of temperature.[30] These reports of exceptional organic semiconductor mobilities on single crystals could give us additional insight into the nature of high mobilities in thin films as well.

Due to the insolubility of pentacene, solution delivery routes have been very limited, although several approaches to solubilized pentacene through conversion from solvent-based precursors have been developed.[19] These approaches typically use thermal conversion of soluble precursors, and the resultant TFT mobility is typically less than 0.1 cm^2/Vs, much lower than through vapor deposition routes. Even so, TFT properties using these materials appear sufficient to make functional arrays. Philips recently reported pentacene TFTs converted from such a spincoated precursor solution,[19c] resulting in functional backplane arrays for electrophoretic displays. This approach allows them to use traditional fabrication processes, such as spincoating and photolithography, to begin exploring the utility of merging lower cost materials and flexible substrates.

Tetracene−Bithiophene

We also report here our latest synthetic effort, tetracene-bithiophene, and its device performance and morphology as a function of substrate temperature. A Stille coupling between 2-chlorotetracene and 5-tributylstannyl-2,2′-bithiophene [31] was used to prepare 5-(2-tetracenyl)-2,2′-bithiophene (tetracene-bithiophene), which was then purified to device quality by gradient sublimation. Approximately 50 mg of the purified material was charged in a crucible and placed in a vacuum chamber with test substrates comprised of silicon wafers with alumina sputtered on the front and Al sputtered on the back (Silicon Valley Microelectronics, 1500 Å sputtered alumina, 5000 Å Al backside gate). Samples were coated with 300 Å of thermally evaporated tetracene-bithiophene deposited at 2×10^{-6} T at a rate of 0.5 Å/s, at 5 different substrate temperatures.

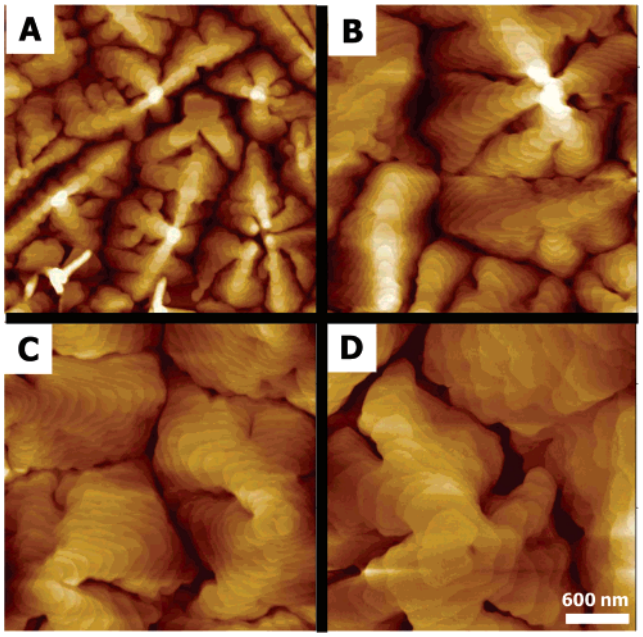

Figure 1. AFM images of tetracene-bithiophene vacuum deposited on alumina substrates held at (A) room temperature, (B) 60 °C, (C) 75 °C, and (D) 100 °C.

The Tapping Mode (Trademark, Digital Instruments) atomic force microscope (AFM) images in Figure 1 show morphological changes indicating increased crystallite size at the higher temperatures (5 separate deposition runs), corresponding to a slight increase in TFT mobilities. Image A was obtained from a sample deposited on a room-temperature substrate; image B from a sample deposited on a substrate held at 60 °C, image C from a sample deposited on a substrate held at 75 °C, and image D from a sample held at 100 °C. An image was also obtained (not included here) for a sample deposited on a substrate held at 125 °C. This image was flat and featureless, and the TFTs were nonfunctional. We conclude that at substrate temperatures of 125 °C, no film formation occurs. It can be clearly seen from the AFM images that grain size increases with increasing substrate temperature. All images share the same z-scale of 30 nm, and there is a slight decrease in grain height (lesser number of terraces) with increasing temperature. Closer inspection of the images also reveals greater interconnectivity between grains for images B and C, corresponding to slightly better device mobilities, and a drop in the interconnectivity for image D, also corresponding to a dip in the mobility. Similar behavior has been reported for pentacene devices as a function of deposition conditions, and seems to indicate that the first several device layers, and the extent to which they are connected across large areas of the substrate, are more important to determining mobility than are more obvious features, such as grain size.[25,27] In Figure 1 grain size dramatically increases with increasing substrate temperature, but the largest grains showed devices with a lower mobility, implying that grain size alone is not well-correlated with device performance. A typical TFT trace from this set of samples is shown in Figure 2, and averaged TFT characteristics are summarized for the samples of

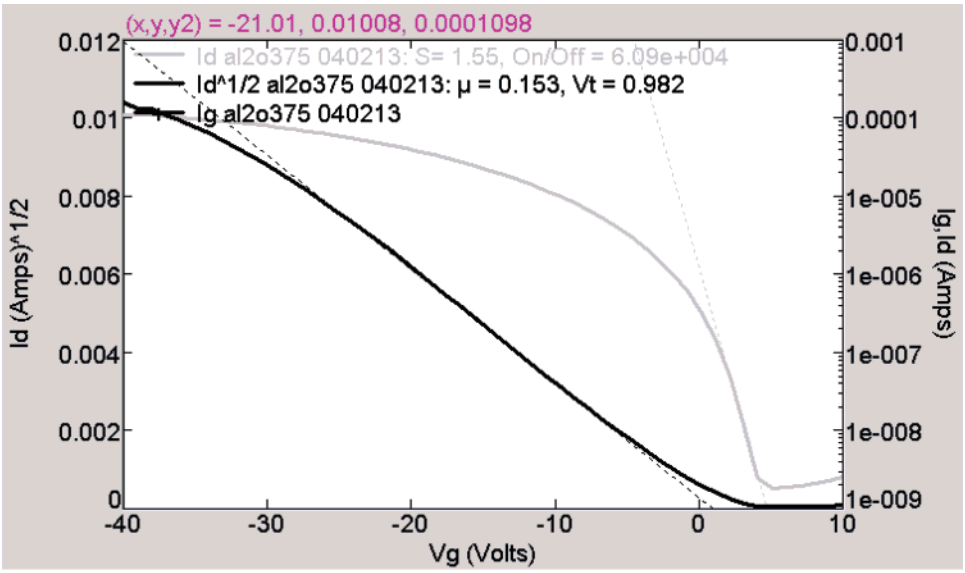

Figure 2. Representative output characteristics for tetracene-bithiophene TFTs on alumina. These characteristics were taken from a single device trace, where the substrate was held at 75 °C during deposition. Transfer characteristics were obtained at $V_d = -40$V, with V_g swept from +10 to −40 V.

Table 1. TFT Output Characteristics for Tetracene−Bithiophene Device Series Described in Figure 1

substrate T (°C)	mobility (cm^2/ Vs)	threshold voltage (V)	subthreshold slope (V/dec)	on/off ratio
25−35	0.067	−2.5	1.8	1.1×10^5
60	0.13	+0.3	2.8	2.4×10^4
75	0.15	−0.2	2.0	2.6×10^4
100	0.08	−0.2	2.4	1.8×10^4
125	N/A	N/A	N/A	N/A

Figure 1 via the device parameters at varying temperatures shown in Table 1. Results shown in the table are averages of measurements on three separate TFTs for a single deposition run at each temperature.

Device Layers

While the development of semiconductor materials and processes has been critical, other important materials challenges remain with insulators and electrodes. Inexpensive, nonoxidizing electrodes present a challenge, and many groups have chosen to use very thin layers of traditional noble metals, including Au, Pd, and Pt, and have explored potential uses of other metals including Al, Cr, Cu, and Ni. Additionally, surface modifications have been performed on metal contacts to alter their injection properties,[32] either through serving as an organic template to promote more favorable crystal growth or to reduce the charge injection barrier to the semiconductor. Even so, ohmic contacts to organic semiconductors are not well understood, although X-ray photoemission spectroscopy (XPS) and microscopic resistance measurements are beginning to contribute to the understanding of the organic−metal interface.[33] Additionally, the resistance requirements in extended device constructions are, in some cases, poorly defined. Groups have attempted to use solution-derived conductive layers in devices, including conducting polymers such as polyaniline and PEDOT:PSS,[34] as well as some particle-based inks.[35] Conducting polymers often contain dopants to boost conductivity, which may migrate during device operation, and possibly affect the operational stability of devices. Particle-based systems often require small-molecule, amphiphilic stabilizers to maintain solubility, and these stabilizers likely increase resistance of the particle-based coated layers, or must be volatilized in an effort to sinter the coated layers.[35] Either way, some contamination, either mobile or attached to the coated particles may remain behind, and could contribute to device instabilities. Polymeric and particle-based systems present an added challenge when fabricating devices on polymeric substrates, in that solvent must be removed and/or particles must be sintered, often at temperatures exceeding 150 °C, requiring designed plastics such as polyimides and PENs that withstand the thermal loads.

High quality, low-temperature dielectrics and nondamaging encapsulants each present challenges as well. Recent reports have included designed systems where the semiconductor and dielectric are tethered, leading to an interface formed through phase segregation, while simultaneously allowing two deposition steps to be combined.[36] As mentioned above, several groups have reported dramatic improvements in device performance through the use of directly applied surface modifications on top of the dielectric itself. Other groups have demonstrated high performance TFTs using polymeric dielectrics or high dielectric constant inorganic layers.[37]

As a further complication, the seemingly best materials combinations for devices often present manufacturing issues such as throughput, increased equipment cost, solvent sensitivity of previously deposited layers, temperature constraints, or reproducibility limitations over extended areas. Solution deposition of device layers also requires independent solvent systems to avoid mixing of the applied layers with those already coated. The interfaces between these device layers, those deposited both from solution and from the vapor phase, also appear to be critically important, as indicated above, but designing in control of those interfaces often adds additional process steps and/or complexity to the devices.

In any case, more devices are made each year, and improvement continues. In Figure 3 we compare the

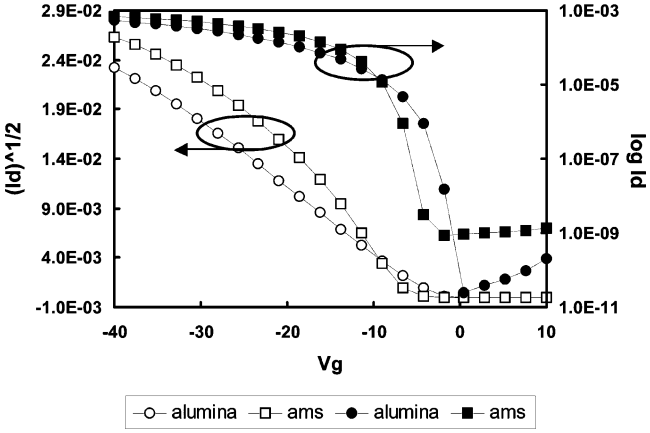

Figure 3. Pentacene TFT output characteristics for untreated alumina device (circles), compared to surface treated alumina (squares).

output characteristics for TFTs prepared with an untreated alumina dielectric and a poly(α-methyl styrene) treated alumina dielectric. Device results shown in Figure 3 were prepared as follows: pentacene (Aldrich Chemical) was purified once by gradient sublimation at reduced pressure (~5 T) with a carrier gas of 2% H_2 in N_2 flowing at 35 sccm, and a maximum source of temperature of 300 °C. Wafers were obtained as above (Silicon Valley Microelectronics, 1500 Å sputtered alumina on doped Si wafers, with 5000 Å Al serving as backside gates). Pieces of one wafer quarter were used as received for the untreated alumina, and a second quarter was spincoated with a 0.1 wt % solution of poly(α-methylstyrene) from toluene (500 rpm for 20 s, 2000 rpm for 40 s), dried in an oven for 30 min at 100 °C, and pieces were cleaved for the treated alumina samples. At a chamber base pressure of 2×10^{-6} T and a rate of 0.5 Å/s, 50 mg of purified source material was charged into a crucible/wire basket thermal source and deposited onto the selected samples, to a final thickness of 300 Å. Samples were removed from the chamber and placed in a second vacuum chamber where 600 Å of Au was thermally evaporated (base pressure of 4×10^{-6} T and a rate of 5 Å/s) onto the samples through a Si shadow mask to complete the TFT construction. Device parameters extracted from the curves, under saturation conditions, are as follows: (for treated alumina dielectric) mobility, $\mu = 6.4$ cm^2/Vs, threshold voltage, $V_t = -6.3$ V, subthreshold slope, $S = 0.96$ V/decade and on−off ratio = 1.5×10^7; (for untreated alumina dielectric) $\mu = 1.5$ cm^2/Vs, $V_t = -3.8$ V, $S = 0.85$ V/decade, and on−off ratio = 1.9×10^7. These values were taken from single devices, although they were representative of several TFTs measured on each sample.

Processing

We achieved a measure of process control with our high mobility devices: repeatable transistor characteristics with average mobilities of 5 cm^2/Vs, achieved consistently over a six-week period where the vacuum chamber was dedicated to pentacene depositions. This optimized process for test structures was successfully transferred to fully patterned integrated circuits, as shown in Table 2. Table 2 compares results obtained from transistors fabricated on test structures (prepared wafers where we spincoated a surface treatment, deposited a blanket layer of pentacene, and patterned Au source and drain pads); and integrated circuits, where we build up all four patterned layers of a TFT on glass substrates (e-beam evaporated Ti/thermally evaporated Au (15/600 Å) gate layer, e-beam evaporated alumina layer (1500 Å), spincoated surface treatment, thermally evaporated pentacene semiconductor layer (300 Å) and thermally evaporated Au source and drain, 600 Å). Integrated circuit layers are patterned using flexible polymeric shadow masks fabricated by laser ablation. Holes in each mask correspond to features we wish to produce on the integrated circuit substrate. For each circuit design, we typically use four differently patterned aperture masks, one for each device layer, which are aligned by hand under a microscope using clamping jigs and/or micromanipulators. Interconnects for the integrated circuits are formed as combinations of the features in the gate and source/drain layers. Additional layers may be added for encapsulation or the construction of more complicated device structures.

Table 2. Extracted TFT Parameters for High Quality Alumina Test Substrate (Purchased Wafer Substrate, Blanket Layer of Pentacene, Patterned Source and Drain Electrodes), Compared to E-beam Deposited Integrated Circuit (Four Patterned Device Layers, Built Up on Glass Substrate)

	high-quality alumina	e-beam deposited alumina
mobility	5.35	5.28
threshold voltage	−6.2	−4.8
subthreshold slope	0.8	2.4
on/off ratio	8.5×10^5	2.8×10^6

Under more typical lab conditions, where the chamber is shared for a variety of materials depositions, average integrated circuit mobilities are ~3 cm^2/Vs. Although the average surface roughness of the deposited oxides is often a factor of 10 higher than on the test oxides, the mobilities are similar. The high TFT mobilities we have been able to achieve in the lab encouraged us to fabricate organic integrated circuits.

It has been encouraging to see several reports of increasingly complicated devices that require more complete understanding of overall device performance (on/off ratio, threshold voltage and its stability, and mobility) as well as lifetime, stability, interconnects, and contact resistance.[38] Rough specifications are beginning to emerge, centered on broad classes of applications such as RFID and displays. We too have made initial efforts to understand device behaviors. Figure 4 shows results taken from samples with measured mobilities of ~2 cm^2/Vs, where characteristics were obtained via a stepped voltage sweep and a pulsed voltage sweep to investigate some of the threshold voltage changes often present in these devices, as first reported by researchers at PARC.[12b] Figure 4 shows two I_d-V_g traces for two separate pentacene TFTs fabricated simultaneously, one obtained via the stepped sweep and one via the pulsed voltage sweep methods. Although output device parameters are nearly identical, a marked difference in the high V_g region of the curves can be seen. Researchers have speculated that this current rollover at high gate voltage seen via the stepped sweep has been attributed to charge collecting at the contacts. Alternate explanations include charge trapping at the dielectric interface, contributing to a shifting threshold voltage during the

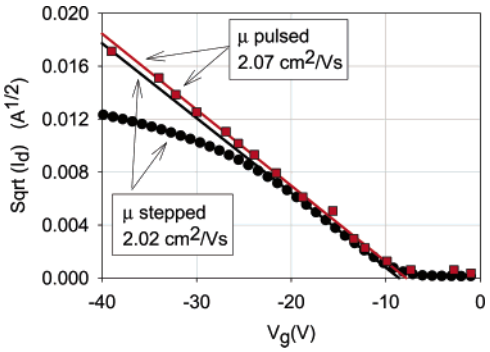

Figure 4. Stepped vs pulsed gate voltage output characteristics of pentacene TFTs on alumina, bearing a polymeric surface treatment.

sweep.[12b] Experiments to understand the origin of this high voltage rollover are in progress in several groups. The pulsed scan remains linear to the end of the voltage sweep, indicating that the threshold voltage shift is minimized during the measurement, allowing for a more accurate extraction of device parameters.

Further work is underway in our labs to investigate this high gate voltage behavior for TFTs with higher mobilities, where stepped voltage sweep measurements often show more extreme departure from ideal curves. If the pulsed gate voltage measurements can highlight differences between charge injection and trapping in the TFTs and their constituent layers, it may help us better understand the nature of high-mobility pentacene devices.

Integrated Circuits and Devices. RFID

Integrating organic semiconductor-based TFTs was accomplished early on by some of the pioneers in organic electronics. Jackson's group, Lucent, and IBM were among the first contributors to publish results from integrated organic TFTs and to explore the boundaries of these new electronic materials.[39] Eager to see if our elevated mobilities enabled new or more complicated device constructions, we built inverters and ring oscillators and measured their output characteristics against literature reports of similar circuits. More complex circuits began to seem feasible, and we designed our first radio frequency transponder circuit components: ring oscillators as logic, rectifiers, and large gate-width TFTs as current amplifying output buffers.

Radio frequency identification (RFID) is a very broad-based technology that encompasses many application areas where identification, verification, tracking, and/or general logistics are important. An RFID system is generally comprised of a single reader instrument and many transponder circuits (tags). The transponders are attached to an article that needs to be identified. The reader and transponder communicate, typically with near-field or far-field electromagnetic coupling. Depending on the application the performance requirements of an RFID system can vary substantially.[40] For example, some applications require the ability to periodically write (store) information on the transponder circuitry, while others may require greater read ranges (the distance between the transponder and the reader). There are a number of RFID primers available (e.g., Finkenzeller, referenced above) that should be consulted for a more in-depth discussion of this technology. For

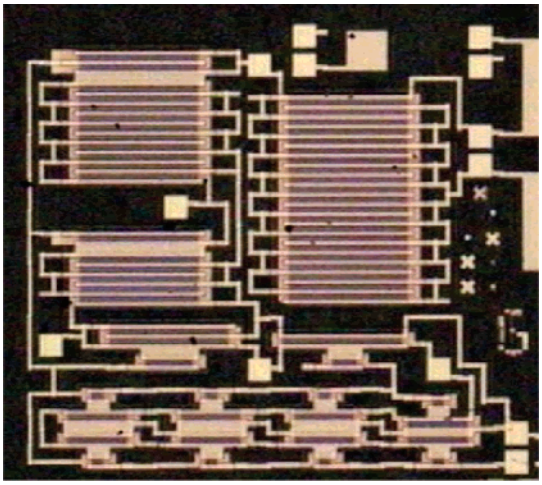

Figure 5. Optical micrograph of four-layer patterned one-bit rf transponder circuit designed for dc operation. Large serpentine TFTs serve as amplification stages. Channel lengths of the TFTs are 20 μm.

RFID applications where there are a high number of articles to track, the price of the transponder becomes important. The low-cost RFID area has long been viewed as a potential opportunity for organic electronics, with the presumption that nonphotolithographic patterning methods, room temperature processing, and simple RFID circuit architecture would result in transponder circuitry at a significantly lower cost than traditional Si tags. The work presented in this section summarizes our efforts to design, fabricate, and characterize a one-bit RFID transponder circuit.[41]

In most cases, pentacene devices have positive threshold voltages, which require additional transistors to compensate,[19c,42] making even simple integrated circuits more complicated and slowing down the overall switching speed of the devices. Jackson et al.[15a] reported tetracene devices with negative threshold voltages fabricated using vapor deposition, enabling faster circuits through simplified device construction. Even though the mobilities of tetracene TFTs were significantly lower than those for pentacene devices, similar circuits made using tetracene as the semiconductor were faster than pentacene circuits due to the simplified circuit layout. Our group observes negative threshold voltages in our pentacene devices, enabling us to take advantage of the higher mobility of pentacene without the need for additional level-shifting circuitry to compensate for the threshold voltage.

We wanted to design and fabricate an organic-semiconductor-based integrated circuit that could communicate one bit of information to a near-field reader system operating at one of the common FCC-regulated RFID carrier frequencies. These bands include 125 kHz and 13.56 MHz. We used hand-wound copper wire for the transponder inductor, and a discrete (non thin-film) resonant capacitor, focusing our development on the pentacene-based circuitry. We note here that as the chip portion of the RFID tag becomes cheaper, the antenna becomes the most important cost element of the transponder, and many groups are exploring how to reduce its cost.

The one-bit transponder circuit that we designed and fabricated, shown in Figure 5, and initially reported in

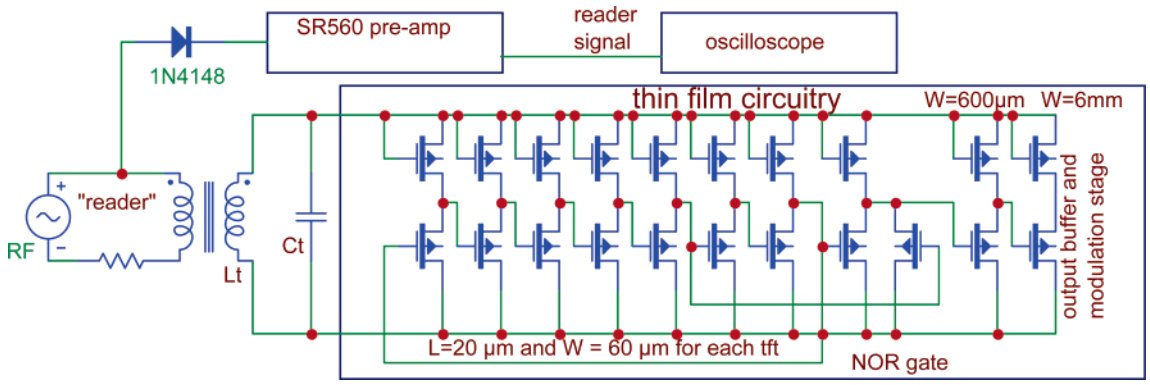

Figure 6. Circuit diagram of ac-powered one-bit rf transponder circuitry shown in Figure 8.

Applied Physics Letters,[39] was demonstrated using direct application of an ac signal at a range of rf frequencies. Pentacene-based transponder circuitry had not been previously reported. Energy absorbed by an inductor/capacitor resonant tank directly powered the pentacene-based logic and modulation circuitry, without the need for a rectification stage. Sufficient modulation of the rf was obtained at 125 kHz, and well above 5 MHz to be detected externally with a simple peak detector circuit.

We optimized the design of our rf circuitry for ac powering and incorporated it in the circuitry discussed below. This design incorporates a 1:1 load-to-driver gate width ratio, a design that would not function under dc power. Lastly, in the output gain stages of our RFID architecture, the impedance matching is accomplished with fewer amplification stages than in the dc design. Only two stages are needed in the ac design, whereas five are needed for dc. Since each amplification stage is large, this has the effect of reducing the overall circuit area. Comparing the dc design, which requires a rectification stage, the ac design with fewer amplification stages (and no need for a rectification stage) requires half of the substrate area for full function.

The circuit diagram in Figure 6 shows the design for our ac-powered one-bit tag. Most of the tag and reader (demodulation) components are the same as for the dc design, but there are three distinct differences. The gate width ratio between the driver and load TFTs, in this case, is 1, and in the case of the dc-powered design the ratio was 5. Similarly, the output stages have a driver-to-load gate width ratio of 1, compared to 5 in the dc design, and again, there are fewer stages in the ac design. We based this design on our standard pentacene TFT model with a nominal mobility of 1 cm^2/Vs. Higher mobilities only seem to improve tag performance, but a minimum mobility of $\sim$1 cm^2/Vs is required, particularly for higher carrier frequency operation. Finally, two nodes of the ring-oscillator are tapped and fed into an NOR gate that produces a pulse each time the nodes are low, which occurs once per oscillator cycle. This feature forms the basis for more complicated (multibit) tag designs wherein n pairs of this scheme are produced to generate n pulses per ring-oscillator cycle.

Figure 7 shows two inverters in the ring-oscillator of the ac-powered one-bit tag.

What is readily apparent is the larger electrode on the driver TFT. This large gate/source overlap area provides for additional, and desired, load capacitance for each stage. This additional capacitance has the effect of filtering out more of the rf signal and maintaining the output during each rf cycle, at the cost of slightly reducing the oscillation frequency and increasing the logic gate size. This aspect of the design allows improved performance over the dc design, without reliance on a rectification stage.

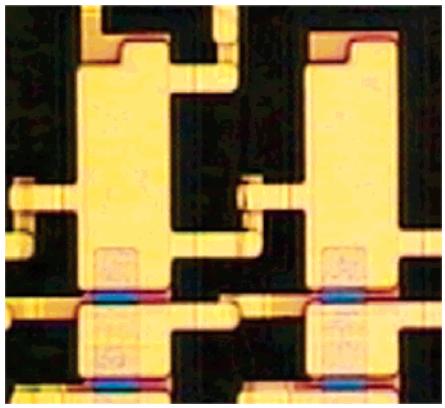

Figure 7. Optical micrograph of two inverters fabricated following the ac powering design described in the text. Channel lengths are 20 μm.

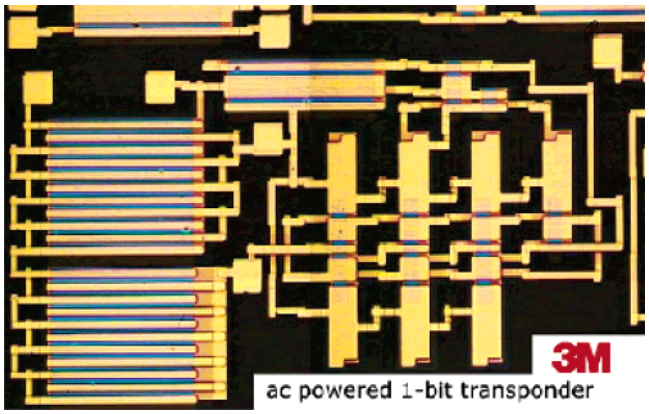

Figure 8. Optical micrograph of one-bit rf transponder circuit fabricated according to the ac-powering design, showing the seven-stage ring oscillator and output buffers described in the text.

Figure 8 shows the completed pentacene-based one-bit RFID tag with a seven-stage ring oscillator, an NOR gate, and two output inverters. The fabrication process flow is very similar to that discussed above. The gate metal is Ti/Au (20 Å/750 Å, respectively), the gate dielectric is Al_2O_3, e-beamed in the presence of oxygen, and the semiconductor is 300 Å of pentacene, thermally evaporated from a crucible. The source/drain metal is

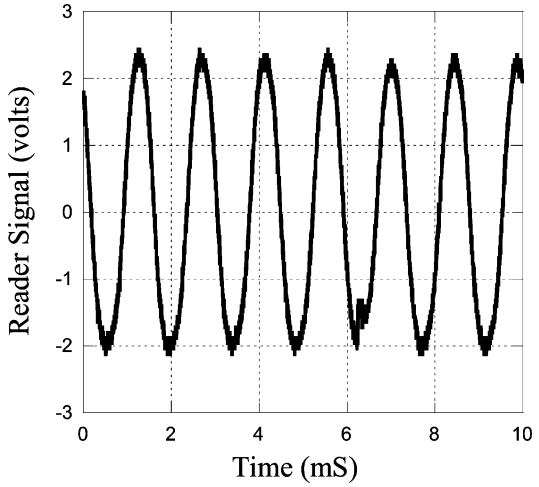

Figure 9. Output signal of one-bit rf transponder shown in Figure 8, with the NOR gate disabled.

thermally evaporated gold. Poly (α-methyl styrene) was spun cast onto the dielectric as part of a surface treatment process that results in improved pentacene hole mobilities. All the layers were patterned using our polymer shadow masking scheme with 30-μm design rules, and 20-μm gate lengths.

In Figure 9, the output of the one-bit RFID tag is shown. In this case, the NOR gate has been shunted and the load modulator is being driven, essentially, by the output of one of the ring-oscillator nodes. The rf signal powering this circuit was derived from a hand-wound transformer with an air gap. The 'reader' side inductor was a single turn loop with an inductance of about 1 μH powered using a simple function generator and an EMI rf amplifier. The rf frequency for the data above was 4.079 MHz. The read range for this tag was approximately 2 cm.

Figure 10 shows results from the same circuit with the NOR gate functioning as intended. The reader output is identical in phase and frequency with the NOR gate output. The peak tag voltage was about 38 V as shown in the plot.

We have recently completed designs for transponder circuitry to store and communicate multiple bits of information to a reader. Remaining challenges include antenna development and reduction in the voltage required to power the tag.

Transistor Arrays

Arrays of TFTs can give insight into deposition uniformity and serve as an efficient means of generating performance statistics. Early work from Lucent and E-Ink showed the possibility of using organic TFT arrays in simple displays,[4a] and PARC has reported progress toward printing arrays of TFTs.[22] Making TFT arrays allowed us to explore the areal extent of our patterning capabilities, yield and deposition uniformity in our process, and the effect of high mobility TFTs in a display configuration. Figure 11 shows an optical micrograph of a single array TFT, patterned solely using polymeric shadow masks and using vapor-deposited device layers and a solution-cast surface treatment layer. Our early arrays were 25 × 25 pixel arrays for possible use as display backplanes. The arrays were patterned using a single approximately 8 in × 8 in shadow mask for each device layer (5 total layers, including an encapsulant to protect the TFTs from additional processing steps in adding a contrast medium). Each device layer was patterned using one contiguous shadow mask and a single vacuum pump down and deposition cycle. Our current efforts include understanding the variation in the output characteristics of TFTs and capacitors in the arrays, as well as failure mechanisms for each component. Depositions across the arrays appear quite uniform, and pattern transfer through our flexible polymeric aperture masks seems excellent over the approximately 6 in × 7 in deposition area for the large pixel arrays. We tested several TFTs from each portion of the TFT arrays, and quickly found that testing the completed arrays, without successful application of a contrast medium, was the largest bottleneck to obtaining complete array statistics.

Test fixturing remains a challenge and in the interest of collecting data for entire arrays, we scaled the arrays down to 5 × 5 pixel arrays, maintaining an identical pixel design and layout, in which each TFT and capacitor can be measured and data recorded in a few minutes, even by hand. Arrays are also monitored for shorted lines and columns as well as discontinuous lines, alignment errors, and shorted capacitors. We fabricate

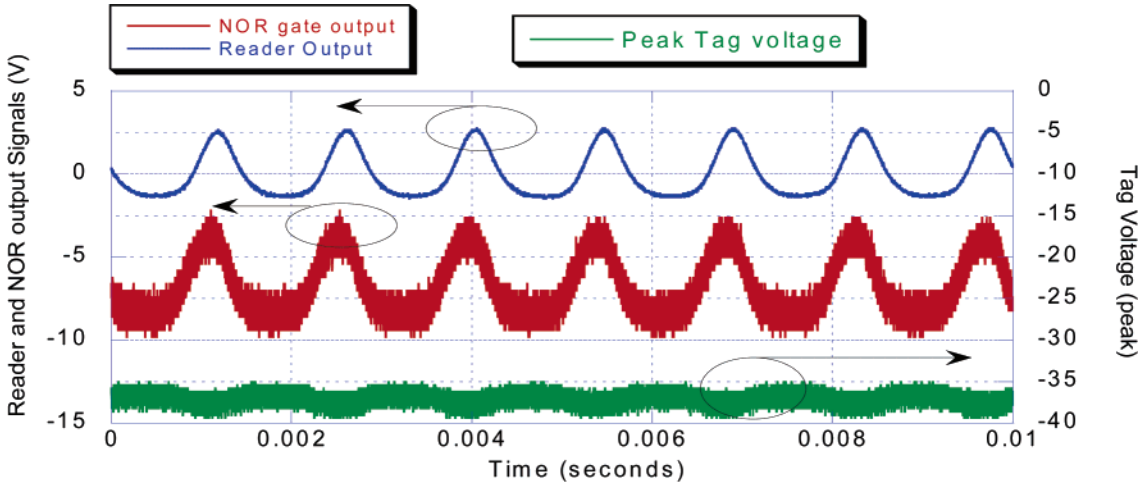

Figure 10. Output of one-bit rf transponder (shown in Figure 8), operated via ac powering, with the NOR gate functioning as intended.

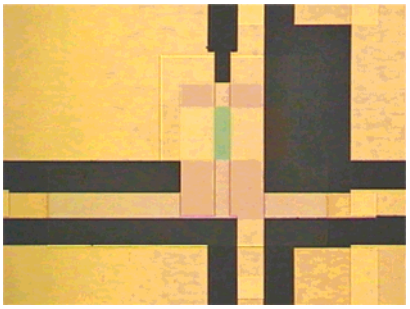

Figure 11. Optical micrograph of a single TFT from the pixel arrays described in Figure 12. $W = 200\ \mu m$; $L = 50\ \mu m$.

1	2	3	4	5	
0	0	2.1229	2.1313	1.4937	1
1.3335	2.2738	2.5122	2.1802	2.2827	2
1.6926	2.3932	2.4976	2.1688	2.3602	3
1.7089	2.334	1.6882	2.418	2.1276	4
0	2.53	2.521	2.2621	2.059	5

1	2	3	4	5	
2.9791	2.6894	0	2.813	2.6043	1
2.1394	2.4702	2.3159	2.0907	1.837	2
1.4771	2.4382	2.4925	2.4006	2.2313	3
1.2117	2.2238	2.5316	2.4673	2.1893	4
1.4468	1.9544	2.2471	2.2639	2.2078	5

1	2	3	4	5	
2.5519	1.8275	2.1595	2.5256	2.3582	1
1.696	1.9715	2.4734	2.8447	2.2605	2
2.0095	2.0243	2.0555	1.8052	1.8207	3
1.9738	2.1335	2.0728	0	1.8083	4
1.8905	1.9284	1.7411	1.7495	1.548	5

Figure 12. Mobility data in array format, as obtained from 3 5 × 5 pixel arrays fabricated simultaneously. "Zeroes" represent shorted or misaligned TFTs. Representative TFT is shown in Figure 11.

3 small arrays per deposition set (5 depositions), using 5 polymeric shadow masks, each bearing 1 device layer pattern for all 3 arrays, and Figure 12 shows some typical mobility results for 3 arrays fabricated simultaneously on a single substrate, obtained from arrays of individual pixel TFTs of the construction shown in Figure 11. Entries of "zero" in the tables indicate shorted or misaligned TFTs. Numbers on the top and right sides indicate columns and rows, respectively.

These results have shown us, through spot checks on large arrays, and fairly uniform results on small arrays, that our patterning method is extendable to at least 6 in × 7 in deposition areas, and that device layer deposition, at least on the lab scale, is adequate for those areas as well. We have fabricated 6 in. × 6 in. arrays of RFID circuits as well (Figure 13), consisting of 25 rows and 25 columns of circuit cells. Several of these functional arrays have been fabricated. TFTs in each of the cells along both diagonals of the arrays were tested to estimate overall yield in the arrays. Typical yields, estimated from measurements of devices along the diagonals, are 80−90%. These large arrays present significant challenges in data management and collection, thus a functional display would allow visual determination of yield simply based on pixel counts. Recent reports from Philips have coupled pentacene-based TFT arrays with electrophoretic ink to make displays similar in nature to E-Ink/Lucent efforts, but with significantly higher resolution and with the potential for adding gray scale through various driving schemes.[22]

Manufacturability

Fabrication and manufacturing of organic electronic devices has largely been neglected until recently, primarily because viable materials and device constructions have only recently emerged from the realm of pure research into the very early development stages. Now that device performance for organic transistors and circuits approaches, and in some cases, exceeds amorphous silicon results (mobilities of 0.1−1 cm^2/Vs), organic devices are being viewed as possible replacements for low-end electronic components. Many groups have taken the approach that any means of fabrication is acceptable, as long as the resultant device performance is acceptable and continues to improve. In many cases, the approaches to produce devices are equipment-intensive and may involve several principal methods, instead of a single manufacturing scheme. It is widely commented in the literature that printing approaches are likely to become the most cost-effective manufacturing schemes for organic electronic materials, but dem-

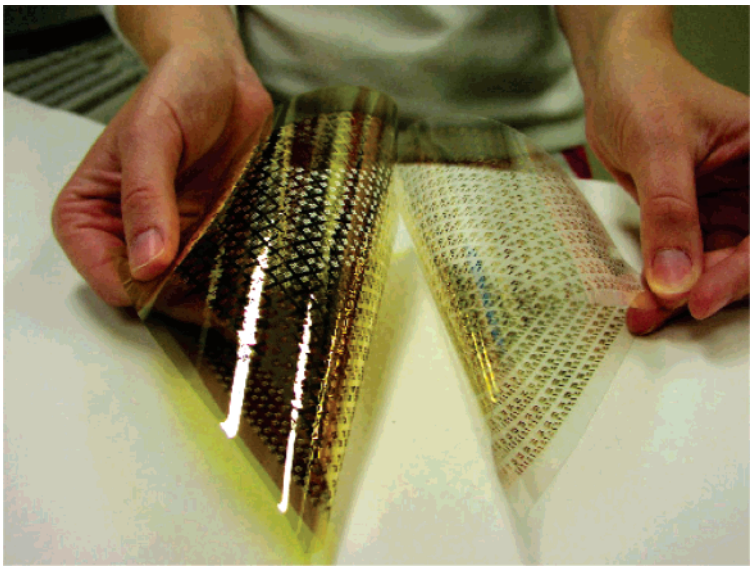

Figure 13. Optical image of 6 in × 6 in RFID circuit array (right) fabricated on polymeric substrate, via the polymeric shadow mask shown at left. Polymeric substrate arrays of this type are still in development, but identical arrays fabricated on glass substrates show an estimated 80−90% yield, based on measurements obtained from devices along the substrate diagonals.

onstrated printing approaches often involve more traditional photolithographic steps and/or vacuum-based depositions at some point during device construction. Plastic Logic reports work on short-channel ink-jet printed transistors. They have developed compatible solvent systems that enable direct deposition of all device layers into functional top gate TFTs that have been shown to successfully switch Gyricon-type electrophoretic displays. The short channel length is required to achieve the necessary current to switch the media at each pixel. Ink-jet printing alone, as reported by Plastic Logic, is not currently capable of 10-μm features. They have developed a single lithographic step, and recently replaced it with a direct-write laser patterning step, wherein a surface energy difference is mapped onto the substrate surface so that the first printed drop splits and forms a 10-μm channel.[43] Plastic Logic's approach, therefore, requires both a high-quality ink-jet system with multilayer registration capabilities, and a laser-patterning system to fabricate printed, direct-deposition of organic TFTs. PARC's approach, while it does not directly apply the device layers, does rely entirely on an acoustic ink-jet system to pattern each device layer. PARC's work requires that some layers are subtractively patterned, through a printed resist ink, using more traditional semiconductor processes including reactive wet and dry etching methods, necessitating clean-room processing facilities in addition to a multilayer ink-jet system.[22] DuPont has demonstrated another approach, dry laser transfer to pattern short channel devices (10 μm), over areas approaching 1 m^2. Three device layers can be built up in this fashion, and the devices are then completed using vapor deposition and shadow masking to pattern a portion of the pentacene layer. DuPont's approach requires a large-format, high-resolution thermal printer, and a shadow masking and vapor deposition system. Jackson's group has demonstrated all photolithographically patterned pentacene TFTs,[38b] where the final step is to subtractively pattern the pentacene layer after it has been vapor-deposited, through a photosensitized poly(vinyl alcohol) layer used as a photoresist. Reliance on the infrastructure developed for traditional Si-based electronics fabrication may erode some of the expected cost advantage potentially provided by organic electronics, but provides a well-developed manufacturing methodology. Philips has taken a similar approach, using spincoating and lithography to pattern their devices starting from a soluble precursor pentacene semiconductor. This approach eliminates a slow vapor-deposition step; it also serves as a drop-in materials set for use in their current processing lines. 3M is developing another approach, that hopes to deliver an all-dry, all-additive device fabrication methodology. We have found our unpatterned surface modification step to be indispensable for high mobility pentacene-based devices, and so we currently add a spin coating step in the middle of our process flow. For devices that could accommodate lower mobilities, the surface modification step may be eliminated. From the examples above, it can be concluded that there is a tradeoff relationship among performance, resolution, and simplicity of manufacturing, the details of which are still emerging.

Table 3. Output Characteristics for Pentacene TFTs Encapsulated Using Shadow-Mask Patterned E-beam Deposited Alumina To Protect the Pentacene Layer from Exposure to Solvent, Steam, and Application of Epoxy[a]

	mobility (cm^2/V s)	V_t (V)	slope (V/decade)	on/off
control	1.0	−8.8	1.8	2.3×10^5
acetone rinse	0.78	−7.8	2.6	6.7×10^5
steam	1.0	−10.3	1.1	3.1×10^6
epoxy heat/UV	0.92	−8.5	3.1	6.7×10^3

[a] Circuits were fabricated on glass substrates using five depositions through five polymeric shadow masks.

Progress is being made for many of these methods, with reports appearing on yield, variability, and device lifetime and stability. Jackson[38b] has shown that effective encapsulation can be achieved simultaneously with subtractively patterning the semiconductor layer, without dramatic degradation of device performance. 3M shows here that simple encapsulation methods, using an additional shadow-mask patterning and deposition step, can be effective against exposure to chemicals and processes, such as acetone, steam, and epoxy cured by UV/heat, that may be encountered during post-TFT fabrication (e.g., application of a contrast medium for displays or attachment of an antenna for RFID). We show in Table 3 results obtained on individual TFTs, encapsulated with a simple layer of shadow-mask patterned e-beam deposited alumina, tested before and after exposure to various environments. The control sample data shown in Table 3 are for an encapsulated device that was not exposed to the various treatments shown in the table. The encapsulated control device shows slightly lower mobility than unencapsulated comparative devices, typically with mobilities of 2−3 cm^2/Vs, likely due to the deposition of alumina on top of the fragile pentacene layer. Unencapsulated devices exposed to the same treatments listed in the table were completely nonfunctional after exposure. Lucent and others have shown that for some applications, encapsulation may not be desired, and that arrays of TFTs fabricated from, for example, oligothiophene materials, may be used to detect organic solvents, simply by exposure and monitoring of the output characteristics.[5]

Conclusion and Outlook

In summary, over the past several years, many aspects of organic electronics research have progressed, and the pace of progress has continued to accelerate. Novel approaches to materials, devices, and fabrication continue to appear in both the reviewed and patent literature. Companies of all sizes are involved in various aspects of organic electronics and many universities have dedicated and multidisciplinary efforts to broaden our understanding of the field. As a community, we seem to be stepping into the development era of organic electronics; we are making integrated devices and turning them into prototypes. We are also exploring manufacturing concerns associated with our devices, and long-term device stability. In essence, we are putting our materials, devices, and processes through the paces, so that we can see what we can do with organic electronics. The next steps involve figuring out the true and unique advantages of organic devices, and bringing them to bear in electronics markets.

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