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CMOS-compatible fabrication of porous silicon gas sensors and their readout electronics on the same chip

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In this work, integration on the same chip of porous silicon gas sensors along with their driving/readout electronic circuits by using an industrial microelectronic process is demonstrated. To ensure maximum compatibility, the porous silicon formation is performed after the integrated circuit fabrication flow is completed. The chip contains three CMOS operational amplifiers, a band-gap voltage reference, an integrated temperature sensor and several porous silicon-based NO_2 sensors. The simultaneous functionality of the electronics and the sensor is demonstrated by using various circuit blocks to implement a simple driving/readout electronic interface for the sensor.

1 Introduction

Porous silicon (PS) has been a topic of active research for several years to now, and different applications have been proposed for this material, supported by the exploitation of its peculiar morphological, optical, chemical, and physical properties. Applications range today from (but are not limited to) silicon-based LEDs [1] to biomedics [2], from gas sensing [3] to MEMS [4]. In most, if not all, of these applications, the compatibility of PS with standard silicon integrated circuit (IC) technologies (basically the CMOS process) is claimed or implied. As a matter of fact, the integration on the same silicon chip of PS-based devices with standard electronics is often presented as a strong point of PS applications, justifying at least in part the large amount of applied research in this field. However, in most cases this compatibility reduces to the obvious considerations that PS technology is based on the same material of the standard CMOS process, and uses compatible chemicals (basically hydrofluoric acid).

The actual compatibility of PS fabrication with a standard CMOS process flow, composed by tens of distinct operations (lithographies, thin film depositions, thermal oxidations, plasma and wet etchings, each one presenting specific issues with respect to PS compatibility) has received inadequate and sporadic attention in the vast literature on the subject. Early works [5] (predating the discovery of efficient light emission from PS in 1990 [6]) demonstrated the fabrication of complementary MOS transistors on a silicon-on-insulator (SOI) substrate obtained by a PS based process. Fauchet and coworkers [7] demonstrated the integration of a PS LED and a bipolar transistor on the same silicon chip by using thermally reoxidized silicon dioxide. In these works, thermal treatment (up to about 1000 °C) of the PS is necessary to ensure its chemical and mechanical stability and allow the PS to withstand the following CMOS process steps (implants, depositions, etc.) without introducing contamination in the process line. Unfortunately, thermal treatment is not a viable option for several PS applications: its luminescence properties

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are known to degrade, and the sensing properties of the material are virtually lost. The sensors proposed by Lewis and coworkers [8] overcome this problem by fabricating PS as one of the last steps in the process, an approach similar to the one presented in this work. Their technology, based on the use of a SiC mask, is in principle largely compatible with CMOS, but actual integration with CMOS devices on the same chip is not demonstrated.

To actually integrate PS-based devices with an IC industrial process, some basic compatibility needs have to be fulfilled: 1) PS integration has to leave the standard process flow unmodified, because changes in a well established process flow are not easily accepted by microelectronic industries; 2) PS formation can not be an intermediate step of a standard process, in order to avoid degradation of PS by the previously cited technological steps and (most important in an industrial process line) contamination *from* the PS to the processing equipment. As a consequence, in order to ensure the full compatibility of PS with an industrial IC process, the PS formation has to be performed as the last step.

On the basis of these requirements, we developed a fabrication sequence which includes the PS formation as a post-processing option of a standard CMOS process. This allowed the fabrication of PS-based sensors and standard electronics on the same chip, without modification of the process flow, and with the addition of a single lithographic step to be applied at the end of the standard flow. This represents a significant technological improvement not only for gas sensing applications: the availability of PS devices and standard electronic components on the same die could push the functionality of silicon chips towards new applications.

2 Chip design, fabrication and post-processing

The chip was developed according to three main steps: 1) design of the electronic blocks and PS sensors, whose structure is detailed below, with a standard IC design environment (CADENCE™); 2) fabrication, performed by using the 0.35 μm BCD6 (Bipolar + CMOS + DMOS) process of STMicroelectronics; 3) post-processing, consisting in an anodisation step to produce the PS sensing layer in specific chip areas, selected by means of a photoresist mask.

2.1 Electronics

The chip includes three operational amplifiers, an instrumentation amplifier, a voltage reference/temperature block, and a ring of DMOS power transistors, arranged around the sensor area. The aim of the DMOS ring is to provide a power heater to vary the chip temperature and perform purge operations or empirically seek the best temperature for the PS sensors operation. This option was not used in this work.

Here we will briefly describe only the operational amplifier and the band-gap circuit, since these cells have been used to build the simple interface described in the next section. The schematic view of the op-amp is shown in Fig. 1(a). For this cell, a compact topology offering low voltage – low power operation has been chosen [9]. The complementary input stage and the push-pull common source output stage allow rail-to-rail input range and output swing, respectively. In this way, the full supply voltage range can be exploited for the signal range. This is particularly useful since the circuit has been designed to work with a 3.3 V power supply in order to easily allow battery powered operation. The op-amp has been designed to yield a 130 dB static voltage gain, a 3 MHz gain-bandwidth product, a maximum input offset voltage of 3 mV, and an input voltage noise of 20 μV peak-to-peak in the frequency band 0.01–10 Hz. The class AB output stage delivers a 8 mA maximum current with only 2.15 mW quiescent power consumption.

The band-gap circuit, shown in Fig. 1(b), produces the reference voltage V_{REF} and a voltage V_{TEMP} proportional to the absolute temperature. The operating principle is that of "delta V_{BE}" circuits [10]. The nominal reference voltage is 1.157 V with a total variation of 1 mV over the temperature interval −20–100 °C.

The area occupancy of the op-amp and of the band-gap cell is 360 × 230 μm^2 and 100 × 110 μm^2, respectively.

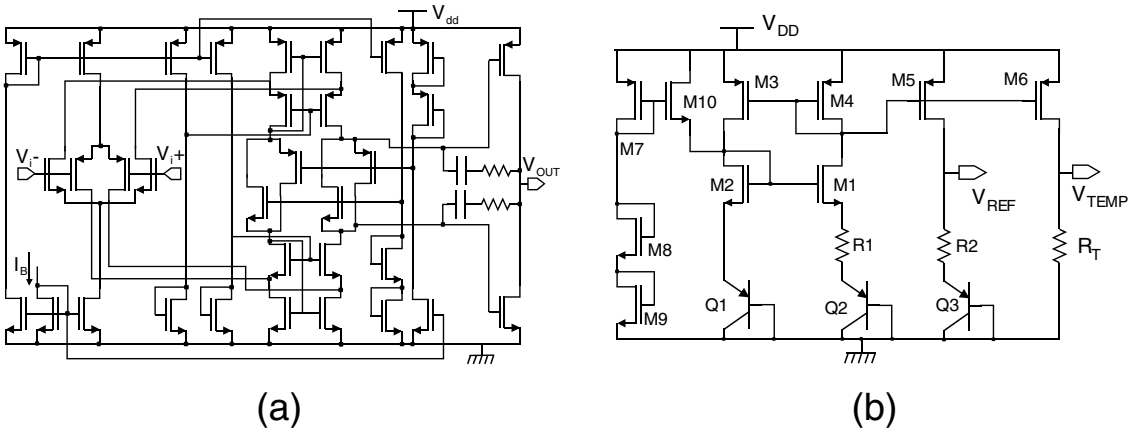

Fig. 1 Schematic view of the operational amplifier (a) and band gap voltage reference/temperature sensor cell (b) integrated on the same substrate of the PS sensors.

2.2 PS sensors

The chip contains a 2 × 4 PS sensor array constituted of four couples of APSFETs (Adsorption PS FET) [3], differing in the doping concentration of the sensing region. The APSFET is basically a FET device with a PS layer between drain and source terminals acting as a floating sensing gate. A sketch of the APSFET structure is given in Fig. 2 (left). Adsorption of molecules into the PS changes the concentration of free carriers in the crystalline silicon under the PS itself, and, in turn, the conduction current. The current variation of the sensor depends on the concentration of the sensed species in the testing chamber, so that the PS layer plays, for the gas concentration, a role similar to that of the gate voltage of a standard FET device.

The APSFET is fabricated in a p-type doped region, that is the active area, simultaneously with electronic components. The standard n^+ implant used to fabricate the NMOS drain and source of the electronics is also used for the drain and source contacts of the APSFET. In order to maximize the sensing area, a comb-like geometry was chosen for drain and source of the sensor. As mentioned above, the PS production is performed as the last technological step, and hence after the fabrication of electronics, in the active area.

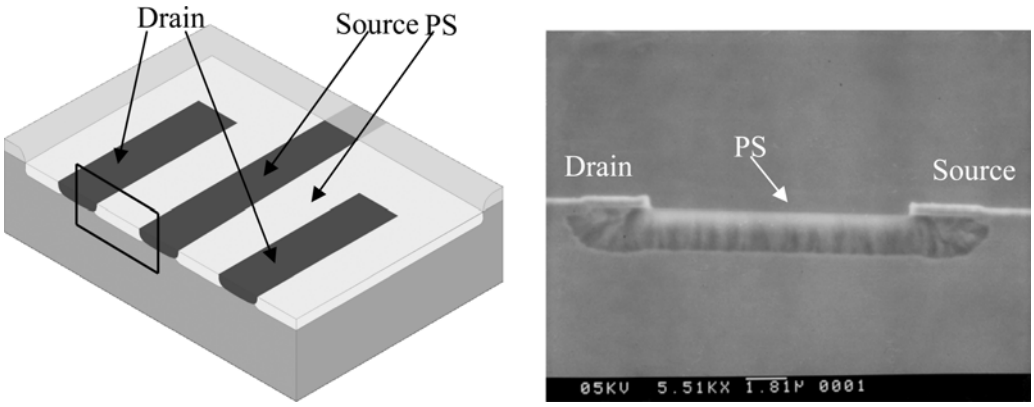

Fig. 2 Schematic view of an APSFET in BCD6 (left) and SEM cross-section showing the PS layer between adjacent drain and source contacts.

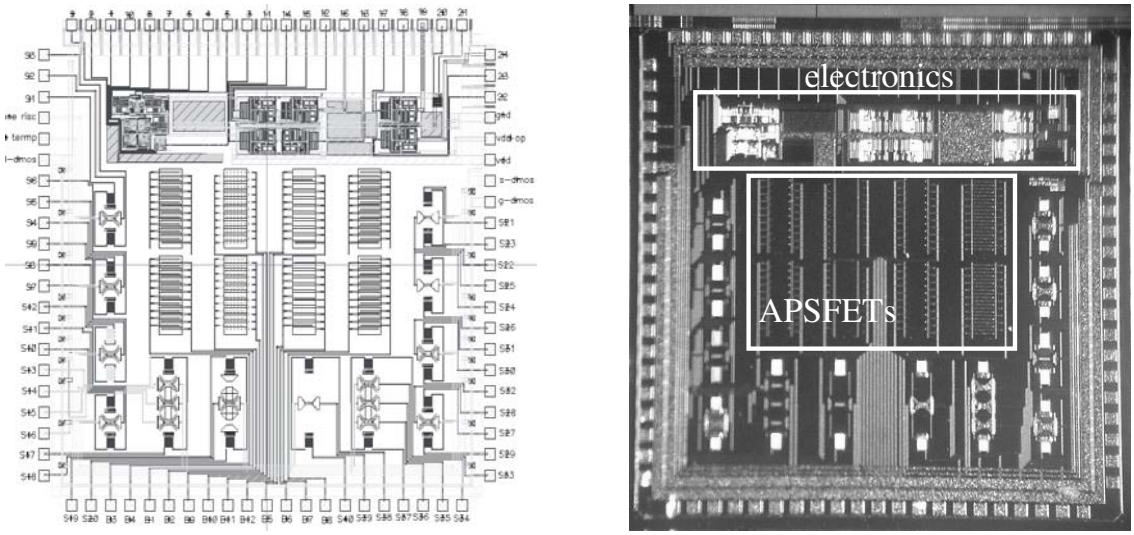

Fig. 3 Chip layout (left) and optical photograph of the fabricated die (right) containing several electronic blocks and an array of PS-based sensors.

The chip layout and an optical photograph of the fabricated silicon die are shown in Fig. 3. The fabricated chip contains: the electronics (upper part of the die), the PS sensors (centre of the die), and other structures not involved in this work. The overall chip dimension is 4 mm × 4 mm.

2.3 Post-processing

After the electronics fabrication has been completed, that is at the end of the BCD6 process flow, the silicon is covered by several silicon dioxide passivation layers, intended to protect the electronics itself. A few post-processing steps are then required to remove these layers and uncover the silicon in correspondence of the active area of sensors for the PS formation. A 6 μm thick AZ4562 photoresist layer, properly defined by using a standard photolithographic step, is used to protect the electronics from post-processing technological steps, while leaving the active area unprotected to allow the anodisation of the silicon substrate. In order to expose the silicon surface for subsequent anodisation, a BHF etch is performed on the sample. At this point, the anodisation is carried out and the PS layer is fabricated. As this step takes place in the dark, only the exposed p-type material is converted into PS, while the n-type drain and source implants are not etched. Typical anodisation times, in the order of few minutes, give rise to PS layers a few microns thick. The sample is finally rinsed in acetone, to remove the photoresist, and in ethanol and pentane, to reduce cracking during the next drying step, performed in a controlled atmosphere. A SEM cross-section of an APSFET with the PS layer between drain and source is shown in Fig. 2 (right).

3 On-chip driving/readout interface

Retaining the correct operation of the electronics after the post-processing steps is not a trivial issue: the hydrofluoric acid in the anodisation solution could damage the electronic components during the PS formation and degrade their performance. To test the simultaneous operation of the electronics and sensors, the simple interface of Fig. 4 (left) was implemented. One of the APSFETs was connected to an operational amplifier mounted in a current–voltage converter configuration and biased with a 3.3 V supply. The voltage reference V_{REF}, about 1.1 V, used to bias the APSFET drain through the virtual ground at

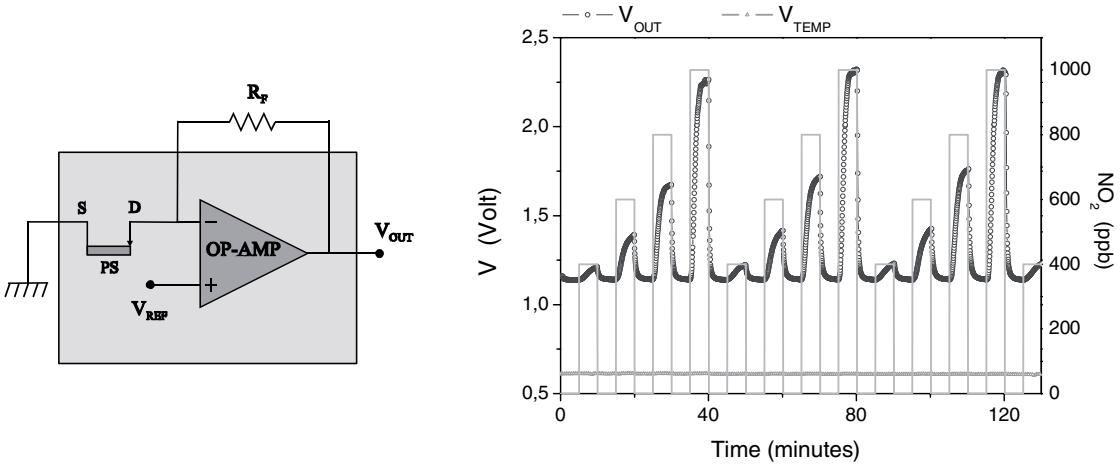

Fig. 4 On chip driving/readout electronic interface connected to an APSFET (left) and output voltage signal V_{OUT} in presence of different NO_2 concentrations.

the amplifier input, is generated with the band-gap circuit described above. Components included into the grey box of Fig. 4 (left) are all integrated on the chip, and the only external component is the feedback resistor R_F.

The circuit was tested at room temperature for NO_2 concentrations in the 400 to 1000 ppb range, using synthetic dry air as a carrier gas. The time evolution of NO_2 concentration and of the amplifier output V_{OUT} are shown in Fig. 4 (right). The output voltage closely follows the transient response of the sensor. The response time, which in our experimental set-up is limited by the testing chamber volume, can be estimated as a few minutes. As NO_2 increases the APSFET conduction current, the presence of the gas results in an increase of the amplifier output. When the NO_2 is removed, the output is restored to its initial value, and no significant drift of the output is observed. The die temperature was monitored during the circuit operation time by using the on-chip temperature sensor, and the corresponding signal V_{TEMP} is reported in Fig. 4 (right).

4 Conclusions

The proposed approach of applying post-processing steps to a standard microelectronic process, in order to fabricate porous silicon layers in selected areas of a silicon die, was shown to be an effective method to integrate PS-based sensors with electronic circuits. The latter worked properly after the sensor fabrication was completed, as demonstrated by the simple interface built up using the on-chip integrated analog cells. This method can be, in principle, extended to develop smart PS sensors with advanced on-board signal processing capabilities.

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