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SHORT PAPER

Switched-Capacitor Fractional-Step Butterworth Filter Design

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Abstract Switched-capacitor fractional-step filter design of low-pass filter prototypes with Butterworth characteristics is reported in this work for the first time. This is achieved using discrete-time integrators which implement both the bilinear and the Al-Alaoui s-to-z transformations. Filters of orders 1.2, 1.5 and 1.8 as well as 3.2, 3.5, and 3.8 are designed and verified using transistor-level simulations with Cadence on AMS 0.35 μm CMOS process. Digital programmability of the fractional-step filters is also achieved.

1 Introduction

Fractional-order calculus is a powerful tool employed into many applied and interdisciplinary branches of engineering [7,15]. For example, the modeling of viscoelasticity as well as of biological cells and tissues has long been performed through the utilization of fractional-order impedances [8]. In circuit design, a lot of effort has been made to migrate concepts of fractional-order calculus into circuit theory and design [1,6,7] with particular emphasis on fractional-step analog filters [2,4,9,10,13] and fractional-order oscillators [16]. In comparison with their integer-order counterparts, fractional-order

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filters offer two advantages: (i) precise attenuation of $-6(n+a)$ dB/octave where n is filter's integer order and a is the fractional step and (ii) extra degree of design freedom since the filters' design parameters (quality factor, bandwidth and pole frequencies) are all functions of a. For example, the cutoff frequency of a fractional-step RC filter would become $\omega_c = (1/\mathrm{RC})^{1/(1+a)}$ instead of $\omega_c = 1/\mathrm{RC}$ in a conventional first-order filter.

Voltage-mode fractional-order analog filters have been already introduced in discrete component form, using operational amplifiers (op-amps) and second-generation current conveyors (CCIIs) as active elements [4,13] as well as on a field-programmable analog array platform (FPAA) [9]. Current-mode realizations were recently reported in [18,19], where the concept of companding filtering has been employed. Companding filters, however, suffer from increased circuit complexity. An attractive and precise technique for realizing voltage-mode resistorless filters is known to be the switched-capacitor (SC) technique, where the realized time-constants are formed as a product of a clock period and the ratio of the associated capacitors [5,14]. SC realizations of fractional-order integrators and differentiators have been already reported in [17,20–23]. However, to the authors' best knowledge, fractional-step SC filters have not yet been approached, which is the target of this work. In particular, we systematically design SC filters with low-pass Butterworth characteristics.

This work is organized as follows: First a prototype filter of order $(1+a)$, $(0 < a < 1)$ is designed in Sect. 2. In Sect. 3, the prototype filter is used to design a higher-order filter of order $(3+a)$. The performance of the designed filters is verified in Sect. 4 through simulation results using Cadence and MOS transistor models provided by the AMS 0.35 μm CMOS process Design Kit.

2 Design of a $(1+a)$ Filter Prototype

2.1 Design Equations

The transfer function of a $(1+a)$ order low-pass filter with all-pole (Butterworth) response is given by (1) as [13]

$$H_{1+a}^{\mathrm{LP}}(s) = \frac{1}{s^{1+a} + K_1 s^a + K_2} \tag{1}$$

To minimize the error in the frequency response, the factors K_i $(i = 1, 2)$ were calculated to be

$$K_1 = 1.068a^2 + 0.161a + 0.3324, \quad K_2 = 0.2937a + 0.7122 \tag{2}$$

The above transfer function can be approximated by an integer-order circuit after using a suitable second-order approximation for the fractional-order Laplacian s^a, optimized in terms of phase and gain errors. Employing the approximation (normalized to 1 rad/s) given by (3) [11]

$$s^a \cong \frac{(a^2+3a+2)s^2+(8-2a^2)s+(a^2-3a+2)}{(a^2-3a+2)s^2+(8-2a^2)s+(a^2+3a+2)} \tag{3}$$

leads then to

$$H^{\mathrm{LP}}_{1+a}(s) = \frac{a_2 s^2 + a_1 s + 1}{s^3 + b_2 s^2 + b_1 s + b_0} \tag{4}$$

where

$$a_1 = \frac{8-a^2}{a^2+3a+2},\ a_2 = \frac{a^2-3a+2}{a^2+3a+2},$$
$$b_0 = \frac{1.07a^4 - 2.75a^3 + 3.58a^2 + 2.05a + 2.1}{a^2+3a+2},$$
$$b_1 = \frac{-2.14a^4 - 0.91a^3 + 7.45a^2 + 0.64a + 10.36}{a^2+3a+2},$$

and

$$b_2 = \frac{1.07a^4 + 3.66a^3 + 0.78a^2 - 0.23a + 10.09}{a^2+3a+2}$$

The realization of the filter transfer function (4) can be performed using the inverse follow-the-leader feedback (IFLF) topology [14] which has a transfer function given by

$$H(s) = \frac{\frac{G_2}{\tau_1}s^2 + \frac{G_1}{\tau_1\tau_2}s + \frac{G_0}{\tau_1\tau_2\tau_3}}{s^3 + \frac{1}{\tau_1}s^2 + \frac{1}{\tau_1\tau_2}s + \frac{1}{\tau_1\tau_2\tau_3}} \tag{5}$$

Comparing (4) and (5), the filter design equations can then be derived as

$$\frac{\tau_1}{\tau} = \frac{1}{b_2},\ \frac{\tau_2}{\tau} = \frac{b_2}{b_1},\ \frac{\tau_3}{\tau} = \frac{b_1}{b_0},\ G_0 = \frac{1}{b_1},\ G_1 = \frac{a_1}{b_1},\ G_2 = \frac{a_2}{b_2}$$

where frequency is normalized with respect to $\omega_0 = 1/\tau$. In the following section, we focus on implementing the IFLF topology using SC circuits.

2.2 Implementation

A continuous-time IFLF topology can be transposed into its discrete-time counterpart using an appropriate s-to-z transformation resulting in the structure shown in Fig. 1, where $H_i(z)$, $i = 1, 2, 3$ denotes the transfer function of a discrete-time integrator. The two most famous s-to-z transformations widely used for designing digital filters are

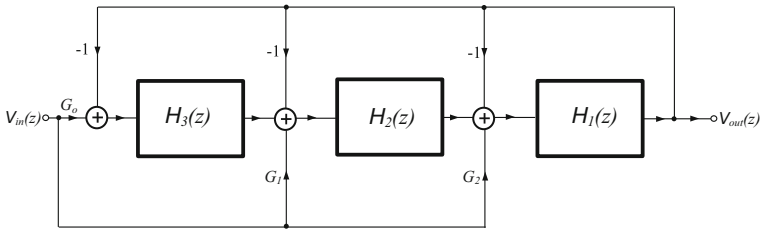

Fig. 1 IFLF discrete-time filter structure for approximating a filter of order $(1 + a)$

the Bilinear and the Al-Alaoui transformations [3,12] using which a lossless integrator $H_a(s) = (1/\tau s)$ would be expressed in discrete form, respectively, as

$$H_d(z) = \frac{T}{2\tau}\left(\frac{1+z^{-1}}{1-z^{-1}}\right), H_d(z) = \frac{T}{8\tau}\left(\frac{7+z^{-1}}{1-z^{-1}}\right)$$

where T is the sampling period. The analog frequency Ω and the digital frequency ω are, respectively, related in these two transforms by

$$\omega = \frac{2}{T}\arctan\left(\frac{\Omega T}{2}\right), \omega = \frac{1}{T}\arctan\left(\frac{4\Omega T}{4-0.4375(\Omega T)^2}\right)$$

Using these two transformations, a lossless SC integrator can be designed and is shown in Fig. 2a, b. Both integrators are insensitive to the effect of parasitic capacitances, and the outputs of all op-amps are held over a clock period. However, the bilinear SC integrator offers a reduced capacitor area and requires less switches. Using the bilinear transformation-based integrator of Fig. 2a, the order $(1+a)$ low-pass filter is designed and shown in Fig. 3. A similar design can be obtained with Al-Alaoui-based integrators and is shown in Fig. 4.

3 Higher-Order $(n + a)$ Filters

Higher-order fractional-step filters with Butterworth characteristics are obtained using the prototype $(1 + a)$ filter since

$$H^{\mathrm{LP}}_{n+a}(s) = \frac{H^{\mathrm{LP}}_{1+a}(s)}{B_{n-1}(s)} \simeq \frac{a_2 s^2 + a_1 s + 1}{s^{n+2} + \beta_{n+1}s^{n+1} + \cdots + \beta_1 s + \beta_0} \tag{6}$$

where in (6) $B_{n-1}(s)$ is the Butterworth polynomial of order $(n-1)$. The normalized cutoff frequency Ω_{on} of the $(n + a)$ filter was derived and found to be

$$\Omega^{2(n+a)}_{\mathrm{on}} = 1 - \Omega^{2(n-1)}_{\mathrm{on}} - \Omega^{2(1+a)}_{\mathrm{on}} \tag{7}$$

For example, in the case of fractional filters of orders 3.2, 3.5, and 3.8, the corresponding cutoff frequencies were calculated to be (0.756, 0.776, 0.792) rad/s,

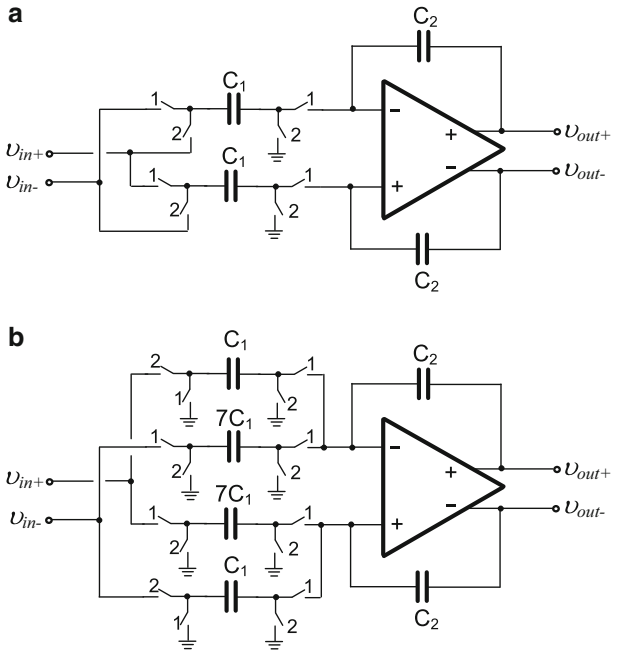

Fig. 2 Lossless integrator based on **a** Bilinear tranformation ($\frac{T}{2\tau} = \frac{C_1}{C_2}$) and **b** Al-Alaoui transformation ($\frac{T}{8\tau} = \frac{C_1}{C_2}$)

respectively. Using an IFLF architecture, an $(n + a)$ filter can also be designed. The realized transfer function in this case is

$$H_{n+a}^{\mathrm{LP}}(s) = \frac{\frac{G_2}{\tau_1\tau_2\ldots\tau_n}s^2 + \frac{G_1}{\tau_1\tau_2\ldots\tau_{n+1}}s + \frac{G_0}{\tau_1\tau_2\ldots\tau_{n+2}}}{s^{n+2} + \frac{1}{\tau_1}s^{n+1} + \frac{1}{\tau_1\tau_2}s^n + \cdots + \frac{1}{\tau_1\tau_2\ldots\tau_{n+2}}} \tag{8}$$

and the design equations are hence

$$G = \frac{1}{\beta_0}, G_1 = \frac{a_1}{a_0\beta_1}, G_2 = \frac{a_2}{a_0\beta_2}, \tau_j = \frac{\Omega_{on}}{\Omega_0} \cdot \frac{\beta_{n+3-j}}{\beta_{n+2-j}}|_{j=1,2,\ldots n+2}$$

where the normalized frequency Ω_{on} is found from (7) and Ω_0 is a de-normalizing frequency.

Using the $(1+a)$ prototype filter, a SC $(3+a)$ filter was built to realize the function $H_{3+a}^{\mathrm{LP}}(s) = H_{1+a}^{\mathrm{LP}}(s)/B_2(s)$ where $B_2(s) = s^2+\sqrt{2}s+1$. Hence, the realized transfer function is

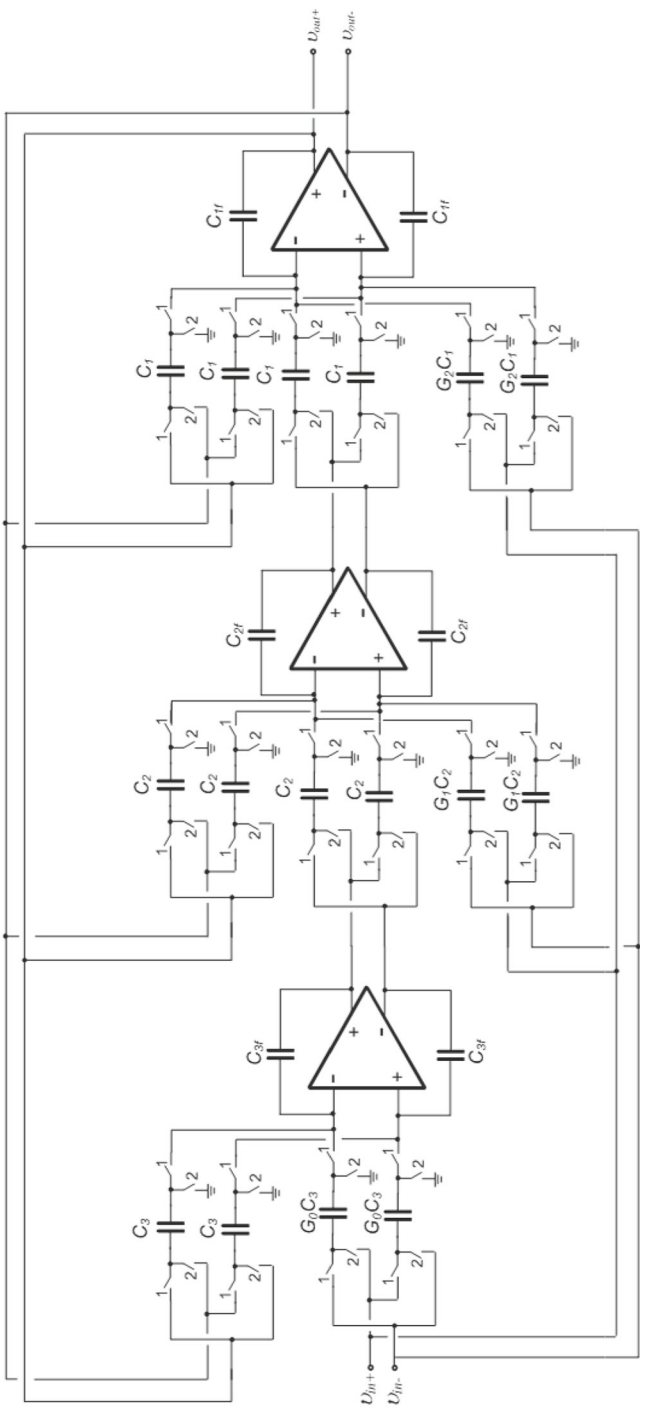

Fig. 3 SC filter topology for realizing a $(1 + a)$ order lowpass filter using the bilinear transformation

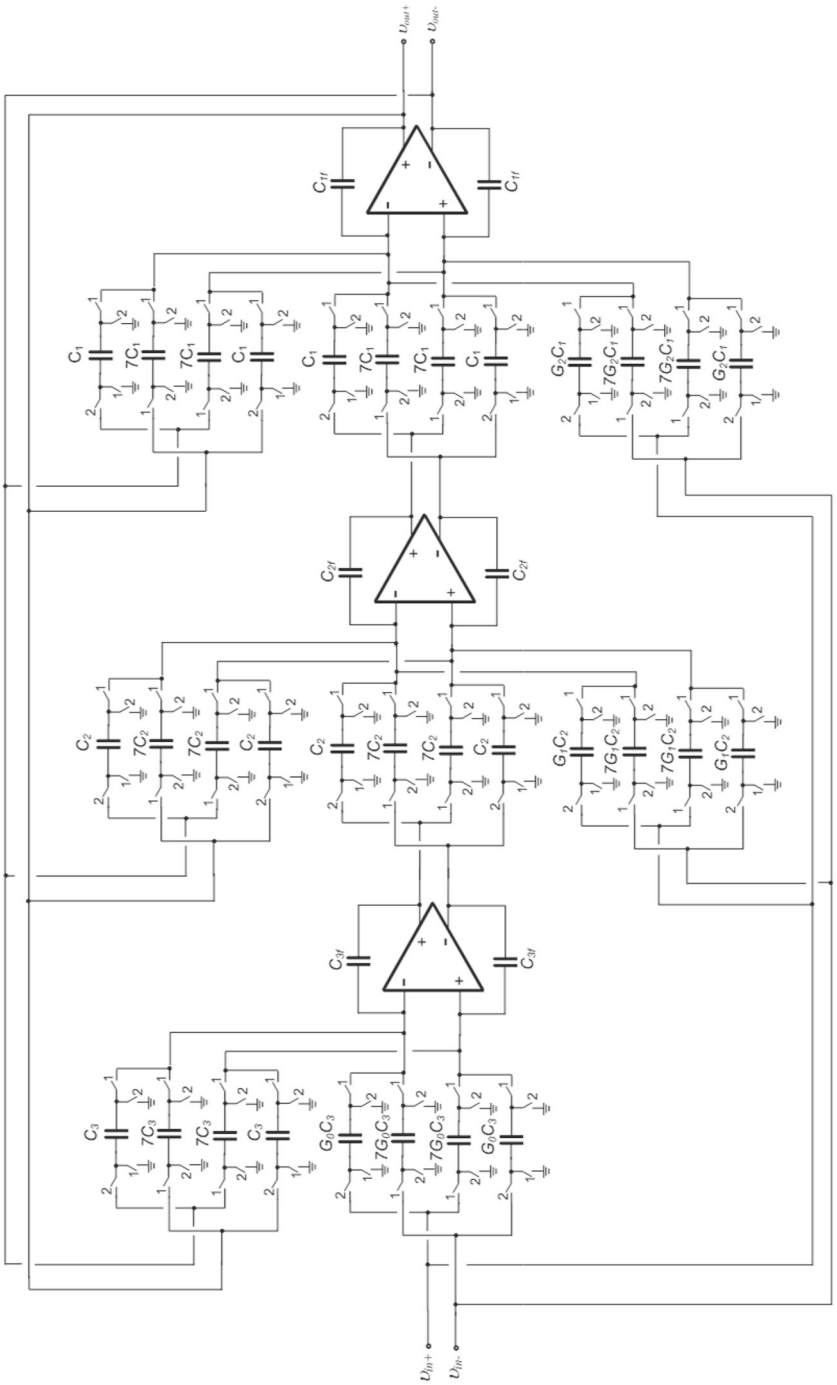

Fig. 4 SC filter topology for realizing a $(1 + a)$ order lowpass filter using the Al-Aloui transformation

$$H_{3+a}^{\mathrm{LP}}(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^5 + (b_2 + \sqrt{2})s^4 + (\sqrt{2}b_2 + b_1 + 1)s^3 + (b_2 + \sqrt{2}b_1 + b_0)s^2 + (b_1 + \sqrt{2}b_0)s + b_0} \tag{9}$$

where $a_{0,1,2}$ and $b_{0,1,2}$ are as given in Sect. 2 for the $(1+a)$ filter prototype. Evidently, a fifth-order function is needed to realize the fractional-step $(3+a)$ filter; which is always the price paid for obtaining precise stepping [1,13]. The complete design of the filter is shown in Fig. 5. It should be mentioned at this point that an alternative solution for realizing high-order fractional filters could be archived by rewriting the expression in (6) as $H_{n+a}^{\mathrm{LP}}(s) = H_{1+a}^{\mathrm{LP}}(s) \cdot H_{n-1}^{\mathrm{LP}}(s)$ where $H_{n-1}^{\mathrm{LP}}(s) = 1/B_{n-1}(s)$ is the transfer function of the $(n-1)$ order Butterworth low-pass filter. Therefore, having available the topology of a $(1+a)$ order filter and taking into account that the derivation of an $(n-1)$ order multi-feedback filter is a trivial procedure, it is readily obtained that the proposed technique offers a significant facilitation of the design procedure of higher-order filters. Other approximations, such as Chebyshev, Bessel, and Elliptic could be implemented using the aforementioned procedure. Some approximations (such as Elliptic and type II Chebyshev) have zeros over the unit circle and suffer from inaccuracy effects in the stopband.

4 Sensitivity Analysis

The sensitivity performance of the SC filters is similar to that achieved by their continuous-time active filters, and this originated from the fact that the starting point for realizing a SC filter is a continuous-time filter function which is transposed into the discrete time through an appropriate transformation. Therefore, well- established low-sensitivity conventional filter design techniques, such as leapfrog or multi-feedback structures, should be also followed in the case of SC filter design. Using the transfer function in (9), the expressions for the normalized sensitivities to a_i, b_i $(i = 0, 1, 2)$ are, respectively, given by

$$S_{a0}^{H_{3+a}^{\mathrm{LP}}} = -a_0 \frac{1}{N(s)}, S_{a_1}^{H_{3+a}^{\mathrm{LP}}} = -a_1 \frac{s}{N(s)}, S_{a_2}^{H_{3+a}^{\mathrm{LP}}} = -a_2 \frac{s^2}{N(s)} \tag{10}$$

and

$$S_{b_0}^{H_{3+a}^{\mathrm{LP}}} = -b_0 \frac{B_{n-1}(s)}{D(s)}, S_{b_1}^{H_{3+a}^{\mathrm{LP}}} = -b_1 \frac{s \cdot B_{n-1}(s)}{D(s)}, S_{b_2}^{H_{3+a}^{\mathrm{LP}}} = -b_2 \frac{s^2 \cdot B_{n-1}(s)}{D(s)} \tag{11}$$

The corresponding sensitivity plots are provided in Fig. 6, where it is readily obtained that the fractional-order filter has reasonable sensitivity characteristics. Another estimation factor of the sensitivity performance of the filter is the quality factor Q of the poles of the transfer function. Following this, the minimum and maximum values of the Q factor of poles for $a = 0.2, 0.5$ were 0.5 and 0.707, respectively.

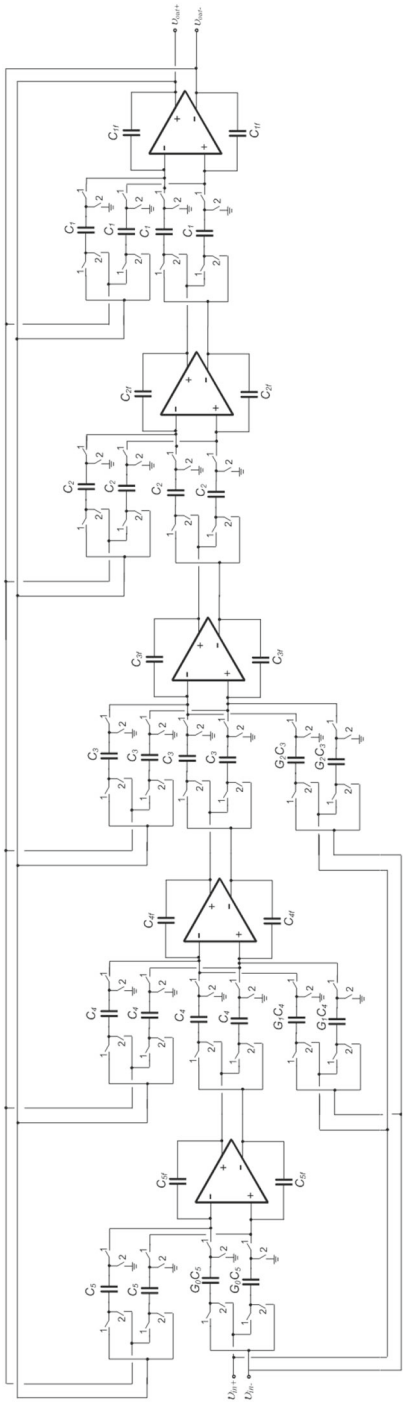

Fig. 5 Implementation of the order $(3 + a)$ lowpass filter

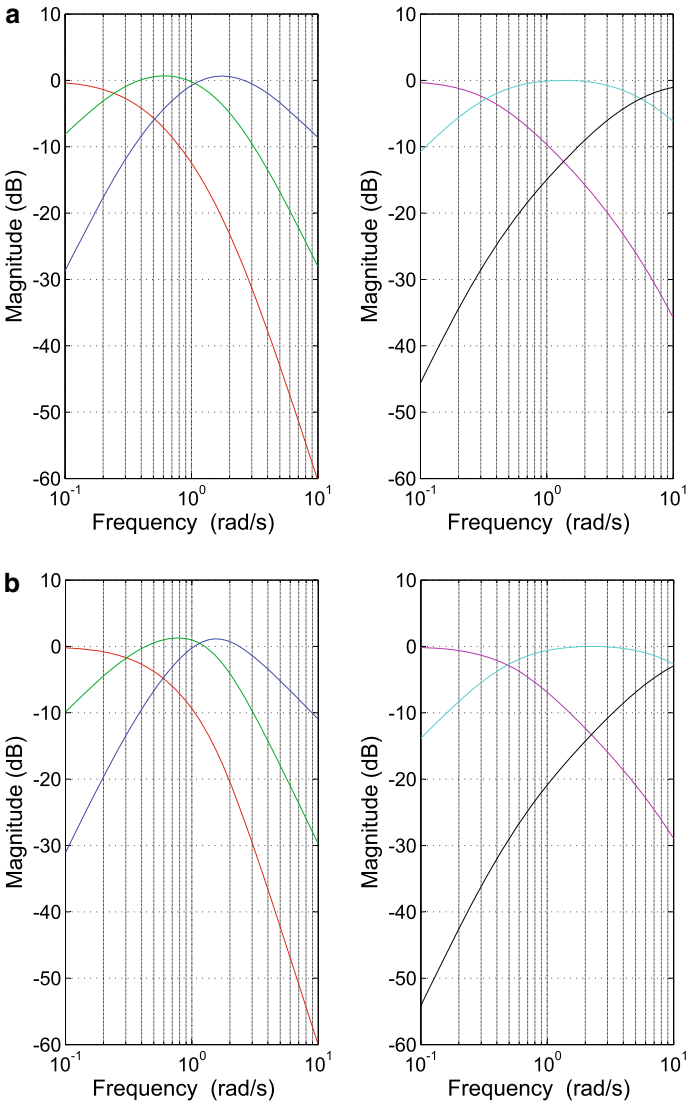

Fig. 6 Sensitivity plots of the fractional-order filter function in (9) with regards to denominator coefficients b_0 (red), b_1 (green), b_2 (blue) and numerator coefficients a_0 (magenta), a_1 (cyan), a_0 (black) for **a** $a = 0.2$ and **b** $a = 0.5$

5 Design Verification

We have verified the filter designs shown in Figs. 3, 4, and 5 using Cadence simulations performed with AMS 0.35 µm CMOS process. In all designs, the fully differential op-amp circuit shown in Fig. 7a, was used. The power supplies were $V_{DD} = -V_{SS} = 1\,V$, while the bias current (I_B) was equal to 10 µA. The compensation resistor and capacitor were, respectively, 0.77 kΩ and 5 pF. In addition, the resistors in the common-mode

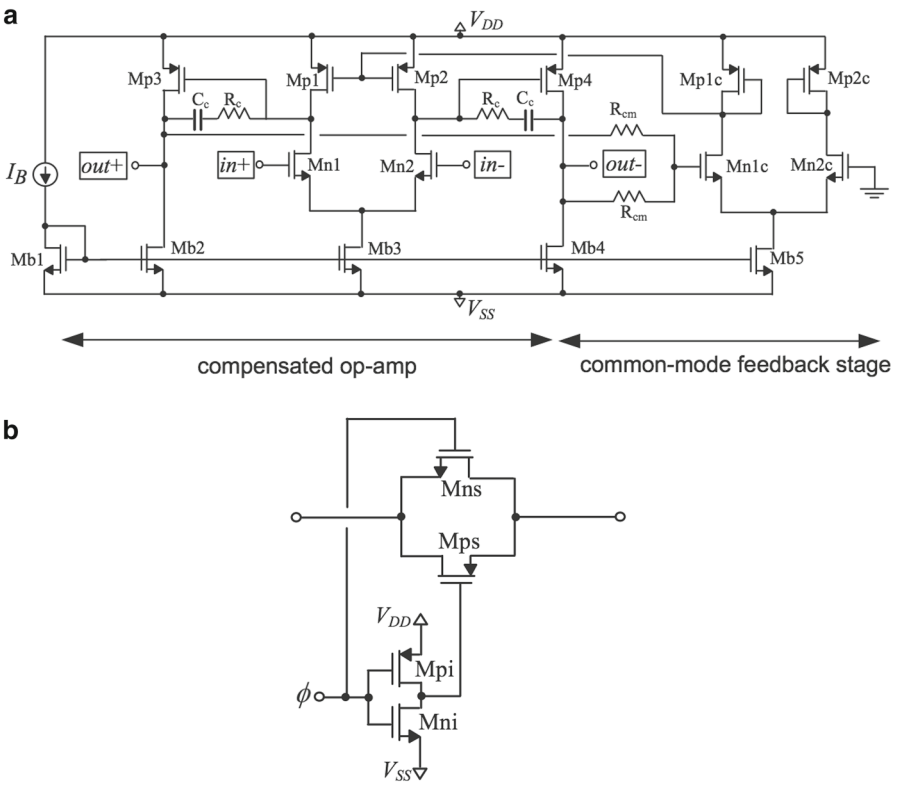

Fig. 7 **a** Fully differential op-amp with common-mode feedback stage. Transistor aspect ratios (μ/μ) are: (50/2),(200/2),(100/2),(200/0.5) and (50/0.5) respectively for M_{b1},$M_{b2,b4}$,$M_{b3,b5}$,$M_{n1,n2,n1c,n2c,p3,p4}$ and $M_{p1,p2,p1c,p2c}$. **b** TG-based switch with transistor sizes (20/1), (10/1), (4/1) and (2/1) respectively for M_{ps}, M_{ns}, M_{pi}, M_{ni}

feedback (CMFB) stage are equal to 10 kΩ. The open-loop gain of this op-amp is 55 dB, while its gain-bandwidth (GBW) product is 12 MHz. In addition, the values of the phase margin and slew-rate are about 50° and 2 V/μs, respectively. The realization of switches was performed by transmission gates (TGs), as shown in Fig. 7b.

5.1 Verification of the $(1 + a)$ Filter Prototype

We designed the SC filter of order $(1 + a)$, with a cutoff frequency of 1 kHz and a sampling frequency of 20 kHz. The capacitor values for each integrator in the filter of Fig. 3 are given in Table 1. The total number of switches and capacitors needed were 64 and 22, respectively. The corresponding values for the same topology when implemented using Al-Alaoui integrators were 138 and 38, respectively. It is thus obvious that to reduce circuit complexity, the bilinear transformation-based structure of Fig. 3 is better. It should be mentioned that switches can be shared, and therefore, their number can be further reduced.

Table 1 Design values for the filter in Fig. 3

C	$a = (0.2, 0.5, 0.8)$	C	$a = (0.2, 0.5, 0.8)$
C_1	(3.5, 7.1, 26.4) pF	C_{1f}	(5.8, 15.8, 66.3) pF
C_2	(0.7, 0.8, 1.1) pF	C_{2f}	(4, 4.5, 5.9) pF
C_3	(0.5, 0.5, 0.5) pF	C_{3f}	(13, 10.4, 8.9) pF
G_0C_3	(0.5, 0.5, 0.5) pF	G_1C_2	(0.5, 0.5, 0.5) pF
G_2C_1	(0.5, 0.5, 0.5) pF	$\frac{C_{\max}}{C_{\min}}$	(25.9, 31.6, 132.6)

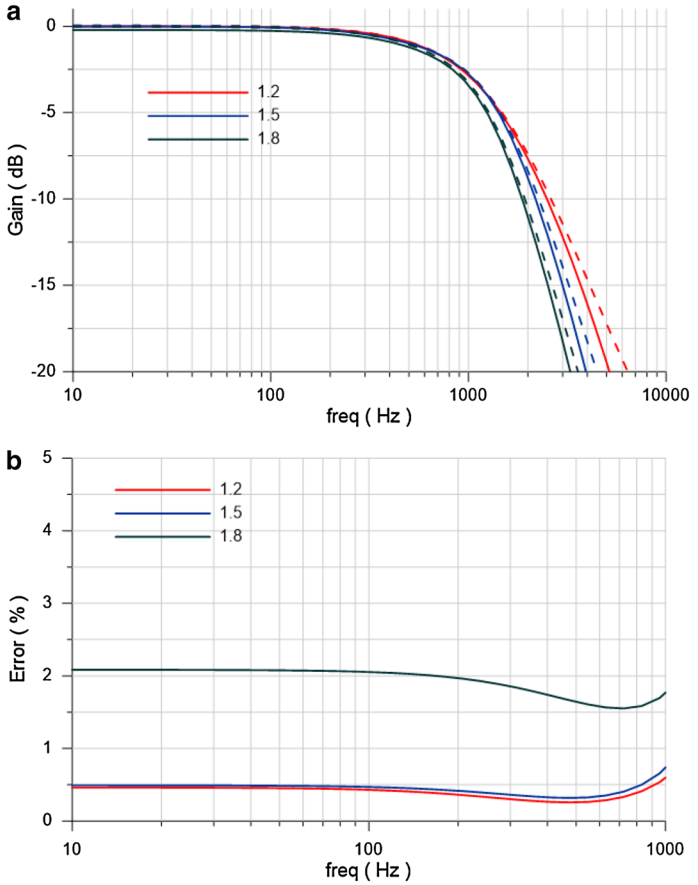

Fig. 8 Simulation results for the filter prototype in Figure 3; **a** frequency response, and **b** passband error

The frequency response of both filters was simulated on Cadence. The results for the filter in Fig. 3 are shown in Fig. 8a (solid lines) where the corresponding ideal responses are also plotted (dashed lines). The passband error is plotted in Fig. 8b, where it is seen that the error is less than 2.1 %. The measured stopband attenuations for the filters of order 1.2, 1.5, and 1.8 were, respectively, (6.7, 9.6, 11.2) dB/octave close enough to the theoretical values of (7.2, 9, 10.8) dB/octave; while the measured cutoff frequencies

Table 2 Design values for the filter in Fig. 5

C	$a = (0.2, 0.5, 0.8)$	C	$a = (0.2, 0.5, 0.8)$
C_1	(0.5, 0.5, 0.5) pF	C_{1f}	(0.5, 0.6, 0.6) pF
C_2	(0.5, 0.5, 0.5) pF	C_{2f}	(1.2, 1.3, 1.3) pF
C_3	(9.7, 21.2, 79.1) pF	C_{3f}	(45.9, 101.8, 388.8) pF
C_4	(0.9, 1.2, 1.6) pF	C_{4f}	(8.4, 10.4, 14.1) pF
C_5	(0.5, 0.5, 0.5) pF	C_{5f}	(13.2, 11.5, 10.6) pF
G_0C_5	(0.5, 0.5, 0.5) pF	G_1C_4	(0.5, 0.5, 0.5) pF
G_2C_3	(0.5, 0.5, 0.5) pF	$\frac{C_{max}}{C_{min}}$	(91.8, 203.6, 777.6)

were, respectively, (1.03, 1.05, 0.98) kHz as compared to the targeted 1-kHz design value. For the $(1+a)$ filter based on Al-Alaoui integrators, similar results were obtained albeit the passband error exceeded 10 %. The measured stopband attenuations for filters of order 1.2, 1.5, and 1.8 were, respectively, (6.3, 8.2, 10.8) dB/octave, while the measured cutoff frequencies were (0.95, 0.92, 0.9) kHz, compared with the targeted 1-kHz design value. We thus conclude that from a circuit complexity point of view and from a performance point of view, the bilinear transform is better than Al-Alaoui transform in the targeted filter prototype.

5.2 Verification of the Order $(3 + a)$ SC Filter

The capacitor values for each integrator in Fig. 5 (to achieve a cutoff frequency of 1 kHz) are given in Table 2.

By inspecting Table 2, it is obtained that the capacitance spread is very large in the case of a 3.8 order filter. Adopting 100 fF for the smallest capacitance, which is limited by the 0.35 μm technology, a capacitance of 78 pF would be required for the realization of this filter which is not feasible. Therefore, a better technology must be adopted in this case.

To examine stability, the time-domain behavior of the filter is shown in Fig. 9a, where the input and output waveforms for a differential input signal with 100-Hz frequency and 100-mV amplitude are simultaneously plotted. The filter's frequency response is given in Fig. 9b where the corresponding theoretical responses are also plotted. According to the error plot in Fig. 9c, the passband error is less that 1.3 %. The measured values for the cutoff frequency were 0.99, 0.97, and 0.94 kHz for the orders 3.2, 3.5, and 3.8, respectively. With respect to the attenuation in the stopband, the measured values were 18.6, 21.4, and 22 dB/octave, respectively, whereas the corresponding theoretical values are 19.2, 21, and 22.8 dB/octave, respectively.

The sensitivity performance of the filter, with respect to the effects of MOS transistors and passive components mismatching as well as process parameters variations, has been evaluated through Monte Carlo analysis offered by Cadence. The simulated values of the standard deviation of cutoff frequency, low-frequency gain, and slope of the stopband attenuation were, respectively, (0.002 dB, 1.83 Hz, 0.044 dB/octave),

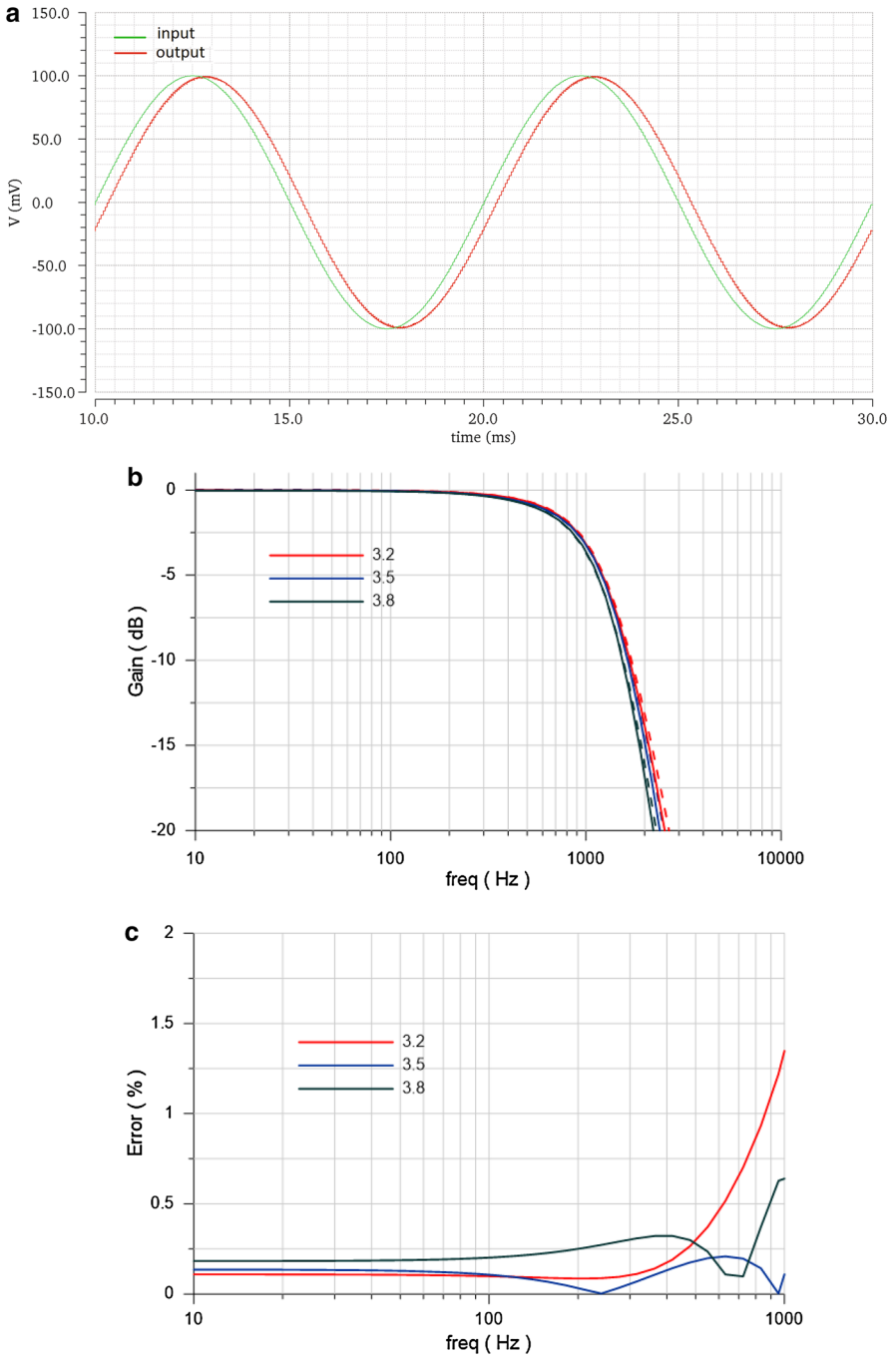

Fig. 9 Simulation results for the filter circuit in Figure 5; **a** time-domain response **b** frequency response, and **c** passband error

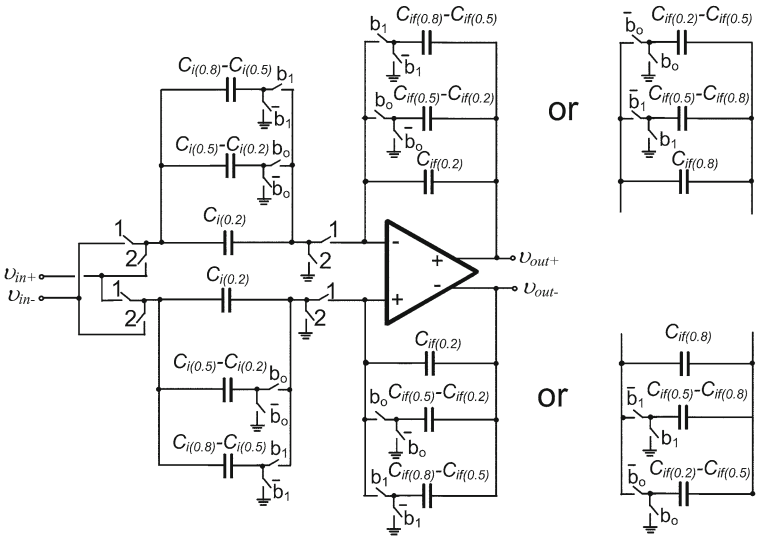

Fig. 10 Bilinear integrator with digital programmability both in feedforward and feedback paths

(0.002 dB, 2.14 Hz, 0.063 dB/octave) and (0.002 dB, 2.45 Hz, 0.065 dB/octave) for orders 3.2, 3.5, and 3.8. These results show that the design is robust.

5.3 Digital Programmability

Introducing digital programming capability into the designed filter was done by incorporating the digitally programmed bilinear integrator, shown in Fig. 10, which realizes the transfer function

$$H_d(z) = D\left(\frac{1+z^{-1}}{1-z^{-1}}\right)$$

where

$$D = \frac{C_{i(0.2)} + b_0(C_{i(0.5)} - C_{i(0.2)}) + b_1(C_{i(0.8)} - C_{i(0.5)})}{C_{if(0.2)} + b_0(C_{if(0.5)} - C_{if(0.2)}) + b_1(C_{if(0.8)} - C_{if(0.5)})}$$

It should be mentioned that the scheme in Fig. 10 is suitable for programming ascending capacitor values. In the case that descending capacitor values should be realized, then the scheme depicted in the inset of Fig. 10 will be employed. In this case:

$$D = \frac{C_{i(0.2)} + b_1(C_{i(0.5)} - C_{i(0.2)}) + b_2(C_{i(0.8)} - C_{i(0.5)})}{C_{if(0.8)} + \overline{b_0}(C_{if(0.5)} - C_{if(0.2)}) + \overline{b_1}(C_{if(0.8)} - C_{if(0.5)})}$$

Consulting Fig. 5 and using Table 2, the following derivations are made: (i) integrators #1 and #2 could be controlled through the least significant bit (b_0) of the control word, due to the fact that the value of the feedback capacitor is the same for orders 3.5 and 3.8, (ii) integrators #3 and #5 are controlled through ($b_1 b_0$), owing to the existence of 3 discrete values of capacitors. The same is true for the integrator #4, but the scheme in the inset of Fig. 10 should be employed in order to realize the feedback paths since the values of feedback capacitor are descending with the order increase. Therefore, the digital word $(b_1 b_0) = (0, 0)$ corresponds to order 3.2, $(b_1 b_0) = (0, 1)$ to order 3.5 and $(b_1 b_0) = (1, 1)$ to order 3.8.

6 Conclusion

Fractional-step switched-capacitor filters of orders $(1 + a)$ and $(3 + a)$ were designed in this work. Simulation results indicate that the bilinear transform offers reduced total capacitor area and circuit complexity and simultaneously improved accuracy in comparison with those achieved through the utilization of the Al-Alaoui transform. Thus, bilinear transformation-based switched- capacitor filters are attractive candidates for realizing high- performance precise fractional-step filters.

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