A 256 $\times$ 256 ELEMENT InSb FOCAL PLANE ARRAY FOR GROUND-BASED ASTRONOMY

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Abstract. A 256 $\times$ 256 element InSb (indium antimonide) focal plane array has been specifically developed for use in ground-based astronomy. The array is an indium bump hybrid of a high-quality InSb detector array fabricated with an improved process, mated to a new, specially-designed low-background multiplexer. The performance parameters have been tuned to best reflect the requirements of ground based astronomy. The circuit is a direct readout detector integrator. It has a well size typically around 1,000,000 electrons, a readout rate of about 400kHz, and has an expected noise level of about 200 electrons.

1. Introduction

The needs of ground-based infrared astronomy in the medium wavelength infrared (MWIR) presents some rather interesting performance challenges. Since the ambient background photon flux can be fairly large in the longer wavelengths of the range, a reasonably deep integration well is required. If this well is entirely located in the detector capacitance, excessive detector bias is required, and a significant dark current penalty will be paid. On the other hand, a circuit such as direct injection with its integrator on the multiplexer, require far more photocurrent than astronomical applications provide to work properly. Also, the larger the capacitance, the larger the noise will be. Fairly high readout speed will be needed in order to keep from saturating with the background flux, but the amplifiers need to be band limited to reduce their noise contributions. Therefore, any design for this application must necessarily be a compromise between performance and usability.

The typical approach taken for astronomical applications is that of a detector integrator source follower. This was used in the Space Infrared Telescope Facility (SIRTF) designs[1] as well as the designs used for the proposed Hubble Space Telescope infrared refurbishment instruments[2]. That same approach is also utilized here, with particular customizations for this specific application. The detector array utilizes a newly developed detector process enhancement which offers some significant advantages in performance.

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2. Detector Array

The detector consists of a 256×256 array of indium antimonide mesa photodiodes. These detectors are made by diffusing a sheet junction into a wafer of indium antimonide material. Afterwards, the diodes are delineated with a deep mesa trench, and then passivated. The wafer is attached to a substrate and thinned to the correct thickness. The individual diodes receive a contact metallization, followed by an indium bump deposition. The die are then sawn from the wafer, screened, and are then ready to be mated to multiplexers.

The detectors used for this focal plane array (FPA) are intended to be the same as are used for both the SIRTF FPA[1] and also for the Cincinnati Electronics 256×256 pixel infrared thermal imaging camera FPA. Thus, there is a considerable savings in cost and technology development realized, and consistent results can be obtained.

3. Multiplexer Design

The multiplexer has a conventional detector integrator source follower design. The unit cell consists of an integration capacitance of approximately 100fF of detector junction capacitance in parallel with a double polysilicon capacitor of 170fF in the multiplexer (see Figure 1). This capacitance is reset through a double reset MOSFET to reset voltage VR which is typically 500mV above the detector substrate bias (normally ground). This reset occurs wherever a particular row and column are accessed, if the reset clock is pulsed. The integration capacitance is connected to the gate of a source follower amplifier which is connected to a common column bus through a FET switch.

Since the detector integration capacitance has been augmented by additional multiplexer capacitance, the well size will be nearly one million electrons at a typical reset voltage. About two thirds of the capacitance is this supplemental double polysilicon capacitor. This supplemental capacitor does not have voltage dependence like the detector junction capacitance has, so it is extremely linear. This improves the overall linearity of the integrator. Also, the use of a second polysilicon layer allows very good electrical shielding of the sensitive integration node from the clocked bus lines in the unit cell.

The reset FET switches are n-type allowing complete reset to ground. This simplifies the task of applying the proper bias to the detector. Both the unit cell source follower amplifier and the output source follower are p-channel to reduce their noise. Unfortunately, this does have the disadvantage of requiring the power supplies to be at a minimum of at least six volts (or even seven volts), to accommodate the loss of amplifier dynamic range due

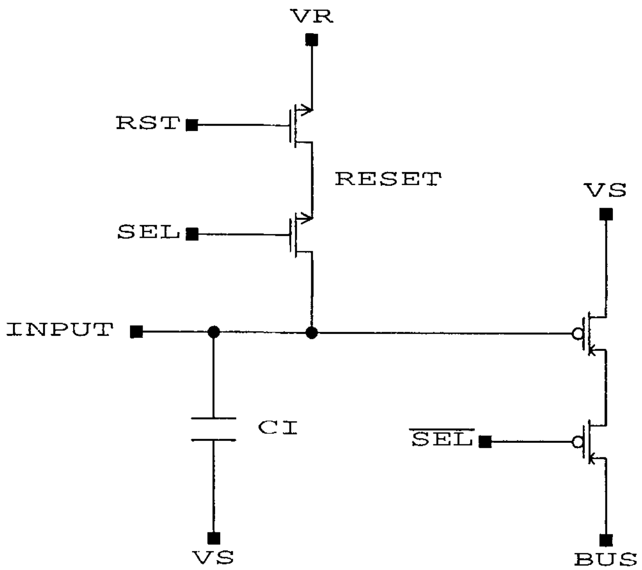

Fig. 1. Schematic of Multiplexer Input Cell.

to threshold voltage drop at each source follower. However, this has proven not to be a limitation.

The unit cell array is divided into four quadrants for parallel readout. At the edge of the quadrant, a set of FET switches are used to scan through each column to connect to the output bus corresponding to that quadrant. An output amplifier is at the end of the bus. The output amplifier is another source follower.

A set of shift registers are used to scan the select and reset switches. They consist of a series of d-type flip flops, cascaded together so that a bit pattern can be cascaded through it. There are four shift registers, one for each half of the array in either direction. The four shift registers are completely independent. Each has a clock, a serial input, and a serial output. Thus, for parallel operation, one would clock each pair of shift registers in parallel. One can also clock the pair of shift registers in series, basically connecting the serial output of the first to the serial input of the second, making one longer shift register. With this arrangement, the outputs operate serially, rather than in parallel. Of course, one also has the option of operating only one or more quadrants to reduce the size of the array.

For noise purposes, the digital and analog circuitry has separate power supplies to minimize digital clock feedthrough onto the analog circuitry. All power supplies are filtered on chip by large 50 to 100pF capacitors. Additional filtering can be supplied off chip.

The output amplifiers are located near their bonding pads to reduce the effects of bias current generated photons in the output amplifiers, thus making it more difficult to couple those photons into the unit cell array. The output amplifiers have been extensively guard banded and covered with a metal layer to maximize their isolation.

The multiplexer circuit has been designed with Orbit Semiconductor's standard 1.2 micron p-well double polysilicon, double metal process design rules. Only standard processing was used as a cost saving measure. It was not expected that these devices would need to be run at temperatures below about 20 to 30K, since the detector dark current will have largely bottomed out by then, so the standard fabrication process is more than adequate.

4. Focal Plane Array Performance

Several focal plane arrays have been fabricated from the multiplexers and detector arrays described above. The FPAs have received preliminary testing and in general meet expectations. All functionality built into the multiplexer is achievable in actual operation. The readout rate can be as high as 400kHz per output, which exceeds expectation by quite a bit. This means that the readout rate can be as high as 30Hz. This is important since the integration time must be the same (or longer) than the frame readout time. All four quadrants can be operated independently, so that the array can be configured as a 128 $\times$ 128 or 128 $\times$ 256 element array, if that is more appropriate.

Although the PFA was designed to run at 20K, operation of the FPA has been demonstrated all the way to liquid helium temperatures (4K). This means that the array can be used in a liquid helium dewar with no active temperature control, greatly simplifying dewar construction. Of course, the detector dark current does not get significantly better at temperatures below 30K, and the noise of the multiplexer will be somewhat higher due to the increase in MOSFET noise. Nonetheless, some applications will benefit from this extra capability.

The detector quantum efficiency has been measured at several astronomical wavelength bands. At L (roughly 3.45 to 4.30 micron), the mean detector quantum efficiency is 0.9. At M(4.15 to 5.40 microns) it is approximately 0.8. The detector fill factor is greater than expected, being about 80 percent. The dark current at 30K is shown in Figure 2. For a detailed report of dark current as a function of temperature, the reader is referred to Reference 1 which gives this data in detail for these detector arrays.

5. Conclusions and Acknowledgments

A focal plane array with performance optimized for use in ground-based astronomy has been developed and demonstrated. It offers a reasonably

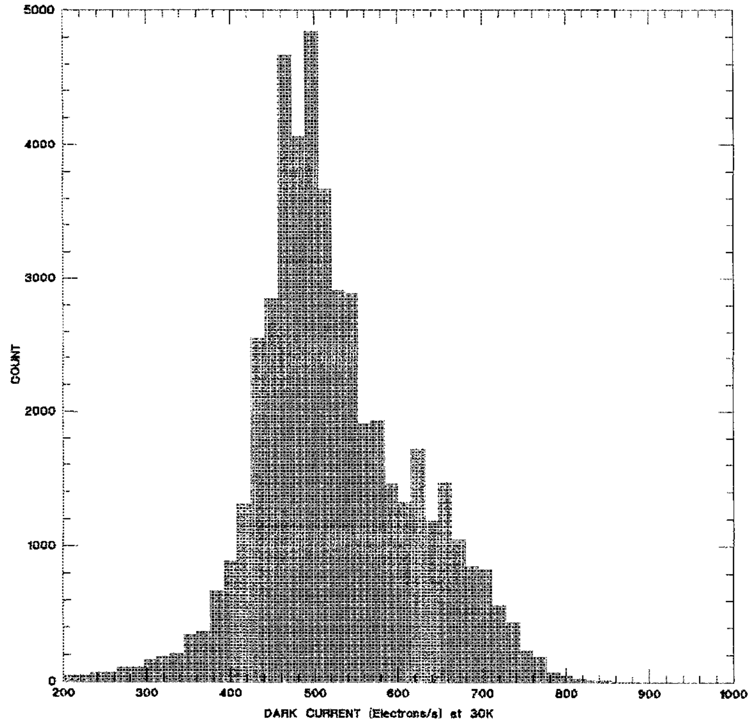

Fig. 2. Typical Dark Current at 30K.

low noise potential, coupled with a sufficiently deep integration well and sufficiently fast readout rate to allow it to be used in a variety of applications.

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