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Time-Resolved Electric Force Microscopy of Charge Trapping in Polycrystalline Pentacene

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Here we introduce time-resolved electric force microscopy measurements to directly and locally probe the kinetics of charge trap formation in a polycrystalline pentacene thin-film transistor. We find that the trapping rate depends strongly on the initial concentration of free holes and that trapped charge is highly localized. The observed dependence of trapping rate on the hole chemical potential suggests that the trapping process should not be viewed as a filling of midgap energy levels, but instead as a process in which the very creation of trapped states requires the presence of free holes.

Introduction. Charge trapping in films of π-conjugated molecules remains poorly understood despite the prominent role that such films are playing in the development of low-cost transistors and high-efficiency solar cells. The relatively poor stability of organic thin-film transistors and organic light-emitting diodes is a major roadblock to their commercialization.[1,2] Charge trapping has been suggested as a source of mobility reduction and turn-on voltage degradation in organic thin-film transistors[3] and luminescence efficiency loss in organic light-emitting diodes.[4,5]

Many mechanisms of charge trapping have been proposed for organic semiconductors. The large charge delocalization length in polymers allows for the possibility of charges forming a bipolaron, which, if stabilized by a structural defect, would lead to trapping. Bias-stress measurements suggest a bipolaron trapping mechanism in polythiophene and polyfluorene.[6,7] In amorphous films of small π-conjugated molecules, trapping is thought to result from potential wells created by randomly oriented dipoles in the substrate.[8] In pentacene, midgap states associated with grain boundaries,[9−15] molecular sliding,[16] and pentacene−quinone impurities[17] have been suggested, as have chemical reactions of pentacene with water and hydrogen[18] and hydrogen-transfer reactions between hydrogenated pentacene impurities and pentacene.[19,20]

Obtaining direct evidence in support of a charge trapping mechanism in pentacene has proven problematic. Transport measurements study traps only indirectly, through their effect on transistor subthreshold slope and field-effect mobility, and interpreting these measurements requires assumptions about trap heterogeneity, charge conduction mechanisms, and contact resistance. The kinetics of trap formation and decay in pentacene have been studied by variable-temperature space-charged current measurements,[20] but these measurements were bulk measurements carried out on a single crystal, so it is not clear whether the conclusions apply to polycrystalline pentacene employed in transistors. Although capacitance-voltage and deep-level-transient spectroscopy have identified a number of trap states near the pentacene/SiO_2 interface,[17] the data analysis requires modeling traps as fixed energy levels, not as states whose creation requires the presence of mobile holes.[19]

Muller and Marohn recently introduced a time-sequenced variation of electric force microscopy capable of directly imaging the location of long-lived traps in a thin-film transistor.[21] Electric force microscopy is a powerful method for studying charge trapping. In contrast with competing techniques, it does not require assumptions about injection at the contact or transport through the bulk and gives quantitative measurements of local trap concentration.

To gain additional information about charge trapping in pentacene, here we introduce *time-resolved* electric force microscopy to probe the evolution of charge traps as a function of initial hole concentration, position, and time. The dependence of *trap formation rate* on hole concentration and location provide important new clues about the mechanism of charge trapping in polycrystalline pentacene. Our data show that charge traps should not be viewed as static defect states but as states which are *created* by the presence of free holes at a film defect. This result indicates that a new level of theory will be required to understand the reactivity of polycrystalline pentacene.

Methods. *Device Fabrication.* Bottom-contact pentacene transistors were fabricated as follows. The electrodes were interdigitated channels of width 5 μm and total length 30 mm. The source and drain electrodes were 50 nm of Au deposited over 5 nm of Cr. The dielectric, SiO_2, was thermally grown to a thickness, h_{SiO_2}, of 900 nm. Prior to pentacene deposition, the transistor substrate was cleaned with Microposit Remover 1165, acetone, and isopropyl alcohol to remove a protective layer of Microposit S1813 photo resist. The substrate was then treated with a 10 min UV−ozone cleaning to remove any residual organic material and quickly transported to the vacuum deposition chamber. A 25 nm thick layer of pentacene (Aldrich, used as received) was deposited onto the oxide via vacuum evaporation in the dark at a rate of approximately 0.1 Å/s while the substrate was held at a temperature of 60 °C. Following pentacene deposition, the sample was cooled for 2 to 3 h in air and transferred into vacuum within 12 h. The resulting poly-

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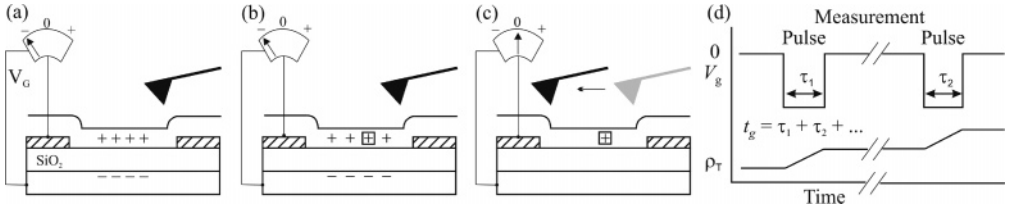

Figure 1. (a) Voltage is applied to the transistor gate, causing mobile charge to accumulate at the pentacene/SiO_2 interface. (b) After a time τ_i, some of this mobile charge becomes trapped, as indicated by the box. (c) The gate voltage is returned to zero, inducing mobile charges to leave the pentacene/SiO_2 interface. Trapped charge remains behind, and is characterized by electric force microscopy (EFM). (d) To measure the kinetics of charge trap growth, the voltage to the gate is pulsed; EFM imaging of the trapped charge density ρ_T is carried out in between gate pulses. Local charge trap density is studied as a function of the time t_g that free holes were available at the pentacene/SiO_2 interface.

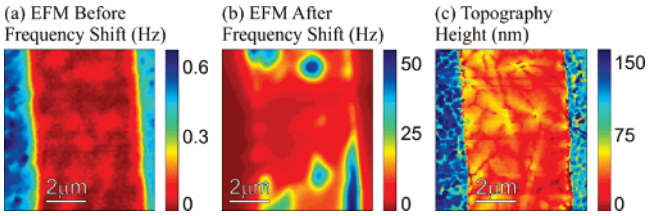

Figure 2. (a) Cantilever frequency-shift image of pristine sample. (b) Cantilever frequency-shift image acquired after the gate had been turned on for $t_g = 5$ min at $V_G = -50$ V. Trapped charge is highly localized. (c) Pentacene transistor topography, by AFM. The contacts appear as 50 nm tall (blue) features on the left and right of the image.

crystalline pentacene film transistors exhibited a saturation mobility of 1.3×10^{-2} cm^2/Vs and a threshold voltage of $V_T = -4$ V.

Atomic Force Microscopy. All microscopy was carried out in high vacuum and in the dark using a custom-fabricated vacuum electric force microscope.[21,22] We employed a commercial cantilever (MikroMasch NSC21/Ti−Pt) with a spring constant, k_0, of 1.0 N/m, a resonance frequency, f_0, of 25 kHz, and a vacuum quality factor, Q, of 1×10^4. Tapping mode atomic force microscopy was carried out using a drive amplitude of $x_{drive} = 180$ nm_{pp}, a set point of x_{drive}, and a linescan rate of 0.125 Hz.

Trap Kinetics. The procedure used to study the kinetics of trap formation in the pentacene transistor is sketched in Figure 1. Holes are introduced into the transistor's pentacene film by applying a negative voltage V_g to the gate electrode (Figure 1a). This results in a planar charge density of injected holes equal to $\sigma_h = C_g(V_g - V_T)$, where C_g is the gate capacitance per unit area and V_T is the transistor's threshold voltage. The gate was held at this voltage for a time step τ_i, which ranged from 50 ms initially to 1000 ms subsequently, during which time some of the mobile charge is converted into trapped charge (Figure 1b). The gate is then returned to zero in order to drive the mobile charge from the transistor channel.

Trapped charge, which decays with a time constant of approximately 45−140 min (see Supporting Information), may now be imaged. To detect the presence of trapped charge, the tip is scanned back and forth between the source and drain electrodes along a line, and at each position in the gap, the cantilever frequency is measured as a function of the tip-gate voltage (Figure 1c). Each such "linescan" typically takes 5 min. The pulse-measure sequence of Figure 3a−c is repeated up to $n_{tot} \sim 50$ times, and the trap density is plotted as a function of the total time $t_g = \sum_i \tau_i$ that holes were allowed to react (Figure 1d). After charge traps have reached steady-state, trapped charge is given 12 h to decay to zero before trap kinetics are studied at the next gate voltage.

Electric Force Microscopy. Frequency-shift electric force microscopy was used to probe local electrostatic potential and capacitance. The imaging resolution in experiments is approximately equal to the tip height, z, which was 200 nm. With no appreciable mobile charge in the transistor channel, the dependence of cantilever frequency f on tip-gate voltage V_{tg} may be approximated by[23]

$$f(V_{tg}) \approx f_0 - \frac{f_0}{2k_0}\frac{\partial^2 C_{tg}}{\partial z^2}(V_{tg} - \Delta\phi_{tg} - \Delta\phi_{tg}(t_g))^2 \qquad (1)$$

where C_{tg} is the tip-gate capacitance and $\Delta\phi_{tg}$ is the contact potential difference between the tip and gate in the absence of trapped charge. Trapped charge at the pentacene dielectric interface shifts the local electrostatic potential by an amount[23]

$$\Delta\phi_{tg}(t_g) \approx \sigma_T(t_g)\, h_{SiO_2}/\epsilon \qquad (2)$$

where σ_T is the planar trap density, h_{SiO_2} is the SiO_2 thickness, and $\epsilon = 4.64\ \epsilon_0$ is the dielectric constant of SiO_2. Equation 2 is derived by modeling the tip and gate as a parallel-plate capacitor and is valid when the dielectric is much thicker than the pentacene film, which is the case here. From a plot of $f(V_{tg})$, we extract both $\partial^2 C_{tg}/\partial z^2$ and $\Delta\phi_T$.

Results. Before the transistor was operated, we verified that no trapped charge was present initially. An image was recorded by measuring cantilever frequency as a function of position at a tip voltage of $V_{tg} = -2$ V (Figure 2a). Linescan data, where $f(V_{tg})$ was collected and fit at each point along a selected line in the sample, indicate that the observed frequency variations in Figure 2a are due mainly to local variations in capacitance (e.g., height); no trapped charge is present initially (see Supporting Information).

We then imaged the steady-state trap distribution to locate trap sites. To generate trapped charge, a gate voltage $V_g = -50$ V was applied for a time $\tau = 5$ min before being switched to zero. When trapped charge is present, the observed frequency variations are due predominantly to local variations in $\Delta\phi_T$. A map of frequency shift is collected again to give the image of Figure 2b; this image is essentially a map of long-lived trapped charge. Approximately one-third of sample points showed evidence of trapping. Comparing this image of trapped charge to the transistor topography shown in Figure 2c, we can see that trapped charge, although it does not appear to be confined specifically to grain boundaries or small grains, is nevertheless highly localized.

We used time-resolved electric force microscopy to examine locally the rate of trap formation. In Figure 3a, we plot the potential $\Delta\phi_T$ vs time observed over two different points in the sample at $V_g = -40$ V. In Figure 3b, we plot the steady-state potential $\Delta\phi_T(\infty)$ as a function of gate voltage V_g. For pentacene stressed at $V_g = -60$ V, we can see that the steady-state density of trapped charge (calculated as $\sigma_T(\infty) = \Delta\phi_T(\infty)\epsilon/h_{SiO_2}$) can be as large as $\sigma_T = 0.7 \times 10^{12}$ holes/cm^2. Comparing the trapped

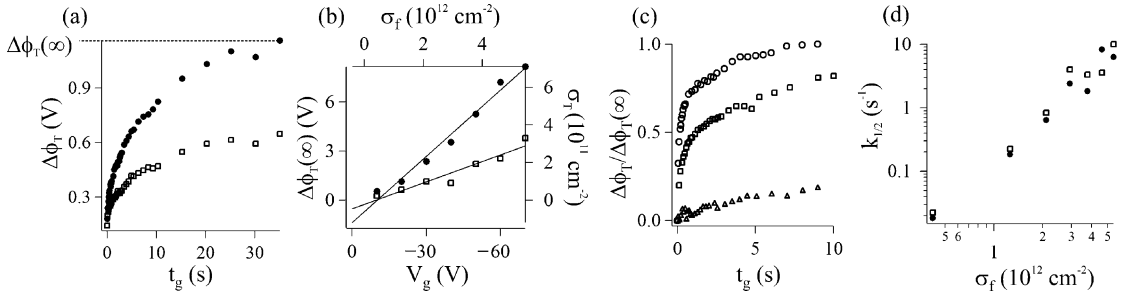

Figure 3. (a) Potential vs gate time at two locations. The potential reaches a steady-state value $\Delta\phi_T(\infty)$, which is different at each location. (b) Steady-state potential (trapped charge density σ_T) vs gate voltage (initial free charge density σ_f) at two locations. The density of trapped charge is linearly proportional to the density of initial free charge. (c) Normalized potential at one location for three different gate voltages: −70 V (circle), −30 V (square), and −10 V (triangle). The rate of trap formation increases with gate voltage. (d) A log−log plot of trap formation rate vs initial free charge density.

charge density to the initial free charge density at this gate voltage, $\sigma_f = 6 \times 10^{12}$ holes/cm^2, we can see that as many as 10% of initially available free holes trap. (The free charge density was calculated as $\sigma_f = C_g(V_g - V_T)/q_e$, using a threshold voltage of $V_T = -6$ V.) Assuming that all of the trapped charge is confined to a single pentacene layer at the SiO_2 interface, at a $V_g = -60$ V bias stress, the maximum observed concentration of trapped charge corresponds to approximately 1 charge per 640 pentacene molecules.

To compare the rate of charge trap formation at different gate voltages, we plot the normalized potential vs time over one point in the sample at three different gate voltages in Figure 3c. We can see immediately that the rate of trap formation depends strikingly on the initial concentration of free holes. To extract a model-free estimate of the trapping rate, we measure $t_{1/2}$, the time to reach half equilibrium, from plots like those in Figure 3c. The trapping rate $k_{1/2} = t_{1/2}^{-1}$ is plotted in Figure 3d as a function of the initial free hole density for two points in the sample.

Discussion. The main finding of this study is that traps in polycrystalline pentacene take at least seconds to reach steady state. This observation suggests immediately that the trapping process in our pentacene sample should not be viewed as a gate-driven filling of midgap energy levels.[8,17,20] Instead, the dependence of trap formation rates on hole concentration seen here indicates that the rate-limiting step in trap formation involves an activated process such as bipolaron formation or a defect-related chemical reaction. The data of Figure 3c,d does not fit well to either first- or second-order kinetics, suggesting that trap formation involves a series of reactions not well approximated by a single reaction which is rate limiting. The linear dependence of trap concentration on gate voltage indicates that free holes are the limiting reagent, not the impurities.

The spatial distribution of trapped charge found here differs markedly from the charge trap distribution observed recently in electric force microscopy experiments by Muller and Marohn,[21] who found that charge traps in their polycrystalline pentacene transistor were distributed in large patches within the transistor gap. Their sample had considerably smaller grains (<0.5 μm diameter) than does our sample (0.5−2 μm diameter) but was otherwise identical. This observation raises the intriguing possibility that two distinct charge trapping mechanisms are at play in pentacene, depending on the grain size. At a minimum, it suggests that comparing bulk measurements of trap density from different samples should be done with great care unless electric force microscopy images are also available to verify the trapping pattern. Our finding of highly localized charge trapping in polycrystalline pentacene suggests that analyzing the temperature dependence of bulk trapping kinetics[20] assuming a spatially homogeneous distribution of traps will considerably *under*estimate the Arrhenius prefactor (attempt rate).

Although seemingly inconsistent with grain-boundary trapping, the localized trapping seen in the polycrystalline pentacene sample studied here can be rationalized using a competing trapping mechanisms. Given the finite time that our samples spend in air, chemical reactions of pentacene with ambient water[18,19,24] are one potential source of traps. The trap image of Figure 3a indicates that these reactions, if occurring, are not occurring uniformly throughout the film or even at grain boundaries. Instead, the reactions would have to be occurring much faster at particular and relatively rare structural defect sites.[25] Another candidate impurity is hydrogenated pentacene;[19] Figure 3a suggests that reactions of holes with hydrogenated pentacene, if present, are ineffectually slow in the bulk. Again, we would need to invoke a structural-defect-assisted chemical reaction (or bipolaron formation) to explain our charge trap image.

Concluding Remarks. We have used time-resolved electric force microscopy to probe the local kinetics of charge trap formation in polycrystalline pentacene. The trapping rate depends strongly on the initial concentration of free holes. Trapped charge is highly localized. These findings suggest grain boundary trapping is not as important in polycrystalline pentacene as one would expect. Instead, our data support the notion that charges trap via an activated process, such as a chemical reaction, that is being assisted by a localized structural defect.

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Supporting Information Available: The following data is presented: (1) plots of hole concentration vs time during trap decay, demonstrating that the trap decay time is indeed much longer than the time required to perform an EFM linescan; (2) representative plots of cantilever frequency vs tip voltage; (3) linescans of potential and capacitance; (4) fits of Figure 3a to first- and second-order kinetics models; (5) plots of the resulting kinetics parameters vs free hole concentration; and (6) pentocene force−distance curves. This material is available free of charge at http://pubs.acs.org.

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