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ARTICLE *in* THE JOURNAL OF PHYSICAL CHEMISTRY B · APRIL 2010

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Polymer Brush and Inorganic Oxide Hybrid Nanodielectrics for High Performance Organic Transistors

Liqiang Li,[†,‡] Wenping Hu,[*,†] Lifeng Chi,[*,‡] and Harald Fuchs[‡]

Beijing National Laboratory for Molecular Sciences, Key Laboratory of Organic Solids, Institute of Chemistry, Chinese Academy of Sciences, Beijing 100191, China, and Physikalisches Institut and Center for Nanotechnology (CeNTech), Universitaet Muenster, Muenster D-48149, Germany

Received: January 31, 2010; Revised Manuscript Received: March 22, 2010

A novel covalence-linked PMMA-SiO_2 hybrid nanodielectrics was prepared by grafting ~10 nm PMMA brush onto the SiO_2 (~9 nm) surface, which effectively combines the respective merits of PMMA and SiO_2. As a result, the hybrid nanodielectrics exhibit excellent dielectric performance (e.g., low leakage density ($<10^{-7}$ A/cm^2 at 6 MV/cm), high breakdown voltage (7 MV/cm), high capacitance (142 nF/cm^2), good operational stability, and good compatibility with organic semiconductors), and enable organic field-effect transistors (OFETs) to work with high performance and low voltage. These results may open a way to build ultrathin dielectrics for high performance transistor and circuit, as well as for microelectronics, nanoelectronics, and organic electronics.

1. Introduction

The development of high performance nanoscaled dielectrics materials is indispensable for the progress of transistors with low operational voltage and high transconductance for high speed devices and circuits.[1−7] A variety of inorganic or organic dielectric materials have been used for micro/nano/organic electronics due to their respective merits,[8−12] such as high dielectric constant, high breakdown strength for inorganic dielectrics, mechanical flexibility, and good compatibility with organic semiconductors for organic (mainly referred to polymer) dielectrics. However, an individual dielectric is difficult to meet all the requirements, and the thickness of the dielectric layer is normally rather thick (>100 nm). It is believed that hybrid dielectric, that is, the integration of inorganic and organic polymer dielectrics is an efficient way to realize high performance dielectrics.[13−17] In this work, we present a novel covalence-linked organic/inorganic ultrathin hybrid nanodielectric layer fabricated by grafting ~10 nm PMMA brush onto SiO_2 (~9 nm) surface (as shown in Figure 1). This hybrid PMMA/SiO_2 nanodielectric exhibits excellent dielectrics qualities such as high capacitance, low leakage, high breakdown strength, good compatibility with organic semiconductors, and good operational stability, naturally resulting in high performance of its organic field-effect transistors (OFETs). It likely opens a new way to fabricate ultrathin dielectric layer for high performance transistors and circuits, as well as for microelectronics, nanoelectronics, and organic electronics.

2. Experimental Section

Pentacene, vanadyl phthalocyanine (VOPc), and perfluorinated copper phthalocyanine (F_{16}CuPc) were purchased from Aldrich Co. Ltd. and were purified two times by sublimation before using. All the other chemical reagents were gotten from Alfa Aesar Ltd. Methyl methacrylate (MMA) was distilled under reduced pressure. (3-Aminopropyl)triethoxysilane, 2,2′-bipyridine (Bpy), and 2-bromo-2-methyl-propionyl bromide were used as received. Tetrahydrofuran (THF) was dried by metal sodium. Triethylamine was dried by phosphorus pentaoxide.

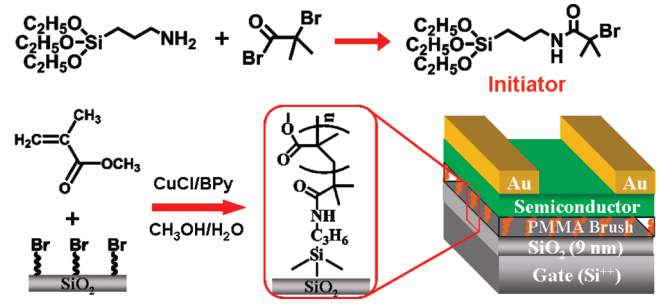

Figure 1. Schematic illustration of synthesis of surface-grafting PMMA brush on SiO_2 as hybrid nanodielectric for organic field-effect transistors.

^{1}H NMR spectra were taken on Bruker DMX-300 spectrometer using chloroform-d as solvent. Infrared spectra were obtained with Bruker Tensor 27 FTIR spectrophotometer. X-ray photoelectron spectroscopy (XPS) measurement was performed on ESCALab220I-XL. AFM measurement was carried out with Nanoscopy IIIa (U.S.A.). Sopra GES5 ellipsometer was employed to determine the thickness. The refractive index of silicon oxide, initiator, and polymer were all 1.50. The FET characteristics were measured with a Keithley 4200 SCS, a micromanipulator 6150 probe station in a clean and shielded box at room temperature in air. Capacitance-voltage measurement was carried out on Keithley CV590 analyzer at an ac signal frequency of 1 MHz.

Synthesis and Immobilization of Silane Initiator. A total of 2 mL (14.3 mmol) of dry triethlyamine, 2 mL (8.55 mmol) of (3-aminopropyl)triethoxysilane, and 70 mL of dry THF were added into a 250 mL flask, and then 2.0 mL (16.1 mmol) of 2-bromo-2-methyl-propionyl bromide was added slowly at room temperature. The solution was stirred for 4 h. After filtration of the precipitate, the THF was evaporated under reduced pressure and then dichloromethane was added. The solution was washed

* Corresponding author. E-mail: huwp@iccas.ac.cn (W.H.); chi@uni-muenster.de (L.C.).
† Chinese Academy of Sciences.
‡ Universitaet Muenster.

10.1021/jp100928d © 2010 American Chemical Society
Published on Web 04/07/2010

with diluted HCl and water and dried with magnesium sulfate. After removal of solvent, colorless oil was obtained (2.8 g, 88%). ^{1}H NMR (300 MHz $CDCl_3$, ppm): δ 6.86 (1H, s, N−H), δ 3.81 (6H, q, OCH_2), δ 3.26 (2H, m, NCH_2), δ 1.95 (6H, CCH_3), δ1.66 (2H, m, $SiCCH_2$), δ 1.22 (9H, t, $OCCH_3$), 0.65 (2H, t, $SiCH_2$).

Immobilization of silane initiator was performed by vapor deposition method. A drop of silane initiator was placed near the clean silicon wafer, and then this system was kept at 90 °C under vacuum for 3 h. After that, the wafer was ultrasonically washed by chloroform and acetone.

Surface-Initiated Atom Transfer Radical Polymerization. The bromo-functioned silicon wafer was placed in a homemade glass container under a N_2 atmosphere. MMA (10 g, 100 mmol) and 10 mL of solvent mixture (distilled H_2O/methanol: 4/1) containing CuCl (174 mg, 1.8 mmol) and BPy (312 mg, 2.0 mmol) was transferred into a container through a syringe. The solution was kept at 26 °C for 3 h. Subsequently, the silicon wafer was taken out of the solution and ultrasonically washed by THF, methanol, and chloroform successively. After that, immersion of silicon wafer in 0.1 M EDTA solution in water for 12 h could remove remained catalyst. Finally, silicon wafer was washed with toluene by Soxhlet extractor for 12 h.

Device Fabrication. Heavy doped silicon wafer was used as the substrate and gate. Hybrid SiO_2/PMMA was used as insulator. Pentacene, VOPc, and F_{16}CuPc was deposited on the substrates by thermal evaporation at the rate of 0.1 Å/s under 10^{-4} Pa at the substrate temperature of 30 °C, and then 30 nm thick gold source and drain electrode were defined via an interdigital shadow mask. The channel length and width were 50 μm and 2.5 mm, respectively. The field-effect mobility (μ) in the saturated region and threshold voltage (V_T) were calculated using eq 1:

$$I_{DS} = \frac{W}{2L} C_i \mu (V_{GS} - V_T)^2 \quad (1)$$

where C_i is the dielectric capacitance, W is channel width, and L is channel length.

3. Results and Discussion

The preparation of PMMA brush was performed via well-defined surface-initiated atom transfer radical polymerization (SI-ATRP) technique[18−21] on thermally oxidized SiO_2 (9 nm) surface, which produces covalence-linked and strongly adherent polymer brush and are therefore stable against delamination. The first step of SI-ATRP was immobilization of a silane initiator onto silicon wafer surface, followed by polymerization of methyl methacrylate (MMA) monomer via ATRP method. The grafting of PMMA can be determined by their XPS spectra (Figure 2a,b), which only exhibits strong C 1s and O 1s peaks and very weak Si 2s and Si 2p peaks. Furthermore, the C 1s core level region (Figure 2b) consists of the C−C species at 284.7, C−O species at 286.2, and O=C−O species at 288.5 eV, and their ratio is near 3:1:1, which also indicates the formation of PMMA layer.[22,23] The characteristic absorption (1730 cm^{-1} for the ester group, 2950 cm^{-1} for the C−H of the polymer chain) in FTIR absorption spectra (Figure 2c) further demonstrate the PMMA has been grafted onto SiO_2 surface. The AFM morphology image (Figure 2d) of the PMMA brush surface shows uniform, smooth, and compact surface. The root-mean-square (rms) roughness value is 0.63 nm, which is nearly comparable to the rms value of pure SiO_2 surface (0.5−0.8 nm).

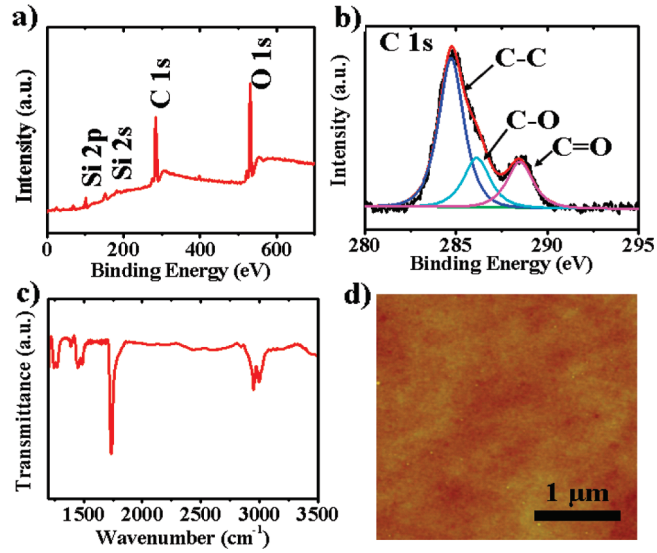

Figure 2. XPS surface analysis of PMMA brush: (a) wide scan and (b) C 1s core level spectra. (c) FTIR spectra of PMMA brush. (d) AFM image of PMMA brush.

Such smooth surface is favorable to promote molecular ordering of semiconductor layer and improve charge carrier mobility.[24]

Figure 3a displays leakage characteristics of several dielectrics, obtained on 15 individual n-Si/dielectric/Au capacitors with an area of 2.25 × 10^{-4} cm^2. Obviously, comparing with pure SiO_2 (9 nm) layer (curve a), attachment of surface-grafted PMMA layer (ca. 10 nm) on SiO_2 surface (curve d) can significantly reduce leakage current density by several orders of magnitude. At a voltage of 5 V (corresponding to an electric field of ca. 2.5 MV/cm), the leakage current density for PMMA/SiO_2 dielectrics is 0.8−3 × 10^{-8} A/cm^2. Even at 6 MV/cm, the leakage current density for PMMA/SiO_2 is still in the range of 3.5−8.5 × 10^{-8} A/cm^2. These leakage characteristics are comparable to (if not better than) those of self-assembled dielectrics, thicker spin-coated polymer, some inorganic dielectrics, and hybrid organic/inorganic dielectrics (10^0−10^{-8} A/cm^2).[8−17,25−38] For further comparison, we also fabricated another two dielectrics, that is, spin-coated PMMA (10 nm) on SiO_2 (9 nm; curve b) and surface-grafting PMMA (20 nm) on silicon wafer with native SiO_2 layer (curve c). The leakage measurement indicates that, under the same thickness, covalence-linked PMMA/SiO_2 exhibits lower leakage than spin-coated PMMA/SiO_2 and pure surface-grafted PMMA. These results indicate that covalence-linked PMMA/SiO_2 bilayer structure is more favorable to lower the low leakage, which may be due to the close packing of polymer brush and cooperative protection effect of bilayer structure (as shown in Figure 3d). The measured breakdown strength (Figure 3b) for PMMA/SiO_2 (curve d) is 7.0 ± 0.5 MV/cm, which is larger than that of pure PMMA brush (3.0 ± 0.5 MV/cm, curve c), and it rivals or exceeds some self-assembled dielectrics, thick polymer dielectrics, and some metal oxides,[8−17,25−38] suggesting the covalence-linked bilayer structure can enhance the breakdown strength of dielectrics.

Capacitance−voltage measurements (Figure 3c) were carried out to investigate the capacitance and hysteresis of these dielectrics. The capacitance of PMMA/SiO_2 is calculated to be 142 nF/cm^2 in the accumulation region, which is much higher than the capacitance of commonly used 300 nm SiO_2 or thick polymer dielectrics (with capacitance of several to tens of nF/cm^2). Furthermore, $C-V$ curves for the PMMA/SiO_2 nanodi-

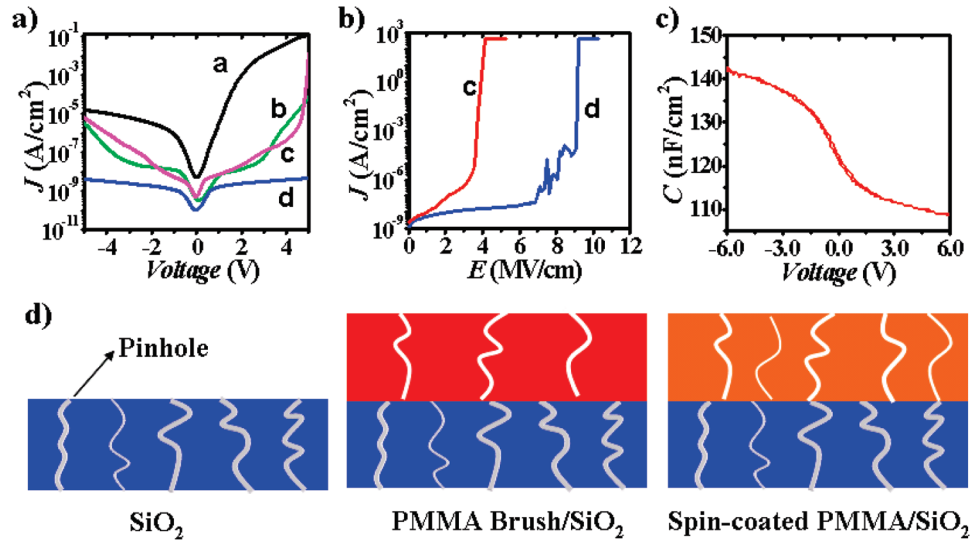

Figure 3. (a) Leakage characteristics and (b) breakdown electric field characteristics for different dielectrics measured with the structure of Au/dielectric/Si capacitor. Curve a, SiO_2 (9 nm); curve b, spin-coated PMMA (10 nm)/SiO_2 (9 nm); curve c, surface-grafting PMMA (20 nm); curve d, surface-grafting PMMA (10 nm)/SiO_2 (9 nm). (c) Capacitance−voltage characteristics for PMMA/SiO_2 dielectrics. $C-V$ curves were measured at an ac signal frequency of 1 MHz. (d) Schematic diagram of distribution of pinhole defect in the dielectrics, indicating the reason why PMMA brush/SiO_2 bilayer dielectrics show the lowest the leakage compared with other dielectrics.

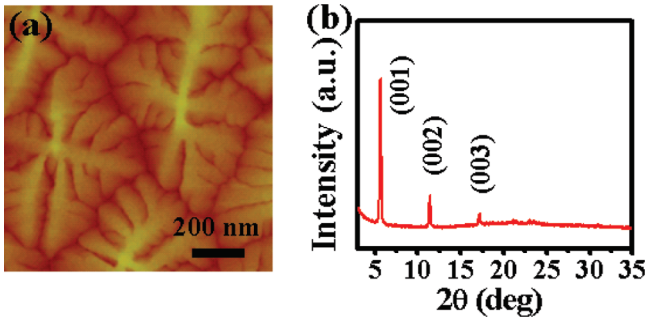

Figure 4. (a) AFM image and (b) XRD patterns of pentacene film on PMMA brush.

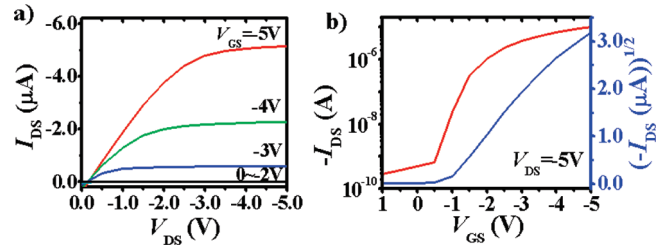

Figure 5. (a) Output and (b) transfer curves of pentacene OFETs with PMMA/SiO_2 nanodielectrics.

TABLE 1: Data of OFETs with PMMA/SiO_2, 300 nm SiO_2, and 350 nm Spin-Coated PMMA Dielectrics

semiconductors	dielectrics	mobility[a] (cm^2/(V s))	threshold voltage[a] (V)	on/off ration
pentacene	PMMA/SiO_2	0.21	−0.81	3.8×10^4
	SiO_2 (300 nm)	0.10	−19.7	2.1×10^5
	PMMA (350 nm)	0.31	−17.5	4.4×10^4
VOPc	PMMA/SiO_2	0.033	−0.54	1.2×10^3
	SiO_2 (300 nm)	5.8×10^{-5}	−25.4	2.3×10^4
	PMMA (350 nm)	0.040	−23.3	3.1×10^4
F_{16}CuPc	PMMA/SiO_2	0.0027	0.24	1.1×10^3
	SiO_2 (300 nm)	0.00078	27.8	2.4×10^3
	PMMA (350 nm)	0.0051	20.2	2.0×10^3

[a] The data for devices with PMMA/SiO_2 nanodielectrics were obtained at operating voltage of ±5 V, the corresponding values for SiO_2 (300 nm) and spin-coated PMMA (300 nm) dielectrics were obtained at ±100 V.

electrics exhibit slight hysteresis (the shift of capacitance), suggesting they contain very little charges traps.

To investigate the performance of the hybrid nanodielectrics in devices, OFETs were chosen as test bed because (1) charge accumulation and transporting in OFETs mainly occur in the several bottommost semiconductor layers adjacent to the dielectrics, and are dramatically influenced by the property of dielectrics. Therefore, the electrical property of OFETs can directly reveal the performance of dielectric; (2) OFETs have been endowed a great promise for low-cost, large-area, and flexible electronic circuits. To realize their practical applications, development of high performance nanodielectrics is still one of highly urgent tasks. Series of top-contact pentacene OFETs were fabricated at substrate temperature of 30 °C. Figure 4a and b show the AFM morphology image and XRD patterns of pentacene layer, respectively. The dentritic morphology and strong diffraction peak indicate high ordering of pentacene film on PMMA brush surface, which is one of prerequisites for high mobility.

Device measurements demonstrate that all the pentacene devices show distinguished low threshold voltage (0 ∼ −1 V) and high mobility (∼0.2 cm^2 V^{-1} s^{-1}). As shown in Figure 5a and b, under low operational voltage (<5 V), the devices with PMMA/SiO_2 dielectrics exhibit good field effect modulation characteristics with well-defined linear and saturated region. Their OFETs data are summarized in Table 1. For comparison, the devices with 300 nm SiO_2 and 350 nm PMMA as gate dielectrics were fabricated under the identical conditions. Their devices data under operational voltage of 100 V were summarized in Table 1 too. Under a different voltage range, the mobility of devices with PMMA/SiO_2 nanodielectrics is comparable to the devices with thick PMMA dielectrics, and better than that with 300 nm SiO_2 dielectrics, which demonstrates good compatibility between PMMA brush and semiconductors. The threshold voltages of the devices with PMMA/SiO_2 dielectrics are near 20−30 times lower than that of devices with thick PMMA or SiO_2 dielectrics. The significantly reduced threshold voltage is mainly due to the large dielectric capacitance. In addition, we also tried to fabricate OFETs with pure 20 nm

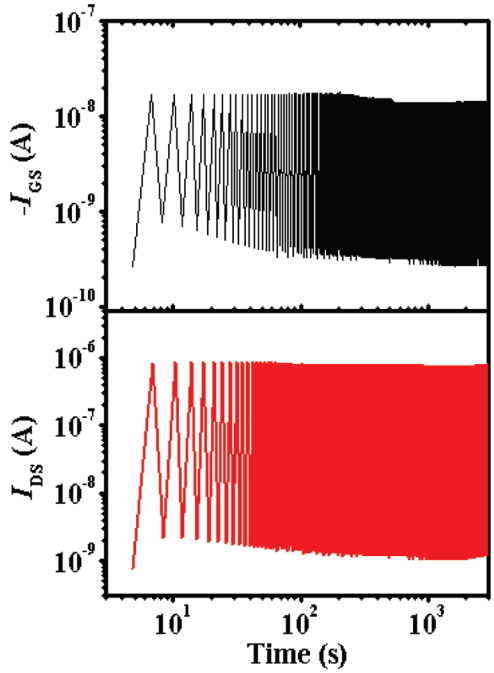

Figure 6. Operational stability of VOPc devices with PMMA/SiO_2 nanodielectrics: upper part, gate leakage current; lower part, drain current. Stability measurements were performed by continuously applying alternative V_{GS} of 0 and −5 V at V_{DS} = −5 V.

PMMA brush or 9 nm SiO_2 dielectrics, but the devices with 20 PMMA brush dielectrics can only be operated safely under 2−3 V, which leads to low performance (mobility <0.06 cm^2 V^{-1} s^{-1}); once the operational voltage increases to 4−5 V, most of devices suffer from large leakage or even break down. The devices with 9 nm SiO_2 dielectrics could not work due to the huge leakage.

To further investigate the generality of the surface-grafted PMMA/SiO_2 dielectrics, another two popular p-type semiconductor (vanadyl phthalocyanine, VOPc)[39−42] and n-type semiconductor (perfluorinated copper phthalocyanine, F_{16}CuPc)[43−46] were also studied with these PMMA/SiO_2 dielectrics. Similarly, their devices with the surface-grafted PMMA/SiO_2 nanodielectrics also yield good field effect behavior with low operational voltage. The parameters of the VOPc and F_{16}CuPc OFETs with different dielectrics are also summarized in Table 1.

Operational stability of the OFETs with the PMMA/SiO_2 nanodielectrics is shown in Figure 6. VOPc devices were used to perform this test due to the excellent stability of VOPc.[19,20] During and after the cycle test over 3000 s, the mobility of VOPc devices show no obvious degradation and the gate leakage current almost remains unchanged. These results demonstrate that the surface-grafted PMMA/SiO_2 dielectrics possessed good operational stability.

The above results demonstrate that linear PMMA brush/SiO_2 nanodielectrics show excellent performance in devices with a vacuum-deposited organic semiconductor. Furthermore, the stability of the polymer brush against the solvent indicates its potential application in solution-deposited organic semiconductors. However, a linear polymer layer brush will be swollen after treatment with some solvent for a long enough time, which is common nature for a polymer, so the application of a linear polymer brush layer may be limited to the solution process with fast solvent evaporation such as spin-coating or dip-coating. Preparation of a cross-linking polymer brush may overcome this problem and widen the application of the type of polymer brush/inorganic oxide nanodielectric in solution deposited devices.

4. Conclusions

In conclusion, we have demonstrated a new high performance polymer brush/inorganic oxide hybrid nanodielectric prepared by grafting 10 nm PMMA brush on a 9 nm SiO_2 surface, which enables OFETs to work with high performance and low voltage. This hybrid nanodielectric possesses three key features: (1) compared with a pure single structure, a covalence-linked bilayer structure significantly reduces dielectric leakage and enhances the breakdown strength; (2) compared with spin-coated polymer film, a surface-grafting polymer brush can form a compact film and lower leakage; and (3) compared with a laminated or blended structure based on physical adsorption, the covalence-linking enables the heterogeneous PMMA and SiO_2 to be strongly combined together and therefore be stable against delamination. Based on the unique structure, this nanodielectric exhibits good dielectric qualities such as smooth surface, high capacitance (142 nF/cm^2), low leakage current density (<10^{-7} A/cm^2 at 6 MV/cm), high breakdown electric field (7 MV/cm), good operational stability, and good compatibility with p- and n-channel semiconductors. These results suggest the bright future of the polymer brush/inorganic oxide hybrid nanodielectrics in micro-, nano-, and organic electronics.

Acknowledgment. The authors acknowledged the financial support from National Natural Science Foundation of China (20721061, 20872146, 50725311), TRR61 (NSFC-DFG Transregio Project), Ministry of Science and Technology of China (2006CB806200, 2006CB932100, 2009CB930400), and Chinese Academy of Sciences.

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JP100928D