Optofluidic encapsulation and manipulation of silicon microchips using image processing based optofluidic maskless lithography and railed microfluidics

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We demonstrate optofluidic encapsulation of silicon microchips using image processing based optofluidic maskless lithography and manipulation using railed microfluidics. Optofluidic maskless lithography is a dynamic photopolymerization technique of free-floating microstructures within a fluidic channel using spatial light modulator. Using optofluidic maskless lithography *via* computer-vision aided image processing, polymer encapsulants are fabricated for chip protection and guiding-fins for efficient chip conveying within a fluidic channel. Encapsulated silicon chips with guiding-fins are assembled using railed microfluidics, which is an efficient guiding and heterogeneous self-assembly system of microcomponents. With our technology, externally fabricated silicon microchips are encapsulated, fluidically guided and self-assembled potentially enabling low cost fluidic manipulation and assembly of integrated circuits.

Introduction

In the integrated circuit industry, encapsulation of a device is necessary for several reasons, such as a protection from external environments,[1–4] a light conversion layer from an LED chip,[5,6] heat transfer,[7] *etc*. The major functionality of encapsulation is protection which prevents certain areas of microchips, such as bond pads, from coming into contact with external environments like a liquid solution. In addition, encapsulants reduce the thermal stress from operating chips and preserve their original geometry. With such encapsulants, mainly plastic, epoxy, or photocurable polymer, the lifetime of each chip can be increased. However, current commercial technologies encapsulate overall areas of the chips during the process, thus it is hard to selectively encapsulate the surfaces of chips considering external contacts for wire-bonding.

Recently introduced in our previous work, the optofluidic maskless lithography (OFML) technique[8] can be applied to the chip encapsulation process combined with image processing overcoming the patterning problem. Since silicon microchips tend to move randomly in a fluidic channel, it is necessary to consider a real-time situation such as rotational alignments or orientation of chips during the polymer encapsulation process.

The chip should be effectively assembled on the appropriate substrate after the encapsulation of each chip. Microdevice assembly technologies can be categorized into several methods: the micromanipulating method,[9] the fluidic self-assembly method,[10–13] stress driven assembly,[14,15] or capillary force based self-assembly[16–18] *etc*. Each technology has its powerful merits to manipulate and assemble devices, but also has limitations. Micromanipulator based assembly or serial pick-and-place robotic assembly is a very deterministic process, allowing high assembly yield with great flexibility in component choice.[9] However, with component size smaller than 200 μm, assembly process time increases and the production cost becomes expensive due to the difficult control requirements needed to position parts with high accuracy. Also, strong stiction forces make the assembly process even more difficult at the microlevel. In contrast, since fluidic self-assembly (FSA) is a parallel process introducing lots of components at once, it is faster and cheaper than serial pick-and-place assembly.[10] However, assembly yield is not as high as conventional robotic assembly due to the probabilistic nature of FSA. It requires unnecessary mass production of microcomponents to increase assembly yield. In addition, both FSA and capillary force based self-assembly need alignment to unique in-plane orientations because reversed or disoriented devices are not filtered during the process.

Railed microfluidics has been recently demonstrated to guide and assemble various microscale components as a high yield and high throughput process to overcome limitations of current assembly techniques.[19] A groove on top of the microfluidic channel, what we call a 'rail', functions as a guide track, thus a photopolymerized finned microstructure is guided along the rail due to the matching shape of the fin and the rail. Also, guided microstructures are fluidically assembled at the end of the rail, a geometrical barrier of the microfluidic channel. It is a fully deterministic way to guide microstructures and assemble them within the fluidic channels without an error in parallel.

In addition to the controllability of photopolymerized structures, externally introduced components such as silicon microchips or living cells can be also guided and assembled. To be assembled, externally introduced components also need guiding-fins, which are essential parts to guide components along the rail. Thus, we need to detect components in real-time and manually expose fins for each component to manipulate using railed microfluidics. The guiding-fins can also be fabricated *via*

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ultraviolet (UV) patterning right onto the exact components using the OFML technique combined with image processing as the encapsulation process.

In this paper, we propose an easy and effective silicon microchip encapsulation method within microfluidic channels called Image Processing based Optofluidic Maskless Lithography (IP-OFML) and assembly of encapsulated microchips using railed microfluidics. Note that encapsulation refers to polymer coating around silicon microchips for chip protection and conveying. IP-OFML allows real-time chip detection and dynamic digital micromirror device (DMD) mask generation of both polymer encapsulants and guiding-fins. Precisely detected and encapsulated silicon chips can be guided and assembled using railed microfluidics. In this process, the depth of the microfluidic channel can be divided into a shallow region for polymer encapsulation, and a deep region allowing dynamic fin fabrication without molding fins by the rail. Polymer encapsulants of silicon chips are generated within a shallow region and when encapsulated silicon chips move to the deep region, fins are fabricated on top of the encapsulants. Finally, encapsulated silicon microchips are assembled using railed microfluidics.

Using the IP-OFML technique, various encapsulation and patterning examples, such as multi-layer coating, selective portion coating, and microdevice top surface patterning are demonstrated. Also, with guiding-fins on top of the encapsulants, we manipulated silicon microchips within microfluidic channels and then assembled successfully. Shape-matching polymer encapsulants for each silicon microchip are also shown for better alignments of silicon microchip assembly.

Results and discussion

Image processing based optofluidic maskless lithography

OFML is an *in situ* photopolymerization technique of various microstructures dynamically within microfluidic channels using MEMS spatial light modulator.[8] Combined with computer-vision aided image processing, real-time DMD mask generation is executed during the lithography process. It enables dynamic detection and patterning of randomly dispersed silicon chips in microfluidic channels. Fig. 1 schematically describes the IP-OFML method. With the lithography method, silicon chips are encapsulated with polymer and guiding-fins are generated on top of the polymer encapsulants. The method starts with the introduction of silicon microchips mixed with polymer resin. An image of dispersed silicon microchips in the channel is taken from the charge-coupled device (CCD) of the optical microscope. The image is then transferred to the computer for the mask generation process. The corresponding DMD mask for polymer encapsulation of silicon chips is generated *via* image processing. The generated mask pattern is loaded onto DMD, and patterned UV light is exposed to the original silicon chips in the microfluidic channel. A total of two steps of lithography are executed to make encapsulated silicon microchips with guiding-fins on top; first for polymer encapsulation and second for guiding-fin fabrication. The fin generation process is the same with the polymer encapsulation process. The whole process from image capturing to UV patterning takes 4–5 seconds. For higher uniformity of the polymer encapsulants, silicon chips should not move during the encapsulation process. Therefore, polymer resin is stopped during the process and flowed after encapsulation. The total number of silicon chips encapsulated within a microfluidic channel depends on silicon device size, encapsulation thickness, field of view, and objective lens magnification of the microscope. For example, the maximum throughput rate of 100 μm × 100 μm sized silicon chips with 10 μm encapsulation thickness using a 4× objective lens is 300 000 chips/min. In the current IC industry, the fixation step of rotated chips is added for precise chip packaging. However, our technique eliminates the alignment step and *in situ* encapsulates the chip conformally with increased encapsulation throughput.

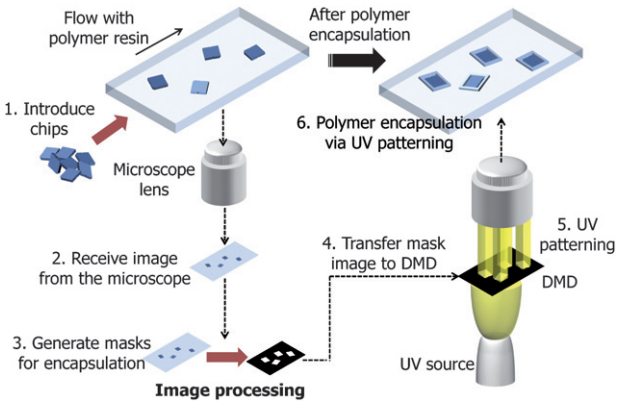

Fig. 1 Schematic diagram of image processing based optofluidic maskless lithography method. (1) Silicon microchips are introduced into the microfluidic channel mixed with polymer resin. (2) CCD takes an image of dispersed silicon chips in the channel. (3) DMD mask pattern for polymer encapsulation or fins generation of corresponding silicon chips is generated *via* image processing. (4) Generated mask is loaded onto the DMD. (5) UV light is patterned *via* DMD. (6) Patterned UV light is exposed to the original silicon chips in the microfluidic channel.

Image processing

In order to consider rotational alignments and orientation of silicon chips during polymer encapsulation or the fin generation

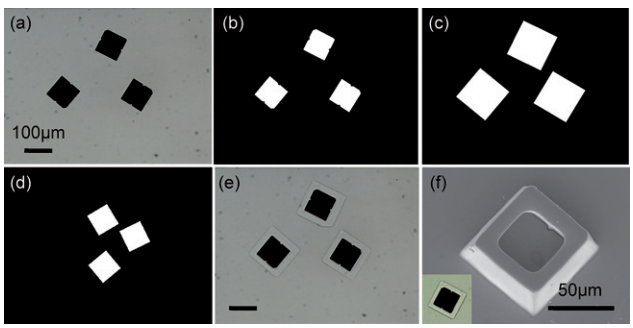

Fig. 2 Image processing for silicon microchip encapsulation. (a) Image of silicon chips taken from CCD. (b) Black and white image conversion. (c) Replace the silicon chip image to the corresponding encapsulant image. (d) Final DMD mask image *via* rotation and resize of the image to fit into DMD. (e) UV patterning with loaded DMD mask to the original silicon chips within the microfluidic channel. (f) SEM image of packaged silicon chip; inset shows corresponding optical microscope image.

process, we use an *in situ* DMD mask pattern generation technique based on image processing using silicon chip images acquired from the CCD. Fig. 2 shows the detailed image processing steps, *i.e.* the encapsulation process. An image of dispersed silicon chips in the fluidic channel is converted into a black and white image as shown in Fig. 2(b). In this step, unwanted objects in the exposure area are eliminated by filtering off the image. After the detection of edges and corners of each silicon chip, the computer calculates rotation angles and positions of chips, and replaces each chip image with the encapsulation image matching the position and rotation, such as white squares, as shown in Fig. 2(c). Since the full original detected CCD image size is 680 × 512 pixels, the generated target image should be rotated, resized, and put to 1024 × 768 white board to fit into the DMD mask image size (Fig. 2(d)). The final mask image is loaded onto DMD and the original target silicon chips are encapsulated *via* UV patterning (Fig. 2(e)).

Owing to the image processing based OFML, the uniform thickness of polymeric encapsulants of silicon chips is easily achieved. We envision that uniform polymer encapsulant layer control will be useful for integrated complementary metal-oxide-semiconductor chip packaging or light emitting diode (LED) phosphor coating. Furthermore, our technique also has applicability in cell detection and encapsulation for surface immunoprotection considering various cell size and shapes which can be a utilized toolset in the lab on a chip field.

Various silicon microchip encapsulation and patterning

Using the IP-OFML described in the previous section, various kinds of encapsulation and patterning are demonstrated for further applications. Each microchip is detected and encapsulated one by one considering each silicon chip's rotation and orientation. This accurate detection enables uniform encapsulation of silicon chips which can be applied to the phosphor coating of an LED. Phosphor converts the light from the LED chip to longer wavelength light, *i.e.* from UV or blue light to yellow, red, green, or white light. Since uniform light distribution emitted from the LED depends on the uniformity of the phosphor layer surrounding the LED chip, a uniform phosphor coating technique with high accuracy and inexpensive production cost is required.

White light emission from an LED can be demonstrated in several ways, such as a single white stack, vertical red green blue stack or horizontal red green blue stack using color mixing. To realize these color mixing methods in a white LED, multilayer coating technology is necessary for each red, green and blue phosphor layer formation. Here, we show a multilayer polymer encapsulation process using silicon microchips instead of LEDs for a proof-of-concept demonstration as shown in Fig. 3(a). In these experiments, we coated a total of three layers by sequentially introducing and photopolymerizing each material one by one within the microfluidic channel for each encapsulant layer. The first layer is made of PEG-DA, the second layer is rhodamine B labelled PEG-DA, and the final layer is fluorescein (FITC) labelled PEG-DA. The thickness of each layer is 30 μm. We envision a multilayer coating method using IP-OFML technique that can be easily applied to uniform RGB phosphor coatings on LED chip.

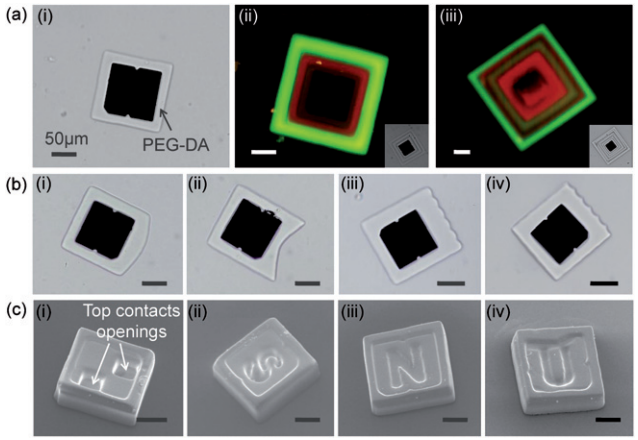

Fig. 3 Various polymer encapsulations. (a) Multilayer heterogeneous silicon microchip coating: (a)(i) one layer coating, PEG-DA; (a)(ii) three layers coating, PEG-DA and rhodamine B labelled PEG-DA, and FITC labeled PEG-DA; (a)(iii) five layers coating, PEG-DA, rhodamine B, FITC, rhodamine B, and FITC labeled PEG-DA. (b) Selective side coating for application of ELED light guiding lens structure fabrication: (b)(i)–(ii) single convex/concave type encapsulation; (b)(iii)–(iv) multi convex/concave type encapsulation. (c) Top surface patterning and encapsulation for application of LED top contacts.

In addition to multi-layer coating application, our lithography technique can be applied to edge emitting LED (ELED) light guiding lens structure fabrication (Fig. 3(b)). To enhance light efficiency from the ELED to the light guiding panel, emitted light should be expanded or focused through the appropriate lenses at each emitting side of the LED. For example, single or compound convex lenses converge emitting light and single or compound concave lenses diverge emitting light. Since we fabricate lens structure and polymer encapsulants by one-time exposure, process time and complexity are reduced a lot compared with current commercial processes.

The final encapsulation example is the top surface (or bottom surface) patterning of devices (Fig. 3(c)). Each semiconductor or LED chip has contacts for an external power source, and these contact parts should not be coated with polymer. Current commercial technology first executes wire-bonding and then packages around the chip. Therefore, if we observe defects on the chip after encapsulation, the spent expense is irreversible. In contrast, if contacts are not coated during the encapsulation process, we can reduce production cost by eliminating defected components before wire-bonding. Therefore, our technology is an easy, cheap and fast process to encapsulate silicon chips, thus more efficient than current technology.

Furthermore, polymeric encapsulation of microdevices in a fluidic environment enables *in situ* material exchange and encapsulant fabrication eliminating conventional sacrificial layer formation and patterning *via* photolithography. For example, in conventional lithography, patterning three different materials in a single substrate requires three separate photolithography steps, three separate alignment steps, and three separate material patterning steps for three-layer polymer coating. However, our technology greatly reduced those steps by fluidically exchanging materials in microfluidic channels and encapsulating the chip for each material as shown in Fig. 3(a)(ii). This fluidic approach also

enables various types of encapsulation in a single microfluidic channel without substrate or photomask exchange as shown in Fig. 3, thus production cost can be reduced a lot.

Railed microfluidics for silicon chip guiding and assembly

Railed microfluidic channel for manipulation and assembly of silicon microchips is composed of three regions (Fig. 4). The first region is a channel layer with 38 μm depth. In this region, silicon chips are encapsulated with polymer. Then, encapsulated silicon chips move to the second region which is a rail layer with 70 μm depth. Here, fins of silicon chips are fabricated on top of the polymer encapsulants without molding fins by the rail. When the encapsulated silicon chip stops moving, fins are formed on top of the encapsulants due to UV patterning from the bottom of the channel. Three microscopic images in Fig. 4(d) show the condition of the silicon microchip in each step. Fig. 4(d)(i) is a bare silicon chip in a microfluidic channel, Fig. 4(d)(ii) shows an encapsulated silicon chip in the first region, and the chip in Fig. 4(d)(iii) has guiding-fins on top of the polymer encapsulants fabricated in the second region. Insets of each image are scanning electron microscope pictures. The final region is the rail-guiding region where the rail layer becomes narrower forming a rail as shown in Fig. 4(a). In this region, silicon chips with fins enter into the rail and are guided along the rail. The railed microfluidic control method enables effective silicon chip manipulation conveying objects to the designated position within the fluidic channels and assembling them in a desired way easily.

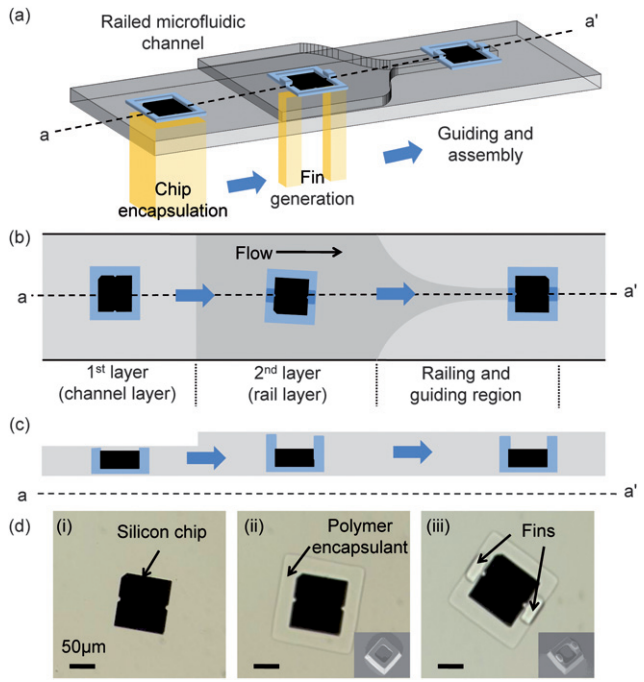

Fig. 4 Rail-guiding and assembly process. (a) Perspective view. First, the silicon chip is encapsulated within the channel layer. When the encapsulated silicon chip is moved to the rail layer, fins are fabricated on top of the encapsulants. In this step, IP-OFML is also executed. Finally, due to the fins on top of the encapsulants, the silicon chip is guided along the rail and assembled at the end of the rail. (b) Top view. (c) Cross-sectional view. (d) Silicon microchip images: (i) floating silicon chip in the channel layer, (ii) encapsulated silicon chip in the channel layer, and (iii) fin-generated silicon chip in the rail layer.

The fluidic control of devices using the railed microfluidic channel is an innovative technique to manipulate microscale silicon chips. Silicon microchips with guiding-fins on the encapsulants flowing in the rail layer approach to the guiding region and finally enter into the rail (Fig. 5(a)). Fig. 5(b)(i) shows the final assembled silicon chips at the end of the rail with equidistance due to the uniform encapsulant thickness. The encapsulant shape of silicon chips can be modified for well-aligned assembly. Since fabricated fin size is smaller than the rail width, the assembled silicon chips can be distorted a little bit in arrangements and each silicon chip can be slanted with respect to the rail. With a shape-matching encapsulant, tilted silicon chips can be aligned along the rail (Fig 5(b)(ii)). Finally, externally fabricated chips are efficiently guided and assembled using the rail. Placing chips with equidistance has commercial implications for an LED-based back-light unit or LED phosphor coatings where a large number of small LED chips can be placed in a larger substrate, such as a glass plate or a silicon wafer.

Since undesirable silicon chips interfering with the well-ordered assembly on the rails should not be used during the process, several detecting schemes in the image processing can be applied to optimize the process for an effective manipulation and assembly. Silicon chips tend to move randomly in the channel, thus various conditions, such as clustered, broken, or flipped chips, should be considered for better alignments. The options can be divided into two parts, encapsulation options (Fig. 6(a)–(b)) and fin fabricating options (Fig. 6(c)–(d)). For encapsulation options, if the distance between two or more silicon chips is smaller than two times the coating thickness, all related silicon chips are filtered out by not encapsulating particles (Fig. 6(a)). In addition, the size of the silicon chips is detected by not encapsulating particles smaller than silicon microchip size, such as dust or broken chips (Fig. 6(b)).

For fin fabrication options, chip orientation and rotation could be big issues. Incorrectly fabricated fins can interfere with the assembly path during rail guiding or mess up the arrangements, thus we should not detect flipped or improperly rotated silicon chips. We assume that a silicon chip with right orientation and direction has flaws at each vertical side and a scar at the right bottom corner. In other words, a scar at the corner first appears

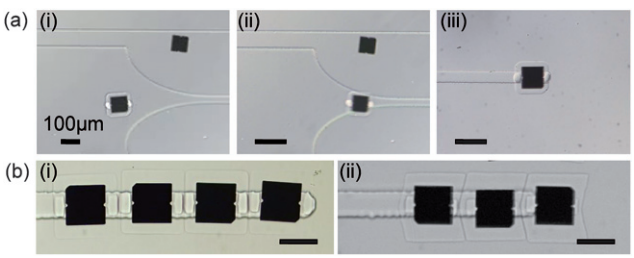

Fig. 5 Rail-guiding and assembly of silicon microchips. (a) Rail-guiding and assembly of silicon microchip. (a)(i)–(ii) Sequential images of rail-guiding; silicon microchip approaches and moves along the guiding rail. (a)(iii) Guided silicon chip is stopped at the end of the rail. (b) One-dimensional self-assembly of silicon microchips with equidistance. (b)(i) With normal rectangular encapsulants. (b)(ii) With shape-fitting encapsulants for well-aligned assembly.

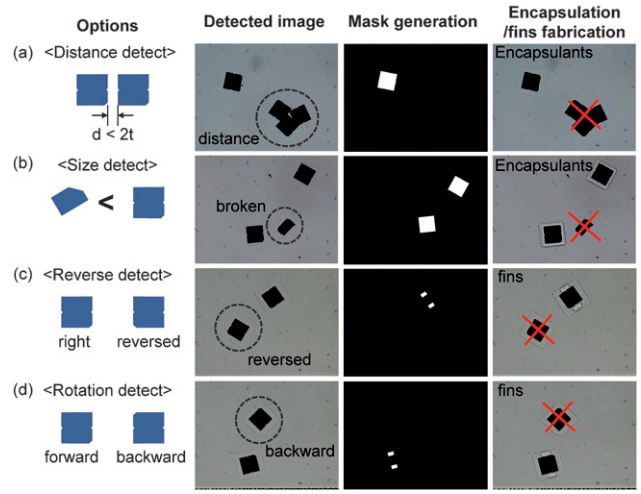

Fig. 6 Optimized detecting schemes for image processing. First column: various detecting options. Second column: detected image from CCD. Third column: actual DMD mask image generated *via* image processing after applied optimized detecting schemes. Final column: encapsulation or fin fabricated image. (a) Distance detection; if the distance between two or more silicon chips is smaller than two times the coating thickness, we do not generate a mask image for those silicon microchips. (b) Size detection; if chip size is smaller than the 100 μm × 100 μm silicon microchip size, broken silicon chips or else, we do not generate a mask image for it. (c) Reverse detection; assume right and forward direction is with flaws at the centre of each vertical side and a scar at the right bottom corner of the chip, reversed silicon microchip shows a scar at the left bottom corner. If the microchip is reversed, we do not generate a mask image for it. (d) Rotation detection; if the microchip is backward with a scar at the left top corner, we do not generate a mask image for it.

in a counterclockwise direction from the one of two flaws. If a scar exists at the left top corner of the chip, a scar at the corner in a clockwise direction from the flaws, it means that silicon chips are reversed, thus we do not fabricate fins in this case (Fig. 6(c)). For rotation detection, we assumed that a scar at the right bottom corner of the chip indicates a forward moving direction. Thus, a silicon chip with a scar at the left top corner is not detected. These detecting schemes allow silicon microchips to be assembled with the same orientation and direction for better alignment.

Since a conventional photolithography technique uses a fixed physical mask to encapsulate arranged microchips on a substrate, a misaligned individual chip could be disregarded during the encapsulation process. However, IP-OFML detects orientation and rotation of an individual chip as shown in Fig. 6, thus the encapsulation yield is increased compared to other techniques.

Conclusion

We have demonstrated an image processing based optofluidic maskless lithography technique that can detect silicon chips in a fluidic channel, encapsulate them, fabricate fins, guide and assemble at the end of the rails. The unique combination of optofluidic maskless lithography and image processing allows us to detect the orientation and rotation of silicon chips and appropriately encapsulate them and fabricate fins. This maskless lithography technique can reduce an extra alignment step with *in situ* encapsulation of microdevices by detecting individual chip rotation and orientation. The technique would be a versatile platform to manipulate microscale silicon devices and fluidically self-assemble to form large-scale systems. We envision that such a technique can find a wide variety of applications in encoded-particle-based biosensors and self-assembled display panels.

Experimental

Silicon microchip fabrication

Silicon microchips have 100 μm × 100 μm dimensions with 20 μm thickness. To fabricate these microchips, a 4 inch-sized SOI (Silicon On Insulator) wafer with a 20 μm-thick device layer was cleaned with 4 : 1 (vol/vol) H_2SO_4/H_2O_2 solution for 360 seconds. Cleaned SOI wafer was spin-coated with HMDS for 7 seconds at 2500 rpm velocity to enhance the adhesion of AZ1512 photoresist. After HMDS coating, AZ1512 positive photoresist was spin-coated for 40 seconds at 4000 rpm velocity. It was then baked for 90 seconds at 95 °C on a hotplate (soft bake). After 20 seconds of UV exposure through a film photomask of 25 000 dpi resolution, the wafer was baked for 60 seconds at 110 °C on a hotplate (post exposure bake). In addition, 3 minutes develop in AZ300MIF developer is processed, and then baked for 10 minutes at 110 °C on a hotplate (hard bake). We used this patterned AZ1512 on a SOI wafer as an etch mask for deep reactive ion etch (Deep Si Etcher, Plasma Therm) through the device layer down to the buried oxide (20 μm). We then removed the remnant photoresist with Asher (Plasma Finish) for 600 seconds. After final cleaning with 4 : 1 (vol/vol) H_2SO_4/H_2O_2 solution for 5 minutes, we released silicon microchips by immersing the wafer in a 49% hydrofluoric acid for 3 hours. By filtering released microchips with filter paper and cleaning with deionized (D.I.) water, we collected 100 μm × 100 μm sized silicon microchips in D.I. water. For the experiments, silicon chips were dispersed in poly(ethylene glycol) diacrylate (PEG-DA, Sigma-Aldrich, $M_n = 258$) with 5 wt% of photoinitiator (2,2-dimethoxy-2-phenylacetophenone).

Railed microfluidic device fabrication

Railed microfluidic channels were prepared using standard photolithography and soft lithography methods. A two-layer microfluidic channel with a groove structure was fabricated using a two-layer mold fabrication process by repeating photolithography twice in the mold preparation phase. For the photolithography process, SU-8 2015 photoresist (Microchem) was first spin-coated on a silicon wafer at 1000 rpm velocity for 30 seconds (approximately 40 μm of SU-8 photoresist thickness). It was then baked for 5 minutes at 95 °C on a hotplate. Second, the channel layer was patterned through a film photomask (designed by AUTOCAD) of 25 000 dpi resolution and baked for 6 minutes at 95 °C on a hotplate. The patterned wafer was then developed for 10 minutes in SU-8 developer. Third, additional SU-8 photoresist was spin-coated on the top of the channel layer, and then the rail-layer was patterned. Finally, hard bake of the patterned wafer was performed for 10 minutes at 110 °C on a hotplate, then a two-layer patterned silicon wafer mold was prepared. For the soft-lithography process, the mold was transferred to Polydimethylsiloxane (PDMS) Silicon l Elastomer (Sylgard 184, Dow

Corning) material with 10 wt% of curing agent by baking for 10 minutes on a hotplate at 150 °C. Then the replica PDMS mold was bonded onto the PDMS-coated slide glass through 20 seconds of the plasma cleaning process under 500–1000 mbar vacuum condition with Plasma Cleaner PDC-32G (Harrick Plasma) to complete the railed microfluidic channel fabrication process. The channels were punched at each inlet and outlet, and connected to pipette tips with silicon tubing to a syringe pump (KD Scientific).

Materials

We used poly(ethylene glycol) diacrylate (PEG-DA, Sigma-Aldrich, $M_n = 575$) with 5 wt% of photoinitiator (2,2-dimethoxy-2-phenylacetophenone) to synthesize polymeric structures. For the experiments with fluorescent microscopy, 3 mM rhodamine B (Sigma-Aldrich) and 3 mM fluorescein (FITC, Sigma-Aldrich) in respective PEG-DA solutions were used.

Computer-vision aided optofluidic maskless lithography set-up

We used an optofluidic maskless lithography system for the photopolymerization set-up. In an optofluidic maskless lithography set-up, a high-intensity mercury-xenon lamp (200 W bulb) is used for ultraviolet photopatterning combined with a digital micromirror device (DLP Technology) to dynamically control the shape of the silicon chip package. Exposure patterns on the digital micromirror device are controlled by a computer program (LabVIEW). We manually equipped an Olympus IX71 optical microscope with the ultraviolet lamp and digital micromirror device. The Olympus IX71 has a wide-excitation blue and green filter set (11012v2, 11007v2, Chroma) for fluorescent microscopy. A ×10 microscope objective lens with a numerical aperture (NA) of 0.28 projects the computer-controlled image pattern on the MEMS spatial light modulator to the final object plane with a demagnification factor of approximately 8.9. Because the pitch of the micromirror array is 13.68 μm in the spatial light modulator plane, the pixel size in the object plane is approximately $1.54 \times 1.54\ \mu m^2$. Visual alignment for photopolymerization was observed with a CCD (charge-coupled device) camera (DP70).

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References

1 D. Suryanarayana, R. Hsiao, T. P. Gall and J. M. McCreary, *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 1991, **14**, 218–223.
2 P. A. Hammond and D. R. S. Cumming, *Microelectronic Engineering*, 2004, **73–74**, 893–897.
3 K. Young-Hwan, S. Kyeong-Sik, K. Ji-Yoon, Y. Eun-Gyeong, P. Kyeong-Kap, S. Dae-Shik and J. Byeong-Kwon, *Journal of Microelectromechanical Systems*, 2006, **15**, 1152–1158.
4 T. G. Leong, C. L. Randall, B. R. Benson, A. M. Zarafshar and D. H. Gracias, *Lab on a Chip*, 2008, **8**, 1621–1624.
5 W. Hao, Z. Xinmin, G. Chongfeng, X. Jian, W. Mingmei and S. Qiang, *Photonics Technology Letters, IEEE*, 2005, **17**, 1160–1162.
6 J.-H. Yum, S.-S. Kim and Y.-E. Sung, *Colloids and Surfaces A: Physicochemical and Engineering Aspects*, 2004, **251**, 203–207.
7 S. Akram and J. M. Wark, Micron Technology, Inc, United States, 2005.
8 S. E. Chung, W. Park, H. Park, K. Yu, N. Park and S. Kwon, *Applied Physics Letters*, 2007, **91**, 041106.
9 C. J. Morris, S. A. Stauth and B. A. Parviz, *IEEE Electron Device Letters*, 2005, **12**, 792–794.
10 E. J. Snyder, J. Chideme and G. S. W. Craig, *Japanese Journal of Applied Physics*, 2002, **41**, 4366–4369.
11 Y. Huang, X. Duan, Q. Wei and C. M. Lieber, *Science*, 2001, **291**, 630–633.
12 W. Salalha and E. Zussman, *Physics of Fluids*, 2005, **17**, 063301.
13 S. A. Stauth and B. A. Parviz, *Proceedings of the National Academy of Sciences*, 2006, **103**, 13922.
14 T. G. Leong, P. A. Lester, T. L. Koh, E. K. Call and D. H. Gracias, *Langmuir*, 2007, **23**, 8747–8751.
15 T. G. Leong, B. R. Benson, E. K. Call and D. H. Gracias, *Small*, 2008, **4**, 1605–1609.
16 D. H. Gracias, J. Tien, T. L. Breen, C. Hsu and G. M. Whitesides, *Science*, 2000, **289**, 1170–1172.
17 K. L. Scott, T. Hirano, H. Yang, H. Singh, R. T. Howe and A. M. Niknejad, *Journal of Microelectromechanical Systems*, 2004, **13**, 300–309.
18 U. Srinivasan, D. Liepmann and R. T. Howe, *Journal of Microelectromechanical Systems*, 2001, **10**, 17–24.
19 S. E. Chung, W. Park, S. Shin, S. A. Lee and S. Kwon, *Nature Materials*, 2008, **7**, 581–587.

