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Sub-10-nm Nanochannels by Self-Sealing and Self-Limiting Atomic Layer Deposition

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ABSTRACT We report on a novel fabrication method of a nanochannel ionic field effect transistor (IFET) structure with sub-10-nm dimensions. A self-sealing and self-limiting atomic layer deposition (ALD) facilitates the fabrication of lateral type nanochannels smaller than the e-beam or optical lithographic limits. Using highly conformal ALD film structures, including TiO₂, TiO₂/TiN, and Al₂O₃/Ru, we have fabricated lateral sub-10-nm nanochannels with good control over channel diameter. Nanochannels surrounded by core/shell (high- k dielectric/metal) layers give rise to all-around-gating IFETs, an important functional element in an electrofluidic-based circuit system.

KEYWORDS Nanofluidics, electrofluidics, nanochannel, atomic layer deposition

Electrofluidics, the combined research area of “electronics” and “nanofluidics”, is a promising topic for applications of the sensing and manipulation of biomolecules.^{1–9} In particular, DNA manipulation via optical, magnetic, and electric properties may offer new opportunities for a fast and low-cost DNA sequencing method.^{10–19} In pursuit of real-time solid-state DNA sequencing devices, electronic functional devices in liquid environments need to be developed, ideally utilizing the compatibility with the current complementary metal oxide semiconductor (CMOS) based fabrication technology.^{20,21} Electrical rectifying or gating functions have been demonstrated in electrofluidic devices; nanopores and nanochannels have shown diode or transistor components.^{22–26} These devices serve as good platforms to study biomolecular motion, such as DNA translocation or DNA recoiling, in which the underlying sensing or detecting mechanisms have been studied.^{10,11,13,17} However, the *active* manipulations of biomolecules in an electrical manner, such as trapping, capturing, and controlling the speed of the motion, are still ongoing subjects which have significant implications for the ultimate goal of solid-state DNA sequencing device.^{27,28}

Recently, the ionic field effect transistor (IFET) has been studied as one of the active electronic devices in a liquid environment.^{3,4,22,23} Typically, the ionic transport through nanopores or nanochannels has been manipulated by using a gate bias, analogous to the conventional metal–oxide–semiconductor FET (MOSFET). Since the nanochannel is dominantly filled by the countercharged ions which screen

the surface charges, the countercharged ions serve as majority transport carriers with unipolar transport behavior when the size of pores or channels become as small as Debye length (λ_D).^{3–5,22} When the electrolyte concentration becomes very low, the Dukhin length (l_{Du}) which depends on the amount of surface charge should be considered in ionic transport, instead of Debye length (λ_D).²⁹ By pushing and pulling the majority carrier ions with the gate bias, we can manipulate the concentration of ions, which eventually allows control of the channel conductivity. In IFET, the efficient electric manipulation of ions may give rise to the control of charge-embedded biomolecules including DNA.

Despite the development of the advanced e-beam-based lithographic technology, fabrication of devices with sub-10-nm geometry is still challenging.^{30–32} Also, in the case of nanopore or nanochannel fabrication, the precise, repeatable control of the dimensions (typically diameter) is hard to achieve at sublithographic scale. To overcome some of these limitations, focused ion or electron beams have been utilized to physically drill nanopore structures to demonstrate sublithographic dimension.^{10,33,34} In the case of the lateral type structure, a nanowire (NW) assembly followed by the selective gas-phase etching has allowed lateral nanochannel void structures whose dimension is determined by the original NW dimensions.⁴ Recently, the liquefaction of line or dot geometries has been reported to generate nanochannel void structures with improving line-edge roughness.^{35,36} Despite these successful demonstrations of sub-10-nm pore or channel geometries, these approaches have limitations in terms of the process throughput, the assembly or the delicacy for complicated structures including electrode-embedded nanopore or nanochannel structures, and dimensional repeatability. Reliable fabrication techniques for nanopores or surface-based nanochannels are critical to the demonstration and scale-up of func-

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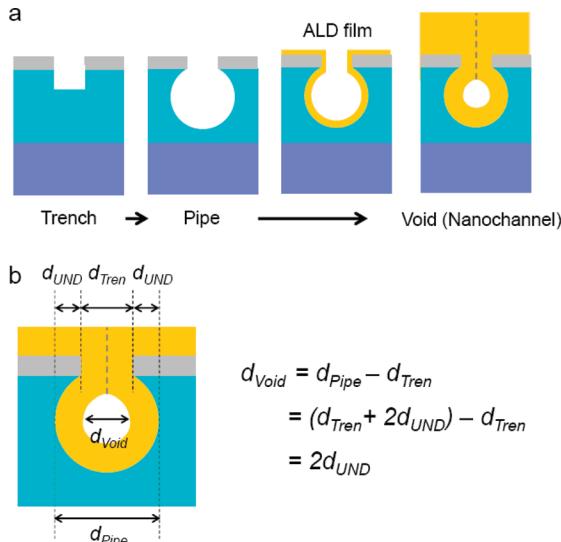


FIGURE 1. Sequence of self-sealing and self-limiting atomic layer deposition (SS-ALD) for sub-10-nm nanochannel structures. (a) The procedure of nanochannel fabrication (gray, amorphous silicon; cyan, SiO₂; blue, silicon substrate; yellow, ALD film). (b) The estimation of size determination behavior by self-limiting process.

tional nanofluidic electronic devices. The use of conventional Si processing technology for nanofluidic fabrication is desired based on the widespread availability of processing tools, coupled with the fairly deep understanding of Si-based materials and integration. One goal of this paper is to provide pathways for reliable sub-10-nm nanofluidic fabrication using generic CMOS-based processing technologies.

We have developed a novel fabrication method for nanochannel structures using an atomic layer deposition (ALD) process which is compatible with sub-10-nm dimensions. The methods depend strongly on the observed high degree of conformity of ALD films, as well as the precise control of film thickness in the <1 nm range. Figure 1a shows schematic figures of the nanochannel fabrication. The fabrication strategy starts with a thin Si layer (20 nm) deposited over a thicker silicon dioxide layer (100 nm) onto which a line structure defined by electron beam lithography (EBL) followed by the reactive ion etching (RIE) process to remove or open the Si layer. The resist material was poly(methyl methacrylate) (PMMA), and the resulting trench in the Si was typically 40–60 nm wide. Wet chemical etching of the underlying SiO₂ layer through the Si line leads to an undercut geometry, resulting in a roughly circular cross section for the trench. In this report, we used a dilute HF (1:500 DHF) to selectively etch the SiO₂ layer without altering the Si mask layer. Conformal deposition with ALD uniformly coats the inside of the circular trench (or pipe structure). Continued ALD deposition can result in a pinch-off structure at the top of the pipe, resulting in a buried, open tube. It should be noted that if a wide, padlike structure is included at the ends of the original line feature, the ends of the tube will remain open at each pad following the precise control of ALD

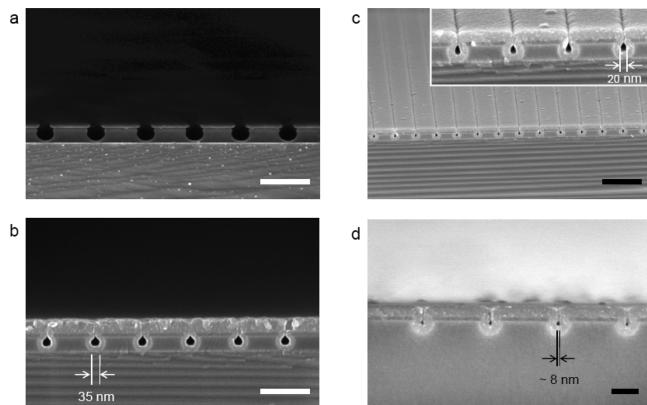


FIGURE 2. Cross-sectional scanning electron microscope (SEM) images of (a) pipe structures, (b) 35 nm void structures (10 nm wet etching) (c) 20 nm void structures (5 min wet etching), and (d) 8 nm void structures (3 min wet etching). To generate void structures, we deposited SS-ALD TiO₂ film on pipe structures in a-Si (20 nm)/SiO₂ (100 nm) on Si substrate. (Scale bars are (a, b) 250 nm, (c) 500 nm, and (d) 100 nm.)

deposition, allowing easy access for fluids to enter the nanochannel.

In the nanochannel fabrication, the ALD process has two unique advantages. First, the conformal film deposition can allow for a *self-sealing* process of nanochannels during the ALD, if the film thickness is adequate to cover the whole trench region. Second, the diameter of the nanochannel is automatically determined during the ALD regardless of the deposited ALD film thickness. Figure 1b describes the size determination process of the nanochannel, namely, the *self-limiting* process during ALD. Supposing that the ALD film is completely conformal and uniform, the dimension of the void (d_{VOID}) is expressed as

$$d_{\text{VOID}} = d_{\text{PIPE}} - d_{\text{TRENCH}} \\ = (d_{\text{TRENCH}} + 2d_{\text{UNDERCUT}}) - d_{\text{TRENCH}} \\ = 2d_{\text{UNDERCUT}}$$

where the dimensions of the pipe, the trench, and the undercut are d_{PIPE} , d_{TRENCH} , and d_{UNDERCUT} , respectively, as noted in Figure 1b. This estimation implies that the d_{VOID} is completely dependent on the d_{UNDERCUT} which is only determined by the wet-etching process, rather than by the lithography process. It is worth noting that the nanochannel dimension d_{VOID} is capable to be shrunk down beyond the lithographic limit, namely sub-10-nm, since d_{UNDERCUT} can be controlled by the wet-etching rate with usually having ~1 nm/min range controllability. Therefore, this “self-sealing and self-limiting ALD” (SS-ALD) process is ideal for a repeatable sub-10-nm nanochannel fabrication with high process reliability.

As a proof-of-concept experiment, we carried out the SS-ALD process using a TiO₂ dielectric film as described in Figure 2. Using a-Si/SiO₂ bilayer structures, we generated the pipe

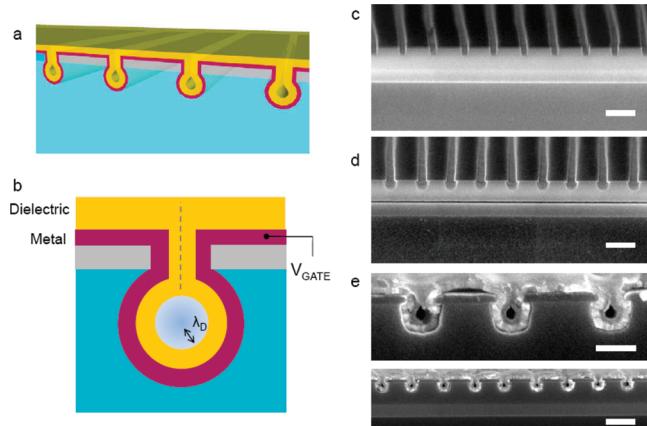


FIGURE 3. The concept of all around gating (AAG) ionic field effect transistor (IFET) (gray, amorphous silicon; cyan, SiO_2 ; yellow, ALD dielectric film; purple, ALD metal film). (a) Schematic picture of nanochannel AAG-IFET. (b) The ionic strength within the nanochannel can be controlled by electric gate bias (V_{GATE}), when the channel size becomes as small as Debye screening length (λ_D). Cross-sectional SEM images of (c) trench, (d) pipe, and (e) core/shell nanochannels. Nanochannels are surrounded by Al_2O_3 dielectric/Ru metal. (Scale bars are (c, d) 250 nm, (e) 100 nm (top), and 250 nm (bottom).)

geometry as shown in Figure 2a. For the different DHF wet-etching times such as 10, 5, and 3 min, the various undercut dimension could be controllably altered. Then, using the SS-ALD process with TiO_2 , the pipe geometries were sealed by leaving the nearly circular shaped voids with different sizes of 35, 20, and even 8 nm, as shown in panels b, c, and d of Figure 2. As a control sample, we tried a plasma-enhanced chemical vapor deposition (PECVD) process for void generation, instead of ALD (Figure S1 in Supporting Information). However, the void shapes by PECVD were not as uniform and circular as those generated by ALD, implying that highly conformal film deposition is prerequisite for the controllability. We believe that this ALD-based approach is meaningful to extend the state-of-art CMOS top-down based Si technology into the nanofluidic or electrofluidic channel fabrication.

We designed an IFET structure which uses the embedded electrode as a gate, coupled with a dielectric layer functioning as a gate dielectric. Figure 3a shows the core/shell self-sealed and self-limited nanochannels for IFET. According to our SS-ALD process, the core/shell structure was constructed by the sequential deposition of an ALD metal which does not pinch off at the top of the tube, followed by an ALD dielectric layer which does pinch off the top. This composite structure forms a cylindrical or all-around-gating (AAG) structure. From an IFET device point of view, an AAG structure is promising for very highly efficient gate-modulating behavior compared to a planar top or bottom gate device, as described in Figure 3b. A cylindrical gate structure also has some geometrical advantages over a planar structure at low electric field since the fields in the channel region can be more uniform across the channel. The high dielectric constant (k)/metal structure and the ultralow leakage property of dielectric layers such as TiO_2 or Al_2O_3 will be

beneficial for the efficient gate-capacitor coupling property.^{37,38} Additionally, in contrast to our previously reported nanopore IFET device with a relatively short-channel length (10 nm), the lateral nanochannel IFET structure is expected to be free from the FET short-channel effects, for instance, direct leakage-path generation between source and drain, one of the significant problems in FET scaling.³⁹

Panels c, d, and e of Figure 3 show the cross-sectional scanning electron microscope (SEM) images of core/shell nanochannel structures for AAG-IFET. Both trench and pipe structures were defined through e-beam lithography, RIE, and DHF wet etching processes, as shown in Figure 3c and 3d. Upon the open pipe structures, a 20 nm ALD Ru was deposited, and then a thick (40 nm) Al_2O_3 was deposited by the SS-ALD process. Figure 3e shows 20 nm sized void structures surrounded by $\text{Al}_2\text{O}_3/\text{Ru}$ (core/shell) layers. In the SEM image, the internal layers show a clear contrast difference between dark Al_2O_3 layer and bright Ru layer. The initially deposited Ru is utilized as gate electrode for IFET behavior while Al_2O_3 has a role of gate dielectric layer with a relatively high k value.

To examine the control of the self-limiting behavior, we prepared the three different trench structures which have different d_{TRENCH} , (45, 50, and 60 nm) as shown Figure 4a. Then, the DHF wet etching time was constant (5 min) for all three samples, which should result in the same undercut dimension, d_{UNDERCUT} , as shown in Figure 4b. The ALD deposition process was carried out with Ru (20 nm) and Al_2O_3 (40 nm) layer, as shown in Figure 4c. The three different structures have the same void dimension $d_{\text{VOID}} \sim 20 nm, regardless of the initial d_{TRENCH} and the ALD film thickness, consistent with the *self-limiting* process. As plotted in Figure 4d, the d_{VOID} turns out to be only determined by d_{UNDERCUT} , whereas d_{PIPE} (or d_{TRENCH}) is a function of lithographic dimension. This self-limiting behavior is promising for highly controllable nanochannel generation with sub-lithographic dimension. More importantly, this process suggests a controllable, repeatable nanoscale fabrication sequence which is independent of the initial lithographic dimensions, allowing the use of larger-scale lithography (such as optical lithography) to build <10 nm structures.$

We summarize the channel dimensions generated by the SS-ALD process for different wet etching time as Figure 4e. For any combination of ALD films such as TiO_2 , TiO_2/TiN (Figure S2 in Supporting Information), and $\text{Al}_2\text{O}_3/\text{Ru}$, the void dimensions are determined only by the wet etching time in this self-limiting process.

In order to build a functional core/shell nanochannel IFET chip, additional steps are needed. Since the self-sealed nanochannels are embedded within the substrate, a channel opening process is required to guide the fluids into the nanochannel structures. Selective opening of both ends of the embedded nanochannels by reactive ion etching allows us to build both “source” and “drain” reservoirs. In addition, in order to make three-terminal transistor structure, the metal (Ru) must be

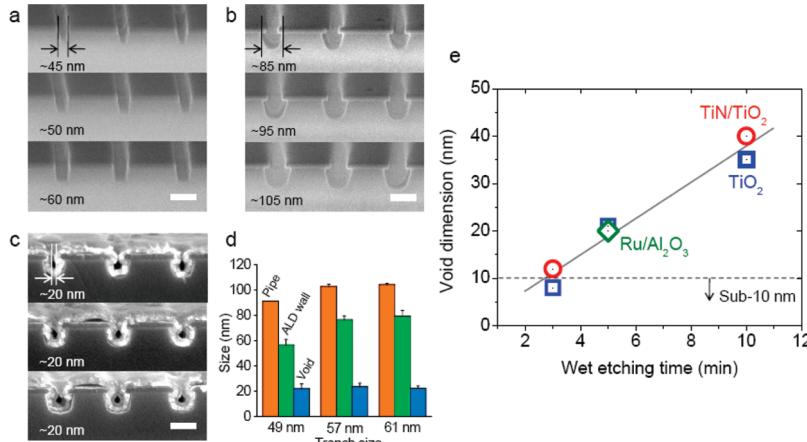


FIGURE 4. Self-limiting behavior of nanochannel fabrication. SEM images of (a) trench, (b) pipe, and (c) void structures. For three different trench sizes, the wet etching time was the same, namely, 5 min. The dimensions of the void were self-limited into 20 nm, regardless of the initial trench size. (d) The plot of dimensions for different sized trenches. (e) The void dimensions as a function of the different wet etching times for various ALD films. (All scale bars are 100 nm.)

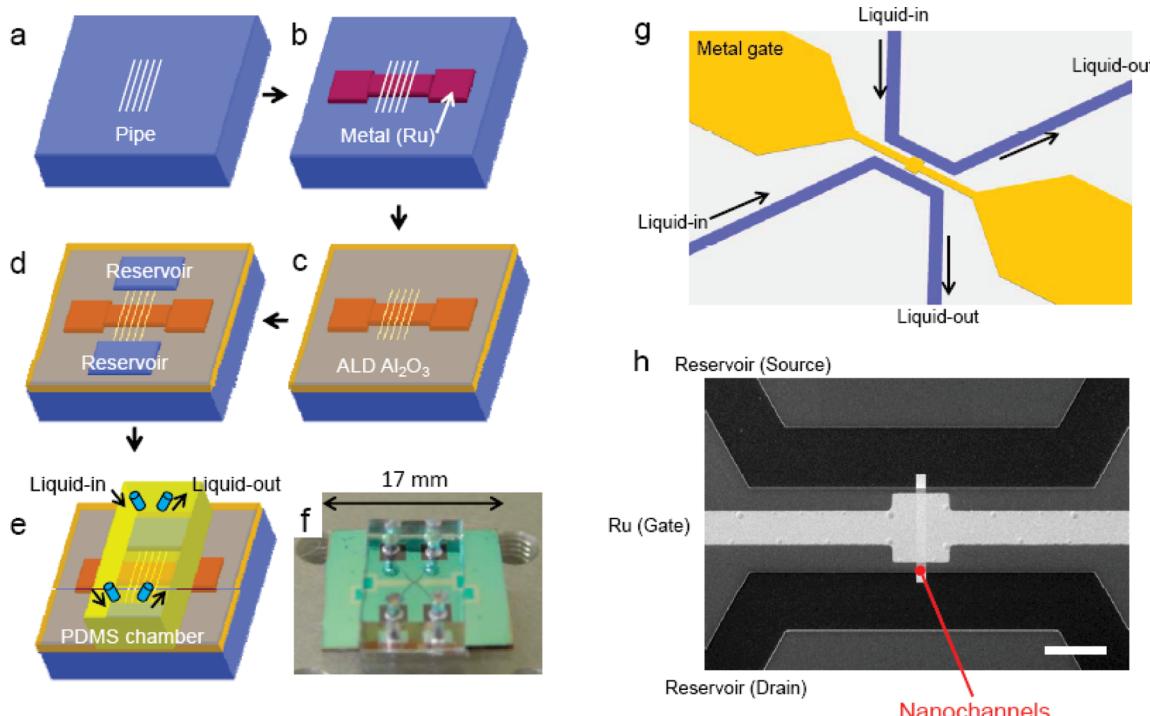


FIGURE 5. Full integration scheme of the nanochannel AAG-IFET based on the SS-ALD process. Schematic pictures of (a) pipe structure, (b) patterned ALD metal layer deposition, (c) embedded nanochannels by SS-ALD, (d) reservoirs with channel opening, and (e) assembly of PDMS microfluidic chamber. (f) Digital camera image of IFET chip after full integration. (g) Architecture of nanochannel AAG-IFET connected by a microfluidic guide channel. (h) SEM image of the core part of AAG-IFET: The nanochannel AAG-IFET is aligned with source, drain reservoirs and a gate electrode. (Scale bar is 100 μ m.)

patterned to form a gate electrode separate from the source and drain regions, and must also be electrically connected.

Figure 5 shows the process flow for the core/shell nanochannel IFET structure, where the gate patterning and the channel opening processes are included. After generating the pipe structures as Figure 5a, the Ru metal layer is deposited by an ALD process. The pipe should not be completely sealed before the gate dielectric layer is deposited. To isolate the gate from the source and drain, the Ru

metal layer is patterned by a wet-etching process as Figure 5b. The isotropic wet-etching process is essential to remove Ru layer underneath the undercut geometry. To seal the Ru-covered pipe structures, the SS-ALD process of Al_2O_3 is carried out for nanochannel generation, as Figure 5c. After the nanochannels are nominally sealed by SS-ALD, an additional SiO_2 layer is deposited by chemical vapor deposition (PECVD) in order to completely seal the seam above the nanochannels. Then, the channel opening by RIE forms

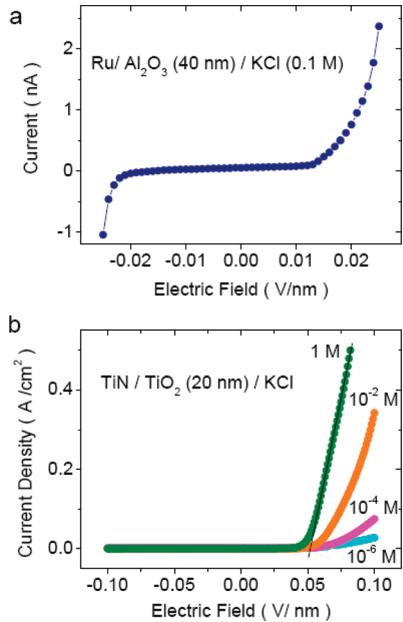


FIGURE 6. Current (I)–voltage (V) characteristics of metal–insulator–liquid (MIL) junctions. (a) Ru/Al₂O₃ (40 nm thickness) in KCl electrolyte and (b) TiN/TiO₂ (20 nm thickness) in KCl electrolyte. The metal layer was connected to the ground while a bias was applied in the KCl electrolyte. In both devices, we could identify asymmetric behavior in terms of bias polarity.

source and drain reservoirs as Figure 5d. The final step is the assembly of a poly(dimethylsiloxane) (PDMS) chamber with the substrate as shown in Figure 5e to facilitate fluidic connections to the reservoirs. The SiO₂ on top of Al₂O₃/Ru ALD films also functions as the surface-activation layer when the PDMS fluidic chamber is glued with the substrate. All process details regarding Figure 5a–e are described in the Supporting Information (Protocol, Figures P1–P11). The PDMS assembled IFET is pictured in Figure 5f. In this IFET device, biomolecules dissolved in liquid can be supplied through either the source or drain reservoir, and panels g and h of Figure 5 show the schematic and the SEM image of the self-sealed and self-limited nanochannel AAG-IFET architecture. The nanochannels at the center of both Figure 5h are clad by the Ru gate electrode while both ends of the nanochannel are open to source and drain reservoirs.

We carried out an electric characterization of metal–insulator–liquid (MIL) junction structures which is important as a reference for operating an IFET device. Figure 6 shows I – V characteristics of both Ru/Al₂O₃ and TiN/TiO₂/ using KCl. We applied voltage bias in KCl electrolyte with the internal metal layers grounded. In terms of the bias polarity, the I – V curves have asymmetric behaviors in both MIL junctions. This asymmetry in I – V might be attributed to the liquid–solid interface where electric-double-layer (EDL)/surface-charge contact may function as an asymmetric junction, similar to a metal–semiconductor junction, metal-oxide Schottky junction, or p–n junction. This possibility is consistent with the suggestion by Jiang and Stein⁸ where the oxide in an electrolyte environment behaves as buffer layer with low dielectric strength. However,

a more rigorous investigation is still required to evaluate the asymmetric I – V behavior in the MIL junction.

In summary, we report the fabrication of nanochannel structures with sublithographic dimension through top-down based, conventional semiconductor fabrication methods. The SS-ALD fabrication process allows the nanochannels to be surrounded by dielectric/metal layers, which give rise to an AAG structure, which is one of the most efficient electric-gating structures. The nanochannel structures with sub-10-nm dimension promise to be an interesting electrofluidic platform to study the motion of single molecules, including DNA. This reliable nanochannel fabrication method at dimensions well below the lithographic limit may provide a novel means for nanofluidic or electrofluidic applications.

Methods. Electron Beam Lithography (EBL), Reactive Ion Etching (RIE), and Dilute HF (DHF) Wet Etching. In order to fabricate the nanochannels, we started with a double layer of amorphous silicon (a-Si, 20 nm)/silicon oxide (SiO₂, 100–300 nm) on p-type (100) silicon substrate. The a-Si was deposited by low-pressure chemical vapor deposition (LPCVD) and the SiO₂ was deposited by plasma-enhanced chemical vapor deposition (PECVD) with tetraethyl orthosilicate (TEOS) precursor to enhance the DHF wet etching selectivity. For the e-beam lithography (EBL) process, PMMA (Microchem, A4) was spun on the substrate with 160 nm thickness and then soft baked at 95 °C for 1 min. The 100 keV incident electron beam (JEOL JBX-6300FS) was exposed with different line doses (10–20 nC/cm). (We used a 3 nm pixel lines width with area doses from 33000 to 67000 μ C/cm².) The exposed PMMA was developed in methyl isobutyl ketone (MIBK):isopropyl alcohol (IPA) = 1:3 developer solution for 1 min. Then the PMMA patterns were baked at 95 °C for 4 min. For the pattern transfer from PMMA to the substrate, a two-step RIE (Oxford Plasmalab 80) was carried out to etch the Si into a trench structure. During the first step RIE, SF₆(35 sccm) + O₂(15 sccm) plasma was used for 15 s at 10 mTorr and 30 W rf power. During the second step RIE, CHF₃(25 sccm) + Ar(25 sccm) plasma was used for 2 min at 30 mTorr and 100W rf power. The first step RIE etches the a-Si layer and the second step RIE opens into the SiO₂ layer, during pattern transfer. An O₂ plasma is used to remove the remaining PMMA resist. To generate the undercut, pipelike structure, the sample was dipped in 1:500 DHF wet etchant for various times.

Atomic Layer Deposition (ALD). To deposit the TiO₂ conformal films, we used a home-built multichamber plasma-enhanced (PE)-ALD system designed for up to 8 in. wafers. Titanium isopropoxide, Ti(OCH(CH₃)₂)₄, was used as the precursor molecule and the substrate temperature was 120 °C. One cycle of the TiO₂ ALD process consists of precursor pulsing (1 s), vacuum (3 s), Ar purging (3 s), vacuum (3 s), O₂ plasma (rf 120 W, 7 s), and vacuum (3 s). This process provides 0.65 A/cycle deposition rate of TiO₂ film. For an ALD process of Ru and Al₂O₃, we used a shower-head type GENI-MP1000 ALD system (ASM-Genitech, Inc.). The sub-

strate temperature was 300 °C and working pressure was 3 Torr. As Ru precursor, we used bis(ethylcyclopentadienyl)-ruthenium, Ru(EtCp)₂. One cycle of Ru ALD consists of precursor pulsing (5 s), Ar purging (5 s), O₂ gas (20 sccm, 10 s), and Ar purging (5 s). In the case of Al₂O₃, we used trimethylaluminum (TMA), Al₂(CH₃)₆, as precursor. One cycle of Al₂O₃ ALD consists of precursor pulsing (1 s), Ar pulsing (5 s), H₂O pulsing (1 s), and Ar purging (5 s).

Ru Patterning Process. Starting with the pipe structures, we deposited a sequence of Al₂O₃ (5 nm), Ru (20 nm), and Al₂O₃ (5 nm). The first Al₂O₃ (5 nm) layer serves as a nucleation promoting layer of Ru. Following the Ru deposition process (which did not close the nanochannels), we carried out a photolithography process using AZ 1512 photoresist (PR) and a simple mask to expose only the ends of the nanochannels. The pattern was transferred to Al₂O₃ by dipping the sample in buffered-oxide-etchant (BOE). Then, by utilizing PR/Al₂O₃ as hard mask, Ru was wet-etched in Ru wet etchant. The PR was removed by AZ 700 removal. It should be noted that since the pipe structures have an undercut geometry, all etching and PR removal processes must be based on wet processes, which are isotropic. Dry etching processes, such as RIE or ion beam etching, would not remove the etch-target material below the undercut.

Nanochannel Opening Process. To completely seal the seam over the nanochannel, we deposited additional ALD Al₂O₃ (40 nm) and PECVD SiH₄ SiO₂ (100 nm). To open the ends of the embedded nanochannels, multilayer films (SiO₂ (100 nm)/Al₂O₃ (45 nm))/a-Si (20 nm)/SiO₂ (~100 nm)) were etched out to expose the end of the embedded nanochannel. We carried out a three-step RIE process: CHF₃ based RIE (for SiO₂ removal, CHF₃ 25 sccm + Ar 25 sccm, 30 mTorr, rf 100 W for ~15 min), SF₆ based RIE (for a-Si removal, SF₆ 35 sccm + O₂ 15 sccm, 10 mTorr, rf 30 W for ~30 s), and CHF₃ based RIE (for Al₂O₃ removal, CHF₃ 25 sccm + Ar 25 sccm, 30 mTorr, rf 100 W for ~5 min). After the three-step RIE process, an O₂ plasma (O₂ 100 sccm, 50 mTorr, rf 100 W for 10 min) was treated to clean the sample surface. However, sometimes during the three-step RIE process, the channel entrance was blocked by the redeposition of etching byproduct. To remove byproduct, SC1 treatment (NH₄OH: H₂O₂ = 1.5:1 at 60 °C) was carried out.

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Supporting Information Available. Images of PECVD and ALD processes and process details related to Figure 5. This material is available free of charge via the Internet at <http://pubs.acs.org>.

REFERENCES AND NOTES

- Craighead, H. *Nature* **2006**, *442*, 387.
- Siwy, Z.; Heins, E.; Harrell, C. C.; Kohli, P.; Martin, C. R. *J. Am. Chem. Soc.* **2004**, *126*, 10850.
- Schoch, R. B.; Han, J. Y.; Renaud, P. *Rev. Mod. Phys.* **2008**, *80*, 839.
- Karnik, R.; Fan, R.; Yue, M.; Li, D. Y.; Yang, P. D.; Majumdar, A. *Nano Lett.* **2005**, *5*, 943.
- Stein, D.; Kruithof, M.; Dekker, C. *Phys. Rev. Lett.* **2004**, *93*, No. 035901.
- Polonsky, S.; Rossnagel, S.; Stolovitzky, G. *Appl. Phys. Lett.* **2007**, *91*, 153103.
- Wu, D. P.; Steckl, A. J. *Lab Chip* **2009**, *9*, 1890.
- Jiang, Z.; Stein, D. *Langmuir* **2010**, *26*, 8161.
- DeRocher, J. P.; Mao, P.; Han, J. Y.; Rubner, M. F.; Cohen, R. E. *Macromolecules* **2010**, *43*, 2450.
- Li, J.; Stein, D.; McMullan, C.; Branton, D.; Aziz, M. J.; Golovchenko, J. A. *Nature* **2001**, *412*, 166.
- Dekker, C. *Nat. Nanotechnol.* **2007**, *2*, 209.
- Liang, X. G.; Chou, S. Y. *Nano Lett.* **2008**, *8*, 1472.
- Turner, S. W. P.; Cabodi, M.; Craighead, H. G. *Phys. Rev. Lett.* **2002**, *88*, 128103.
- Clarke, J.; Wu, H. C.; Jayasinghe, L.; Patel, A.; Reid, S.; Bayley, H. *Nat. Nanotechnol.* **2009**, *4*, 265.
- Sigalov, G.; Comer, J.; Timp, G.; Aksimentiev, A. *Nano Lett.* **2008**, *8*, 56.
- Eid, J.; Fehr, A.; Gray, J.; Luong, K.; Lyle, J.; Otto, G.; Peluso, P.; Rank, D.; Baybayan, P.; Bettman, B.; Bibillo, A.; Bjornson, K.; Chaudhuri, B.; Christians, F.; Cicero, R.; Clark, S.; Dalal, R.; Dewinter, A.; Dixon, J.; Foquet, M.; Gaertner, A.; Hardenbol, P.; Heiner, C.; Hester, K.; Holden, D.; Kearns, G.; Kong, X. X.; Kuse, R.; Lacroix, Y.; Lin, S.; Lundquist, P.; Ma, C. C.; Marks, P.; Maxham, M.; Murphy, D.; Park, I.; Pham, T.; Phillips, M.; Roy, J.; Sebra, R.; Shen, G.; Sorenson, J.; Tomaney, A.; Travers, K.; Trulson, M.; Vieceli, J.; Wegener, J.; Wu, D.; Yang, A.; Zaccarin, D.; Zhao, P.; Zhong, F.; Korlach, J.; Turner, S. *Science* **2009**, *323*, 133.
- Keyser, U. F.; Koelman, B. N.; Van Dorp, S.; Krapf, D.; Smeets, R. M. M.; Lemay, S. G.; Dekker, C. *Nat. Phys.* **2006**, *2*, 473.
- Peng, H. B.; Ling, X. S. S. *Nanotechnology* **2009**, *20*, 185101.
- Service, R. F. *Science* **2006**, *311*, 1544.
- Stern, E.; Klemic, J. F.; Routenberg, D. A.; Wyrembak, P. N.; Turner-Evans, D. B.; Hamilton, A. D.; LaVan, D. A.; Fahmy, T. M.; Reed, M. A. *Nature* **2007**, *445*, 519.
- Li, Z.; Chen, Y.; Li, X.; Kamins, T. I.; Nauka, K.; Williams, R. S. *Nano Lett.* **2004**, *4*, 245.
- Nam, S. W.; Rooks, M. J.; Kim, K. B.; Rossnagel, S. M. *Nano Lett.* **2009**, *9*, 2044.
- Fan, R.; Huh, S.; Yan, R.; Arnold, J.; Yang, P. D. *Nat. Mater.* **2008**, *7*, 303.
- Vlassiouk, I.; Siwy, Z. S. *Nano Lett.* **2007**, *7*, 552.
- Kalman, E. B.; Vlassiouk, I.; Siwy, Z. S. *Adv. Mater.* **2008**, *20*, 293.
- Cheng, L. J.; Guo, L. J. *ACS Nano* **2009**, *3*, 575.
- Levy, S. L.; Craighead, H. G. *Chem. Soc. Rev.* **2010**, *39*, 1133.
- Siwy, Z. S.; Howorka, S. *Chem. Soc. Rev.* **2010**, *39*, 1115.
- Bocquet, L.; Charlaix, E. *Chem. Soc. Rev.* **2010**, *39*, 1073.
- Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. *Science* **1996**, *272*, 85.
- Lee, H. S.; Kim, B. S.; Kim, H. M.; Wi, J. S.; Nam, S. W.; Jin, K. B.; Arai, Y.; Kim, K. B. *Adv. Mater.* **2007**, *19*, 4189.
- Yang, J. K. W.; Cord, B.; Duan, H. G.; Berggren, K. K.; Klingfus, J.; Nam, S. W.; Kim, K. B.; Rooks, M. J. *J. Vac. Sci. Technol., B* **2009**, *27*, 2622.
- Storm, A. J.; Chen, J. H.; Ling, X. S.; Zandbergen, H. W.; Dekker, C. *Nat. Mater.* **2003**, *2*, 537.
- Fischbein, M. D.; Drndic, M. *Nano Lett.* **2007**, *7*, 1329.
- Chou, S. Y.; Xia, Q. F. *Nat. Nanotechnol.* **2008**, *3*, 295.
- Xia, Q. F.; Morton, K. J.; Austin, R. H.; Chou, S. Y. *Nano Lett.* **2008**, *8*, 3830.
- Kim, S. K.; Choi, G. J.; Lee, S. Y.; Seo, M.; Lee, S. W.; Han, J. H.; Ahn, H. S.; Han, S.; Hwang, C. S. *Adv. Mater.* **2008**, *20*, 1429.
- Lee, D. J.; Yim, S. S.; Kim, K. S.; Kim, S. H.; Kim, K. B. *J. Appl. Phys.* **2010**, *107*, No. 013707.
- Taur, Y. *IBM J. Res. Dev.* **2002**, *46*, 213.