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Coaxial Metal-Oxide-Semiconductor (MOS) $Au/Ga_2O_3/GaN$ Nanowires

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ABSTRACT

Coaxial metal-oxide−semiconductor (MOS) Au−Ga_2O_3−GaN heterostructure nanowires were successfully fabricated by an in situ two-step process. The Au−Ga_2O_3 core−shell nanowires were first synthesized by the reaction of Ga powder, a mediated Au thin layer, and a SiO_2 substrate at 800 °C. Subsequently, these core−shell nanowires were nitridized in ambient ammonia to form a GaN coating layer at 600 °C. The GaN shell is a single crystal, an atomic flat interface between the oxide and semiconductor that ensures that the high quality of the MOS device is achieved. These novel 1D nitride-based MOS nanowires may have promise as building blocks to the future nitride-based vertical nanodevices.

In recent years, GaN has shown its huge potential in many applications, such as blue/ultraviolet light emission diodes, optoelectronics, and high-temperature/high-power electronic devices.[1,2] Meanwhile, being stimulated by the numerous discoveries with respect to the richness of carbon nanotube novel properties, one-dimensional nanostructures have a great potential for addressing many fundamental issues related to dimensionality and space-confined transport phenomena. Han et al. reported the synthesis of GaN nanorods through a carbon-nanotube-confined reaction.[3] Since then, many attempts on the growth of GaN nanorods have been reported, including vapor−liquid−solid (VLS) growth,[4] laser-assisted catalytic growth (LCG),[5] vapor−solid (VS) growth,[6] oxide-assisted growth (OAG),[7] and the hydride vapor-phase epitaxy (HVPE) method.[8] On the other hand, monoclinic Ga_2O_3 nanowires with a wide band gap of 4.9 eV have been fabricated by various methods, including the VLS method,[9] silica-assisted catalytic growth,[10] and the thermal evaporation method.[11] Among these approaches, the vapor−liquid−solid method has been considered as the most promising method, owing to the fact that the size of the nanowires can be precisely controlled by the metal catalyst. A variety of functional 1D nanostructures, including silicide nanowires,[12,13] metal-oxide nanowires,[14−17] and nitride-based core−shell nanowires,[18] have been successfully fabricated by various methods. However, there is still a lack of reports on the fabricatation of a one-dimensional nitride-based logic device, such as a metal-oxide−semiconductor (MOS) capacitor or MOS transistor with an atomically flat interface between the oxide and semiconductor, which is essential for a high-quality MOS device.

In this paper, we demonstrate a novel but simple synthetic method to produce the one-dimensional metal-oxide−semiconductor $Au/Ga_2O_3/GaN$ nanowires by the silica-enhanced and nitridized in situ two-step process. The Au/Ga_2O_3 core−shell nanowires were synthesized by a reaction of Ga, Au, and silica substrates via the VLS growth mechanism. Subsequently, the Au/Ga_2O_3 core−shell nanowires were nitridized under ambient ammonia to form the MOS $Au/Ga_2O_3/GaN$ nanowires at 600 °C, which is a much lower formation temperature than that in the previous reports.[19,20] High-quality $Au/Ga_2O_3/GaN$ sandwich nanowires can be produced in large quantity on a wafer-scale 6 in. Si substrate, that is, by the batch production process. These novel 1D nitride-based MOS nanowires would not only enrich a well-established bank of nanostructures but are also promising as the building blocks to the future vertical high-power and high-frequency nitride-based logic nanoelectronics.

A horizontal furnace with a three-zone controlling system was used to heat the quartz tube to 800 °C with a ramping rate of 20 °C/min. A Ga (purity 99.9999%) metal powder of 0.3 g and an amorphous SiO_2 substrate were placed into the quartz furnace tube, which was 5.8 cm in diameter and 150 cm in length. Prior to loading the Ga source and silica substrate into the furnace, an ordered monolayer of polystyrene (PS) spheres that were 488 nm in diameter were dispersed on a Si(100) substrate with a 350 nm SiO_2 capping

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layer. Subsequently, a 40 nm Au layer was deposited by the electron beam evaporation process onto the substrate with a monolayer of PS spheres. After removing the PS spheres by CH_2Cl_2 solution at 60 °C for 30 min, the honeycomb-patterned substrate was obtained. The reaction temperature of 800 °C was held for 30 min and cooled down to room temperature at a pressure of 1×10^{-2} Torr. Subsequently, the 1D MOS Au−Ga_2O_3−GaN nanowires were achieved by nitrifying the as-grown Au−Ga_2O_3 core−shell nanowires under ambient ammonia and a temperature of 600 °C for 48 h; both the hydrogen and the ammonia flows were introduced into the furnace with a flow rate of 60 sccm (denoted standard cubic centimeter per minute at standard temperature and pressure, STP) and then were cooled down to room temperature under a hydrogen environment at a pressure of 10 Torr. For microstructure analysis, the as-synthesized nanowires were dispersed by the ultrasonic method in methanol solution and subsequently were transferred onto a copper grid covered by a hollow carbon film. The morphologies and crystal structures were characterized by field-emission scanning electron microscope (FESEM, JSM-6500F) and field-emission transmission electron microscope (FETEM, JEM-3000F), respectively. A field-emission transmission electron microscope equipped with an energy-dispersive spectrometer (EDS) and a Gatan GIF 2001 electron energy loss spectrometer (EELS) operated at 300 kV with a point-to-point resolution of 0.17 nm were used to characterize the crystal structures and chemical compositions. Electrical measurements were carried out by sequential procedures including electrodes defined by electron beam lithography, metal evaporation, and device evaluation. The 30 kV cold field-emission scanning electron microscope (FESEM, FEI-SIRION) with a nano pattern generation system (NPGS) was utilized for the purpose. A LabView program was used to control the $I-V$ and $C-V$ testing processes.

In present study, the PS spheres were utilized to control the density and the size distribution of the nanowires. Figure 1a shows the SEM image of the ordered PS spheres with a 40 nm Au layer. The inset of Figure 1a shows the patterned Au nanostructures after removing the PS spheres. The top view and 30° tilted SEM images of the as-synthesized sample are shown in Figure 1b and c, respectively. The nanowires were uniformly grown on a silica substrate with the length up to 10 μm. A typical low-magnification TEM image of a single nanowire is demonstrated in Figure 2a, revealing the core−shell structure of the nanowire with a distinctly smooth interface. The inset of Figure 2a shows the high-magnification TEM image at the tip region of the core−shell nanowire. A gold nanoparticle capped at the top of the core−shell nanowire can be clearly recognized, indicating that the growth mechanism follows the VLS process proposed by Wagner and Ellis.[21] In addition, the analytical TEM techniques were performed to further investigate the core−shell nanowires in the present study. The corresponding high-angle annular dark field (HAADF) image of individual Au−Ga_2O_3 core−shell nanowires marked in Figure 2a is presented in Figure 2b in order to highlight the relatively large differential

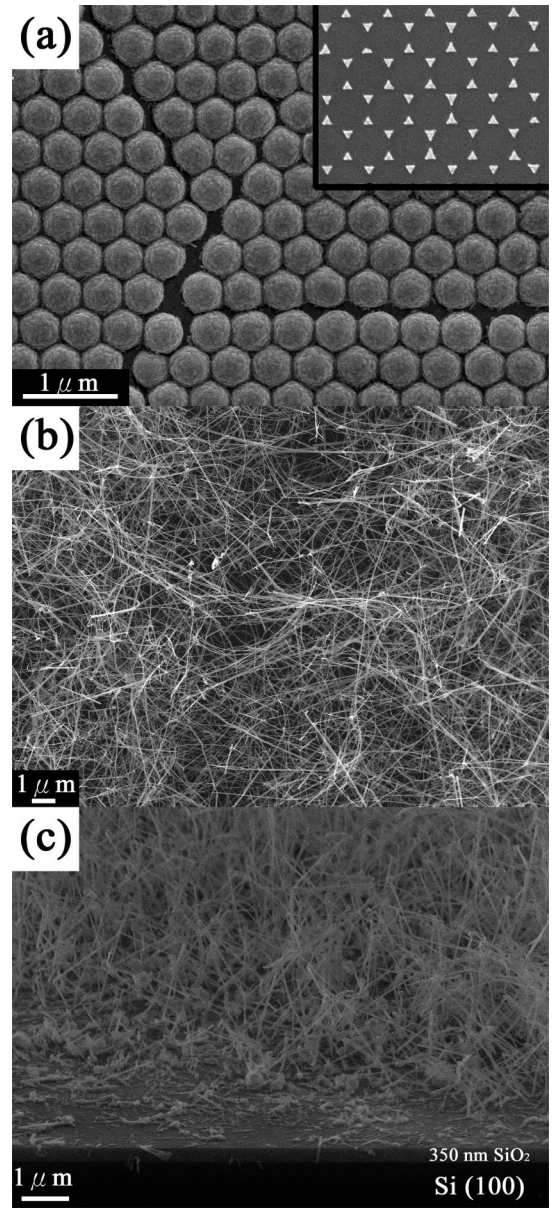

Figure 1. (a) Top-view SEM image of a monolayer of self-assembled polystyrene (PS) spheres covered with 40nm Au films. Inset shows the patterned honeycomb substrate after removing the polystyrene spheres. (b) & (c) Top-view and 30° tilted SEM images, respectively, of Au−Ga_2O_3 core−shell nanowires grown on 350nm silica substrate.

of atomic numbers between Au, Ga, and O elements. According to the composition line profile, characterized by EDS and marked in Figure 2b, the Au nanowire core is seen clearly at the center area of the nanowire. In the meantime, the high-resolution TEM image of the core−shell nanowire shown in Figure 2c reveals the single-crystalline nature and atomically smooth surface between the core and shell layers. Moreover, the fast Fourier transform (FFT) and inversed fast Fourier transform (IFFT) of the high-resolution image marked in Figure 2c is shown in Figure 2d and e, respectively. According to Figure 2d, the microstructure of the material can be identified as monoclinic β-Ga_2O_3 with a [112] zone axis, which is consistent with the previous report (JCPDS card: No. 41-1103). In addition, the measured d

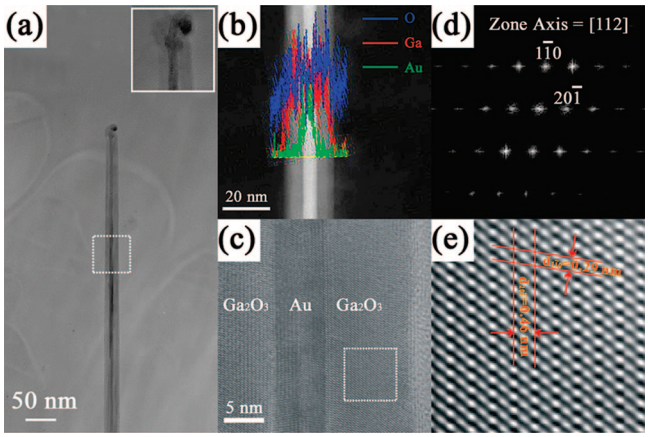

Figure 2. (a) TEM image of the individual Au−Ga_2O_3 core−shell nanowire with a gold nanoparticle capped at the tip region. (b and c) The corresponding HAADF image with a composition line profile and the high-resolution TEM image of the Au−Ga_2O_3 core−shell nanowire. (d and e) Fast Fourier transform (FFT) diffraction pattern and inverse fast Fourier transform (IFFT) image of Ga_2O_3 marked in (c).

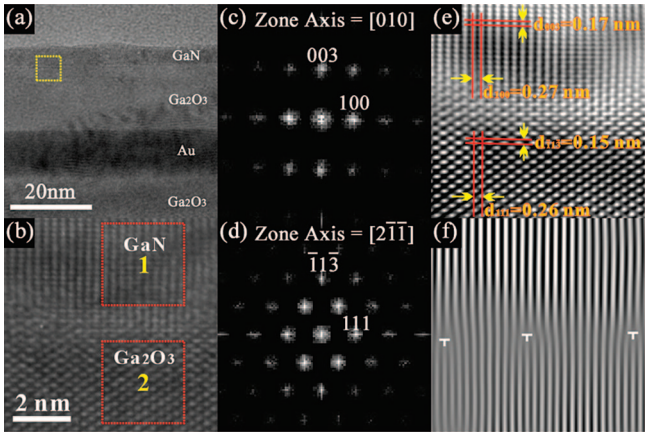

Figure 3. (a) Low-magnification TEM image of the MOS nanostructure. (b) HRTEM image of the interface between Ga_2O_3 and GaN. (c and d) FFT diffraction patterns of GaN and Ga_2O_3 marked in (b). (e and f) IFFT images of GaN and Ga_2O_3 marked in (a).

spacings of 0.46 and 0.29 nm shown in Figure 2e match well with the (2 0 $\bar{1}$) and (1 $\bar{1}$ 0) planes of β-Ga_2O_3, respectively.

The growth of Au−Ga_2O_3−GaN nanowires was achieved by the heteroepitaxy of a GaN layer on a Au−Ga_2O_3 core−shell nanowire. Normally, the concept of heteroepitaxy is based on the similar crystal structures and small lattice mismatch between the two materials. However, the heteroepitaxy between wurtzite GaN and monoclinic Ga_2O_3 is rather different. To overcome the barriers, a relatively low reduction rate of Ga_2O_3 to form GaN at the temperature of 600 °C was utilized. Here, we demonstrate the low-magnification TEM image of the high-quality 1D MOS Au−Ga_2O_3−GaN nanowire in Figure 3a. In addition, the HRTEM image of the interface between Ga_2O_3 and GaN revealed the atomically smooth interface, which is shown in Figure 3b. This approach has successfully achieved the 1D coaxial heteroepitaxy between the metal oxide and oxide−semiconductor. Moreover, the heteroepitaxial relationship between Ga_2O_3 and GaN was also investigated by HRTEM. Figure 3 panels c and d are the fast Fourier transform (FFT) of the high-resolution image marked as areas 1 and 2 in Figure 3b, respectively. In Figure 3c and d, the diffraction patterns were identified to correspond to the zone axes of the GaN[010] wurzite structure and the [101] β-Ga_2O_3 monoclinic structure. In addition, in Figures 3e and f, the corresponding inverse fast Fourier transform (IFFT) images also illustrated the atomically flat interfaces, although with some misfit dislocations present around the interface. The measured lattice mismatch between the wurzite GaN(100) and monoclinic β-Ga_2O_3(111) planes is 0.01 nm (wurzite GaN $d_{100} = 0.27$ nm; monoclinic β-Ga_2O_3 $d_{111} = 0.26$ nm). Due to the small lattice mismatch and hence reduced interfacial strain energy, the preferred heteroepitaxial orientation on the monoclinic β-Ga_2O_3(111) plane is along the axial direction of the coaxial nanowire, which is the wurzite GaN(100) plane. HRTEM analysis also identified the other preferred heteroepitaxial orientation between the wurzite GaN(003) and monoclinic β-Ga_2O_3($\bar{1}1\bar{3}$) planes (wurzite GaN $d_{003} = 0.17$ nm; β-Ga_2O_3 $d_{\bar{1}1\bar{3}} = 0.15$ nm), which is perpendicular to the axial of the coaxial nanowire, as illustrated in Figure 3e. Furthermore, the misfit dislocations caused by the lattice mismatch, were found around the interface between GaN and β-Ga_2O_3, as shown in Figure 3f. By the inverse fast Fourier transform (IFFT) technique, the inverse image was produced by the two pairs of diffraction spots in Figure 3c and d, including GaN(100), GaN($\bar{1}$00), β-Ga_2O_3(111), and β-Ga_2O_3($\bar{1}\bar{1}\bar{1}$).

The rate-limiting step for the fabrication of 1D MOS Au−Ga_2O_3−GaN nanowires is the successful synthesis of Au−Ga_2O_3 core−shell nanowires. A detailed schematic illustration of the formation procedure is illustrated in Figure 4. The formation of Ga_2O vapor was commonly proposed by using the mixtures of carbon nanotubes and Ga_2O_3 as a source.[22] However, the formation temperature of Ga_2O is considerably higher (around 1100 °C) owing to the large driving force from the reaction of carbon nanotubes and Ga_2O_3. In addition, the uneven Ga_2O vapor produced by the reaction of Ga and Ga_2O_3 powders is usually difficult to control. As a result, using the Ga metal ball instead of the mixture of Ga and Ga_2O_3 as a source was adopted in present work. The steady supply of the gallium vapor flow at lower temperature is due to the fixed surface area of the molten Ga ball. On the basis of the Au−Ga phase diagram,[23] the liquid alloy droplet of Au−Ga is easily formed at 800 °C by incorporating a small amount of Ga. Once the Ga vapors reach the silica surface, the Ga_2O vapor is produced by the reaction of Ga and SiO_2, which was already proposed in the previous literature, and it was based on the Ga−SiO_2 reaction system.[24] The possible chemical procedures are suggested by the following reactions:

$$4Ga(g) + SiO_2(s) \rightarrow 2Ga_2O(g) + Si(s) \quad (1)$$

$$3Ga_2O(g) \rightarrow Ga_2O_3(s) + 4Ga(s, 1) \quad (2)$$

Figure 4a and b shows the suggested growth models of Au−Ga_2O_3 core−shell nanowires. The Ga_2O vapor formed by the reaction of Ga with silica is continuously absorbed

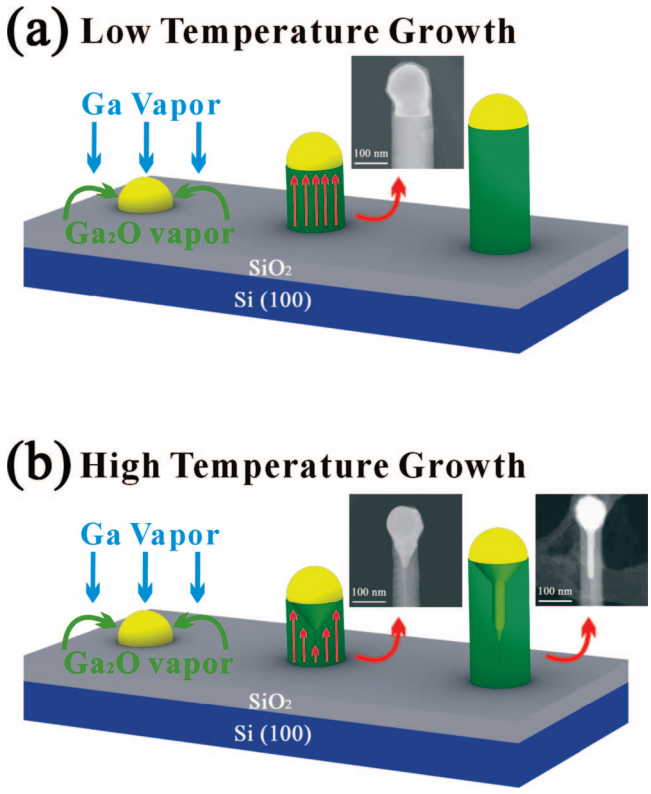

Figure 4. (a and b) The schematic illustration of the growth models for pure Ga_2O_3 and Au−Ga_2O_3 core−shell nanowires.

by the Au−Ga liquid alloy droplet, resulting in the nucleation of Ga_2O_3 at the interface between the droplets and silica substrate, owing to the supersaturation of the alloy. Subsequently, the Ga_2O_3 nanowires will continuously grow along the axis during the early stage of the growth at a temperature lower than 800 °C. A twin boundary was found at a temperature around 800 °C, shown in the inset of the Figure 4b. Subsequently, the Au−Ga nanowire was induced and grown along the twin boundary. In the meantime, Ga atoms will diffuse out from the Au−Ga nanowire to form Ga_2O_3, resulting in the formation of nearly pure Au nanowires inside of the nanowire, owing to the unlike reaction between the Au and O elements.

For electrical measurements, 1D MOS capacitors were made and characterized; Figure 5a and b shows the low- and high-magnification SEM images of a single Au−Ga_2O_3−GaN core−shell nanowire device. Moreover, the $I-V$ characteristics between the 14 and 15 and 15 and 16 electrodes demonstrated in Figure 5c and d, respectively, reveal the Ohmic behavior with corresponding resistances of 17.93 and 17.44 Gohm. In addition, the resistivity of the GaN shell layer was calculated by the following equation:

$$\rho = R \times \frac{A}{L} \tag{3}$$

where ρ is the resistivity, R is the resistance, and A and L are the cross-sectional area and length of the GaN shell layer, respectively. As a result, the obtained resistivity of the single nanowire was illustrated in the Table 1; the data are quite comparable with the early report of the GaN nanowire's resistivity from $\sim 10^7$ to $\sim 10^{-3}$ Ω cm.[25] However, the field-

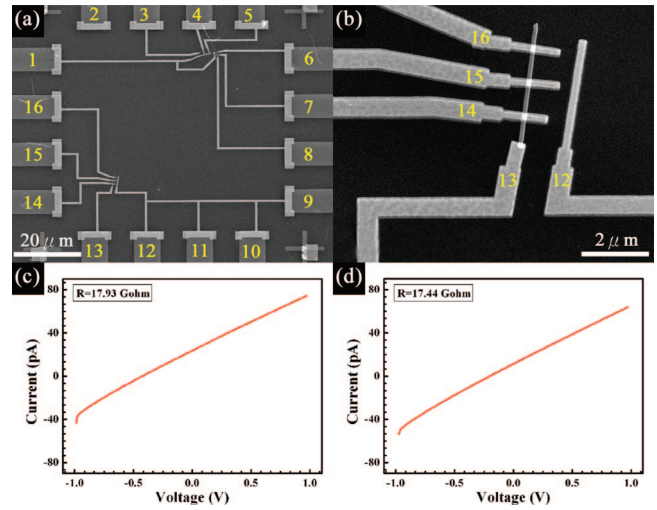

Figure 5. (a) The low- and (b) high-magnification SEM images of the single Au−Ga_2O_3−GaN core−shell nanowire device. (c and d) $I-V$ characteristics between electrodes 14 and 15 and 15 and 16.

Table 1. The Measured Electrical Results for Electrodes 14 and 15 and 15 and 16

nos.	A_{GaN} (m^2)	L (m)	R (GΩ)	ρ (Ω cm)
14−15	2.77344×10^{-15}	1.1834×10^{-6}	17.93	4.202×10^3
15−16	2.77346×10^{-15}	1.1469×10^{-6}	17.44	4.217×10^3

effect measurements of a single MOS nanowire capacitor were carried out, but the results were not yet satisfactory in the present study. It may be due to the largely too thick dielectics (Ga_2O_3) and/or the relatively high trapping centers due to the misfit dislocations and impurities around the semiconductor−oxide interface.

In summary, the coaxial metal-oxide−semiconductor (MOS) Au−Ga_2O_3−GaN heterostructural nanowires were successfully fabricated by an in situ two-step process. The Au−Ga_2O_3 core−shell nanowires were first synthesized by the reaction of Ga powder, a mediated Au thin layer, and a SiO_2 substrate at 800 °C. Subsequently, these core−shell nanowires were nitridized in ambient ammonia to form a GaN coating layer at 600 °C. An atomic flat interface between the oxide and semiconductor, which ensures the high quality of the MOS device, is achieved. The crystal structure of the GaN characterized by field-emission transmission electron microscopy indicated the single-crystalline nature. These novel 1D nitride-based MOS nanowires would not only enrich a well-established bank of nanostructure morphologies but also may have promise for the building blocks to the future nitride-based vertical high-power and high-frequency logic nanoelectronics.

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