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Abnormal temperature-dependent stability of on-plastic *a*-Si:H thin film transistors fabricated at 150 °C

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We investigated the temperature-dependent stability on the inverted-staggered back-channel-etched *a*-Si:H thin film transistors (TFTs) made at a process temperature of 150 °C on plastic foil substrates. The shift of threshold voltage (ΔV_t) increases with the stressing time and the stressing temperature. Different from TFTs made at temperatures of 300 °C or above, our low-temperature processed TFTs show an abnormal saturation of ΔV_t at 50 °C (323 K) in a constant gate-bias stress experiment. Around the same temperature, we observed abrupt increases in both the gate leakage current and the off current. Because of the low process temperature, the gate dielectric is less stable and more defective compared to that made at high process temperatures. A substantial amount of charges, trapped inside the dielectric during TFT fabrication and gate-bias stressing, was thermionically emitted into the channel by the Poole–Frenkel emission mechanism at a stressing temperature of 50 °C, leading to the abnormal phenomena. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2969789]

I. INTRODUCTION

Despite the rapid development of organic electronics and metal-oxide transistors, hydrogenated amorphous silicon thin film transistors (*a*-Si:H TFTs) are still the mainstream industrial technology for active matrix backplanes of displays. In the past decade, a lot of researches focused on developing high quality low-temperature processed *a*-Si:H TFTs fabricated on plastic substrates to achieve nonbreakable flexible electronics.[1–9] Although some experimental transparent polymer foil substrates can sustain high TFT process temperatures of 280–300 °C,[10–12] most of the *commercially available low-cost* transparent polymer foil substrates can only tolerate a process temperature of 200 °C or below. These on-plastic *a*-Si:H TFTs processed at low temperatures are less stable and more defective in comparison to conventional *a*-Si:H TFTs made at 300 °C or above.[1,10–12]

Two mechanisms cause the instability of *a*-Si:H TFTs: charge trapping in SiN_x mainly through tunneling and creation of metastable dangling bonds in the *a*-Si:H channel near the gate dielectric.[11,13–17] Although the TFT stability has been widely studied,[1,10–21] the stability of *low-temperature processed* on-plastic *a*-Si:H TFTs operated at elevated temperatures (293–333 K, 20–60 °C) has not yet been investigated.

This paper presents the effect of stressing temperature on the stability of inverted-staggered back-channel-etched *a*-Si:H TFTs made on 51 μm thick Kapton E polyimide foil substrates processed at 150 °C. The stability and *I-V* characteristics of the TFTs were studied at temperatures ranging from 20 to 60 °C. What was discovered is that the temperature dependency of the stability is different from that of *a*-Si:H TFTs made at a conventional process temperature.[18–21] An abnormal saturation of the threshold voltage shift ΔV_t at a stressing temperature of ~50 °C was observed. Based on the quantitative analyses of gate leakage current and off current, we also identified the mechanism responsible for this abnormal stressing temperature dependent stability.

II. EXPERIMENT

The *a*-Si:H TFTs were fabricated on 51 μm thick Kapton E polyimide foil substrates at 150 °C. These TFTs have inverted-staggered back-channel-etched structure with channel dimensions of $W=400$ μm and $L=40$ μm. A schematic cross section of the TFT on plastic substrate is shown in Fig. 1(a). Prior to the device fabrication, the polyimide substrate was passivated with silicon nitride (SiN_x) layers on both sides to render better TFT performances.[22] First, 100 nm Cr/Al/Cr gate metal was deposited and patterned, followed by the deposition of 350 nm SiN_x gate dielectric, a 200 nm undoped *a*-Si:H channel layer, a 50 nm n^+ *a*-Si:H source-drain layer by plasma enhanced chemical vapor deposition, and about 100 nm Cr metal by thermal evaporation. Then the source-drain electrodes and TFT islands were defined by photolithography and dry/wet etched. Last, the gate contact hole was opened by dry etching through the gate dielectric.

The TFT performances were evaluated by a HP 4155B semiconductor parameter analyzer. Transfer characteristics were studied at source-drain voltages (V_{ds}) of 1 and 10 V, and gate voltages V_{gs} from −10 to 25 V with medium integration time setting under a dark environment. Electrical gate-bias stress experiments were carried out by applying 20 V to the gate while keeping the source and the drain grounded at vari-

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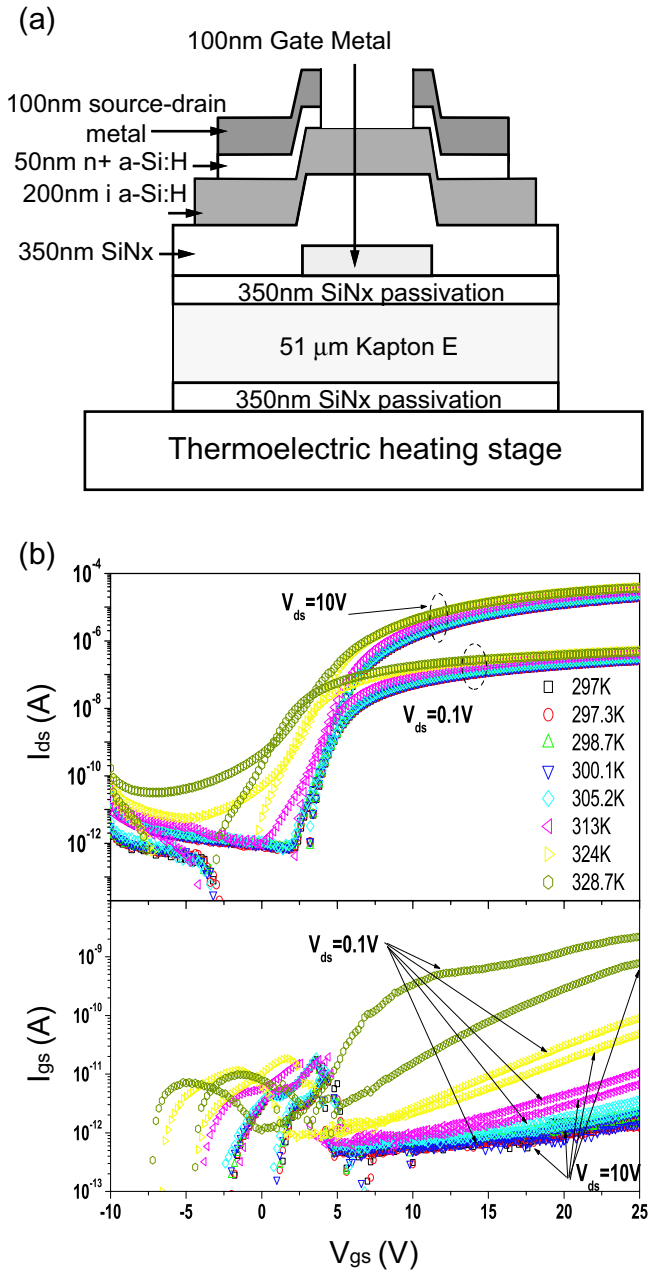

FIG. 1. (Color online) (a) Cross section of bottom-gate back-channel-etched TFT. Thermoelectric device is used to adjust the TFT operation temperature. (b) Transfer and gate leakage current curves characterized at various temperatures.

ous temperatures. The samples were heated using a thermoelectric heating stage. For each temperature, the measurements were performed after the temperature reached steady state.

III. RESULTS AND DISCUSSION

Figure 1(b) shows the TFT transfer curves and gate leakage current curves at various temperatures. With the increase in temperature, the transfer curves shift to the left and the gate leakage currents increase significantly. The rise and fall of the gate leakage current between V_{gs} of −5 and 5 V are caused by the displacement current at the onset of charge accumulation. The "mound" feature becomes significant especially for TFTs with large channel dimensions (W/L $=400/40$ μm in our case). Beyond the onset of charge accumulation, the gate leakage current increases exponentially with gate voltage, which is the typical carrier transport mechanism inside a dielectric dominated by tunneling or field emission.[23] We extract the threshold voltage V_t at I_{ds} $=10^{-8}$ A, the on current I_{on} at $V_{gs}=25$ V, and the off current at $V_{gs}=-5$ V from the transfer curves of $V_{ds}=10$ V. Figure 2 shows the threshold voltage and on-off current ratio (I_{on}/I_{off}) against the substrate temperature. Raising the temperature from 20 °C (293 K) to 55 °C (328 K), the threshold voltage drops about 4 V, which is mainly caused by the thermal excitation of carriers. The on current increases from 10 to 40 μA while the off current increases more than one order of magnitude, which leads to the decrease in I_{on}/I_{off} at high temperatures. The I_{on}/I_{off} drops dramatically from 10^7 to 10^6 at ~50 °C (323 K).

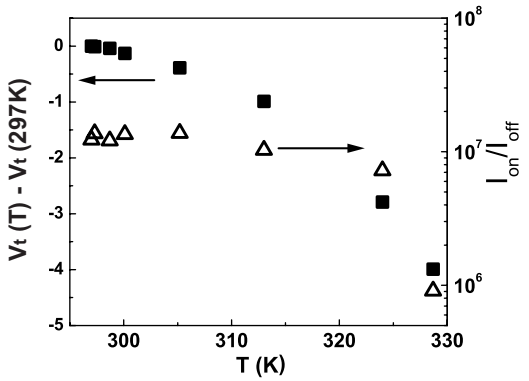

FIG. 2. (Color online) Drop of threshold voltage and on-off current ratio vs temperature.

The off current in the TFT arises from charge injection at the contacts, thermal generation in the channel, charge emission from the channel[24–26] (the off current is called "leakage current" in the cited references), and gate leakage current due to a nonideal gate dielectric. In our devices, charge injection from the contacts and charge emission from the channel are both negligible because the $n+$ source-drain contacts block the hole injection, and the TFT measurements were taken when temperatures reached steady state.[25,26] Therefore, the off current in our devices mainly results from the thermal generation and the gate leakage current. The rise in off current for more negative V_{gs} indicates the conduction of hole current,[25] with holes supplied from thermal excitation. Figure 3 shows that the gate leakage current increases with temperature. This temperature dependency of gate leakage current $I_{gs} \sim 1/T$ is the evidence for Poole–Frenkel emission of trapped charges inside SiN_x gate dielectric.[23] The dramatic increase in the gate leakage current also occurs at ~50 °C (323 K), around the same temperature that the I_{on}/I_{off} suddenly drops. Therefore, the sudden increase in the off current above 323 K is mainly caused by the gate leakage current.

The sudden rise in gate leakage current and off current at ~50 °C (323 K) is also supported by the phenomenon observed in gate-bias stress experiments performed at elevated temperatures. Figure 4 shows the threshold voltage shift ΔV_t versus stressing time for TFTs under gate-bias stressing at different temperatures. Electrical gate-bias stressing causes

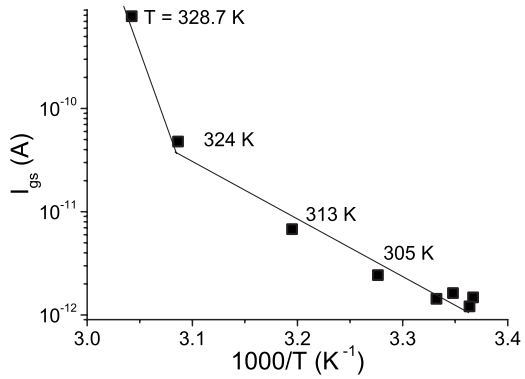

FIG. 3. Arrhenius plot of gate leakage current vs temperature.

very severe ΔV_t at high temperatures because of the faster defect creation rate inside the *a*-Si:H layers.[18–21] ΔV_t of *a*-Si TFT can be formulated as a function of temperature T, stressing time t, and stressing gate-bias voltage V_{gs},[16]

$$\Delta V_t = \pm A|V_{gs}|^{\beta} t^{\gamma} \exp(-E_a/kT), \quad (1)$$

where the sign on the right hand side corresponds to that of the polarity of gate bias, E_a is the activation energy, k is the Boltzmann constant, A is a constant, and β and γ are exponents. β depends mostly on the gate bias voltage polarity and γ depends on the device parameters and bias polarity.

With the increase in temperature in TFT gate-bias stress experiments, the exponent γ gets larger and becomes almost constant beyond 50 °C (323 K). Figure 4(a) clearly shows a saturation of ΔV_t beyond 50 °C (323 K). The Arrhenius plot of ΔV_t after 1850 s of gate-bias stressing is shown in Fig. 4(b). The activation energy dramatically drops and becomes constant for temperatures greater than 50 °C (323 K). This saturation phenomenon beyond a certain temperature is different from the results reported in the literatures,[18–21] where TFTs being studied were fabricated at temperatures of 300 °C or above. In these previous studies, no such saturation phenomenon was observed at the same temperature range (Fig. 1 in Ref. 18, Fig. 3 in Ref. 19, Fig. 3 in Ref. 20, and Fig. 11 in Ref. 21) under the gate-bias stress condition.

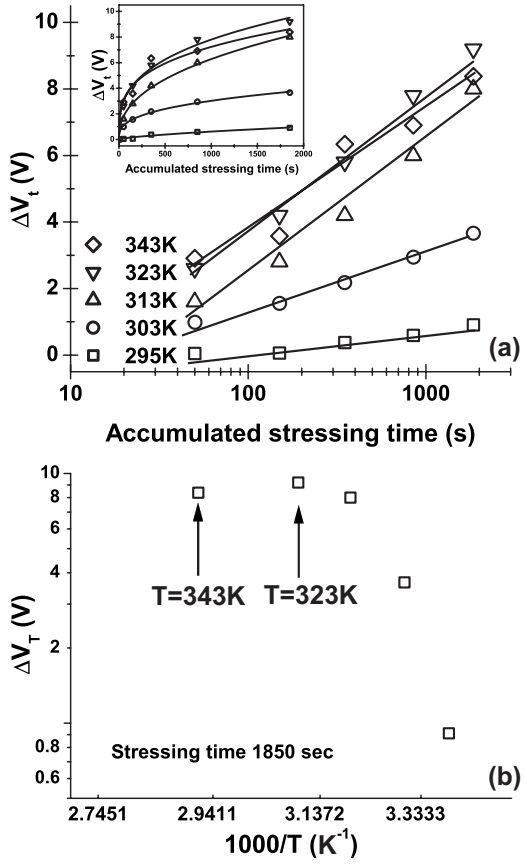

FIG. 4. (a) Shift of threshold voltage ΔV_t under electrical gate-bias stressing at various temperatures. (b) Arrhenius plot of ΔV_t after 1850 s of gate-bias stressing.

Based on the above observations, this study concludes that *a large amount* of charges, trapped inside the dielectric SiN_x during TFT fabrication and gate-bias stressing, was thermionically emitted into the channel by the Poole–Frenkel mechanism at a temperature of 50 °C (323 K). Since the charges trapped inside the gate dielectric cause ΔV_t,[11,13–17] the thermionic emission of the trapped charges leads to the saturation of ΔV_t and exponent γ. This phenomenon was observed in our low-temperature processed TFTs because the gate dielectric is less stable[1,10–12] and the trapped charges are much easier to release at relatively low temperatures. The defect level can be estimated by the product of the *Boltzmann constant* and *the saturation temperature* (kT), which is around 31 meV below the conduction band edge of SiN_x. This also implies that low-temperature processed on-plastic *a*-Si:H TFTs can be prestressed to improve the operation stability at elevated temperatures (20–60 °C).

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