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# Light-induced bias stress reversal in polyfluorene thin-film transistors

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Gate bias-stress effects in the high-performance semiconducting polymer poly-9,9′ dioctyl-fluorene-co-bithiophene (F8T2) were studied. The bias stress in F8T2 was characterized in devices having various gate dielectric materials—different types of $SiO_2$ and a polymer—and a variety of chemically modified dielectric/semiconductor interfaces. A bias-stress effect was reversed by illuminating the transistor structure with band gap radiation. The recovery rate was directly related to the absorption characteristics of F8T2. We conclude that bias stress in F8T2 is due to hole charge trapping inside the polymer, close to the dielectric interface and not to a structural change in the polymer, or to charge in the dielectric. © *2003 American Institute of Physics.*
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## I. INTRODUCTION

The performance of polymer thin-film transistors (TFTs) has improved steadily in recent years due to the development and synthesis of organic and polymeric semiconductor materials.[1] Organic TFTs are typically characterized in terms of carrier mobility ($\mu$), threshold voltage ($V_T$), and subthreshold slope, but literature data on environmental stability, reproducibility, and reliability are much more limited. In particular, the reproducibility of transfer characteristics after extended gate bias stress is poorly documented but is critical for device applications. The occurrence of bias stress is detrimental per se, as it limits the useful range of the transistor. It also generates uncertainties in the extraction of materials parameters from TFT characteristics.

A shift of the transfer curve after bias stress is well known to occur in other disordered semiconductors, such as hydrogenated amorphous silicon, and has spurred intensive research in the physics of the bias-stress effects.[2] Bias stress was also observed in polycrystalline organic semiconductors.[3–7] In pentacene-based TFTs, a threshold voltage shift of the same sign as the gate bias is observed after either positive or negative gate bias.[3] The transfer characteristics recover after several hours and illumination does not accelerate the recovery process.[3] To our knowledge, no systematic study of bias-stress effects in semiconducting polymers has been published to date. The data available in the literature are mostly limited to the observation of $V_T$ shifts of a few volts upon repetitive measurements[8–10] or hysteresis in current–voltage characteristics of two-terminal devices.[11,12] Katz *et al.* observed large $V_T$ shifts in organic TFTs with polymer dielectrics after applying gate biases of the order of 50–200 V.[13] The authors do not explain in detail the physics of this effect as the main purpose of their work is to demonstrate organic-based nonvolatile memory devices. Rep *et al.*[14] reported hysteresis in the $I-V$ characteristics of poly(3-hexylthiophene) devices fabricated on glass and were able to relate them to $Na^+$ diffusion in the polymer.

This work describes the bias-stress effects in a high-performance semiconducting polymer: poly-9,9′ dioctyl-fluorene-co-bithiophene (F8T2). In particular, we observe that the bias-stress effect was reversed by illuminating the transistor with band gap radiation. This result provides insight into the stress mechanism. Section II describes the various TFTs and the experimental measurements. Section III first characterizes the bias-stress effect, including measurements in devices having different gate dielectrics—different types of $SiO_2$ and a polymer—and a variety of chemically modified dielectric/semiconductor interfaces. Next, we describe the light-induced stress recovery and relate this to the absorption characteristics of F8T2. The results are discussed in Sec. IV.

## II. EXPERIMENTAL MEASUREMENTS

### A. Device fabrication and characterization

Transistor device geometries and illumination conditions are sketched in Fig. 1. Three types of transistor structures were made with different dielectrics and geometries to compare the stress and recovery process. The dielectrics were thermal $SiO_2$ grown on a *p* type doped Si wafer, vapor deposited parylene on a doped Si wafer, and plasma enhanced chemical vapor deposition (PECVD) $SiO_2$ on a glass wafer. The effect of the dielectric/semiconductor interface on the bias-stress effect was studied by preparing samples with a chemically modified thermal $SiO_2$ surface.

The first structure was a staggered top contact TFT in which the gate electrode was a heavily doped Si wafer with a 100 nm layer of thermally grown $SiO_2$ as the gate dielectric. The capacitance of the dielectric was $3.5\times10^{-8}$ F/cm$^2$. Chemical modification of the dielectric was accomplished by immersion in different organic trichlorosilane solutions (5–10 mM in hexadecane or heptane) to form a monolayer on the surface of the oxide.[15] The trichlorosilanes investigated were octadecyltrichlorosilane (OTS), 7-octenyltrichlorosilane (VTS), benzyltrichlorosilane (BTS), and the carboxyltrichlorosilane (CTS) obtained by oxidizing the VTS monolayer.[16] Polymer semiconductor films were spin coated from a 0.5 wt.% solution in xylene, to a thick-

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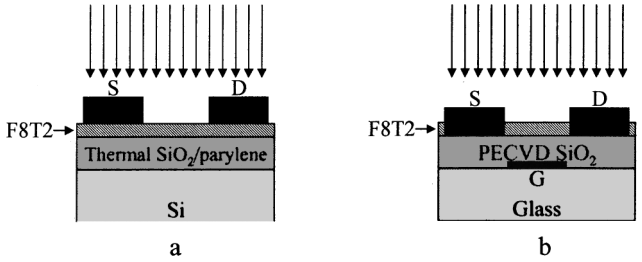


FIG. 1. Sketch of the bottom gate staggered (a) and coplanar (b) transistor structures and illumination direction.

ness that varied between 25 and 40 nm. Source and drain gold contacts were thermally evaporated through a shadow mask. The channel length of the devices varied between 40 and 200 $\mu$m.

The second type of structure was a top contact staggered TFT with an 800 nm layer of parylene as a dielectric. Its gate capacitance was much smaller ($2.5\times10^{-9}$ F/cm$^2$) because of the thickness of the dielectric.

Finally, in the third type of structure, TFTs were fabricated on $SiO_2$ (thickness 100 and 300 nm) deposited at low temperature by PECVD on glass wafers and treated with OTS. These devices had the coplanar bottom contact geometry.

TFTs are characterized by measuring their transfer and output curves. The curves are fitted using the standard field-effect transistor model to obtain values of the mobility, $\mu$, and the threshold voltage, $V_T$. The carrier mobility may be calculated in either the saturation [Eq. (1)] or the linear regime [Eq. (2)][17]

$$\mu_{\text{sat}}=\frac{2L}{WC_0}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_G}\right)^2, \tag{1}$$

$$\mu_{\text{lin}}=\frac{L}{WV_{DS}C_0}\frac{\partial I_{DS}}{\partial V_G}, \tag{2}$$

where $I_{DS}$ is the drain current, $L$ and $W$ are, respectively, the channel length and width of the TFT and $C_0$ is the areal capacitance of the gate dielectric. $V_T$ is extracted by determining the intercept at $\sqrt{I_{DS}}=0$ in the saturation regime. In an ideal device, the mobilities calculated in the linear and saturation regime are equal.

During characterization the devices were enclosed in a light-proof box at room temperature and in air. Unless otherwise specified, the gate bias sweep direction was from positive to negative voltage. Transfer curves were measured in two modes. In the continuous mode, a bias was applied to the gate electrode and progressively increased at a controlled rate (typically between 1 and 0.1 V/s). In the pulsed-gate mode, a pulse generator (Hewlett-Packard 214B) was used to produce short voltage pulses of duration 1–13 ms, on the otherwise unbiased gate electrode. The drain current was amplified (Ithaco 1211 current amplifier) and measured at the end of the pulse with a digital oscilloscope. A transfer measurement was completed with ~10–15 gate bias pulses.

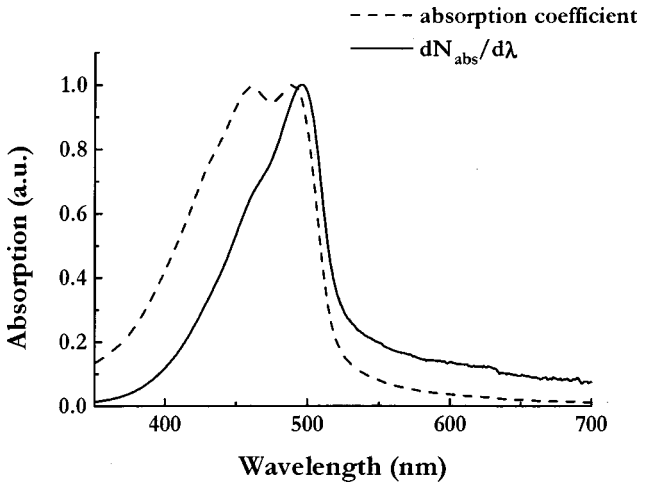


FIG. 2. Absorption spectrum and spectral dependence of the absorbed photon flux calculated according to Eq. (5).

### B. Illumination experiments and calculation of the absorbed photon flux in the films

Recovery experiments were carried out by illuminating the TFTs with a calibrated incandescent lamp (GE 764) driven by a variable power supply to control the light intensity. The devices were initially stressed by biasing the gate electrode at −20 V for 1 min. Before applying the bias, the transfer curve of the devices was measured with the pulsed-gate technique in order to extract the mobility and threshold voltage. After stressing, we verified that $V_T$ was more negative than −10 V. The device was then illuminated with light filtered through bandpass interference filters. Illumination was periodically interrupted in order to measure the drain current well into the linear regime ($V_{DS}=-1$ V and $V_G=-10$ V) for staggered devices and into the saturation regime ($V_{DS}=-15$ V, $V_G=-15$ V) for coplanar devices, in order to reduce the effect of contact resistance. All the measurements were performed with the pulsed-gate technique in order to avoid additional stressing of the TFT. At the end of each experiment, the photon flux was measured at the TFT location with a calibrated Si photodiode. During the illumination experiment the photodiode was used to verify that the light intensity was constant.

We characterized the illumination source in order to allow the accurate determination of the absorption in the film within the broadband transmitted by the interference filters. The spectral windows defined by the filters were centered at 607 nm, 557 nm, and at the absorption peak (507 nm) of the polymer, and the width of the transmitted band was 40 nm. Films of F8T2 have a strong absorption band in the visible: our measurement of the absorption is shown in Fig. 2. The absorption edge displays the characteristic exponential Urbach tail due to structural disorder in the material, as expected in an amorphous polymer, with a slope of approximately 70 meV.

The output power of the lamp is well approximated by the blackbody radiation equation

$$P(\lambda)=\frac{P_0 8\pi hc}{\lambda^5}\left(\frac{1}{e^{hc/\lambda kT}-1}\right), \tag{3}$$

where $T$ is the temperature of the blackbody and $P_0$ is a factor that takes into account the efficiency of the emitter and the distance between the source and the sample, which is fixed in our experiment. The average optical power contained in the bandwidth $\Delta\lambda$ is

$$\bar{P} = \frac{P_0 8\pi hc}{\Delta\lambda} \int_{\Delta\lambda} \frac{d\lambda}{\lambda^5 (e^{hc/\lambda kT} - 1)}. \quad (4)$$

We verified that at a driving voltage $V_L = 6$ V, the lamp spectrum was equivalent to the radiation of a 3175 K blackbody, as specified by the manufacturer. The ratio $R$ of the optical power at different lamp driving voltages to $V_L = 6$ V was measured. Numerical integration of Eq. (4) combined with the measured $R$ provided an estimate of the equivalent blackbody temperature at each driving voltage. $P_0$ was then calculated at each driving voltage. The internal consistency of this method is good as $P_0$ calculated at different driving voltages varied by less than 5%. The photon flux absorbed at a wavelength $\lambda$ through a film of thickness $t$ having an absorption coefficient $\alpha(\lambda)$ is then

$$dN_{\text{abs}}(\lambda) = P_0 \frac{8\pi}{\lambda^4} \frac{(1 - e^{-\alpha(\lambda)t})}{e^{hc/\lambda kT} - 1} d\lambda, \quad (5)$$

which integrated over a bandwidth $\Delta\lambda$ provides the total absorbed photon flux

$$N_{\text{abs}} = P_0 \frac{8\pi}{\Delta\lambda} \int_{\Delta\lambda} \frac{1 - e^{-\alpha(\lambda)t}}{\lambda^4 (e^{hc/\lambda kT} - 1)} d\lambda. \quad (6)$$

Equation (5) represents the true absorbed photon flux in the film as it takes into account both the emission from the source and the absorption spectrum of the material. The wavelength dependence of the absorbed photon flux is significantly different from the absorption spectrum of the material (Fig. 2).

## III. BIAS-STRESS MEASUREMENTS IN POLYFLUORENE TFTS

One manifestation of the bias-stress effect is a shift of the threshold voltage ($V_T$) towards negative voltage upon successive gate sweeps, as illustrated in Fig. 3(a). The data show that the transfer characteristic is nonlinear, which is also due to the stress effect as we describe below. A semilogarithmic plot of the same data in Fig. 3(b) reveals that the onset voltage ($V_{\text{on}}$) and $V_T$ both shift by the same amount, and there is essentially no change in the subthreshold slope. Therefore, we conclude that the $V_T$ shift is not due to the generation of shallow states near the valence band edge. No positive $V_T$ shift is observed after extended positive gate biasing.

Figure 4 shows a sequence of three successive transfer curves measured on the same device using the pulsed gate technique. Between the measurements, $V_G$ was biased at $-50$ V for approximately 1 min. The transfer characteristics are linear and the slope is hardly affected by the $V_T$ shift. These data confirm that bias-stress effect consists simply in *removing* mobile carriers in the channel without affecting the carrier mobility.

Figure 5 shows measurements of the TFT drain current as a function of time after the gate is turned on for fixed gate and source bias. It is evident that the drain current of the TFTs decays rapidly over time at constant $V_G$; this decay is another manifestation of $V_T$ shift. Figure 5(b) shows that the current decay is more rapid when the gate bias is larger and hence the carrier concentration in the channel is higher. This observation is in agreement with the relatively smaller stress effect measured in TFTs with low gate capacitance.

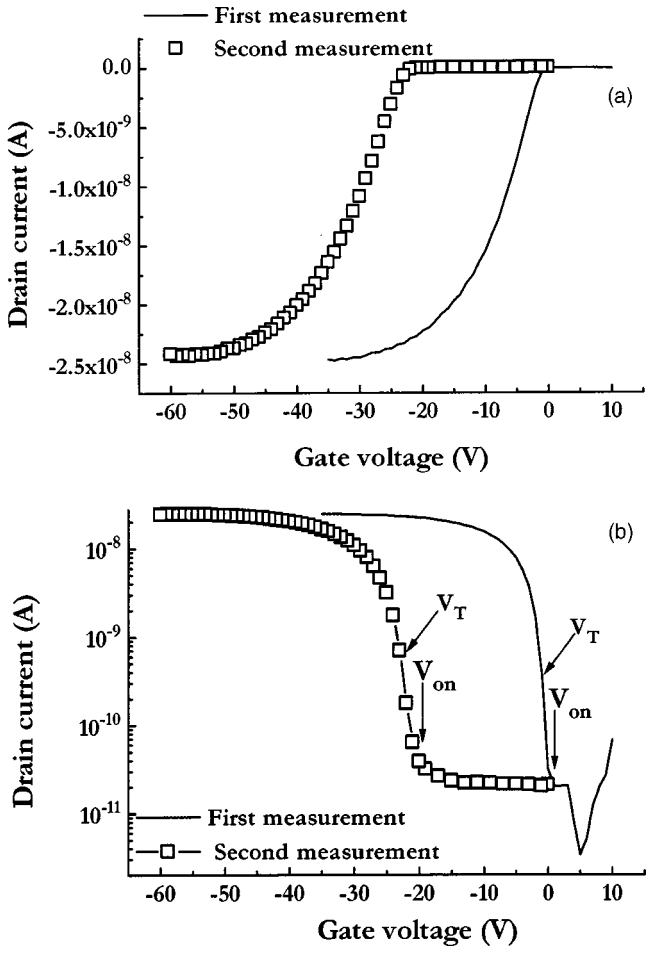


FIG. 3. Example of $V_T$ shift upon consecutive transfer curve measurements of a F8T2 TFT in linear (a) and semilogarithmic (b) scale. $V_{DS} = -10$ V.

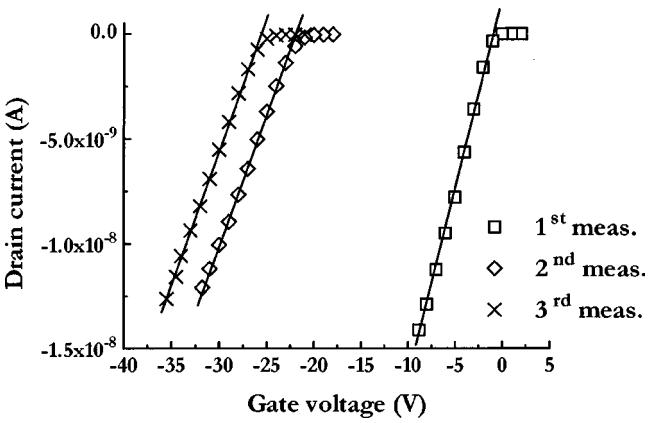


FIG. 4. Sequence of transfer curves measured at $V_{DS} = -5$ V at different bias-stress levels.

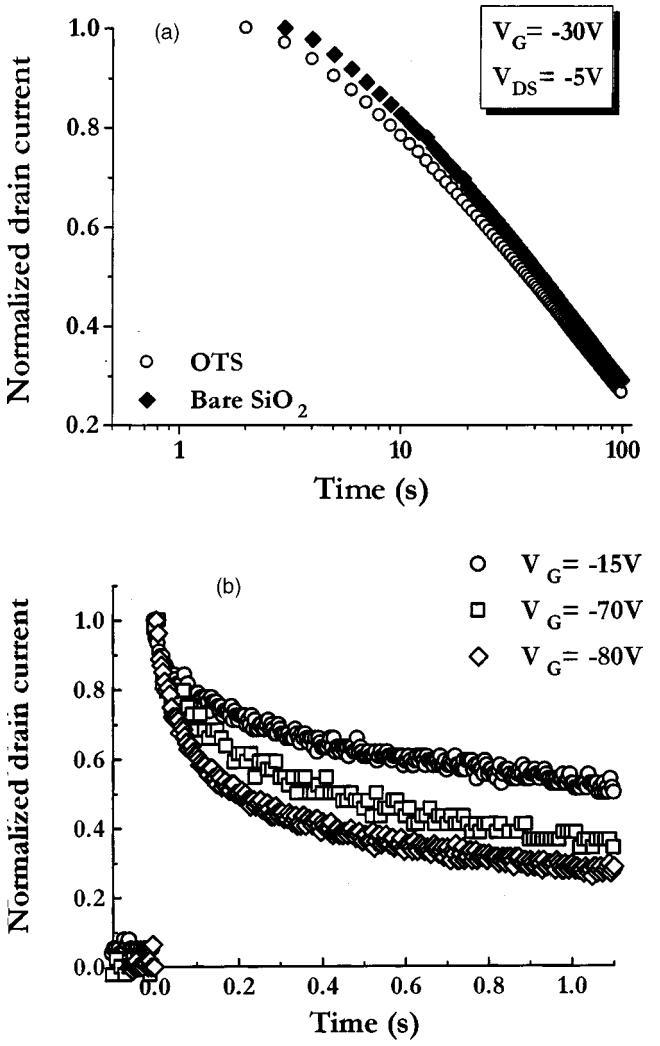


FIG. 5. Examples of long-term decay (a) and short-term decay (b) of F8T2 TFTs fabricated on treated and untreated thermal $SiO_2$. The device shown in Fig. 5(b) was treated with BTS.

The threshold voltage shift therefore occurs during gate biasing and leads to the sublinear dependence of the drain current on gate bias [Fig. 3(a)]. This shift is more apparent in Fig. 6, which compares the transfer characteristics obtained using a continuous gate bias and with a pulsed gate. Both curves start the same, but the transfer characteristic measured with the pulsed gate voltage shows no sign of nonlinearity, while the continuously biased device departs from linearity due to bias stress. The device is not stressed during the pulsed-gate transfer measurement because only a few (~10–15) gate bias pulses are needed to complete the measurement. If the number of pulses is increased, the device eventually undergoes bias stress as illustrated in Fig. 7. Between the two transfer measurements, the device was stressed with 20 $\mu$s pulses ($V_G = -20$ V) at 12 ms intervals for 30 min for a total of 150 000 pulses or 3 s of applied gate bias.

These results confirm that the bias-stress effect arises from the slow accumulation of trapped charge near the channel as a result of the prolonged application of the gate field. The trapped holes screen the gate field, which in turn causes the $V_T$ shift. Positive gate biasing does not cause a $V_T$ shift

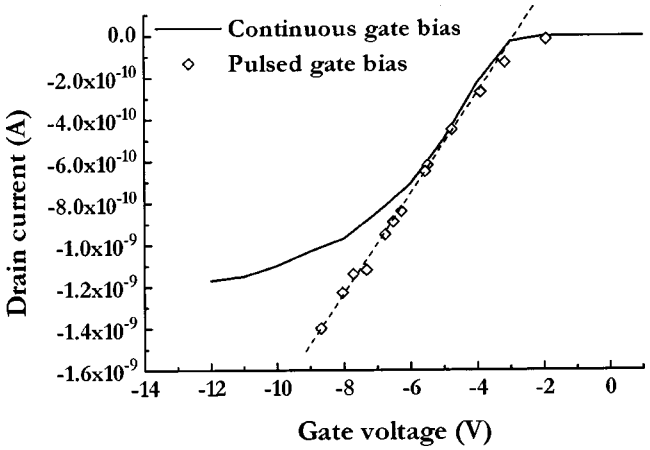


FIG. 6. Comparison of continuous and pulsed measurements for the same device fabricated on OTS-treated thermal $SiO_2$. The curves were taken at $V_{DS} = -0.5$ V.

because under these conditions no charge is accumulated in the channel (F8T2 is a hole conductor). Bias stress can equivalently be measured as a decay of the on current over time or as a $V_T$ shift after consecutive gate sweeps.

Because of bias stress, the drain current of the device decays steadily while held in the on state. Applying Eq. (2) to a device that shows sublinear behavior at high gate bias, such as the one pictured in Fig. 3(a), leads to uncertainties in the estimate of the carrier mobility. The measured mobility can vary by a significant amount depending on the sweep rate and on the dwell time at each gate bias. Figure 8 is an example of such behavior, where the mobility extracted from the same device measured at two different sweep rates varies by more than 30%. Thus, in order to accurately compare mobility values obtained from various measurements, the dwell time and sweep rate of the measurement need to be known.

The apparent carrier mobility also varies with the gate bias sweep direction. If the gate bias is swept from negative to positive voltage, the TFT is initially in its on state and is being gradually shut off by the increasing gate voltage. In

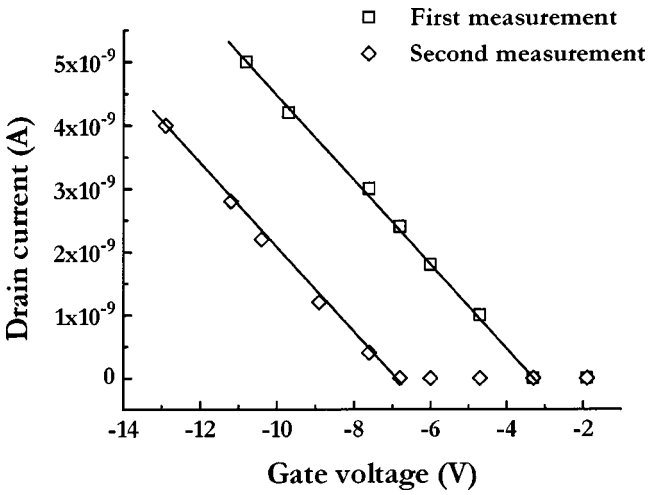


FIG. 7. Pulsed measurements of a TFT before and after stressing it with 20 $\mu$s pulses ($V_G = -20$) V) at 12 ms intervals for 30 min.

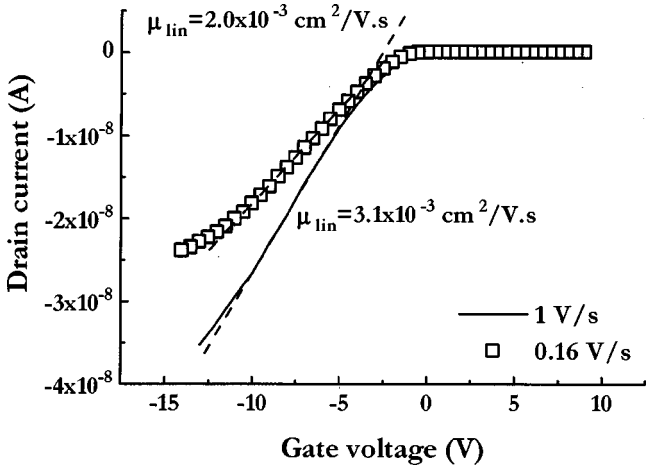


FIG. 8. Variation of apparent mobility on dwell time during the gate bias sweep. The curves were taken at $V_{DS}=-5$ V,

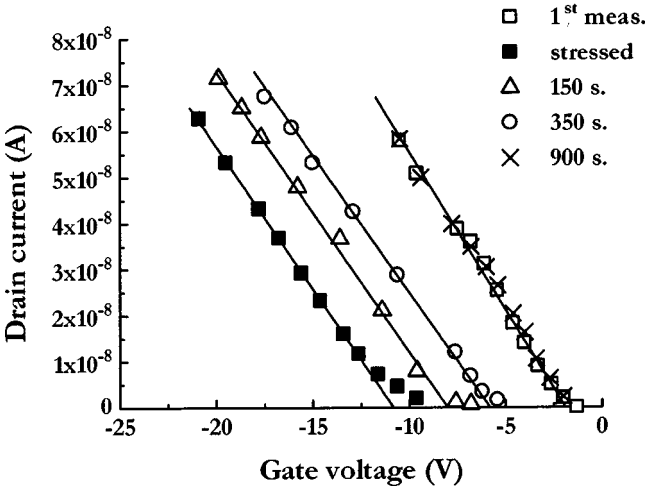


FIG. 10. Recovery of the transfer characteristics of a TFT after different illumination times. The transfer curves were taken with the pulsed gate bias technique at $V_{DS}=-5$ V.

this case, bias stress leads to an even larger current reduction than that due to the change in gate voltage. As a result, the slope of the $I_{DS}$ vs $V_G$ curve is larger, which according to Eq. (2) leads to an overestimate of the carrier mobility.

### A. Material dependence of the bias-stress effects

Measurements were made of the dependence of the bias-stress effect on device materials. Figure 9 shows the equivalent trapped charge ($=C_0\cdot|\Delta V_T|$) after a transfer measurement of devices fabricated on untreated and treated thermal $SiO_2$, on PECVD oxide, and on parylene as a function of the effective stress. Here we define as effective stress the maximum carrier concentration in the channel during the transfer measurement ($=|C_0\cdot(V_G{}^{\max}-V_T{}^0)|$), where $V_T{}^0$ is the threshold voltage of the unstressed device. $V_T{}^0$ of most of our devices was close to 0 V. The devices on thermal $SiO_2$ and parylene were biased up to $V_G=-80$ V. The effective stress in the parylene devices was much lower than that of thermal $SiO_2$ devices because of the lower insulator capacitance. The devices on PECVD $SiO_2$ were biased only to $V_G=-40$ V due to the lower breakdown voltage of the dielectric. In the group of devices with the highest effective stress the $V_T$ shift varies only within a factor of 2, while the carrier mobility (indicated in the same figure) varies over two orders of magnitude.[15] There was no correlation between mobility and $V_T$ shift. In the two remaining groups, devices on both parylene and PECVD oxide show a bias-stress effect very similar to devices on thermal oxide having undergone the same effective gate bias stress. Finally, it should be noted that the data shown in Fig. 9 demonstrate that the trapped charge, hence the $V_T$ shift correlates with the amount of charge in the channel. These data, however, cannot be used to predict the $V_T$ shift only based on $|C_0\cdot(V_G{}^{\max}-V_T{}^0)|$ as the $V_T$ shift depends also on the sweep rate during the measurement (see Fig. 8).

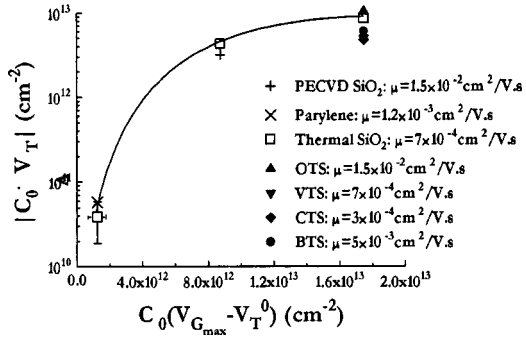


FIG. 9. Effective trapped charge ($=C_0\cdot|\Delta V_T|$) in F8T2 TFTs after a gate sweep. Threshold voltages were measured after sweeping the gate from +10 V to $V_G{}^{\max}$. All the mobility data (except for the data of devices fabricated on parylene and PECVD oxide) were previously reported in Ref. 15.

### B. Light-induced bias-stress recovery

Devices subjected to bias stress recover to their original state within a few days when left in the dark at room temperature.[18] A similar dark recovery is observed in devices fabricated on thermal $SiO_2$ treated with a variety of self-assembled monolayers (SAMs) as well as in devices with PECVD oxide and parylene as the gate dielectrics. Recovery is much faster, however, when the TFT is subjected to illumination. Figure 10 shows the result of illumination and it is seen that 10–15 min of illumination restores the device to its initial state. At the end of the recovery process, the transfer characteristic is essentially identical to that of the unstressed devices. The cycle of stress and recovery by illumination was repeated many times with no sign of a change in behavior.

Measurements were made of the rate of recovery by exposing stressed TFTs to calibrated illumination at different wavelengths and for different exposure times. Results for a staggered device on thermal oxide are shown in Fig. 11. The drain current increases linearly as a function of illumination time due to the progressive recovery of $V_T$. Stronger illumi-

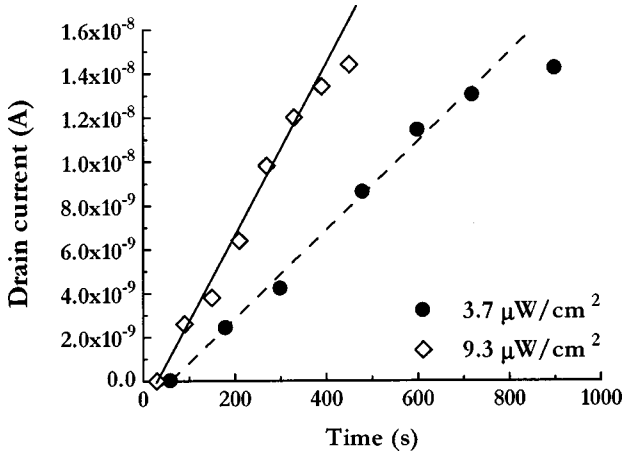


FIG. 11. Drain current recovery ($V_G=-10$ V and $V_{DS}=-1$ V) of a device fabricated on OTS-treated thermal $SiO_2$ at two illumination intensities as a function of time.

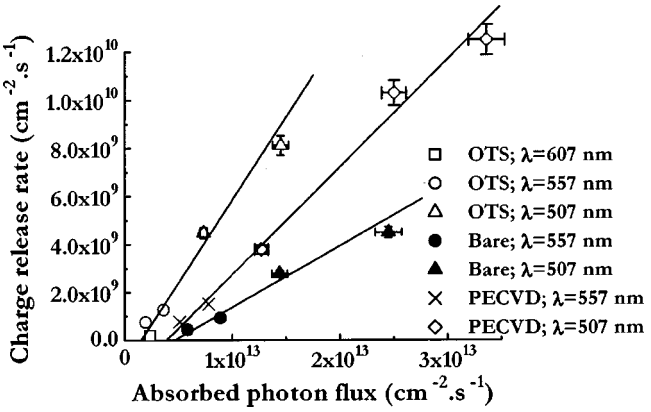


FIG. 12. Dependence of the charge release rate on absorbed photon flux.

nation results in a proportionally faster recovery rate. A departure from linearity occurs when the TFT approaches the initial unstressed state. In the sample shown, the current in the relaxed state was 14.5 nA. Since these staggered devices were operated in the linear regime, the threshold voltage as a function of illumination time $t$ can be extracted from the measurement of $I_{DS}(t)$

$$V_T(t)=V_G-\frac{I_{DS}(t)}{A\times V_{DS}}, \tag{7}$$

where $A=W\mu C_0/L$.

We showed earlier that bias stress is due to the presence of a trapped sheet of charge near the interface, and hence the recovery reflects the removal of this charge. We next measure the efficiency of the light-induced recovery by comparing the rate of release of charge to the rate of photon absorption, as calculated by Eq. (6). The threshold voltage shift $\Delta V_T$ is due to trapped charge of magnitude $C_0\cdot\Delta V_T$. In order to generate $\Delta V_T=-20$ V, approximately $6.4\times10^{-7}$ C/cm$^2$ must be trapped in the TFTs fabricated on thermal $SiO_2$, corresponding to a trapped carrier density of $4\times10^{12}$/cm$^2$. Bias-stress reversal is due to the release of these trapped charges. The charge release rate $r$ is

$$r=\frac{dQ}{dt}=C_0\frac{dV_T(t)}{dt}=\frac{L}{W\mu V_{DS}}\times\frac{dI_{DS}(t)}{dt}. \tag{8}$$

The recovery rate for staggered devices on OTS-treated and untreated thermal $SiO_2$ along with the recovery rate for a coplanar treated PECVD $SiO_2$ device (see below) are plotted in Fig. 12 as a function of the absorbed photon flux for various illumination wavelengths. In each case the recovery rate depends nearly linearly on the absorbed photon flux in the film, independent of the wavelength. The various samples exhibit slightly different slopes giving different recovery efficiencies: approximately 0.07% for the device on thermal $SiO_2$ treated with OTS, 0.023% for the device on bare thermal $SiO_2$, and 0.055% for the device on PECVD $SiO_2$. Evidently, most of the photons absorbed in the film do not participate in the recovery process.

The light-induced recovery of the coplanar PECVD $SiO_2$ TFTs is shown in Fig. 12 for different wavelengths and fluxes. Figure 13(a) shows measurements as a function of illumination time, and Fig. 13(b) shows the same data as a function of exposure. Although the recovery is qualitatively similar to Fig. 11, the details are different. Instead of a linear recovery, the charge release saturates slowly with a nearly logarithmic dependence on exposure. For the purposes of the data in Fig. 12, the recovery rate of the PECVD devices was defined as $1/\tau_{1/2}$, where $\tau_{1/2}$ is the time where half of the trapped charge is recovered.

## IV. DISCUSSION

Threshold voltage shift is commonly attributed to a built-in electric field near the dielectric/semiconductor interface caused by the presence of a sheet of charge.[17] Our measurements show that the same general mechanism applies in F8T2, since the data also clearly reveal a shift in threshold voltage without significant changes in the other TFT parameters.

### A. Location of the bias-stress induced trapped charge

There are several possible mechanisms as to why charge trapping occurs and where this charge is located, including (a) trapping in near-surface defects of the dielectric; (b) trapping in localized states at the dielectric/semiconductor interface; (c) trapping in the semiconductor; (e) ion migration in the dielectric or in the semiconductor; and (f) structural changes in the semiconductor. We find that in F8T2 TFTs bias stress occurs in broadly similar ways with gate dielectrics having very different electronic properties. The defect density of PECVD silicon oxide deposited on glass is approximately five orders of magnitude higher than that of thermal $SiO_2$, and the stress effect occurs with a polymer dielectric as well. Moreover, experiments with a variety of SAMs and in the absence of any SAM again show that a similar bias-stress effect is observed with different dielectric/semiconductor interfaces. Therefore, possibilities (a) and (b) can be ruled out as causes of bias stress.

The fast recovery with illumination indicates that the stress phenomenon is electronic in nature, thus ruling out

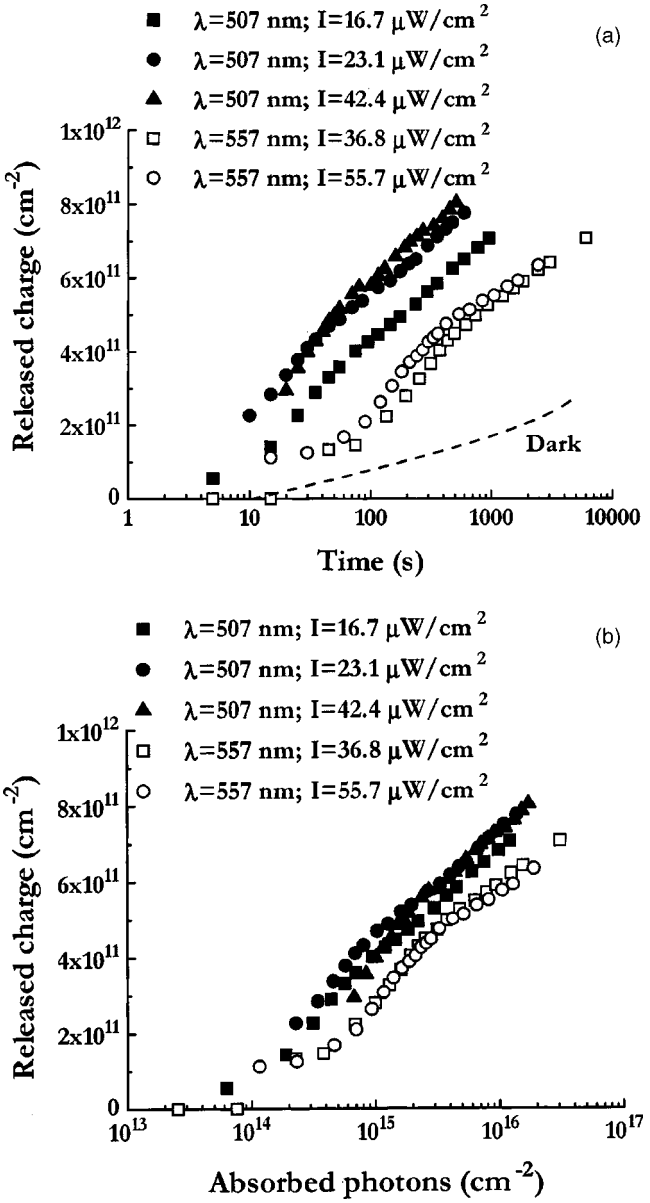


FIG. 13. Released charge in a coplanar TFT as a function time (a) and absorbed photons (b). The released charge in the dark is indicated in the figure.

possibilities (e) and (f) as causes of bias stress. In all cases, the results of the illumination experiments show that the recovery rates, as defined earlier, depend approximately linearly on the photon flux absorbed in the polymer film, independent of excitation wavelength. These results can be summarized by stating that bias stress is rather insensitive to both the dielectric and the dielectric/semiconductor interface but is directly related to the properties of the polymeric semiconductor. Furthermore, the very different bias-stress effect observed with a high-performance regio-regular polythiophene on TFT structures that are otherwise identical to those described here confirms the strong dependence of bias stress on the properties of the semiconductor polymer.[18]

This evidence, therefore, clearly suggests that the bias-stress effect is due to trapped charge located within the semiconductor polymer, near the dielectric interface. Indeed, if bias stress was due to charge trapping in the dielectric, it would depend strongly on the defect density at the dielectric surface—namely it would be minimized on thermal $SiO_2$—and it would not recover under exposure to visible radiation, as the band gap of $SiO_2$ is approximately 8.5 eV. Moreover, if charge was trapped at the interface, and was freed by photon absorption, the recovery would be slower at wavelengths absorbed by the polymer since in this case the incident photon flux at the interface would be lower.

### B. Process of light-induced recovery

Based on the above discussion we assume that light-induced recovery of the bias-stress effect results from the recombination of photoinduced carriers with deep trapped holes within the semiconductor.

Photoexcitation in the film relaxes quickly through non-radiative or radiative processes: F8T2 is strongly fluorescent. Because the illumination-induced recovery process has a low efficiency (0.02%–0.07%), only a small fraction of the photogenerated species needs to reach the channel and recombine with the trapped holes to reverse the bias-stress effect. Illumination of a polymer film with above-band gap radiation can generate strongly correlated electron-hole pairs (excitons) or uncorrelated (free) electron-hole pairs.[19,20] Although the photophysics and charge transport in F8T2 have not been studied in detail, data obtained from other conjugated polymers and polyfluorenes are available in the literature.[21–24]

Campbell *et al.*[24] studied electron and hole mobility in poly(9,9-dioctyl-fluorene) (PFO)—a polymer similar to F8T2—with time-of-flight techniques and concluded that the electron mobility in PFO is several orders of magnitude lower than the hole mobility and that electron transport is highly dispersive at room temperature: electrons are quickly trapped after photogeneration. Even under these conditions, the thickness of the illuminated F8T2 films (~25–40 nm) is such that the number of electrons photogenerated throughout the film diffusing to the channel is comparable to the number of electrons generated directly in the channel. Indeed, the diffusion coefficient of the electrons $D_e$ is related to the drift mobility $\mu_e$ by $D_e = kT/e\mu_e$, where $e$ is the elementary charge. For instance, assuming an average electron mobility of $10^{-16}$ $cm^2/V\,s$, diffusion times of few tens of microseconds are sufficient for free electrons to drift through the entire thickness of the film. If free charges are the predominant photoexcited species, low electron mobility combined with short lifetime may be responsible for the low efficiency of the recovery process.

Excitons, on the other hand, are known to be mobile in conjugated polymers.[21,22,25,26] At low exciton concentration (i.e., when photogeneration does not occur through the use of a laser source), exciton depopulation occurs through decay (radiative and nonradiative) as well as diffusion-limited annihilation.[21,27] The exciton diffusion length in conjugated polymers depends on the degree of inter-chain coupling which in turn depends on the degree of order in the polymer.[20–23] Exciton lifetimes typically vary between 0.1

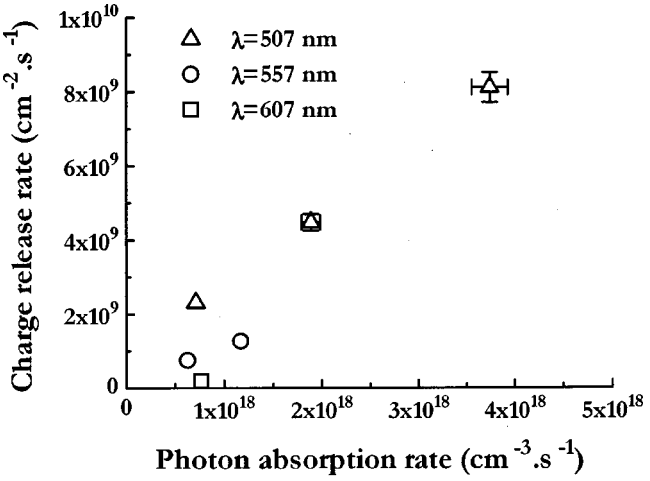


FIG. 14. Trapped charge recovery as a function of the rate of photon absorption in the channel.

and a few nanoseconds. Photophysical modeling of experimental results predicts exciton diffusion lengths in conjugated polymers on the order of 5–30 nm, if exciton diffusion and radiative as well as nonradiative decay are taken into account.[20–23] Thus, excitons generated throughout the thickness of the film are likely to contribute significantly to the recovery process by diffusing to the interface.

The recovery mechanism can occur by direct recombination of the trapped holes with free electrons or with excitons. In the latter case the result of recombination is a free hole. We do not presently have experimental evidence to discriminate in favor of either mechanism. In both cases, the concentration of photoexcited species able to diffuse from the bulk of the film to the channel is comparable to the concentration of photoexcited species generated directly in the channel.

Shorter wavelength radiation is attenuated more than longer wavelength radiation since the transmission through the film is 0.64, 0.95, and 0.98, respectively, at 507, 557, 607 nm. Correspondingly, at shorter wavelengths, the diffusion of photoexcited species from the bulk of the film is the source of a relatively larger contribution to the total concentration of photoexcited species in the channel. Figure 14 is a plot of the recovery rate as a function of photons absorbed only in the channel per unit time and volume. The channel thickness was estimated to be 1 nm.[28] In our illumination conditions, the photon absorption rate is proportional to the generation rate of photoexcited species. In Fig. 14 the charge recovery rate does not depend monotonically on the number of photons absorbed directly in the channel: at shorter wavelengths there is a deficiency of photogenerated species. Thus the data in Fig. 13 illustrate the significance of diffusion of photogenerated species throughout the whole film in the recovery process. Diffusion through the film would be even more significant if the devices were fabricated with films thicker than several absorption lengths.

The dependence of the recovery rate on the absorbed photon flux is strictly linear and independent of excitation wavelength only when the generation of photoexcited species occurs homogeneously throughout the thickness of the film and the recombination processes in the bulk are independent of the excitation wavelength. Nonuniform generation in the thickness of the film due to strong absorption, in addition to the known dependence in conjugated polymers of fluorescence efficiency on excitation wavelength,[19,27] produce the deviations from linearity observed in Fig. 12.

### C. Sample differences

In staggered devices, the recovery rate is constant (Fig. 11) and is therefore equal to the flux of photogenerated species that recombine with the trapped holes. Since only a small fraction of the photoexcited species participate in the recovery process, small variations in the absolute number of photoexcited species that recombine in the bulk away from the channel lead to large variations in the relative number of photoexcited species available to reverse the bias-stress effect. It is thus not surprising that different recovery efficiencies are observed in different films. Our data are insufficient to determine whether these variations carry implications in terms of structural order of the polymer film.

### D. Implications for devices

Because of bias stress, the effective mobility extracted from transfer data depends on the $V_G$ range over which the data fitting is carried out. In particular, bias stress is more marked when the carrier concentration in the channel $[=C_0\cdot(V_G-V_T)]$ is large and may not be noticeable at low gate bias or alternatively when the gate capacitance is small. As an illustration of this point, $V_T$ swings of only 1–2 V were observed with a gate bias $V_G<-60$ V.[8] These devices were fabricated using a polymer dielectric [poly(vinylphenol)] with a thickness varying between 300 and 1300 nm. At the same $V_G$, the charge induced in the channel in therefore smaller by a factor of 6–20 than the charge induced in our devices fabricated on thermal oxide. Similarly, other investigators[29] used 200 nm polymer dielectric layers to fabricate F8T2 TFTs and kept $|V_G|<15$ V during operation. Therefore, measurements made at small carrier concentration (i.e., low $V_G$ and/or low capacitance gate dielectric) are likely to be inadequate estimates of device performance as bias-stress effects will appear at higher carrier concentrations.

Polymer TFTs are being investigated as candidate materials for applications such as display drivers. Transistor data obtained at low carrier concentration neglect bias stress thus they cannot be reliably extrapolated to operation at higher carrier concentration. Moreover, bias stress is not limited to continuous gate biasing but occurs during pulsed gate biasing approximately representative of display operation (Fig. 7) as well. Because bias stress causes the drain current to decrease over time, it is important to design the pixel drive TFTs in such a way as to mitigate this shortcoming. In order to minimize bias stress, the carrier concentration in the channel must be kept as low as possible. On the other hand, a current on the order of 1 $\mu$A must be supplied by the TFT in order to drive the pixel. These two apparently conflicting requirements can be met simultaneously only by increasing

W/L [see Eqs. (1) and (2)]. This design approach was taken by Huitema *et al.*[30,31] and Matters *et al.*[32] in their polymer TFT circuits, where W/L is, respectively, 80 and 500. The total footprint of the transistors was kept to a reasonable size by reducing the channel length to 1–2 $\mu$m, which involves the use of photolithography. We estimate that bias stress appears in F8T2 TFTs when the carrier density is approximately $1.5\times10^{12}$ $cm^{-2}$. Assuming a mobility of 0.01 $cm^2/V\,s$, which has been demonstrated in F8T2, and $V_G = V_{DS} = -20$ V (device operating in saturation), a minimum W/L$\sim$40 is needed to output 1 $\mu$A of current and keep the device below the onset of bias stress. Therefore, we expect that the transport characteristics of F8T2 will require the use of high-resolution techniques such as photolithography to define the critical dimension of the TFT. A polymeric semiconductor material less sensitive to bias stress than F8T2 may enable low-cost processes by removing the high-resolution design constraint. Ink-jet printing of etch masks[33] and thermal imaging[34] are promising nonlithographic low-cost alternative techniques, as they have already been demonstrated in TFT arrays.

## V. CONCLUSIONS

F8T2 is a promising polymer semiconductor material for TFTs in terms of its mobility, turn-on voltage, and environmental stability. A more careful evaluation of the material shows that it suffers from deleterious bias-stress effects that lead to current reduction in the on state of the transistor and hysteresis of the TFT characteristics. Bias stress occurs when positive charge is induced in the channel by turning on the transistors. Bias stress also causes significant uncertainties in the measurement of transistor properties such as mobility and $V_T$ making it difficult to predict the behavior of TFTs in real operation. Applying only a few short bias pulses to the gate electrode allows measurements of transistor characteristics that reflect more accurately the transport properties of the semiconductor material.

Similar bias-stress effects are observed with different dielectric materials: parylene, two types of $SiO_2$ having different surface defect densities as well as in TFTs where the dielectric/semiconductor interface is modified with a variety of SAMs. Moreover, light-induced recovery correlated well with the number of absorbed photons in the polymer film. Based on this evidence, we propose that bias stress in polymer TFTs is an intrinsic property of the polymer and is due to charge trapping in the semiconductor material. A possible trapping mechanism involves the pairing of two mobile holes to form a nonconducting bipolaron.

Bias stress can severely limit the functionality and application range of polymers as semiconducting materials for TFTs. A better understanding of what causes bias stress is a necessary step towards the design of materials free of such effect.

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