Monolithic integration of plasmonic waveguides into a complimentary metal-oxide-semiconductor- and photonic-compatible platform

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Monolithic integration of plasmonic waveguides into a complimentary metal-oxide-semiconductor- and photonic-compatible platform

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A silicon-based plasmonic waveguide was designed and fabricated for use at telecommunications wavelengths. This waveguide is interfaced to the silicon photonics platform by use of a tapered silicon-on-insulator waveguide. Simulations indicate that this scheme excites the transverse magnetic plasmonic mode and that the electric fields are confined to the silicon-gold interface. Transmitted power is measured for several device lengths and the propagation distance and coupling efficiency are found to be 2.00 μm and 38.0%, respectively. These results demonstrate the potential for integration between silicon photonics and silicon plasmonic devices and demonstrate the ability to incorporate silicon-based plasmonic devices into complimentary metal-oxide-semiconductor electronic and photonic circuitry. © *2010 American Institute of Physics*. [doi:10.1063/1.3365020]

For decades, silicon has played a fundamental role in information processing devices and the development of interesting devices that exploit its unique physical properties remains an area of intensive research. In addition to being a key component in complementary metal-oxide-semiconductor (CMOS) electronics, there have been significant developments in the area of silicon photonic devices.[1] Ultimately, the minimum dimensions of silicon photonic devices are restricted by the light wave diffraction limit, which is large when compared to CMOS devices. In an effort to reduce the dimensions of photonic devices and facilitate integration with the existing CMOS technology, it is natural to consider devices that incorporate nanoscale metallic features and are designed to support plasmonic modes.[2–4] When designing the geometry and dimensions of such a waveguide, there exists a trade-off between the mode confinement and the propagation distance of the mode. Notably, the development of a silicon-based plasmonic platform allows for potential integration of existing CMOS technology with nanoplasmonic structures and devices. It is envisioned that such a platform could allow for development of processing chips composed of plasmonic waveguides that carry both electrical and optical signals simultaneously. Furthermore, significant enhancement and localization of the fields in plasmonic modes allows for ultradense integration of hybrid CMOS active plasmonic circuitry.

To date, relatively few silicon-based nanoplasmonic devices have been demonstrated. A silicon waveguide buried in a gold film[5] guides plasmonic modes, but requires side metallic coverage, making it unsuitable for planar integration with CMOS electronics. A gold-coated silicon prism wedge waveguide was shown to effectively confine optical far fields to near-fields.[6] However, more elaborate devices (e.g., 3 dB couplers, ring resonators, and Fabry–Perot cavities) cannot be implemented in this configuration and the overall size of the coupling prism makes it too large for nanoscale integration. Another key challenge to nanoplasmonic device implementation has been their efficient integration with existing photonic systems and the macroscopic world. Various schemes such as a silicon-on-insulator (SOI) photonic waveguide combined with a plasmonic taper,[5] a prism wedge structure,[6] evanescent coupling from a dielectric waveguide,[7] or end-fire coupling from a tapered SOI waveguide[8] have been shown to couple light into plasmonic waveguides. When designing a coupling scheme, it is highly desirable that both active CMOS components along with nanoplasmonic structures are accommodated in a manner that allows for simple fabrication and integration.

In this letter, we present a class of silicon-based nanoplasmonic devices that are integrated to a SOI photonic platform. The silicon-based nanoplasmonic devices consist of a SOI waveguide capped by a thin gold film on the top, allowing for high electric field confinement at the silicon-gold interface. The propagation characteristics of the devices as well as the coupling efficiencies between these two platforms are examined to demonstrate potential for integration and interfacing between SOI photonic and silicon-based plasmonic waveguides. It is important to note that this class of devices can accommodate a variety of configurations that require complex light coupling schemes necessary for the development of dense optical circuitry.

The plasmonic device under investigation consists of a 300×340 nm^2 SOI waveguide capped by a 50 nm layer of gold on the top. In order to excite a pure plasmonic mode in this structure, we end-fire couple *y*-polarized [as shown in Fig. 1(a)] light to it using a $w_1=2$ μm wide SOI waveguide that tapers linearly to a width of $w_p=300$ nm over a distance of $L_t=55$ μm. An identical taper collects the light that is transmitted by the nanoplasmonic waveguide and delivers it to a detector. The input and output SOI waveguides are aligned to input/output lensed fibers using piezocontrolled positioning stages. The nanoplasmonic waveguide and couplers are fabricated on a SOI wafer consisting of a 340 nm thick Si layer on top of a 1 μm thick SiO_2 layer. In order to create the desired waveguides, two layers of electron beam lithography (EBL) are required as follows: one to define the plasmonic features and the other to define the SOI waveguide couplers. After developing the features of the first EBL exposure, a 5 nm Cr adhesion layer is sputtered on the sample, followed by a 50 nm Au layer. A standard lift-off in

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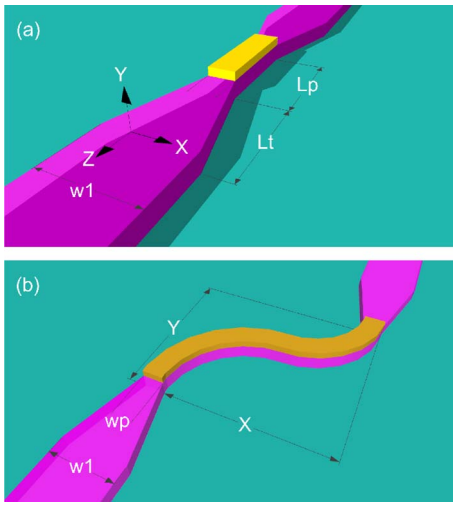

FIG. 1. (Color online) Schematic representation of (a) linear waveguide with dimensions $w_1=2$ μm, $w_p=300$ nm, $L_t=55$ μm, and $L_p=2$, 3, 4, and 5 μm, and (b) s-bend structures with dimensions $w_1=2$ μm, $w_p=400$ nm, $x=2$ μm, and $y=5.8$ μm.

acetone reveals the plasmonic features, as shown in Fig. 2(a). After defining a mask for the SOI waveguide couplers in the second EBL exposure, reactive ion etching (RIE) is used to define both the plasmonic and SOI features in the silicon, as depicted in Figs. 2(b) and 2(c). Scanning electron microscope images of fabricated straight and s-bend waveguides are shown in Fig. 3.

A fundamental concern that must be addressed is whether the proposed excitation scheme will excite the desired plasmonic mode. In order to investigate this matter, three-dimensional (3D) finite-difference time-domain (FDTD) simulations were performed on a basic SOI waveguide interfaced to a silicon-based plasmonic waveguide. Figure 4(a) is a schematic representation of the geometry used in this simulation. Here, a 300 nm$\times$340 nm$\times$3 μm SOI waveguide is excited with a y-polarized $\lambda=1550$ nm continuous-wave source. The propagating mode then excites the silicon-based plasmonic structure that consists of the same 300×340 nm^2 SOI waveguide capped by a 50 nm layer of gold. Plotting the time-averaged intensity at different cross-sections along the structure reveals the manner in which the plasmonic mode is excited and provides the propagation characteristics of the silicon-based plasmonic waveguide. The mode profile at four slices in this structure is

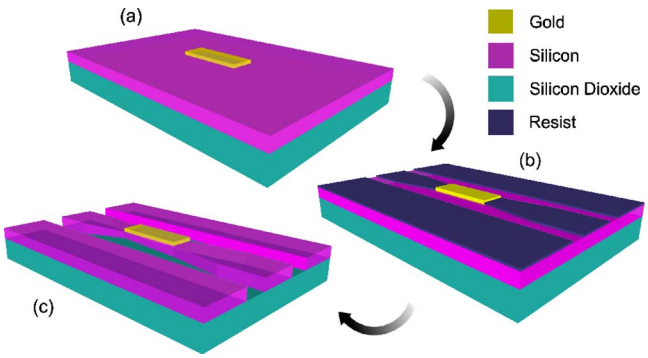

FIG. 2. (Color online) Three key steps of the fabrication process: (a) First layer of EBL followed by standard lift-off process defines plasmonic structures; (b) second layer of EBL defines mask for RIE process; and (c) final structure following RIE process.

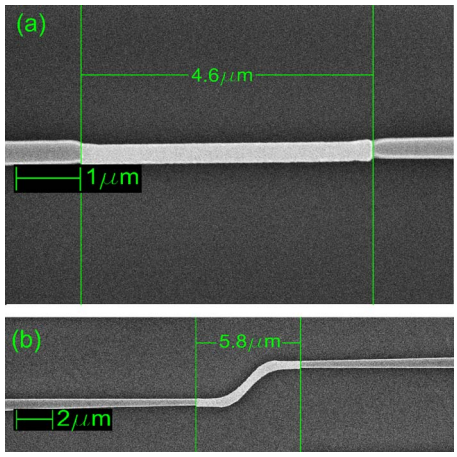

FIG. 3. (Color online) Scanning electron microscope images of typical fabricated devices: (a) Linear $w_p=300$ nm wide waveguide and (b) $w_p=400$ nm wide s-bend waveguide.

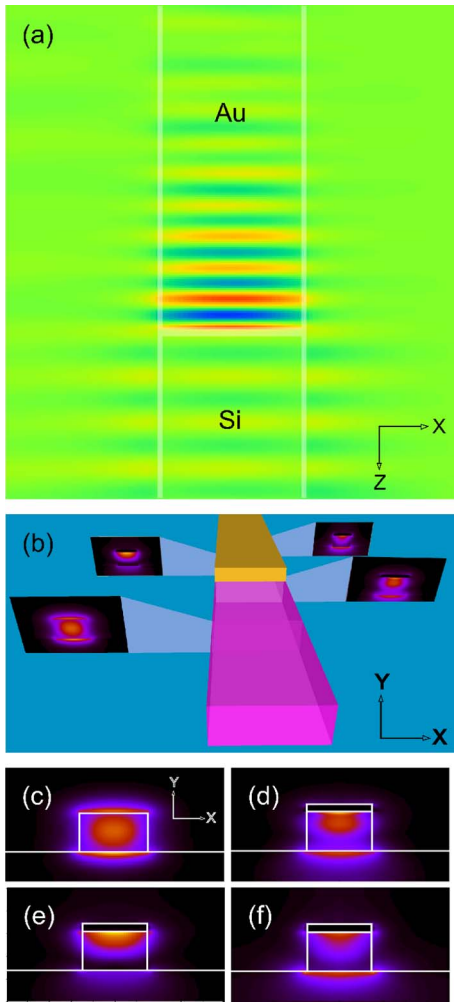

FIG. 4. (Color online) Electric field intensity distributions at various cross-sections: (a) Field distribution at silicon-gold interface, (b) schematic depiction of mode evolution in device, (c) fundamental mode in SOI waveguide, (d) interface between SOI waveguide and plasmonic waveguide, (e) mode after propagating 500 nm through plasmonic waveguide, and (f) mode after propagating 1 μm through plasmonic waveguide.

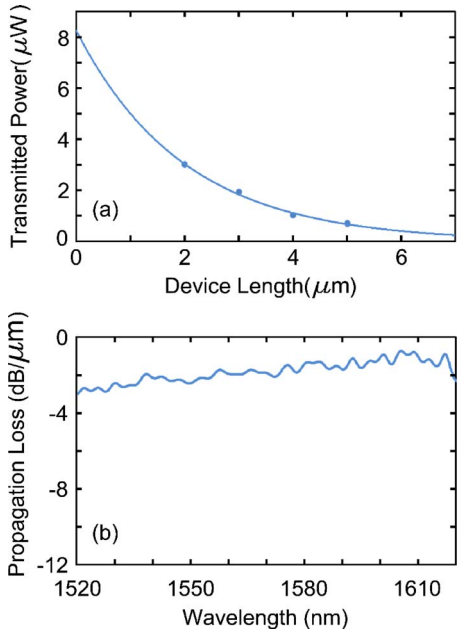

FIG. 5. (Color online) Power transmitted by 300 nm wide linear silicon-based plasmonic waveguides. (a) Power transmitted through devices with lengths ranging from 2 to 5 μm at $\lambda=1550$ nm. (b) Broadband propagation loss characteristics.

shown in Fig. 4(b) and enlarged versions are shown in Figs. 4(c)–4(e). The fundamental mode obtained after propagating 3 μm in the SOI waveguide is shown in Fig. 4(c). Multiple modes are present at the interface between the SOI waveguide and the silicon-plasmonic waveguide as shown in Fig. 4(d). However, after propagating 500 nm through the plasmonic waveguide, the mode becomes confined to the gold-silicon interface as shown in Fig. 4(e). The propagation distance of this structure was calculated to be 1.9 μm.

Four different lengths, $L_p=2$, 3, 4, and 5 μm, of silicon-based plasmonic waveguides having widths of $w_p=300$ nm were used to investigate this structure experimentally. Transmitted powers for this set of waveguides at $\lambda=1550$ nm are shown in Fig. 5(a) from which one can obtain a propagation distance of 2.00 μm (−2.17 dB/μm). This value is in a very good agreement with the predicted 1.9 μm from the FDTD calculation and the measured value of 2.5 μm for a silicon wedge waveguide.[6] As shown in Fig. 5(b), this waveguide exhibits similar propagation characteristics over a wide bandwidth (1520–1620 nm), demonstrating that this structure is not restricted to operate at a single wavelength and is suitable for monolithically integrated CMOS schemes that involve wavelength multiplexing.

The *y*-intercept (8.3 μW) of the propagation curve in Fig. 5(a) provides the overall coupling losses resulting from the input/output facets of the SOI waveguide, taper, and impedance and mode mismatches between the SOI waveguides and silicon plasmonic devices. To deduce the coupling losses due to the SOI input facet, measurements are performed on a straight 2 μm × 340 nm × 3 mm SOI reference waveguide without any Au features. The power transmitted through the reference waveguide at $\lambda=1550$ nm was found to be 56.5 μW. The coupling efficiency between the SOI platform and the silicon-based plasmonic platform is deduced to be 38.0% per interface. The overlay alignment procedure required for the second layer of EBL limits the alignment between the silicon taper and the plasmonic waveguide to a few tens of nanometers and close examination of Fig. 3(a) reveals that a misalignment of 35 nm is present. In the ideal case of perfect alignment, there would be a higher overlap between the excitation mode from the photonic taper and the plasmonic mode, and the coupling efficiency would be higher.

Along with the ability to guide a desired mode, it is important that a waveguide is able to transport optical energy around sharp bends to allow for routing that resembles modern CMOS circuits. In order to demonstrate such routing, an s-bend silicon plasmonic waveguide having a width of $w_p=400$ μm and transverse displacement of $x=2$ μm and length of $y=5.8$ μm (6.3 μm overall length) is fabricated, as shown in Fig. 3(b). The power transmitted through this structure at $\lambda=1550$ nm was measured to be 0.41 μW. Based on the propagation curve found for the straight $w_p=300$ nm plasmonic waveguide, this power transmission corresponds to a device length of 6.0 μm. Simulations performed for a straight 400 nm wide waveguide predict a propagation distance of 2.1 μm. It should be noted that the FDTD simulation underestimated the propagation distance for the 300 nm by 5%. Taking this into consideration, the predicted power transmission through a 400 nm wide, 6.3 μm long straight waveguide would be 0.48 μW, and a bending loss of 0.07 μW (14.6%) can be deduced for the s-bend. In addition to demonstrating efficient guiding around sharp bends, this result provides additional confirmation that a guided mode is being observed in this experiment.

In conclusion, we have fabricated and characterized a class of silicon-based plasmonic devices that can be monolithically incorporated into CMOS fabrication processes and interfaced them to the SOI photonic platform. The measured results agree well with those from previous silicon-based plasmonic devices and with results obtained from 3D FDTD simulations. These results provide the basic propagation characteristics of this class of devices and form a basis for investigation into a wide range of plasmonic devices with complex geometries and into CMOS electronic-plasmonic hybrid applications.

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