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Citation: [Applied Physics Letters](#) **63**, 1625 (1993); doi: 10.1063/1.110716

View online: <http://dx.doi.org/10.1063/1.110716>

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# Observation of step bunching on vicinal GaAs(100) studied by scanning tunneling microscopy

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(Received 29 March 1993; accepted for publication 12 July 1993)

Similar step bunchings which consist of 7–9 single steps were observed by scanning tunneling microscopy on both vicinal GaAs(100) surfaces grown by metalorganic chemical-vapor deposition (MOCVD) and annealed in AsH<sub>3</sub> atmosphere. Growth parameters, including deposition rate, layer thickness, V/III ratio, and growth temperature, did not affect the morphology of the step bunching. These results indicate that step bunching is induced during the annealing process and its surface morphology is preserved during MOCVD growth for a wide range of growth parameters.

On a vicinal surface of the kind which is ordinarily used for metalorganic chemical-vapor deposition (MOCVD), steps play an important role in determining the characteristics of a growth layer. One well-known phenomenon concerning steps is step bunching, in which monosteps assemble and form a multistep. It is well known that step bunching occurs on vicinal GaAs(100) grown by vapor-phase epitaxy,<sup>1,2</sup> and recently, similar step bunching has been observed by atomic force microscopy on MOCVD grown layers. To shed some light on the mechanism of step bunching and its surface morphology, we carried out a series of scanning tunneling microscopy (STM) studies on GaAs(100) grown by MOCVD and on GaAs annealed in an AsH<sub>3</sub> atmosphere. In this letter we report the results of the observation of step bunching and the dependence of the morphology of it on the MOCVD growth parameters. Furthermore, we show that similar step bunching occurs on the annealed surface, indicating that the annealing process induces this phenomenon.

A GaAs(100) vicinal surface tilted 2° along [010] was used. This surface was chosen since it is typically used for MOCVD growth. Before the MOCVD growth, the sample was cleaned by H<sub>2</sub>SO<sub>4</sub> dipping, followed by chemical etching in a H<sub>2</sub>SO<sub>4</sub>, H<sub>2</sub>O<sub>2</sub>, H<sub>2</sub>O solution. After chemical etching, the substrate was placed on a GaAs-coated carbon susceptor and annealed to the growth temperature by rf heating. The annealing temperature was monitored by a thermocouple inserted into the susceptor. The temperature was increased at a rate of approximately 50 °C/min to the growth temperature and kept constant during the MOCVD growth. MOCVD growth was performed using trimethylgallium (TMG) and AsH<sub>3</sub> as raw material gases and H<sub>2</sub> for a carrier gas. The total pressure during MOCVD growth was 100 Torr, and the typical flow rates of AsH<sub>3</sub> and H<sub>2</sub> were 40 and 4000 sccm; therefore the partial pressure of As was approximately 1 Torr. After MOCVD growth, the temperature was decreased at the rate of 100 °C/min to room temperature.

Since the STM measurement was performed in an air ambient, the GaAs surface was oxidized. It is not clear what kind of disturbance would be caused by this oxidized layer; however for Si(111)<sup>4</sup> and GaAs(100)<sup>5</sup> surfaces a single step can be observed by atomic force microscopy in air ambient. These results imply that a single-step corrugation remains even on an oxidized surface.

A STM image of a vicinal GaAs(100) surface obtained after etching is shown in Fig. 1. The surface is not atomically flat but covered with pits of ~30 nm in diameter. These pits seem to have no ordering and are randomly distributed. From the net misorientation angle it is expected that single steps exist every 80 Å in the [010] direction, which cannot be observed in Fig. 1. This means that the surface is not etched uniformly, and pits are generated, by which the original steps are concealed.

A typical vicinal GaAs(100) surface grown by MOCVD is shown in Fig. 2. The surface morphology has drastically changed, and periodically arranged structures

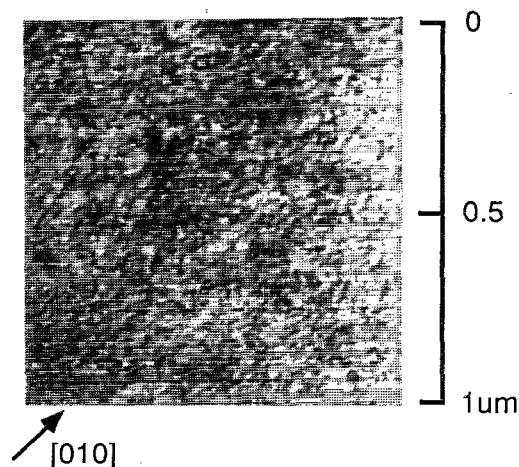


FIG. 1. STM image of GaAs(100) after chemical etching. Tunneling voltage is -2.6 V. Tunneling current is 0.17 nA.

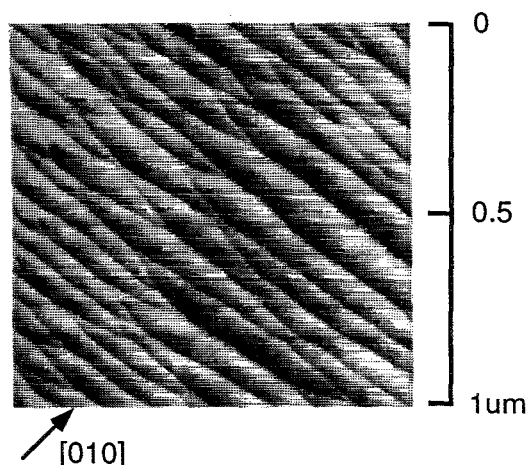


FIG. 2. STM image of the typical step bunching. Tunneling voltage is  $-2.1$  V. Tunneling current is  $0.17$  nA.

running in the direction perpendicular to  $[010]$  can be observed. A higher-resolution image of the surface is shown in Fig. 3(a). Figures 3(b) and 3(c) are the parallel and the perpendicular cross sections of the structures shown in Fig. 3(a). The undulation in the parallel direction is less than  $5$  Å, which suggests that the surface is atomically flat in this direction. In the perpendicular direction there exists a hill-and-valley structure which has good periodicity.

These results can be explained assuming that the steps have assembled into facet B shown in Fig. 3(c), a phenomenon called step bunching. The step-bunching structure of Fig. 2 will be referred to as typical step bunching, hereafter. Due to the low resolution we cannot conclude whether or not a single step exists in terrace A. If we assume that all the steps have gathered into facet B and no steps exist in terrace A, the misorientation of the surface can be calculated using the mean height of the facet,  $25$  Å, and the mean distance between them,  $650$  Å. The calculated misorientation was approximately  $1.9^\circ$ , which is in good coincidence with the net misorientation angle  $2.0^\circ$  of the sample. This means that the density of steps in the terraces is very low even if steps are present, thus the step bunching consists of 6–8 single steps.

Under the assumption that MOCVD growth is the cause of step bunching, growth parameters such as growth temperature, growth rate, and layer thickness were varied to investigate their influence on step bunching. Only one

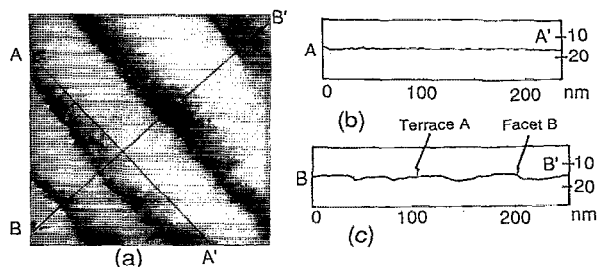


FIG. 3. (a) is a high resolution STM image of the typical step bunching, (b) is the cross section of AA' and (c) is that of BB'.

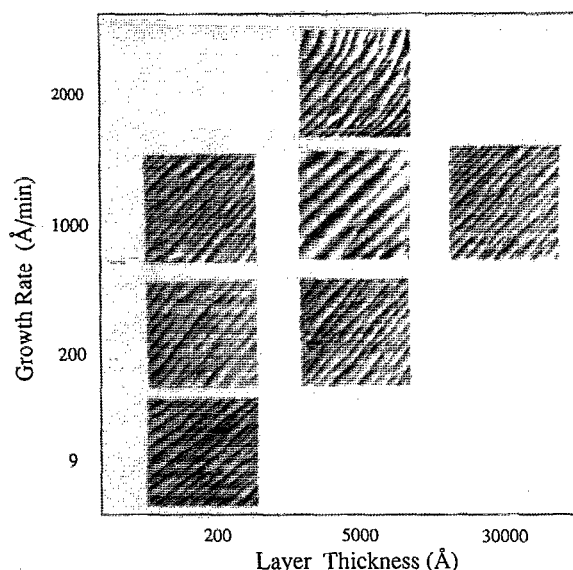


FIG. 4. STM image of MOCVD grown layers differing in growth rate and layer thickness. The scale of the images are about the same, except the image of the sample where the growth rate is  $1000$  Å/min and layer thickness is  $5000$  Å.

parameter was varied at a time, while the others were kept at the same value. At first, the growth temperature was varied to  $650$ ,  $700$ , and  $750^\circ\text{C}$ , while the growth rate, layer thickness, and V/III ratio were kept at  $1000$  Å/min,  $5000$  Å, and  $40$ , respectively. Contrary to our expectation, no marked difference among these sample surfaces was observed, always the typical step bunching surfaces was observed. A series of STM observations for samples differing in growth rate and layer thickness are shown in Fig. 4. The growth thickness was varied in the range from  $200$  Å to  $3$  μm, and the growth rate in the range from  $9$  to  $8000$  Å/min, while the growth temperature was  $700^\circ\text{C}$  for all of the samples. Again, contrary to our expectation, the same step-bunching structures were observed among all of these samples, as can be seen from Fig. 4. No conspicuous differences could be detected among these samples. These results suggest that changes in growth parameters such as growth temperature, layer thickness, growth rate, and V/III ratio have little influence on step-bunching under typical MOCVD growth conditions.

The above results strongly suggest that MOCVD growth itself does not play an important role in organizing the step bunching. Therefore, we studied vicinal GaAs(100) substrates annealed in  $\text{AsH}_3$  atmosphere to investigate whether thermal treatments play an important role. The experiment was carried out under similar conditions to those described above, except the sample was not exposed to TMG.

A vicinal GaAs substrate annealed at  $700^\circ\text{C}$  for  $5$  s in  $\text{AsH}_3$  atmosphere also showed the typical step bunching. This means that the annealing process induces the step bunching. Kasu and Fukui<sup>3</sup> have observed similar step bunching on vicinal GaAs(100) surfaces, though they have attempted to explain its formation mechanism in terms of MOCVD growth. Our experimental results show

that this is not the case. Regarding MOCVD growth or the annealing process as the origin of step bunching will lead to a great difference in the explanation of its mechanism, since MOCVD growth is usually executed under nonequilibrium conditions, while an annealing process can be interpreted as changing the surface morphology into a near-to-equilibrium configuration.

To investigate whether the duration of annealing affects the surface morphology, samples annealed for different time periods up to 40 min were studied. No conspicuous surface morphological difference could be detected, and the typical step bunching was always observed, indicating that this structure is very stable. According to Herring's<sup>6</sup> theoretical studies on vicinal surfaces, in which he discussed the equilibrium shapes of substrates in terms of surface-free energy, step bunching is more energetically favored than a regular monostep array. Since an annealing process will change the surface into a more energetically favored configuration, annealing of a regular monostep array is expected to result in step bunching. The fact that the step-bunching structure did not alter with increasing annealing time suggests that the step bunching is a near-to-equilibrium structure. This is in contrast with Herring's theoretical point of view which argues that once faceting, the facets must continue to grow indefinitely, because the larger the facet, the greater the energy gain. The experimental fact that typical step bunching is stable suggests that several kinetic restrictions such as surface diffusion and elastic energy prevent it from growing.

Step bunching has also been observed on Si(111) surfaces.<sup>7-9</sup> Summarizing the results reported so far, there seem to exist two different step-bunching mechanisms. We compare them with the step bunching observed here, showing that they must have a different origin. Latyshev *et al.*<sup>7</sup> reported that annealing Si(111) by direct-current heating causes step bunching, which is considered to be related to electromigration.<sup>8</sup> This step bunching occurs only if the Si(111) is annealed by direct current and not by alternating current or rf radiation. Hence our annealing process

was carried out by rf radiation. Hence our annealing process was carried out by rf radiation, this type of step bunching differs from the one we observed. The other type of step bunching is considered to be related to the  $(1\times 1)-(7\times 7)$  phase transition. The  $(7\times 7)$  region energetically dislikes steps; thus the steps are pushed away from the  $(7\times 7)$  unit cells and gather as the  $(7\times 7)$  region grows larger under the  $(1\times 1)-(7\times 7)$  transition temperature.<sup>9</sup> This is not the case which we observed in this study, since a phase transition such as  $(1\times 1)-(7\times 7)$  does not take place on GaAs when the substrate is cooled to room temperature after MOCVD growth. From the above discussion we conclude that the typical step bunching we observed is not related to the step-bunching process so far reported for Si(111); ours is caused by a different mechanism.

In conclusion, we have studied MOCVD grown vicinal GaAs(100) surfaces by STM. It was found that similar step bunching occurs for a wide range of MOCVD growth parameters. Annealing GaAs in AsH<sub>3</sub> atmosphere for 5 s resulted in the formation of similar step bunching; thus it was interpreted that annealing GaAs in AsH<sub>3</sub> induces the step bunching and the surface morphology is preserved during MOCVD growth. A change in the duration of annealing time up to 40 min did not affect the step bunching, indicating that it is a near-to-equilibrium structure.

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