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Causes of driving voltage rise in phosphorescent organic light emitting devices during prolonged electrical driving

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We studied the driving voltage stability of typical phosphorescent organic light emitting devices (PHOLEDs) based on 4,4′-bis(carbazol-9-yl)biphenyl and Tris(2-phenylpyridine)iridium(III) host:guest system. The results show that the gradual increase in voltage often observed with prolonged electrical driving is mainly governed by the accumulation of holes at the emission layer/hole blocking layer interface. Reducing the build-up of hole space charges in this region, for example, by means of eliminating guest molecules from the vicinity of the interface, leads to a significant improvement in the stability of PHOLED driving voltage. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4764021]

Due to their potential to achieve 100% internal quantum efficiency, phosphorescent organic light emitting devices (PHOLEDs) have been studied extensively in the last few years, with the aim to increase their efficiency and reliability, especially their electrical (i.e., operational) stability.[1–5]

Several root causes for the limited electroluminescence stability in organic light emitting devices (OLEDs) in general, i.e., the gradual decrease in brightness under constant driving current, have been identified. These include the chemical instability of organic molecules in certain charged states,[6,7] the presence of fixed positive space charges,[7] the diffusion of mobile ionic impurities,[8] the leakage of charge carriers and excitons,[9] and various bimolecular interactions such as triplet-triplet annihilation (TTA) and triplet-polaron quenching (TPQ).[10,11] Contrary to electroluminescence stability, the root causes behind the increase in OLED driving voltage, which also occurs during prolonged electrical driving, have not been deliberately investigated, and remain essentially unknown, especially for PHOLEDs. Kondakov *et al*. suggested that the accumulation of positive space charges at the hole transport layer (HTL)/electron transport layer (ETL) interface plays a role in voltage rise in bilayer fluorescent OLEDs.[12] However, the causes of this phenomenon in PHOLEDs, which generally utilize different materials and contain more layers in comparison to fluorescent OLEDs, remain essentially unknown. Changes in PHOLED driving voltage is a critical issue, especially for active matrix display applications in which each pixel is driven by its own integrated circuit. Since the circuits are typically designed to provide a certain power output, a significant change in the voltage required to drive an OLED creates challenges.

In this work, we report results from a study to elucidate the mechanisms behind the continuous increase in driving voltage during electrical driving in typical PHOLEDs. The results show that the increase in voltage is mainly caused by the accumulation of holes at the emission layer (EML)/hole blocking layer (HBL) interface. Reducing the build-up of hole space charges in this region, for example, by means of eliminating guest molecules from the vicinity of the interface, leads to a significant improvement in the stability of PHOLED driving voltage.

In this study, PHOLEDs based on archetypical 4,4′-bis(carbazol-9-yl)biphenyl (CBP) and Tris(2-phenylpyridine)-iridium(III) [$Ir(ppy)_3$] host:guest phosphorescent system in the emitting layer are used. In these devices, N,N′-di(naphthalene-1-yl)-N,N′-diphenyl-benzidine (NPB) and aluminum tris(8)-hydroxyquinoline (Alq_3) are utilized to form the HTL and ETL, respectively. Indium-tin-oxide (ITO) is used as an anode, and Mg/Ag is employed as a cathode. In some cases, a 2,9-dimethyl-4,7-diphenyl-1,10-phenanthroline (BCP) and aluminum (III) bis(2-methyl-8-quinolinate)-4-phenylphenolate (BAlq) HBLs are inserted in between the emitting and electron transport layers. All organic materials are purchased from Luminescence Technology Corp., Taiwan and used as received. The devices are fabricated by thermal deposition in vacuum at a base pressure of 5×10^{-6} Torr on ITO coated substrates. All measurements are carried out while the devices are kept in a pure nitrogen environment. Details of delayed EL measurement setup are reported in our previous work.[13,14]

We recently found that the accumulation of holes inside the emission layer (EML) accelerates electroluminescence degradation of PHOLEDs.[14] It was shown that increasing the confinement of holes inside the EML, for example, by means of using a HBL, accelerates the decrease in luminance efficiency. In order to investigate if the same phenomenon also plays a role in the gradual increase in device driving voltage during prolonged electrical driving, we conduct a comparative study on PHOLEDs containing HBLs (BAlq or BCP) or no HBL. The devices have the following structures

- Device A: ITO/MoO_3(10 nm)/NPB(40 nm)/CBP:$Ir(ppy)_3$ (8%) (40 nm)/Alq_3 (30 nm)/Mg:Ag.
- Device B: ITO/MoO_3(10 nm)/NPB(40 nm)/CBP:$Ir(ppy)_3$ (8%) (40 nm)/BAlq(10 nm)/Alq_3 (30 nm)/Mg:Ag.
- Device C: ITO/MoO_3(10 nm)/NPB(40 nm)/CBP:$Ir(ppy)_3$ (8%) (40 nm)/BCP(10 nm)/Alq_3 (30 nm)/Mg:Ag.

Figure 1 shows typical change trends in device driving voltage required to maintain a constant current density of

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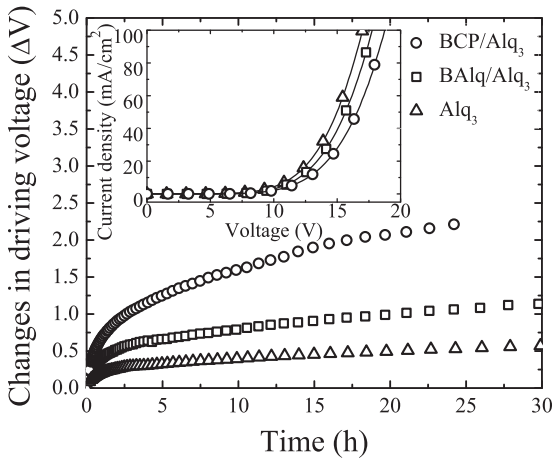

FIG. 1. Changes in driving voltage of typical PHOLEDs without and with BAlq and BCP hole blocking layers.

$20\,mA/cm^2$, represented as ΔV, where ΔV the driving voltage V (at any time t) − V (at t = 0). At this current density, the initial driving voltages of devices A, B, and C are 12.8 V, 13.4 V, and 14.2 V, respectively. The inset of Figure 1 shows the J-V characteristics of the same devices. As shown, the differences in the J-V characteristics among the devices increase at high current density. For example for devices A and C, the difference is ~1.1 V when the current density is $1\,mA/cm^2$ whereas it becomes ~1.8 V at $100\,mA/cm^2$. The differences in the initial voltages can be attributed to the various hole blocking capacities of the devices.[14] The highest occupied molecular orbital (HOMO) energy levels of Alq_3, BAlq, and BCP are 5.7 eV, 5.9 eV, and 6.5 eV, respectively.[15,16] In case of device A, since EML/Alq_3 interface does not significantly block holes, holes can easily drift from the EML into the adjacent electron transport layer. On the other hand, in devices B and C, holes are confined inside the emission layer by the hole blocking barrier at the EML/HBL interface caused by deeper HOMO of the HBL material in comparison to that of the EML (the HOMO energy levels of $Ir(ppy)_3$ and CBP are 5.5 eV and 6 eV, respectively). This barrier is lower in case of BAlq HBL that can mainly block holes transported on $Ir(ppy)_3$ sites, causing the hole blockage to be only partial.[14] As can be seen from Figure 1, the voltage rise trends correlate with the extent of hole confinement in the EML, where the device with the strongest hole confinement in the EML (i.e., with BCP HBL) displays the fastest rise in voltage whereas the device with the least hole confinement (device A) displays the slowest rise. The results suggest that the ΔV trends depend on the concentration of accumulated holes at the EML/HBL interface.

In order to verify this and further understand the possible role of holes in the voltage rise, we fabricate and test a series of devices, which include a neat CBP, of various thicknesses, next to the EML/HBL interface. In these devices, the thickness of the $Ir(ppy)_3$-doped layer is adjusted so as to keep the total device thickness the same. The general device structure is ITO/MoO3 (10 nm)/NPB (40 nm)/CBP:$Ir(ppy)_3$ (40-x nm)/CBP (x nm)/BAlq (10 nm)/Alq3 (30 nm)/Mg:Ag, where x represents the thickness of the neat CBP layer. The electroluminescence characteristics of these devices are summarized in Table I. All devices exhibit comparable EL levels

TABLE I. Electroluminescence characteristics of the devices with different thicknesses of neat CBP layer at the EML/HBL interface.

CBP (x nm)	Voltage (V)	Brightness (cd/m^2)	CIE
0	13.3	3810	0.328, 0.603
3	12.29	3870	0.331, 0.596
5	12.63	3880	0.329, 0.597
10	13.3	3730	0.329, 0.598

despite the differences in the thickness of the $Ir(ppy)_3$-doped layer. This shows that the electron-hole (e-h) recombination zone within the EML is located close to the HTL, which agrees well with previous reports.[17,18] Figure 2 shows the luminance intensity and operating voltage of these devices versus time of driving at $20\,mA/cm^2$ current density. As can be seen from Figure 2, all devices show comparable EL stability trends, suggesting EL stability is not primarily governed by phenomena at the EML/ETL interface. Conversely, and quite surprisingly, the presence of a neat CBP layer affects the voltage rise trends quite significantly. For instance, the control device (i.e., without a neat CBP layer) shows a voltage rise of about 1 V after 70 h of operation whereas the voltage rise in the device with the 3 nm neat CBP layer is only about 0.1 V over the same period of time. Clearly, this observation suggests that the two device stability aspects (i.e., EL stability and driving voltage stability) are not always coupled.

In PHOLEDs of the structure NPB/CBP:$Ir(ppy)_3$/ETL, due to the large energy barrier for hole injection from NPB onto CBP, holes are injected into the EML mostly onto $Ir(ppy)_3$ sites directly.[19,20] Subsequent to injection, the holes are transported into the EML by hopping on both $Ir(ppy)_3$ sites and (but to a much less extent) on CBP sites.[20] On the other hand, due to the very small energy difference between CBP and BAlq LUMO levels (2.8 eV and 2.9 eV, respectively), electrons are mostly injected and transported onto CBP sites.[21] This is also evident from the initial driving voltage and brightness levels of devices containing the neat CBP layer, where the absence of $Ir(ppy)_3$ from the region adjacent to the HBL interface does not result in an increase in the initial driving voltage or a decrease in the luminance, as would

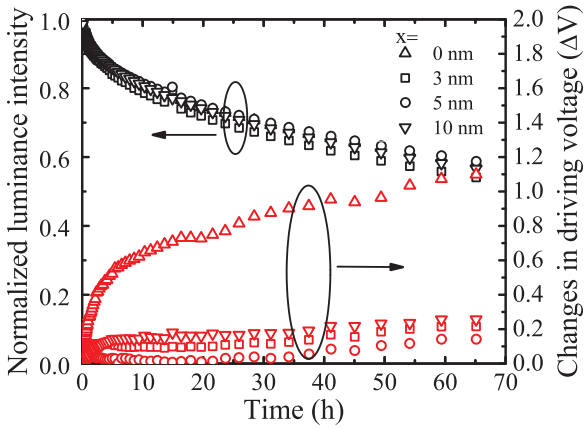

FIG. 2. Normalized luminance intensity and changes in driving voltage of devices which include a neat CBP, of various thicknesses, next to the EML/HBL interface under electrical aging at $20\,mA/cm^2$ current density.

be expected should $Ir(ppy)_3$ be assisting electron injection and/or transport in the EML. As holes mostly reside on $Ir(ppy)_3$ sites whereas electrons are transported efficiently on CBP, some holes that reach the HBL, possibly still reside on $Ir(ppy)_3$ or other interfacial trap sites without recombination. One would expect that the number of such "unrecombined" holes near the EML/HBL interface to increase during device operation. Therefore, in order to offset the effect of these trapped positive charges at the EML/HBL interface and maintain the electric field inside the EML that is required to sustain the same current, the positive potential applied on the anode with respect to the cathode must increase, hence the increase in driving voltage. In case of the devices with the neat CBP layer, as $Ir(ppy)_3$ is absent from the region near the HBL, the number of holes that can reach the HBL interface, where they can become trapped, is less (due to the absence of $Ir(ppy)_3$ conduction paths), hence the much smaller voltage rise.[22]

It should be pointed out that introducing a neat CBP layer at the HTL/EML interface (instead of the EML/HBL interface) is found to have no effect on driving voltage stability (results are not shown here in the interest of brevity). This is not surprising considering that the e-h recombination zone is located close to the HTL, and therefore the concentration of any holes that may remain without recombination "permanently" on $Ir(ppy)_3$ or at the interfacial trap sites at this region of the EML can be expected to be small.

In order to obtain more insights about the role of the neat CBP layer at the EML/HBL interface in improving driving voltage stability, we use delayed EL measurements to study devices with and without such layers. In this technique, a device is driven using a square pulse driving scheme, with a forward bias of 10 V and a pulse width of 0.5 ms (the pulse is sufficiently long for prompt EL to reach its steady-state intensity). An optical shutter opens to collect delayed EL around 0.3 ms after the end of the forward bias pulse, which is significantly longer than the lifetime of $Ir(ppy)_3$ triplet state lifetime ($<1\,\mu s$), hence ensuring the absence of any contributions from prompt EL in the collected signal. As such, any collected signal will arise from the radiative decay of excitons that are formed after the end of the forward bias pulse. In general, this delayed EL can be the product of:[14,20] (i) recombination of trapped charges that get released after the end of the forward bias pulse; (ii) various bimolecular interactions such as TTA, which in this case will be primarily due to the fusion of host triplet excitons (i.e., host-host TTA). This is because any contributions from guest-guest TTA to delayed EL in the milliseconds time frame due to the much shorter lifetime of phosphorescent guest triplet excitons are insignificant. In order to differentiate between these processes, a 0.5 ms reverse bias pulse (of magnitude −0.5 V) is applied on the devices during the delayed EL signal collection, and subsequent changes in delayed EL characteristics are monitored. Figure 3 displays the delayed EL signal versus time elapsed from the end of the forward bias pulse collected from devices containing a neat CBP layer (3, 5, or 10 nm thick) at the EML/HBL interface and also from a control device that does not contain a neat CBP layer (device structure: ITO/MoO3 (10 nm)/NPB (40 nm)/CBP:$Ir(ppy)_3$ (40-x nm)/CBP (x nm)/BAlq (10 nm)/Alq_3 (30 nm)/Mg:Ag, where x represents the thickness of the neat CBP layer). Time 0 on the x-axis corresponds to 0.3 ms after the end of the forward bias pulse. It should be noted that spectral measurements show that the delayed EL corresponds to $Ir(ppy)_3$ emission. As can be seen from the figure, the delayed EL from all devices with a CBP layer exhibits a sudden decrease on the application of the reverse bias pulse, but rebounds, at least partially, at the end of the reverse bias pulse. This recovery is partial in case of the device with the 3 nm CBP layer but is almost complete in case of the devices with the 5 and 10 nm CBP layers. (note: delayed EL characteristics from a control device and from a device with 5 nm CBP layer that are not subjected to the reverse bias pulse, labelled "no reverse bias" is also shown on the same axis for comparison). In contrast, the control device (i.e., without a neat CBP layer) shows only a modest decrease in delayed EL at the beginning of the reverse bias pulse, and also a relatively much smaller recovery at the end of the pulse. As a recovery at the end of the reverse bias indicates that host-host TTA contributes significantly to the observed delayed EL,[19] the results indicate that the concentration of host triplet excitons is higher in devices containing a neat CBP layer, and generally increases with the thickness of the layer. It follows therefore that these triplet excitons originate in the neat CBP layer. That this effect appears to saturate as the thicknesses of the layer exceeds 5 nm can be due to the fact that only excitons in this neat layer that are within a distance from the CBP/ $Ir(ppy)_3$ layer interface equal to the Forster radius for energy transfer (typically ~5 nm) are able to undergo efficient energy transfer to $Ir(ppy)_3$, and hence contribute to the delayed EL signal. Figure 4 shows delayed EL from the same devices measured before and again after 80 h of continuous electrical driving at a current density of 20 mA/cm^2, denoted to by "fresh" and "aged," respectively. As can be seen from the figure, prolonged electrical driving affects the extent of recovery in delayed EL at the end of the reverse bias pulse, causing it to almost disappear in case of the control device (Figure 4(a)) and to become clearly lower in the devices with the 3 nm and 5 nm CBP neat layers (Figures 4(b) and 4(c), respectively). On the other hand, the extent of recovery remains almost unchanged in case of the device

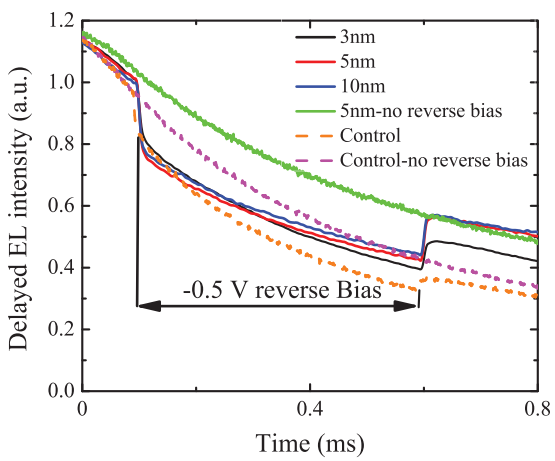

FIG. 3. Delayed EL intensities of the devices with different thicknesses of neat CBP layer under −0.5 V reverse bias.

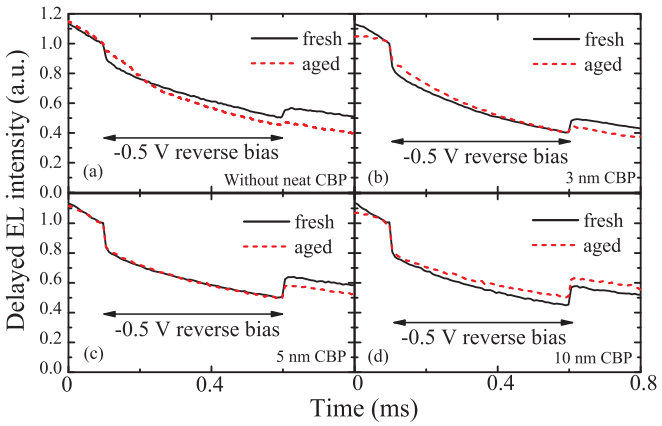

FIG. 4. Delayed EL signal of devices (a) without a neat CBP layer, with (b) 3 nm CBP, (c) 5 nm CBP, and (d) 10 nm CBP layer before and after 80 h of electrical aging at 20 mA/cm^2 current density.

with the thicker (i.e., 10 nm) CBP neat layer (Figure 4(d)). This reduction in recovery, which reflects a decrease in the underlying TTA process, points to a decrease in the concentration of CBP triplet excitons. The decrease in triplet exciton concentration suggests the increase in charge concentration with prolonged electrical driving, which results in an increased quenching of the triplet states due to triplet-polaron interactions.[23] The results therefore suggest that the use of a neat CBP layer of sufficient thickness (e.g., 10 nm) at the EML/HBL interface reduces the build-up of trapped charges in the vicinity of the interface during prolonged electrical driving, evident in the almost unchanged delayed EL characteristics observed in this case (Figure 4(d)). That the concentration of these charges is higher in devices with a thinner neat CBP layer (and highest in the device with no neat CBP layer) indicates that such charges may be trapped on trap sites, possibly on Ir(ppy)$_3$, in the vicinity of the interface. As Ir(ppy)$_3$ transports holes mostly,[21] such trapped charges would be expected to be holes. Removing Ir(ppy)$_3$ from the vicinity of the interface (i.e., by having a neat CBP layer) reduces the number of holes that can reach the HBL interface, and therefore reduces the build-up of positive space charge in the vicinity of the interface, hence the much higher driving voltage stability observed in Figure 2(b).

In conclusion, the results show that the gradual increase in driving voltage often observed with prolonged electrical driving of PHOLEDs is mainly governed by the accumulation of holes at the EML/HBL interface. Results from delayed EL measurements suggest the build-up of a hole space charge in the vicinity of this interface with prolonged electrical driving. Reducing the build-up of hole space charges in this region, for example, by means of eliminating guest molecules from the vicinity of the interface, leads to a significant improvement in the stability of PHOLED driving voltage.

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