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Anomalous positive charge trapping in thin nitrided oxides under high-field impulse stressing

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An anomalously high density of positive trapped charges was observed in thin (43 Å) nitrided gate oxides subjected to high-field impulse stressing. The hot-hole generation occurs via a regenerative feedback mechanism, with minimal charge relaxation due to the short duration of the impulse stress. This gives rise to an extremely high density of trapped holes that were not observed under direct current stressing conditions. The trapped holes can be easily annealed electrically at room temperature and the annihilation of positive trapped charges is accompanied by a higher number of interface states being created. A better understanding on thin oxide degradation under impulse stressing can help in the choice of a suitable programing/erasing pulse width/amplitude for use in endurance testing of nonvolatile memories. © *2000 American Institute of Physics.* [S0003-6951(00)03943-7]

The write/erase cycling endurance testing of nonvolatile semiconductor memory (NVSM) devices, such as floating-gate tunnel-oxide electrically erasable and programable read-only memories, employs short duration pulses to inject/remove electrons into/out from the floating gate under high-field injection conditions. The use of a shorter pulse duration is feasible if this is properly compensated with a higher programing/erasing voltage[1] to ensure that approximately the same amount of charges are being stored/removed from the floating gate. Ricco and Pieracci have shown the feasibility of using high-voltage tunneling pulses with very short duration to achieve fast programing of NVSMs with acceptable oxide degradation.[2] This implies that the use of shorter duration but higher field impulses could be the future trend in programing NVSMs. We have observed an anomalously high density of trapped holes in thin (43 Å) nitrided gate oxides subjected to impulse stressing, irrespective of the injection polarity. Such high density of trapped holes was not observed under direct current (dc) constant current stressing. Since the generation of trapped charges within the thin tunnel oxide will adversely affect the outcome of the endurance testing, the finding has important implications to the accuracy of the endurance test if a proper pulse width/duration is not chosen.

Devices used in our study are commercial grade p^+-polysilicon gate p-channel metal–oxide–semiconductor transistors (p^+/pMOSTs) fabricated using a 0.25 μm technology, dual-gate twin-well complementary MOS process. The transistors have a gate area of 50×1 μm^2 and an electrical oxide thickness of 43 Å as extracted from high-frequency capacitance–voltage measurements. The impulse stressing [i.e., alternating current (ac) stressing in Fig. 1] was generated from a transmission line pulsing circuit that produces short-duration, high-field constant-current impulses that are usually used to simulate the human-body model electrostatic discharge stressing. The impulse applied has a rise time and duration of 4–7 ns and 200 ns, respectively. Voltage and current wave forms were monitored with a calibrated voltage and current probe, respectively. Substrate (gate) injection was carried out by subjecting the gate (n well) to the short duration, high-field positive-voltage impulses, with the n well (gate) being grounded and source/drain terminals floated. In the case of dc constant current stressing (CCS), a constant current density ranging from ±4 to ±100 mA/cm^2 was supplied to the gate, with the n well connected to ground potential and the source/drain terminals floated. Oxide deg-

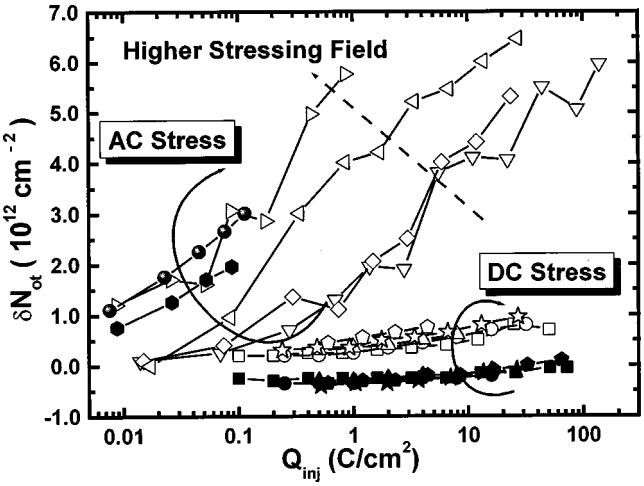

FIG. 1. The change in oxide trapped charge density (δN_{ot}), with respect to the prestress value, following different amount of fluence (Q_{inj}) injection under both ac (38–75 kA/cm^2; $V_{impulse}=14$–23 V; duration$=200$ ns) and dc (±4, 10, 20, 40, and 100 mA/cm^2; $|V_g|=6.1$–7.5 V) stressing. The solid and open symbols represent substrate (i.e., n well) and gate electron injection, respectively. The different symbols represent different devices tested under different stressing field. Positive or negative δN_{ot} indicates net change in trapped hole or electron density, respectively. Significantly higher density of positive trapped charges were observed under ac stressing as compared to dc stressing. A higher impulse amplitude results in more trapped charges as indicated by the direction of the dashed arrow. For ac impulse stressing under substrate injection condition, the samples broke down above 0.1 C/cm^2 (no data above this injected fluence value) because of the much higher oxide electric field.

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radation following different extent of impulse stress was characterized using dc current–voltage (DCIV) measurement.[3] The DCIV technique, configured in the top-emitter configuration, was used to estimate the number of oxide trapped charges (N_{ot}) and interface states (N_{it}) generated from the peak base (n well) recombination current ($I_{base,peak}$) versus gate voltage plot. The shift of $I_{base,peak}$ in the positive (negative) gate-voltage direction (i.e., δV_{peak}) and the change in the $I_{base,peak}$ amplitude (i.e., $\delta I_{base,peak}$) are proportional to the number of negative (positive) oxide trapped charges and interface states generated, respectively. The change in oxide trapped charge density (i.e., δN_{ot}) following electrical stress can be calculated using $(C_{ox}\delta V_{peak}/q)$.

Figure 1 shows the change in oxide trapped charge density after different amount of fluence injection. p^+/pMOSTs were subjected to either a dc (CCS of ± 4 to 100 mA/cm^2 and corresponding $|V_g|$ of 6.1 to 7.5 V) or an ac [impulse current density of 38–75 kA/cm^2 or impulse amplitude ($V_{impulse}$) of 14–23 V] type of stressing and DCIV measurements were carried out to assess the change in oxide trapped charge density and interface states generated. Stressing via substrate (i.e., n well) and gate electron injection are represented by the solid and open symbols, respectively. Results from Fig. 1 show that thin oxides subjected to ac (impulse) stressing have a much larger density of oxide trapped charge (δN_{ot}) being generated as compared to dc stressing, irrespective of the stressing polarity. A higher stressing field, as shown by the direction of the dashed arrow in Fig. 1, will result in larger δN_{ot} for the same amount of fluence injected.

To examine the charge relaxation process under different pulse duration, a pulse generator (HP8114A) was used to supply constant voltage impulses (16 V) with different duration. Several p^+/pMOSTs were subjected to gate injection impulse stressing and DCIV measurements were carried out at specific intervals. The constant amplitude/field impulse was applied at 2 s intervals, that is much longer than the defect relaxation time constant ($\sim$500 ns).[2] Therefore, any difference in oxide degradation arising from these constant voltage impulses should be attributed to the difference in pulse duration. Figure 2 shows δN_{ot} versus the cumulative impulse duration (i.e., pulse width$\times$number of impulses) applied. It is seen that the density of oxide trapped charges generated (indicated by δN_{ot}) is strongly dependent on the impulse duration, and increases when the pulse duration decreases.

The high density of positive trapped charges generated following impulse stressing is electrically unstable. Relaxation or annealing of the trapped charges was observed after carrier-separation measurements[4] for the impulse stressed devices. Relaxation of a higher density of positive trapped charges (as indicated by a higher δV_{peak} shift), is accompanied by a higher number of interface states generated (as indicated by a higher $\delta I_{base,peak}$) as shown in Fig. 3. This transformation of positive trapped charges to interface states is consistent with results published in the literature.[5]

The gate oxide was able to withstand a much higher stressing voltage under impulse stressing because of the relatively short pulse duration. This explains why devices could withstand impulses (duration of 200 ns) up to 1000 pulses at

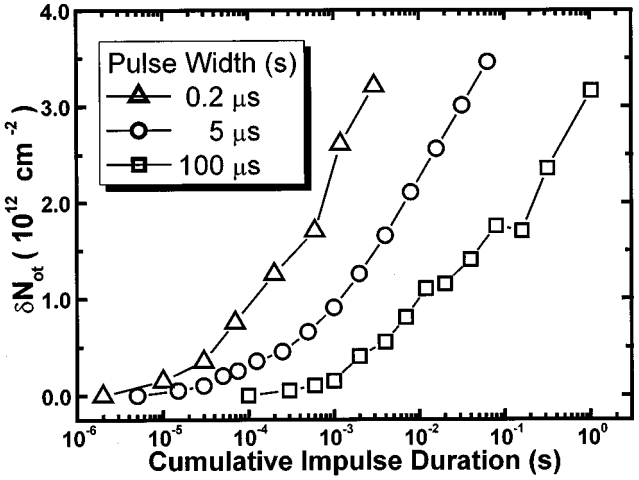

FIG. 2. The change in oxide trapped charge density (δN_{ot}) vs cumulative impulse duration after gate injection impulse stressing. The oxide trapped charges density generated in the thin oxide is strongly dependent on the impulse duration.

23 V without breakdown. Figures 4(a) and 4(b) show the band diagram for the p^+/pMOSTs under gate and substrate injection impulse stressing, respectively. Various possible carrier generation and trapping pathways are shown in the figure. During gate injection impulse stressing as shown in Fig. 4(a), the high-field impulses are likely to drive the n well into deep depletion with substantial voltage drop within the n well. Hot holes could be generated from two main sources: (1) avalanche plasma or interband tunneling within the deep-depletion regions and (2) different hot-hole generation kinetics such as Auger generation, impact generations and impact energy exchange,[6] initiated by p^+-gate valence band electron injection. However, calculations of the oxide field show that valence band electron injection from the gate [not shown in Fig. 4(a)] is less likely to take place for the range of impulse amplitudes applied. Energetic holes, either with sufficient energy to surmount the silicon dioxide (SiO_2) energy barrier or tunneling into the oxide valence band, will drift under the oxide electric field towards the gate, where

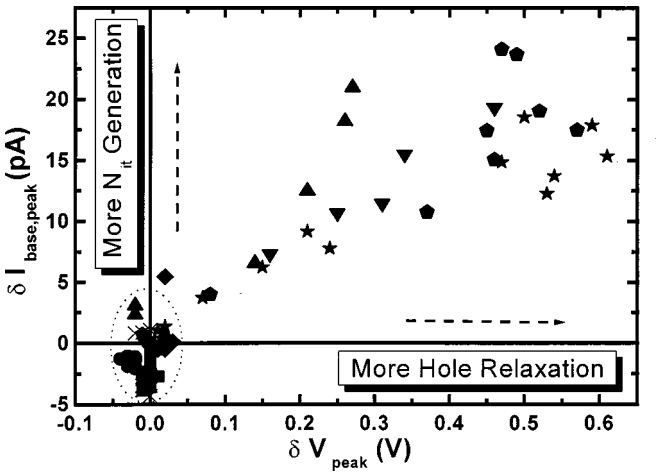

FIG. 3. Scatter diagram showing the shift in V_{peak} (i.e., δV_{peak}) and the corresponding change in $I_{base,peak}$ (i.e., $\delta I_{base,peak}$) after carrier-separation measurement for the ac (impulse) and dc stressed devices. The data points surrounded by the circle are mainly contributed by the dc-stressed devices, which do not produce observable shifts in V_{peak}.

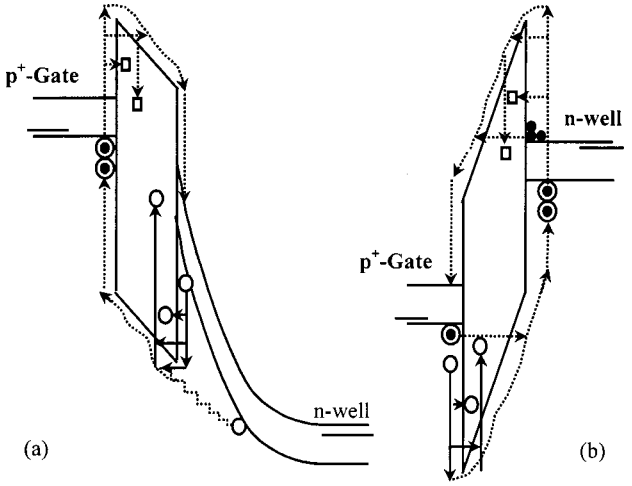

FIG. 4. Energy band diagram showing carrier injection and hole generation pathways during high-field impulse stressing: (a) deep depletion (gate injection impulse stress) and (b) accumulation (substrate injection impulse stress). Electrons and holes are indicated by solid and open circles, respectively.

they will undergo thermalization. A fraction of these holes may be captured from the oxide valence band by the oxide traps. In view of the electron mean-free-path of 10–32 Å[7,8] as compared to the oxide thickness of 43 Å in this case, no significant hole generation is expected from impact ionization within the oxide. Hole trapping could also arise from direct tunneling of hot holes into the oxide traps located at the proximity of the silicon/oxide (Si/SiO_2) interface. Hot holes that have escaped capture could transfer their energy to a valence band electron and excite it into the conduction band. The excited valence electron could generate electron traps in a similar way as the hot holes. If the ejected valence band electrons possess sufficient energy, they may surmount or tunnel through the SiO_2 barrier, giving rise to the back injection. Upon reaching the *n* well, more holes may be generated as a regenerative feedback loop is formed together with the initial hole generation via interband tunneling or avalanche plasma.

Figure 4(b) shows the energy band diagram and the various carrier generation and trapping pathways under substrate injection impulse stressing. Since both the p^+ gate and *n* well are biased into accumulation, most of the impulse voltage is expected to drop across the oxide layer. A similar regenerative feedback loop, generating hot electrons/holes in the same manner as the case of gate injection impulse stressing, is expected, except that the initial injection is triggered by *n*-well conduction band electrons instead and the deep depletion layer is not present to generate hot holes via avalanche or interband tunneling. The absence of a deep-depletion layer under substrate injection impulse stressing is compensated by a much higher oxide electric field. Hole injection from the p^+ gate (or anode) without feedback is also possible.

The high density of positive trapped charges following high-field impulse stressing of either polarity could be attributed to the formation of a regenerative feedback loop, generating substantial hot holes for trapping. The relatively low stressing voltage under dc stressing condition may not initiate the formation of this regenerative feedback loop. Devices subjected to a high number of impulses were observed to fail as a result of oxide breakdown, which could be due to the excessive number of holes being generated.

Besides the high stressing voltage that results in excessive positive charge trapping, a charge relaxation process is also taking place concurrently. The presence of a sustained oxide electric field in the case of dc stressing could detrap charges effectively from the thin oxide, resulting in a small charge trapping observed. On the other hand, in the case of impulse stressing, the oxide field vanishes after the short impulse duration, making the charge relaxation process very inefficient. This argument could account for the results shown in Fig. 2. It is the higher stressing voltage and short impulse duration that cause an excessive number of hot holes being generated in a regenerative feedback manner. This, together with the limited charge relaxation, could explain why a high density of oxide trapped holes was observed under impulse stressing but not under dc stressing.

Most of the trapped charges are formed at the proximity of the Si/SiO_2 interface, making it easier for charge relaxation to take place even under a small oxide field. Annealing of the positive trapped charge was found to be correlated with an increase in the N_{it} as illustrated in Fig. 3, suggesting that these defects are possibly located close to the Si/SiO_2 interface.

In summary, this study has shown that high-field impulse stressing of either polarity could generate a high density of positive trapped charges in the thin nitrided oxide, as opposed to the general observation that there is negligible charge trapping in the thin oxide under dc stressing. These positive trapped charges can be easily annealed electrically at room temperature and the annihilation of the trapped holes is accompanied by a higher number of interface states being created. The high impulse amplitude and short impulse duration were found to be responsible for the excessive oxide trapped charges. This finding should be taken into consideration when deciding on a proper programing/erasing pulse to use during endurance testing of NVSM.

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