Nanoscale

Cite this: *Nanoscale*, 2012, **4**, 6365

www.rsc.org/nanoscale

PAPER

Performance evaluation of electro-optic effect based graphene transistors

Gaurav Gupta,[a] Mansoor Bin Abdul Jalil,[a] Bin Yu[b] and Gengchiau Liang*[a]

Received 15th June 2012, Accepted 3rd August 2012
DOI: 10.1039/c2nr31501g

Despite the advantages afforded by the unique electronic properties of graphene, the absence of a bandgap has limited its applicability in logic devices. This has led to a study on electro-optic behavior in graphene for novel device operations, beyond the conventional field effect, to meet the requirements of ultra-low power and high-speed logic transistors. Recently, two potential designs have been proposed to leverage on this effect and open a virtual bandgap for ballistic transport in the graphene channel. The first one implements a barrier in the centre of the channel, whereas the second incorporates a tilted gate junction. In this paper, we computationally evaluate the relative device performance of these two designs, in terms of subthreshold slope (SS) and I_{ON}/I_{OFF} ratio under different temperature and voltage bias, for a defect-free graphene channel. Our calculations employ pure optical modeling for low field electron transport under the constraints of device anatomy. The calculated results show that the two designs are functionally similar and are able to provide SS smaller than 60 mV per decade. Both designs show similar device performance but marginally top one another under different operating constraints. Our results could serve as a guide to circuit designers in selecting an appropriate design as per their system specifications and requirements.

I. Introduction

Smaller and faster transistors, dissipating lower power than their contemporaries, are required to bring about more functionality in a standard package for application in high-performance computing and consumer electronics.[1] Specifically, a low subthreshold slope (SS) is required to achieve high "switch-on current" (I_{ON}) for faster charging of load capacitors, and low switch-off current (I_{OFF}) for lower static dissipation within the available gate voltage swing. The optimization of power against speed in CMOS system-on-chip, limits SS to 60 mV per decade at room temperature,[2,3] owing to traditional MOSFET architecture. With other MOS architectures,[3] such as feedback MOSFETs, impact ionization MOSFETs, nano-electromechanical FETs, and tunnel FETs, to overcome the constraints of the conventional Si-MOSFET architecture, these result in trade-offs against other critical device performance metrics, like device reliability, intrinsic area, ideal *I–V* characteristics, *etc.* Therefore, as of now, to the best of our knowledge, no ideal solution exists for silicon-based transistors.

Graphene, discovered in 2004,[4] has been touted to replace silicon in electronic nano-devices because of its smaller atomic size, high mobility and long mean free path. However, the absence of a bandgap in graphene results in small I_{ON}/I_{OFF} in conventional graphene field effect transistors (GFETs), thereby restricting their possible applications mainly to RF amplifiers,[5,6] Although several approaches have been proposed to create a bandgap in graphene-related materials, such as chemical modification and quantum confinement, they usually alter the electronic properties of graphene adversely,[7] like reduction in electron mobility. Therefore, non-conventional graphene transistors which exploit new physical phenomena like Klein tunneling,[8] electro-optic effect,[7,9–13] and pseudospin[14] have been proposed to circumvent the bandgap limitation.

Recently, computational analysis[11–13] of electron transport in a graphene channel, which is analogous to optical transmission in fibers, and its experimental verification[13] have led to two proposals of graphene electro-optic transistor (GEOT),[7–9] as shown in Fig. 1, where a bandgap is opened artificially by blocking certain electron energies in analogy with 2D-optics. In design A, electrons are injected from a point source, and are blocked by a barrier placed at the centre of the graphene channel, while in design B, a slanted gate is placed across the channel, and electron blockade is effected *via* total internal reflection. The resulting high I_{ON}/I_{OFF}, small SS and virtual bandgap of both designs make them apt for logic devices. However, detailed analysis is still required to analyze trade-offs in device design and the operational parameters of these proposed devices.

Therefore, this work focuses on investigating and comparing the relative device performance of the two GEOT designs, and the influence of device geometry, voltage and temperature. The original proposal of design B posits its transistor mechanism on basis of the Klein paradox.[8] However, given the controversial

[a]*Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576, Republic of Singapore. E-mail: elelg@nus.edu.sg*
[b]*College of Nanoscale Science and Engineering, State University of New York, Albany 12203, NYUSA*

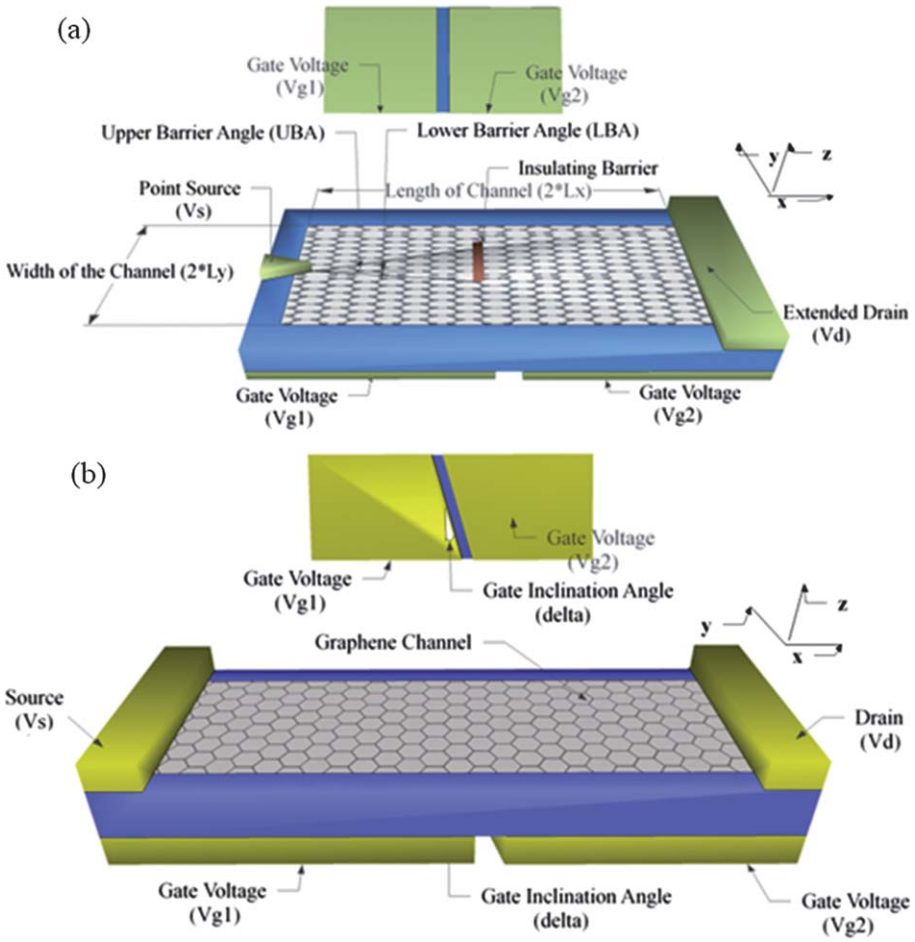

Fig. 1 Device structure of analyzed proposals for four terminal graphene electro-optic transistor (GEOT). Both induce a bandgap by blocking certain energies by emulating 2-D ray optics. The graphene channel, in the x–y plane, rests over substrate/dielectric. Both have two back gates, which electrostatically segment the channel into region 1 (n-side) and 2 (p-side), under V_{G1} and V_{G2} respectively, with a relative refractive index η_{21} and critical angle θ_C ($\sin^{-1}\eta_{21}$). (a) Ref. 7, The electron stream (circular wavefront) from the point electron injection source is blocked by an insulating barrier placed in the centre of the channel. The junction is formed in the y-direction along the barrier. In addition, the electron incident at junction with angle (θ_i) greater than θ_C is blocked. θ_B is barrier subtended at source for a symmetrically placed barrier *i.e.* for Upper Barrier Angle (UBA) = Lower Barrier Angle (LBA). (b) Ref. 8 and 9 electron injected from source (planar wavefront) is blocked from traversing from region 1 to region 2, if the critical angle of its wavefront is less than the gate inclination angle (δ).

nature of this effect with both proof of its existence,[15–21] and repudiation,[22–27] we have presented the operation of design B in terms of its electro-optic behavior, and found it to be similar to design A. Specific advantages and disadvantages of both designs are highlighted and discussed. Additionally, we also suggested modification in the original design to overcome the limitation of non-zero V_{G2} for I_{OFF} point.

II. Theory and methodology

In design A, two back gates, V_{G1} and V_{G2}, are implemented to control the current in the undoped channel. On the other hand, in design B, the channel is chemically doped *in lieu* of gate voltages. To investigate the physical insights and performance of both designs, this work considers an ideal (pure 2D) undoped channel with two gates, with an abrupt junction and without edge effects. The gate bias under the right and left graphene segments can dope the segments to either n-type or p-type, respectively. If biasing dopes both graphene segments to n-type, it is described as "nn-config." whereas if segment 1 is n-type and segment 2 is p-type, it is referred as "np-config". By utilizing the different doping configurations between graphene segments, one can block electrons within a certain energy range from traversing from source to drain. This is similar to inducing an actual bandgap in graphene, which is more challenging from the fabrication's point of view.[6] The device dimensions can be considered to be within the limits of ballistic transport for graphene, due to graphene's long mean free path.[4] Within these ballistic limits, electron transport in the graphene channel can be approximated to wave propagation, as was done by Cheianov *et al.*[11] Therefore, in calculating the transmission $T(E)$[7] which is required by the current equation (eqn (3) in the Appendix), it is assumed that the point source in design A generates a circular wavefront, while the extended source in design B forms a planar wavefront.

In device A, the origin (0, 0) is taken to be the point at the intersection of electrostatically separated graphene segments and

normal to the point source, whereas for design B, the origin is set at the midpoint of the inclined gate junction. In design A, an insulating barrier of finite dimensions is placed in the center of the channel to inhibit normally incident electron waves from the point source (by Klein tunneling) up to the angle subtended by barrier at the source, *i.e.* UBA (upper barrier angle) in the $+y$ plane and LBA (lower barrier angle) in the $-y$ plane. Additionally, because of different doping profiles, *i.e.*, different V_{G1} and V_{G2} values on the two graphene segments, the electron waves from segment 1 to 2 will see the relative refractive index η_{21} and critical angle θ_C ($\sin^{-1}\eta_{21}$), which occludes electrons incident at the junction with an angle (θ_i) greater than θ_C (total internal reflection).[7] However, for smaller θ_i, electron waves will traverse into segment 2 at a refracted angle $\theta_r = \sin^{-1}((\sin\theta_i)/\eta_{21})$. In the OFF state of the transistor, a large fraction of the energy spectrum of injected electrons will have its critical angle θ_C smaller than the barrier angle; therefore, irrespective of the incident angle θ_i, the electron wavefront will be blocked. However, in the ON state, only small fraction of energies have θ_C smaller than the barrier angle. Under this condition, only electrons with incident θ_i smaller than the barrier angle, as well as electrons with a large incidence angle θ_i exceeding θ_C, are blocked. The rest of the electrons can transmit through, thereby driving the transistor into saturation. Generally, by varying the control parameters, one may induce steeper changes in I_{OFF} than I_{ON}.

On the other hand, design B inclines the gates by angle δ to attain the universal condition of $\theta_i = \delta$ and, thereby, block electrons which have energies such that their $\theta_C < \delta$. In the OFF state, a broad range of electron energies satisfy these criteria as η_{21} (eqn (1)) tends to zero. In this work, the OFF (I_{OFF}) and ON (I_{ON}) currents are set as the minimum and maximum source-drain current (I_D) for a given configuration, irrespective of 'np' or 'nn' configuration. Besides, since θ_C depends on the voltage bias and energy of individual electrons, the transistor-switching action in both designs is achieved by toggling V_{G2} while keeping V_{G1} fixed. The equations governing the electron transmission in both designs are consolidated and described in detail in the Appendix.

III. Results and discussion

Firstly, we study the effects of the barrier position and geometry. In design A, we investigate the effect of moving the barrier along the y-axis, while for design B we investigate the influence of the orientation of the gate inclination. As illustrated in Fig. 2, it can be observed that designs A and B are symmetrical about the x and y-axis, respectively, as depicted by the overlap of the red and black curves. Thus, if there are two variants, labeled m and n, of design A (or B) such that (UBA_m, LBA_m) = (LBA_n, UBA_n) (or $\delta_m = -\delta_n$), they will have the same transfer characteristics. This agrees with the symmetry of the two devices about their respective axes. Next, for design A, the lowest I_{OFF} and the highest I_{ON}/I_{OFF} ratio is achieved when UBA = LBA (blue line in Fig. 2(a)). Under this condition, the maximum fraction of electron energies is blocked. In the asymmetrical scenario, electrons with low θ_i and/or energies may be able to pass *via* either the positive or the negative y-plane, depending on which part of the barrier (upper or lower) subtends a lower angle to the source, thereby increasing both I_{ON} and I_{OFF} (leakage current). Although the symmetric

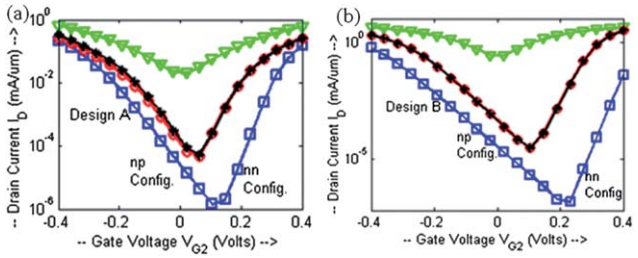

Fig. 2 Effect of moving the insulation barrier of fixed dimensions along the y-axis in design A and polarity of gate inclination for design B. (a) Minimum I_{OFF} is achieved for a symmetrically placed barrier *i.e.* when UBA = LBA (20° in our case) (blue line). Drain current remains the same for barrier positions mirrored about the x-axis along the barrier's y-axis (black overlapping with red line). The black line stands for intermediate barrier position *i.e.* UBA = 2 LBA. (b) Gate inclination (δ) in design B has similar transfer characteristics in the graphene channel as θ_B in design A. Moreover, black ($\delta = +20°$) overlap with red ($\delta = -20°$) lines predicts the functional independence of the device of the polarity of δ. The green trend corresponds to absence of barrier for both (a) and (b).

barrier configuration lowers I_{ON}, it results in an even steeper decline in I_{OFF}, due to the blocking of a large spectrum of energies, thus improving the I_{ON}/I_{OFF} ratio. Therefore, a symmetric barrier configuration is optimal to the operation of devices based on design A.

Secondly, we investigate the effect of widening the insulating barrier along the y-axis, *i.e.*, increasing θ_B subtended at the source (UBA = LBA = θ_B) for design A, and the gate inclination angle δ for design B. As shown in Fig. 3, the drain current decreases with the increase in θ_B (δ) (Fig. 3(a) and (d)), because a larger θ_B (δ) would exceed the critical angle over a wider range of electron energies. However, for design A, there is a steeper roll-off in I_{OFF} than I_{ON}, because of the blockage of large energy spectrum, thus enhancing the I_{ON}/I_{OFF} ratio and lowering the SS for design-A. The reason can be attributed to the steep declivity of the I_{ON} *versus* θ_B slope in contrast to design B. Thus, this indicates that design A marginally outperforms design B with respect to the transistor action under the influence of the gate geometry. Moreover, there is an optimal range for θ_B and δ. When θ_B (δ) > 30–35°, I_{ON} becomes too small for high frequency applications, whereas when these two angles are smaller than 10°, I_{OFF} or the leakage current becomes appreciable. For circuit design, the favorable angle ranges from about 17 to 21°. However, the final value also depends on selected region of operation. For instance, for a given value of I_{ON}, nn-operation allows for smaller magnitudes of θ_B (δ) than np-operation, although at the cost of smaller I_{ON}/I_{OFF} ratio. Next, it can be observed that I_{OFF} (OFF-state) corresponds to non-zero V_{G2}. This may lead to significant static dissipation if the circuit is designed with an OFF-state voltage of zero. Furthermore, the 'nn-config.' yields SS < 60 mV per decade over a substantial range of θ_B (δ), giving room to tune other parameters, in contrast to the 'np-config.'. With increase in θ_B (δ), V_{G2} corresponding to I_{OFF} shifts towards higher positive values, thereby making device asymmetrically bipolar w.r.t 0 V bias point. In fact, for unipolar operation, design B offers I_{ON} and I_{OFF} for same polarity of V_{G2} up to certain δ (25.2° in our simulations). However, if design-A is operated in a unipolar mode then I_{ON} and I_{ON}/I_{OFF} are

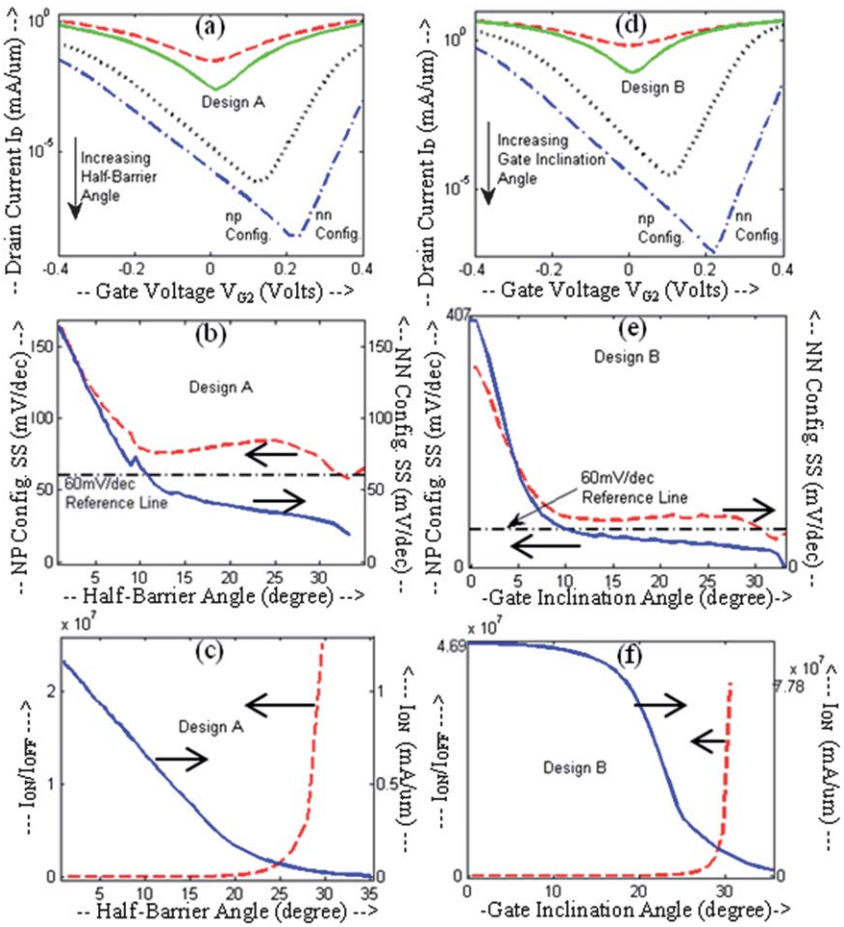

Fig. 3 Impact of the half-barrier angle (design A) and gate inclination (design B) for $V_{G1} = 1$ V at 300 K. For designs A and B, width along the y-axis of a symmetrically placed insulation barrier subtending θ_B at the source and gate junction inclination (δ) w.r.t y-axis is swept respectively. Both I_{ON} and I_{OFF} decrease with an increase in θ_B (δ), but I_{ON}/I_{OFF} improves continuously due to steeper fall in I_{OFF}. SS < 60 mV per decade can be achieved for nn-config. for a wide range ((b) and (e)) of θ_B (δ) which gives flexibility in the selection of I_{ON} and I_{ON}/I_{OFF} ((c) and (f)) for the circuit design.

approximately halved. Finally, from a circuit and fabrication perspective, the symmetry about both the x and y-axis for design B, like traditional MOSFET, makes it easier to place in VLSI environment and fabrication processes giving it an edge over design A, because the transistor layout can be mirrored and interconnects routed easily among them.

Next, we study the effect of temperature on the device performance of both designs, to determine the operational temperature range of the GEOT device. As shown in Fig. 4, it can be observed that increasing temperature degrades the performance because of higher SS (Fig. 4(b) and (e)) and lower I_{ON}/I_{OFF} (Fig. 4(c) and (f)) for both designs. The reason can be attributed to the aggravated contribution of the electron injection at energies far from the equilibrium chemical potential due to the tail of Fermi distribution at higher temperature and therefore, increased leakage current at I_{OFF}. This indicates that, even though the operation principle of these GFETs is not the same as MOSFETs, thermionic currents still play an important role in determining the magnitude of I_{OFF}. However, SS for nn-config. still remains lower than MOSFET benchmark of 2.3 k_BT, for the entire temperature range, due to the dependence of allowed energies on V_{G2}, as expressed in eqn (4) of the Appendix (also see eqn (4) of ref. 7).

Furthermore, it is observed that I_{ON} fractionally increases with temperature around the saturation point (Fig. 4(c) and (f)) for design A, whereas the reverse trend is observed for design B. This is because of the interplay between three competing factors, namely: (i) increasing temperature, the magnitude of the difference in the Fermi distribution (Δf) between the quasi-fermi levels of the source and drain (μ_S and μ_D respectively) gets smaller, (ii) Δf increases in energy range about μ_S and μ_D where η_{21} and therefore θ_C is higher (eqn (1)) and iii) fixed θ_i (=δ) for design B whereas for design A, $\theta_i \in [-\pi/2,\pi/2]$. However, in design B, factor (i) mentioned above dominates, resulting in a negative slope for Fig. 4(f)). Moreover, the decay of I_{ON} with temperature for design-B excludes the possibility of a thermal runaway thereby making it better than design-A with respect to the thermal response.

Next, we investigate the effect of V_{G1} on the device performance with a fixed V_{G2}. Electrostatically, V_{G1} defines the static doping profile of one segment of the device, and the range of the relative refractive index (η_{21}) (eqn (1)) for optical emulation of the device characteristics. An optimum value of V_{dope} (eqn (8)) can also be used to have an equivalent chemical doping of the entire graphene channel to get rid of V_{G1},[8] thereby reducing one electrical connect per transistor. As shown in Fig. 5, both designs

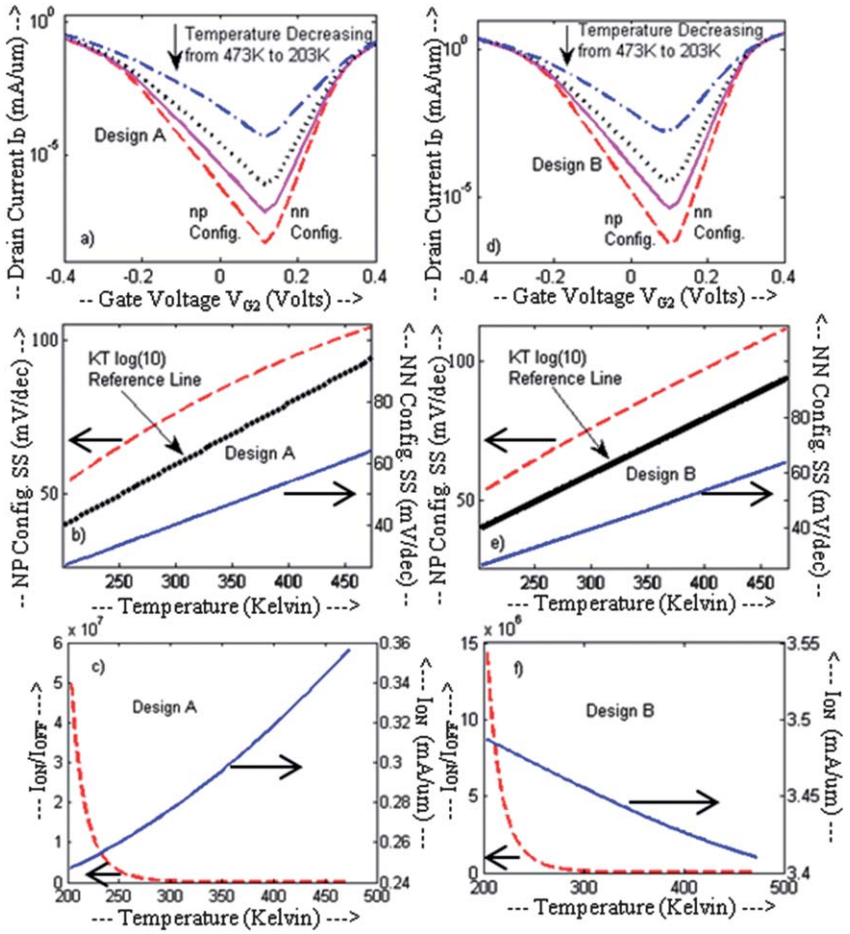

Fig. 4 Impact of temperature for $V_{G1} = 1$ V at θ_B (δ) = 20°. (a and d): I_{OFF}, which corresponds to leakage current in circuits, decreases with temperature, but V_{G2} corresponding to I_{OFF} remains constant. (b and e): Subthreshold slope (SS) degrades with increase in temperature for both np and nn config. (c and f) I_{ON} fractionally increases and decreases with increase in temperature for np and nn configurations, respectively.

have a symmetrical response for bipolar V_{G1} with respect to both drain currents (Fig. 5(a) and (d)) and SS (Fig. 5(b) and (e)) *i.e.*, nn-configuration is equivalent to pp-configuration. As shown in Fig. 5(c) and (f), I_{ON} has a local maxima over the full swing voltage of V_{G2} for either polarity. This is because of the competing effect of the density of states (DOS) for electron transport, and total internal reflection on the source side. Based on our approximation, for a full swing of V_{G2} ($\pm$0.4 V), the DOS in the current equation (eqn (3)) is determined by its value in graphene under V_{G1} from 0 to V_{G2}, beyond which the DOS in segment 2 becomes the limiting factor and keeps the DOS factor constant in the equation. This is a simple approximation for DOS and the experimental results should show relatively smooth maxima instead of the sharp peak observed in our simulation. I_{ON} then decays beyond the maximum because the total internal reflection within segment 1 becomes stronger with increasing V_{G1}. In addition, for higher magnitudes of V_{G1}, I_{OFF} decreases considerably because the relative refractive index is inversely proportional to V_{G1} (eqn (1)). Therefore, it becomes easier to achieve total internal reflection for a given θ_B (δ) leading to lower leakage or OFF-state current. Owing to the steeper decline in I_{OFF}, the I_{ON}/I_{OFF} ratio invariably increases with increasing magnitude of V_{G1}, resulting in lower sub-threshold slopes. In summary, it can be found that (a) designs A and B are equivalent w.r.t. V_{G1}, (b) a bias voltage of either polarity can be used, (c) SS < 60 mV per decade is achieved for $V_{G1} > 0.5$ V, and (d) for V_{G1} beyond 0.5 V, the SS is nearly constant; therefore V_{G1} bias is a function of I_{ON} and I_{ON}/I_{OFF}.

Finally, a modification, which is applicable to both designs, is proposed to overcome the problem of non-zero V_{G2} *cf.*, Fig. 3. Based on the mathematical analysis of this problem as presented in the Appendix, it can be found that the problem may be resolved by chemically doping the channel to the equivalent of V_{dope},[8] or by placing a top gate and applying a compensation voltage V_{dope} with a capacitance transfer factor 'β'. The latter would electrostatically shift DOS for the entire result in an electrostatic shift in the channel by βV_{dope}. Therefore, with careful tuning of doping or gate voltages in both designs, one can have a shift in the drain current profile so as to achieve zero V_{G2} at the I_{OFF} point, as shown in Fig. 6. This would thereby reduce static power dissipation, although this improvement comes at the cost of additional terminal or increased number of fabrication steps.

Before concluding, we would like to note that in this work, the ray-optics based model and an ideal graphene channel with abrupt junction without edge effects are assumed. However, for

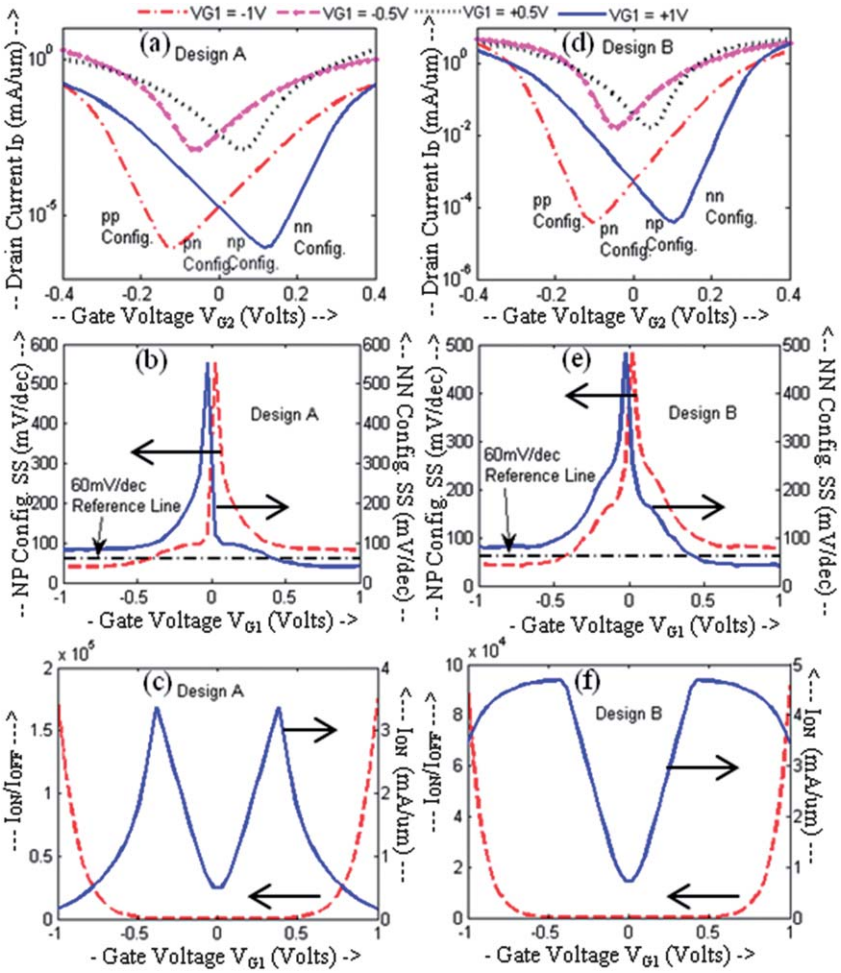

Fig. 5 Impact of the gate voltage over segment 1 (V_{G1}) for θ_B (δ) = 20° at 300 K. Note the independence of the device behavior of the polarity of V_{G1}. ((a) and (d)) The drain current decreases with increase in V_{G1} because of emulation of the smaller critical angle leading to blockage of a wider energy spectrum for injected electrons. ((b) and (e)) SS declines with increasing magnitude of V_{G1} to fall below 60 mV per decade benchmark and finally becomes relatively constant for $V_{G1} > V_{G2max}$ because of the density of states (DOS) factor in the current equation (eqn (3)) which we have crudely taken to be lesser of the two segments (eqn (1) of ref. 28) because a segment with smaller DOS acts as a stronger impediment in the current flow. ((c) and (f)) I_{ON} peaks for a full swing voltage of V_{G2} in either polarity, because of the competing effect of DOS for electron transport and total internal reflection on the source side.

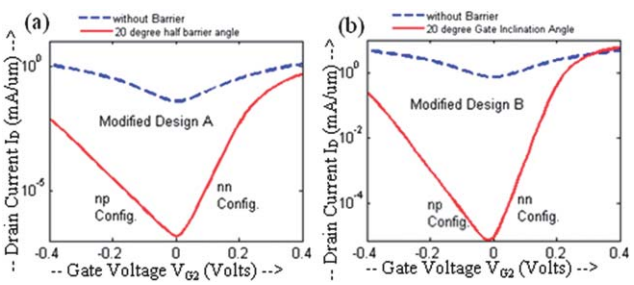

Fig. 6 Impact of chemical doping or the top gate on V_{G2} translation at 300 K and V_{G1} = 1 V. The graphene channel is doped to equivalent of V_{dope} eV or the top gate is used to materialize the effect. The main objective is to attain zero V_{G2} for I_{OFF} to match the switch-off for contemporary logic levels. V_{dope} is a function of θ_B (or δ), V_{G1} and the gate transfer capacitance factor (β), if the top gate is used for tuning. Refer to the Appendix for derivation. As per eqn (8), for both designs, V_{dope} = 0.1345 eV (red).

the realistic devices, with finite transition width across the p–n junction, transmission is expected to decrease[28] for both designs because of decreased angular bandwidth ($2\theta_C$ and $2\delta_{effective}$ for designs A and B, respectively), and therefore, decreased current. However, taking abrupt junction and neglecting self-consistent calculations for the charge profile in the transition region lead to overestimate E_{DOS} under the high bias (eqn (3) of the Appendix) which projects larger currents than the calculations using NEGF for np-config. at large biases.[28] Nevertheless, for nn-config., the recommended device operation region for GEOT, the results from two models are comparable.[28] Next, for neglecting edge effects, we have presumed an infinitely wide channel for both designs, however, in a real device, especially B, some electron transport is expected along the edges[29] which increases the current (counter-effect of the finite transition width). Therefore, since capturing these effects is beyond the ray-optic model, for future evaluation, more sophisticated simulation with self-consistent potential calculations should be implemented to

simulate accurate device characteristics despite of its high computational resource requirements.

IV. Conclusion

Within the scope of the ray-optic model, Table 1 summarizes the key findings both qualitatively and quantitatively of these two designs with respect to variation of the above stated parameters. We found that, firstly, both designs have a similar response to V_{G2} dynamics and generate the best response for symmetrical device geometry for barrier position or gate inclination. Secondly, for $\theta_B \sim \delta = 19°$, though SS is almost the same, but I_{ON} for design-B is expected to be higher (factor of 24.67 in Table 1) whereas I_{ON}/I_{OFF} for design-A betters B by a factor of 2. We have also suggested a range for θ_B (δ) for fabrication for the optimal performance of the transistor. Thirdly, we observed an opposing thermal response of I_{ON} and glossed over it later in discussion. Fourthly, we have observed that both designs have a similar response about the polarity of V_{G1}. Finally, a solution is proposed for the issue of non-zero V_{G2} for I_{OFF} for the proposed devices.

In summary, by sweeping V_{G1}, V_{G2}, the temperature and device geometry (input parameters), we expect the two design proposals to have a similar effect on the drain current. Therefore, a comparable I_{ON}, I_{OFF}, SS and I_{ON}/I_{OFF} ratio (output parameters) should be achievable for given electrical specifications for a transistor with a prudent choice of device geometry. Secondly, unipolar operation *i.e.* 'nn' (V_{G1}, $V_{G2} > 0$) or 'pp' (V_{G1}, $V_{G2} < 0$) is recommended to attain sub-60 mV per decade slope for the entire temperature range of interest. Anyhow, suitable device geometry has been suggested in Table 1 according to the region of operation to aid circuit designers, though we suggest quantum transport model based calibration for exact modeling and optimization before parameter extraction.

V. Appendix

The source is externally connected to the anode of the battery and therefore injects electrons into the graphene channel, whereas the drain is connected to the cathode and collects the electrons. Therefore, the current flows from drain to source *via* the graphene channel, which is electrostatically segmented into two parts, each of which is controlled by different gate voltage over it *i.e.* V_{G1} and V_{G2}.

In unbiased state, the electrochemical potential of the entire graphene channel (μ_1 and μ_2), source (μ_S) and drain (μ_D) is in equilibrium ($V_{eq} = 0$ V) *i.e.* at the same level. When we apply a small positive drain to the source voltage V_{DS}, μ_S remains at V_{eq} but μ_D moves down to $V_{eq} - V_{DS}$. μ_1 and μ_2 move down to $V_{eq} - V_{DS}/2$. Now, if the capacitive gate transfer factor is 'α' for both gates (taken to be one in this simulation), then the application of gate voltage changes the electrochemical potentials to $V_{eq} - \alpha V_{G1} - V_{DS}/2$ and $V_{eq} - \alpha V_{G2} - V_{DS}/2$ for segment 1 and 2 respectively. In our simulations, we have considered V_{eq} to be zero because all voltages used in the equations are relative to V_{eq}. Note that all energies are in eV. The set of equations we have used is described as follows.

Relative refractive index,

$$\eta_{21} = \frac{E - (V_{eq} - \alpha V_{G2} - V_{DS}/2)}{E - (V_{eq} - \alpha V_{G1} - V_{DS}/2)} \quad (1)$$

where E is the injected electron energy in eV.

Transmission probability[4] across the electrostatically separated graphene segments is

$$T(E) = A_1 \frac{\cos\theta_i \cos\theta_r}{\cos^2\left(\frac{\theta_i + \theta_r}{2}\right)} \quad (2a)$$

$$\text{for design A: } A_1 = \Theta(\theta_C - |\theta_i|)\,\Theta(|\theta_i| - |\theta_B|) \quad (2b)$$

$$\text{for design B: } A_1 = \Theta(\theta_C - |\theta_i|) = \Theta(|\theta_C| - |\delta|) \quad (2c)$$

where Θ is the unit Heaviside step function.

The drain current for ballistic transport is given as follows,

$$I_D = \frac{2q}{h}\int dE \frac{hD(E)v_F}{2L} T(E)(f_S(E) - f_D(E))$$

$$\Rightarrow \frac{I_D}{W} = \frac{2q}{h}\int dE \frac{\pi\hbar D(E)v_F}{WL} T(E)(f_S(E) - f_D(E))$$

where the density of states/area is

Table 1 Comparing the behavior of design A with design B

Swept parameter	Design A	Design B
Moving barrier position ($\pm\theta_B$) for design A or orientation of gate inclination ($\pm\delta$) for design B	Drain current same for designs m and n if (UBA_m, LBA_m) = (LBA_n, UBA_n) Lowest I_{OFF} and highest I_{ON}/I_{OFF} for UBA = LBA	Drain current same for designs m and n if ($\delta_m = -\delta_n$)
Increasing θ_B (δ)	(a) Drain current decreases (b) I_{ON}/I_{OFF} increases (c) SS decreases (d) For $I_{ON} > 0.1$ mA μm^{-1} and $I_{ON}/I_{OFF} > 10^4$: nn region: 14–21° np region: 14–26° (e) At $\theta_B = 19°$: nn region: $I_{ON} \sim 0.15$ mA μm^{-1}; $I_{ON}/I_{OFF} \sim 11 \times 10^4$; SS ~ 40 mv per decade; np region: $I_{ON} \sim 0.28$ mA μm^{-1}; $I_{ON}/I_{OFF} \sim 20 \times 10^4$; SS ~ 82 mV per decade	(a) Drain current decreases (b) I_{ON}/I_{OFF} increases (c) SS decreases (d) For $I_{ON} > 0.1$ mA μm^{-1} and $I_{ON}/I_{OFF} > 10^4$: nn region: 16–26° np region: 16–36° (e) At $\delta = 19°$: nn region: $I_{ON} \sim 3.7$ mA μm^{-1}; $I_{ON}/I_{OFF} \sim 6 \times 10^4$; SS ~ 44 mV per decade; np region: $I_{ON} \sim 2.5$ mA μm^{-1}; $I_{ON}/I_{OFF} \sim 3.5 \times 10^4$; SS ~ 81 mv per decade
Increasing temperature	I_{ON} slightly increases	I_{ON} slightly decreases
Effect of V_{G1} (equivalent for both designs)	Device characteristic symmetrical about the polarity of V_{G1}	Device characteristic symmetrical about polarity of V_{G1}

$$\frac{D(E_{DOS})}{WL} = \frac{1}{2\pi\hbar^2 v_F^2}|E_{DOS}|$$
$$\Rightarrow \frac{I}{W} = \frac{2q}{h}\frac{1}{4\pi}\frac{1}{\hbar v_F}\int dE|E_{DOS}|T(E)(f_S(E) - f_D(E)) \quad (3)$$

where $E_{DOS} = \min(E - (V_{eq} - \alpha V_{G2} - V_{DS}/2), E - (V_{eq} - \alpha V_{G1} - V_{DS}/2))$.

Note that, in general, above E_{DOS} the approximation is valid only if the difference in the two compared values is large. Nevertheless, it gives a qualitative picture and in fact holds good for the ballistic model even quantitatively in purview of our simulation constraints.

For a symmetrically placed barrier ($\phi = \theta_B$ in design A) and gate inclination ($\phi = \delta$ in design B), the range of energies E_1 to E_2 blocked are given by,[7]

$$+\sin\phi = \frac{E_1 - (V_{eq} - \alpha V_{G2} - V_{DS}/2)}{E_1 - (V_{eq} - \alpha V_{G1} - V_{DS}/2)}$$
$$-\sin\phi = \frac{E_2 - (V_{eq} - \alpha V_{G2} - V_{DS}/2)}{E_2 - (V_{eq} - \alpha V_{G1} - V_{DS}/2)}$$
$$E_1 = V_{eq} - \frac{\alpha(V_{G2} - V_{G1}\sin\phi)}{1 - \sin\phi} - \frac{V_{DS}}{2} \quad (4)$$
$$E_2 = V_{eq} - \frac{\alpha(V_{G2} + V_{G1}\sin\phi)}{1 + \sin\phi} - \frac{V_{DS}}{2}$$
$$\Rightarrow \Delta E = E_1 - E_2 = \text{BandGap} = \frac{2\alpha(V_{G1} - V_{G2})\sin\phi}{\cos^2\phi}$$

Moreover, analytically I_{OFF} will correspond to V_{G2} at which barrier angle blocks maximum of Fermi distribution *i.e.* when E_1 and E_2 are symmetrical about the peak for '$f_S(E) - f_D(E)$' which lies at $(-V_{DS}/2)$. Therefore, $E_1 - (-V_{DS}/2) = (-V_{DS}/2) - E_2$. Hence, the corresponding V_{G2} is given as,

$$V_{G2} = V_{G1}\sin^2\phi + \frac{(V_{eq})}{\alpha}\cos^2\phi \quad (5)$$

Since V_{eq} is taken to be zero, eqn (5) implies non-zero V_{G2} for I_{OFF}, which is a drawback given the voltage levels of contemporary switching logic.

However, if we physically eliminate V_{G1} and chemically dope the graphene channel[8] to V_{dope} in an equilibrium unbiased state, then

$$V_{G2} = -V_{dope}\cos^2\phi + \frac{(V_{eq})}{\alpha}\cos^2\phi \quad (6)$$

This still leads to non-zero V_{G2} corresponding to I_{OFF}.

On the other hand, if we retain V_{G1} along with doping V_{dope}, then eqn (5) becomes,

$$V_{G2} = V_{G1}\sin^2\phi - V_{dope}\cos^2\phi + \frac{(V_{eq})}{\alpha}\cos^2\phi \quad (7)$$

Now, it is possible to attain zero V_{G2} for I_{OFF} by tuning V_{dope} for a given specification of V_{G1} and ϕ. Moreover, we can have a top gate, with a transfer factor 'β', as a compensation pin to tune the operating logic voltages such that,

$$V_{dope} = \frac{(V_{G1} - V_{G2})}{\beta}\tan^2\phi - \frac{V_{G2}}{\beta} + \frac{(V_{eq})}{\alpha\beta}\cos^2\phi \quad (8)$$

Note that for chemical doping we have taken β to be one.

Acknowledgements

This work at the National University of Singapore was supported by MOE under Grant Nos. R263000689112. The authors would like to thank Dr Tony Low for helpful discussions.

References

1 System Drivers, 2011 Chapter, International Technology Roadmap for Semiconductors.
2 J. P. Collinge, D. Flandre and F. Van de Wiele, Subthreshold slope of long channel, accumulation mode p-channel SOI MOSFETs, *Solid-State Electron.*, 1994, **37**, 289–294.
3 A. Tura and J. C. S. Woo, Performance comparison of silicon steep subthreshold FETs, *IEEE Trans. Electron Devices*, 2010, **57**(6), 1362–1368.
4 A. H. C. Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov and A. K. Geim, The electronic properties of graphene, *Rev. Mod. Phys.*, 2009, **81**, 109–162.
5 F. Schwierz, Graphene Transistors 2011, *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, 2011, pp. 1–2.
6 F. Schwierz, Graphene transistors, *Nat. Nanotechnol.*, 2010, **5**, 487–496.
7 R. Sajjad and A. Ghosh, High efficiency switching using graphene based electron 'optics', *Appl. Phys. Lett.*, 2011, **99**, 123101–123103.
8 T. Sohier and B. Yu, Ultralow-voltage design of graphene PN junction quantum reflective switch transistor, *Appl. Phys. Lett.*, 2011, **98**, 213104–213106.
9 T. Low and J. Appenzeller, Electronic transport properties of a tilted graphene p–n junction, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 2009, **80**, 155406.
10 Z. Wu, Electronic fiber in graphene, *Appl. Phys. Lett.*, 2011, **98**, 082117–082119.
11 V. Cheianov, V. Fal'ko and B. Altshuler, The focusing of electron flow and a Veselago lens in graphene p–n junctions, *Science*, 2007, **315**, 1252–1255.
12 C. Y. Sung, Post Si CMOS graphene nanoelectronics, *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, 2011, pp. 1–2.
13 J. Williams, T. Low, M. Lundstrom and C. M. Marcus, Gate-controlled guiding of electrons in graphene, *Nat. Nanotechnol.*, 2011, **6**, 222–225.
14 S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy and A. H. MacDonald, Bilayer pseudospin field-effect transistor (BiSFET): a proposed new logic device, *IEEE Electron Device Lett.*, 2009, **30**, 158–160.
15 M. I. Katsnelson, K. S. Novoselov and A. K. Geim, Chiral tunneling and Klein paradox in graphene, *Nat. Phys.*, 2006, **2**, 620–625.
16 A. F. Young and P. Kim, Quantum interference and Klein tunneling in graphene heterojunctions, *Nat. Phys.*, 2009, **5**, 222–226.
17 O. B. Treidel, O. Peleg, M. Grobman, N. Shapira and M. Segev, Klein tunneling in deformed honeycomb lattices, *Phys. Rev. Lett.*, 2010, **104**, 063901–063904.
18 V. O. Klein, *Die Reflexion yon Elektronen an Einem Potentialsprung Nach Der Relativistischen Dynamik Yon Dirac*, Springer, Berlin/Heidelberg, 1929, vol. 53, pp. 157–165.
19 N. Stander, B. Huard and D. G. Gordon, Evidence for Klein tunneling in graphene p–n junctions, *Phys. Rev. Lett.*, 2009, **102**, 026807–026810.
20 A. Shytov, M. Rudner, N. Gu, M. Katsnelson and L. Levitov, Atomic collapse, Lorentz boosts, Klein scattering, and other quantum relativistic phenomenon in graphene, *Solid State Commun.*, 2009, **149**, 1087–1093.
21 V. V. Cheianov and V. I. Fal'ko, Selective transmission of dirac electrons and ballistic magnetoresistance of n–p junctions in

graphene, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 2006, **74**, 041403.
22 V. F. Hund, Materieerzeugung im anschaulichen und im gequantelten wellenbild der materie, *Z. Phys. A: Hadrons Nucl.*, 1940, **117**, 1–17.
23 D. Dragoman, Evidence against Klein paradox in graphene, *Phys. Scr.*, 2009, **79**, 015003.
24 A. Hansen and F. Ravndal, Klein's paradox and its resolution, *Phys. Scr.*, 1981, **23**, 1036.
25 F. Sauter, Ober das Verhalteneines elektrons im homogenen elektrischen feld nach der relativistischen theorie diracs, *Z. Phys.*, 1931, **69**, 742–764.
26 M. R. Setare and D. Jahani, Electronic transmission through p–n and n–p–n junctions of graphene, *J. Phys.: Condens. Matter*, 2010, **22**, 245503.
27 A. D. Wiener and M. Kindermann, Signatures of evanescent mode transport in graphene, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 2011, **84**, 245420–245426.
28 T. Low, S. Hong and J. Appenzeller, Conductance asymmetry of graphene p–n junction, *IEEE Trans. Electron Devices*, 2009, **56**(6), 1292–1299.
29 P. Zhao and J. Guo, Modeling edge effects in graphene nanoribbon field-effect transistors with real and mode space methods, *J. Appl. Phys.*, 2009, **105**, 034503.