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Formation of high-quality oxide/$Ge_{1-x}Sn_x$ interface with high surface Sn content by controlling Sn migration

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In this paper, we investigated how Sn migrated during annealing for $Ge_{1-x}Sn_x$ at its surface and in its interior, as well as the Ge oxide formation on $Ge_{1-x}Sn_x$ with controlling surface oxidation. After oxidation at 400 °C, X-ray photoelectron spectroscopy and X-ray diffraction measurements revealed Sn migration from inside the epitaxial $Ge_{1-x}Sn_x$ layer to its surface. Annealing was not the primary cause of significant Sn migration; rather, it was caused mostly by oxidation near the $Ge_{1-x}Sn_x$ surface. This process formed a $Ge_{1-x}Sn_x$ oxide with a very high Sn content of 30%, inducing a wide hysteresis loop in the capacitance–voltage characteristics of its corresponding MOS device. We also found that forming a thin GeO_2 layer by using a deposition method that controls Ge surface oxidation produced low densities of interface states and slow states. From these results, we conclude that controlling Sn migration is critical to forming a high-quality $Ge_{1-x}Sn_x$ gate stack. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4896146]

Germanium-tin alloys ($Ge_{1-x}Sn_x$) have attracted much attention as a channel material for next-generation metal-oxide-semiconductor field-effect transistors (MOSFETs) and tunnel FETs[1–4] because their energy-band structures change with the Sn content. At a Sn content of ~8%, the conduction band minimum crosses over from the L valley to the Γ valley,[1] and the electron effective mass significantly decreases at the Γ point.[5] However, the solid solubility limit of Sn in Ge is ~1%,[6] and the surface energy of Sn is smaller than that of Ge.[7] These characteristics induce Sn precipitation and segregation, making it quite difficult to form a $Ge_{1-x}Sn_x$ layer with high amounts of uniformly distributed Sn. A promising technique to surpass these limits is the combination of low-temperature growth and strain control, with which we achieved epitaxial growth of $Ge_{1-x}Sn_x$ layers with Sn content up to 25%,[8–10] owing to growth at non-thermal equilibrium.

Forming a high-quality MOS interface for $Ge_{1-x}Sn_x$ is still a critical obstacle to realizing high-performance $Ge_{1-x}Sn_x$ MOSFETs and tunnel FETs. For pure-Ge gate stacks, Ge-based oxide interlayers can be used to effectively decrease the interface state density (D_{it}).[11–13] For example, a GeO_2/Ge interfacial structure prepared with thermal oxidation of pure Ge can achieve D_{it} as small as $10^{10}eV^{-1}$ cm^{-2}.[11] In contrast, thermal oxidation of $Ge_{1-x}Sn_x$ layers formed at non-thermal equilibrium has produced complicated results. For example, Han *et al.* found that thermally oxidizing the $Ge_{1-x}Sn_x$ surface decreased the subthreshold swing of its corresponding MOSFET,[3] indicating a decreased D_{it} at the $Ge_{1-x}Sn_x$-oxide/$Ge_{1-x}Sn_x$ interface. However, we have found that, in a $Ge_{1-x}Sn_x$ oxide layer formed by thermal oxidation at 400 °C, the Sn content is higher than that near the surface of the epitaxial $Ge_{1-x}Sn_x$ layer.[14] Sn migration into the oxide layer increases the leakage current density[15] and the hysteresis width in the capacitance-voltage (C–V) characteristics of MOS capacitors.[14] These results show that, to form high-quality $Ge_{1-x}Sn_x$/Ge interfaces, it is critical to clarify the structural properties of the insulator/$Ge_{1-x}Sn_x$ interface and understand Sn migration control.

In the present study, we investigated Sn migration at the $Ge_{1-x}Sn_x$ surface and the oxide/$Ge_{1-x}Sn_x$ interface during thermal annealing and oxidation, considering a greater Sn content than the solid solubility limit. Additionally, we attempted to improve the electrical properties of a $Ge_{1-x}Sn_x$ MOS capacitor by controlling Sn migration with GeO_2 chemical vapor deposition (CVD).[13]

A Ga-doped p-type Ge(001) substrate with a resistivity of 1 Ω cm was used. After the substrate was chemically and thermally cleaned, a $Ge_{1-x}Sn_x$ layer was pseudomorphically grown on the Ge(001) substrate by solid-source molecular-beam epitaxy (MBE). The growth temperature was 150 °C. The thickness of the $Ge_{1-x}Sn_x$ layer was 30 or 50 nm for samples with a Sn content of 8.7% or 7.6%, respectively; the Sn content was evaluated by X-ray diffraction (XRD) two-dimensional reciprocal space mapping. After deposition, the $Ge_{1-x}Sn_x$/Ge surface was cleaned with a 1% HF solution to remove native oxides and Sn precipitated on the surface.[14] Some $Ge_{1-x}Sn_x$/Ge samples were annealed after deposition at 400 °C in N_2 or dry O_2.

For another $Ge_{1-x}Sn_x$/Ge sample, a thin GeO_2 layer was formed by CVD on the $Ge_{1-x}Sn_x$ by pulsing alternating supplies of tetraethoxy-germanium (TEOG) and H_2O for 40 cycles at 300 °C.[13] To make MOS capacitors, a gate stack of Al_2O_3 and Al was deposited. The 5 nm Al_2O_3 layer was formed by atomic layer deposition (ALD) using trimethyl-aluminum (TMA) and H_2O at 150 °C on the Ge(Sn)-oxide/

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$Ge_{1-x}Sn_x$ samples, and the Al gate electrode was formed by vacuum evaporation.

In $Ge_{1-x}Sn_x$ layers formed at non-thermal equilibrium, it is not well understood how the annealing stability differs between Sn atoms in diamond lattice sites and those in interstitial sites. To better understand these properties, we used X-ray photoelectron spectroscopy (XPS) to investigate the chemical bonding states of each element near the surface of the $Ge_{1-x}Sn_x$ layers after annealing, using Mg $K\alpha$ ($h\nu = 1253.6$ eV) as the X-ray source. Figures 1(a) and 1(b) show the Ge 3d and Sn $3d_{5/2}$ photoelectron core spectra of the $Ge_{0.913}Sn_{0.087}$/Ge samples before (only etched with HF; HF) and after N_2 annealing (NA) or oxidation (OD) at 400 °C for 10 min. We corrected the binding energies using the Ge–Ge (or Ge–Sn) bond peak at 29.4 eV, and normalized the intensities with the area intensity of the Ge–Ge (or Ge–Sn) bond peak. For the HF sample, there were no obvious peaks related to Ge- or Sn-oxides in the Ge 3d and Sn $3d_{5/2}$ spectra, respectively, meaning that the HF solution removed the native oxide from the as-deposited $Ge_{1-x}Sn_x$ layer. We found that the Sn content near the $Ge_{1-x}Sn_x$ surface was ~19%, about twice that of the content ratio of Sn atoms incorporated into the diamond lattice site. This result strongly suggests that Sn atoms segregate near the $Ge_{1-x}Sn_x$ surface during growth because of the low surface energy of Sn atoms[7] and their low solid solubility limit.[6] Here, we evaluated the Sn content from the intensity ratios of photoelectron signals in the Ge $3d_{5/2}$ and Sn $3d_{5/2}$ spectra, accounting for attenuation of photoelectron intensities with inelastic electron scattering. The relationships between photoelectron intensity (I^{GeSn} or I^{oxide}) and the atomic density of Ge or Sn (X^{GeSn} or X^{oxide}) in the $Ge_{1-x}Sn_x$ layer and $Ge_{1-x}Sn_x$ oxide layer are shown in following equations:[16]

$$I_i^{GeSn} = \alpha \cdot X_i^{GeSn} \cdot \sigma_i \cdot \lambda_i^{GeSn} \cdot \left\{1 - \exp\left(-\frac{d_{GeSn}}{\lambda_i^{GeSn}}\right)\right\} \times \exp\left(-\frac{d_{oxide}}{\lambda_i^{oxide}}\right), \quad (1)$$

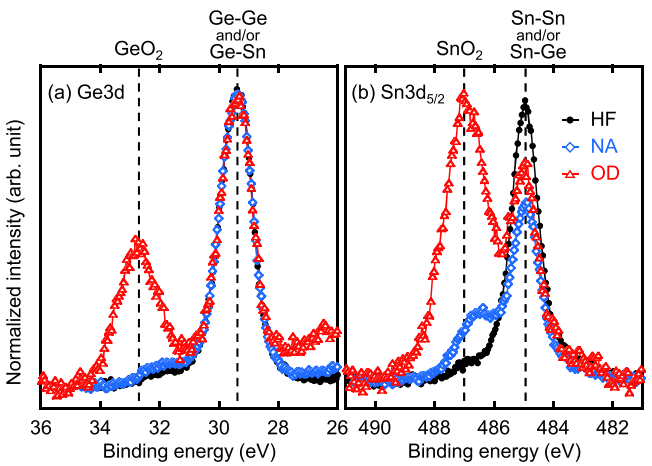

FIG. 1. (a) Ge 3d and (b) Sn $3d_{5/2}$ photoelectron core spectra of $Ge_{0.913}Sn_{0.087}$/Ge before and after N_2 annealing (NA) or thermal oxidation (OD) at 400 °C for 10 min. The binding energies were corrected using the Ge–Ge bond peak at 29.4 eV, and the photoelectron intensities were normalized with the area intensity of the Ge–Ge bond peak.

$$I_i^{oxide} = \alpha \cdot X_i^{oxide} \cdot \sigma_i \cdot \lambda_i^{oxide} \cdot \left\{1 - \exp\left(-\frac{d_{oxide}}{\lambda_i^{oxide}}\right)\right\}. \quad (2)$$

Here, the subscript index i represents a constituent element, Ge or Sn, and the superscript of GeSn or oxide indicates the intended layer. α, σ, and λ are a coefficient related to the X-ray power and the detector used, a photoionization coefficient, and the inelastic mean free path (IMFP) of electrons, respectively. d_{GeSn} and d_{oxide} are the thicknesses of the $Ge_{1-x}Sn_x$ and $Ge_{1-x}Sn_x$ oxide, respectively. Note that we use the IMFP in Ge or stoichiometric GeO_2 rather than in $Ge_{1-x}Sn_x$ or $Ge_{1-x}Sn_x$ oxide; we did this because the physical characteristics of $Ge_{1-x}Sn_x$ and $Ge_{1-x}Sn_x$ oxides are not yet sufficiently understood. Additionally, we assume an infinitely thick $Ge_{1-x}Sn_x$ layer because the thickness of the $Ge_{1-x}Sn_x$ layer was more than 10 times larger than the IMFPs of Ge $3d_{5/2}$ and Sn $3d_{5/2}$ photoelectrons.[14,17] The physical parameters used in our evaluation are summarized in our previous paper.[14]

The normalized intensity of the Sn $3d_{5/2}$ spectrum after N_2 annealing was slightly lower than that of the HF sample, and the Sn content for the annealed sample was ~15%. This behavior was mostly caused by preferential desorption of Sn atoms segregated or precipitated at the $Ge_{1-x}Sn_x$ surface, in turn caused by the high Sn content, although a detailed physical reason has not been clarified. This desorption occurred because the annealing temperature was higher than the melting point of Sn.[18] The change in Sn content between the HF and NA samples indicates Sn migration at the $Ge_{1-x}Sn_x$ surface during annealing at 400 °C. After oxidation at 400 °C, we found clear peaks related to Ge and Sn oxides in the Ge 3d and Sn $3d_{5/2}$ photoelectron core spectra, respectively. Using the area intensity of the Ge and Sn oxide peaks, we found the $Ge_{1-x}Sn_x$ oxide thickness to be 2.0 nm. Here, the $Ge_{1-x}Sn_x$ oxide thickness is the combined thicknesses of the Ge oxide and Sn oxide formed on the $Ge_{1-x}Sn_x$ layer. Using Eq. (3),[16] we separately evaluated the thicknesses of the Ge oxide and Sn oxide from the area intensity ratio of the Ge oxide or Sn oxide peak to the Ge–Ge bond peak, assuming stoichiometric $GeO_2/Ge_{1-x}Sn_x$ and $SnO_2/Ge_{1-x}Sn_x$ stacks, respectively

$$\frac{I_i^{oxide}}{I_{Ge}^{GeSn}} \approx \frac{X_i^{oxide} \cdot \sigma_i \cdot \lambda_i^{oxide}}{X_{Ge}^{GeSn} \cdot \sigma_{Ge} \cdot \lambda_{Ge}^{GeSn}} \cdot \frac{\left\{1 - \exp\left(-\frac{d_{oxide}}{\lambda_i^{oxide}}\right)\right\}}{\exp\left(-\frac{d_{oxide}}{\lambda_{Ge}^{oxide}}\right)}. \quad (3)$$

We estimated the atomic density of Ge in the $Ge_{1-x}Sn_x$ layer (X_{Ge}^{GeSn}) before any annealing from the Ge atomic density in a single crystal and the Sn content. Additionally, we previously confirmed that the Sn content in a $Ge_{1-x}Sn_x$ oxide layer formed by thermal oxidation at 400 °C is ~30%.[14] Assuming that the Ge oxide and Sn oxide separately exist in the $Ge_{1-x}Sn_x$ oxide layer, we estimated that a thickness of 2.0 nm converted to 1.4 nm of Ge oxide in the $Ge_{1-x}Sn_x$ oxide layer. For the homoepitaxial Ge layer, we estimated a Ge oxide thickness of 0.88 nm, even though its oxidation conditions matched those of the $Ge_{1-x}Sn_x$ layer. This difference

suggests that the Sn near the surface of the $Ge_{1-x}Sn_x$ layer enhanced the oxidation reaction, possibly because the Sn or Sn oxide catalyzed the oxidation reaction.[19] After thermal oxidation, the $Ge_{1-x}Sn_x$ oxide layer had a 30% Sn content, much higher than the 19% Sn content near the $Ge_{1-x}Sn_x$ surface. Nevertheless, the OD sample and HF sample had equal Sn contents near the $Ge_{1-x}Sn_x$ surface. The high Sn contents in the $Ge_{1-x}Sn_x$ oxide layer and at the $Ge_{1-x}Sn_x$ surface after oxidation suggest that Sn atoms migrated from both the $Ge_{1-x}Sn_x$ surface and from inside the $Ge_{1-x}Sn_x$ to the $Ge_{1-x}Sn_x$ oxide. This process re-distributed the Sn in the $Ge_{1-x}Sn_x$-oxide/$Ge_{1-x}Sn_x$ stack, similar to impurity re-distribution near the Si oxide and Si interface during thermal oxidation.[20,21] As discussed in Grove *et al.*, this re-distribution can be explained by the small segregation coefficient of the impurities, a ratio of the equilibrium concentrations of impurities in the substrate to that in the oxide layer; in such cases, the impurity concentration at the surface decreases relative to that inside the substrate.[22] However, during re-distribution of Sn in thermal oxidation, the Sn content near the $Ge_{1-x}Sn_x$ surface did not decrease after thermal oxidation, despite the significant Sn migration into the $Ge_{1-x}Sn_x$-oxide layer. This result also indicates the Sn migrated from both the $Ge_{1-x}Sn_x$ surface and interior to the $Ge_{1-x}Sn_x$ oxide interior and surface.

The changes in Sn content may have been caused by migration, which may account for the changes in lattice spacing as the Sn content fluctuated inside the $Ge_{1-x}Sn_x$ layer, as shown in Fig. 1. To confirm these changes, we measured XRD profiles of the $Ge_{1-x}Sn_x$ layers. Figure 2(a) shows the out-of plane ω–2θ XRD profiles around the 004 diffraction point for the HF, FA, and OD samples; here, the Sn content was 8.7%. Also, Fig. 2(b) plots the peak angles of the XRD profiles and the full width at half maximums (FWHMs) of the $Ge_{1-x}Sn_x$ 004 diffraction peaks. The peak angle and FWHM for the NA sample were equal to or slightly greater than those for the HF sample, while the OD sample had a clearly larger peak angle and FWHM. This increase in peak angle corresponds to a decrease in lattice spacing of the $Ge_{1-x}Sn_x$ crystals, which may have been caused by the decrease in Sn content in the $Ge_{1-x}Sn_x$. Accounting for the change in Sn content at the surface of the NA sample, as shown in Fig. 1(b), the slight increases in peak angle and FWHM could have been caused by Sn migration during annealing. The increases for the OD sample agree well with XPS results. Consequently, for both samples, the increases in peak angles and FWHMs indicate a decrease in Sn content in the $Ge_{1-x}Sn_x$ interior and an increase in Sn fluctuation from Sn migration, respectively.

The impacts of Sn migration could appear clearly in the electrical properties of the MOS interfaces. Indeed, in a previous paper, we reported that thermal oxidation decreased the interface state density despite Sn surface segregation, though we found large hysteresis in the *C*–*V* characteristics of oxidized-$Ge_{1-x}Sn_x$/$Ge_{1-x}Sn_x$/Ge MOS capacitors.[14] Nevertheless, we have already established a method of depositing a thin GeO_2 layer on a Ge substrate, which allows for controlled atomic thickness and suppression of Ge surface oxidation (GSO) because of the self-limiting adsorption of TEOG on a Ge substrate and exposure of H_2O, similar to ALD.[13] Henceforth, we refer to this deposition method and the deposited layer as GSO-controlled deposition and the GSO-controlled layer, respectively. GSO-controlled deposition could change the electrical properties of the interface. Figures 3(a) and 3(b) compare the *C*–*V* characteristics of the $Al/Al_2O_3/Ge_{1-x}Sn_x/Ge$ MOS capacitors with a thermal $Ge_{1-x}Sn_x$ oxide layer and a GSO-controlled layer, respectively. Here, using XRD, we estimated the Sn content in the $Ge_{1-x}Sn_x$ layer in the MOS capacitors to be 7.6%. To match the maximum process temperature with that of thermal oxidation, we performed GSO-controlled deposition after N_2 annealing at 400 °C for 10 min. Around $V_g = -1$ V, the frequency dispersion for the thermally oxidized sample was larger than that for the GSO-controlled sample. In fact, the

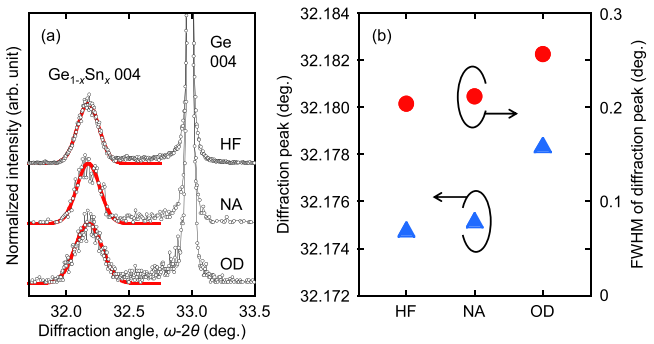

FIG. 2. (a) Out-of plane ω-2θ XRD profiles around the 004 diffraction points for the HF, FA, and OD $Ge_{0.913}Sn_{0.087}$/Ge samples. (b) Peak angles of the XRD profiles and FWHMs of the $Ge_{1-x}Sn_x$ 004 diffraction peaks.

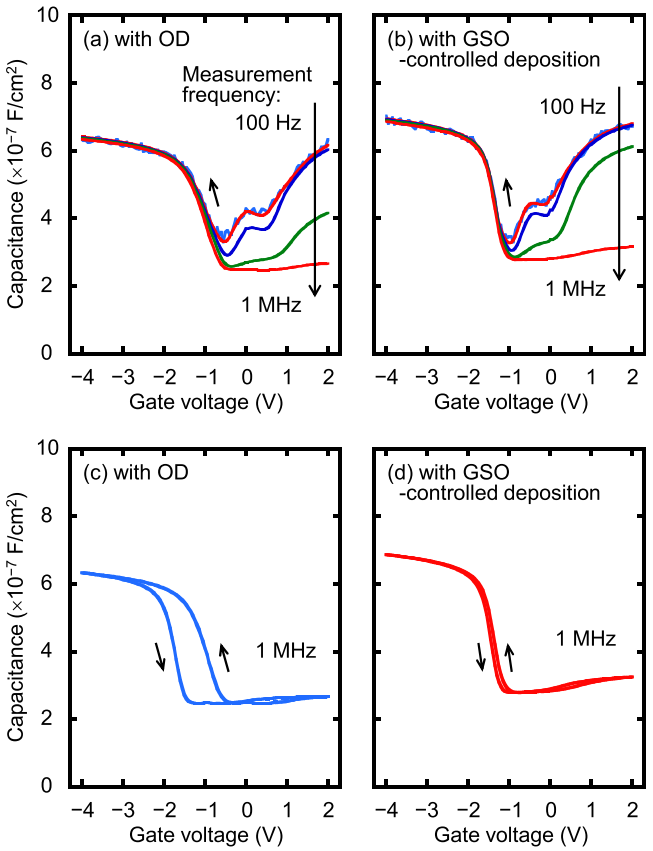

FIG. 3. *C*–*V* characteristics of $Al/Al_2O_3/Ge_{0.924}Sn_{0.076}$/p-Ge MOS capacitors with ((a) and (c)) a thermal $Ge_{1-x}Sn_x$ oxide layer or a ((b) and (d)) GSO-controlled layer, measured from 100 Hz to 1 MHz at 100 K.

D_{it} values of the thermally oxidized and GSO-controlled deposition samples, evaluated by the conductance method at $C/C_{ox} \sim 0.45$, were 1.2×10^{12} and $7.2 \times 10^{11}\,cm^{-2}\,eV^{-1}$, respectively. Here, C and C_{ox} mean the measured capacitance and oxide capacitance, respectively. These results indicate that GSO-controlled deposition decreased the D_{it}. Figs. 3(c) and 3(d) shows the 1 MHz C–V characteristics measured at 100 K of $Al/Al_2O_3/Ge_{1-x}Sn_x/Ge$ MOS capacitors with a thermal $Ge_{1-x}Sn_x$ oxide layer and a GSO-controlled layer, respectively. Although these samples did not differ much in D_{it}, the hysteresis width of the GSO-controlled deposition sample was much smaller than that of the thermally oxidized sample. Considering that hysteresis originates from slow states, this result indicates that forming the oxide layer by GSO-controlled deposition effectively reduced the slow-state density. The conduction band minimum of SnO_2 is lower than that of Ge,[19,23] and the defect levels are located near the conduction band edge when oxygen vacancies are created in SnO_2.[24] Thus, the hysteresis may have been caused by defect states from the anti-bonding states of Sn–O bonds in a phase-separated Sn oxide or $Ge_{1-x}Sn_x$ oxide with high Sn content, point defects such as oxygen vacancies in the Sn oxide or $Ge_{1-x}Sn_x$ oxide, or both. Figure 4 shows the number density of charge evaluated from the hysteresis width at $C/C_{ox} = 0.75$ and the C_{ox} value in the C–V characteristics as a function of the Ge and Sn oxide thicknesses. Here, we evaluated the oxide thicknesses by XPS of the oxide/$Ge_{1-x}Sn_x$ samples without an Al_2O_3 layer. At an oxide thickness of ~0 nm, the charge densities for the Al_2O_3/$Ge_{1-x}Sn_x$/Ge stack were almost identical to those for the Al_2O_3/epitaxial-Ge/Ge stack. From the hysteresis results, we do not believe the MOS slow-state density was significantly affected by differences between the two stacks in Sn migration, segregation, or both. We also found that charge densities did not exhibit a linear relationship with oxide thickness, implying that the charge density cannot be explained by a uniform defect density in the oxide layers. Also, the charge densities at both room temperature and 100 K for GSO-controlled deposition were smaller than those for thermal oxidation, owing to the suppression of Sn migration in GSO-controlled deposition. Consequently, suppressing Sn migration is important to forming $Ge_{1-x}Sn_x$ gate stacks with low densities of slow states and interface states. We found it possible to control the $Ge_{1-x}Sn_x$ surface, realizing a high-quality $Ge_{1-x}Sn_x$ MOS interface.

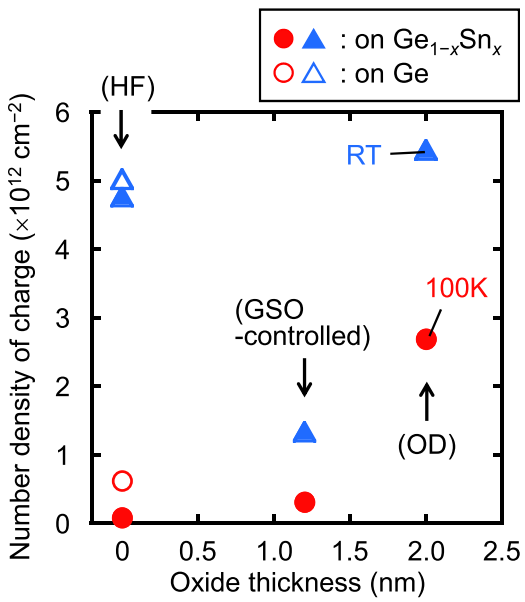

FIG. 4. Number density of charge as function of the oxide thickness, before depositing the Al_2O_3 layer, evaluated from the hysteresis width at $C/C_{ox} = 0.75$ and C_{ox} from the C–V characteristics. Filled and open symbols show results for epitaxial-Ge/p-Ge and $Ge_{1-x}Sn_x$/Ge samples, respectively.

In summary, we investigated Sn migration near the $Ge_{1-x}Sn_x$ surface and in the $Ge_{1-x}Sn_x$ layer after annealing in an effort to form a high-quality $Ge_{1-x}Sn_x$ MOS interface with high Sn content. We also examined controlling oxide formation on the $Ge_{1-x}Sn_x$ surface formed by GSO-controlled deposition. N_2 annealing at 400 °C caused little Sn migration. In contrast, oxidation at 400 °C caused significant Sn migration from inside the epitaxial $Ge_{1-x}Sn_x$ layer to its surface, producing a $Ge_{1-x}Sn_x$ oxide with a high Sn content of 30%, compared with the lower Sn content of 19% at its surface. The high Sn content at the $Ge_{1-x}Sn_x$-oxide/$Ge_{1-x}Sn_x$ interface induced a wide hysteresis width in the C–V characteristics of the corresponding MOS device. In contrast, we also found that GSO-controlled GeO_2 deposition produced low interface state and the slow-state densities. These results indicate that controlling Sn migration is very important to producing high-quality oxide/$Ge_{1-x}Sn_x$ gate stacks.

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